SBOS230A − MARCH 2002 − REVISED JUNE 2002

4-Channel Audio Volume Control

FEATURES

- **DIGITALLY-CONTROLLED ANALOG VOLUME CONTROL:**
  Four Independent Audio Channels
  Serial Control Interface
  Zero Crossing Detection
  Mute Function
- **WIDE GAIN AND ATTENUATION RANGE:**
  +31.5dB to −95.5dB with 0.5dB Steps
- **LOW NOISE AND DISTORTION:**
  120dB Dynamic Range
  0.0004% THD+N at 1kHz (U−Grade)
  0.0002% THD+N at 1kHz (A−Grade)
- **NOISE-FREE LEVEL TRANSITIONS**
- **LOW INTERCHANNEL CROSSTALK:**
  −130dBFS
- **POWER SUPPLIES: ±5V Analog, +5V Digital**
- **AVAILABLE IN AN SOP-28 PACKAGE**

APPLICATIONS

- **AUDIO AMPLIFIERS**
- **MIXING CONSOLES**
- **MULTI−TRACK RECORDERS**
- **BROADCAST STUDIO EQUIPMENT**
- **MUSICAL INSTRUMENTS**
- **EFFECTS PROCESSORS**
- **A/V RECEIVERS**
- **CAR AUDIO SYSTEMS**

DESCRIPTION

The PGA4311 is a high−performance, 4-channel audio volume control designed for professional and high-end consumer audio systems. Using high performance operational amplifier stages internal to the PGA4311 yields low noise and distortion, while providing the capability to drive 600Ω loads directly without buffering. The 3-wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy-chaining of multiple PGA4311 devices.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V_A+	+5.5V
V_A−	−5.5V
V_D+	+5.5V
V_A+ to V_D+	< ± 0.3V
Analog Input Voltage	0V to V_A+, V_A−
Digital Input Voltage	−0.3V to V_D+
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Package Temperature (IR reflow, 10s)	+235°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR(1)	OPERATING TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA4311 (U−Grade)	SOP−28	DW	−40°C to +85°C	PGA4311U	PGA4311U	Rails
				PGA4311U	PGA4311U/1K	Tape and Reel, 1000
PGA4311 (A−Grade)	SOP−28	DW	−40°C to +85°C	PGA4311UA	PGA4311UA	Rails
				PGA4311UA	PGA4311UA/1K	Tape and Reel, 1000

(1) For the most current specifications and package information, refer to our web site at www. ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_A+ = +5V, V_A− = −5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

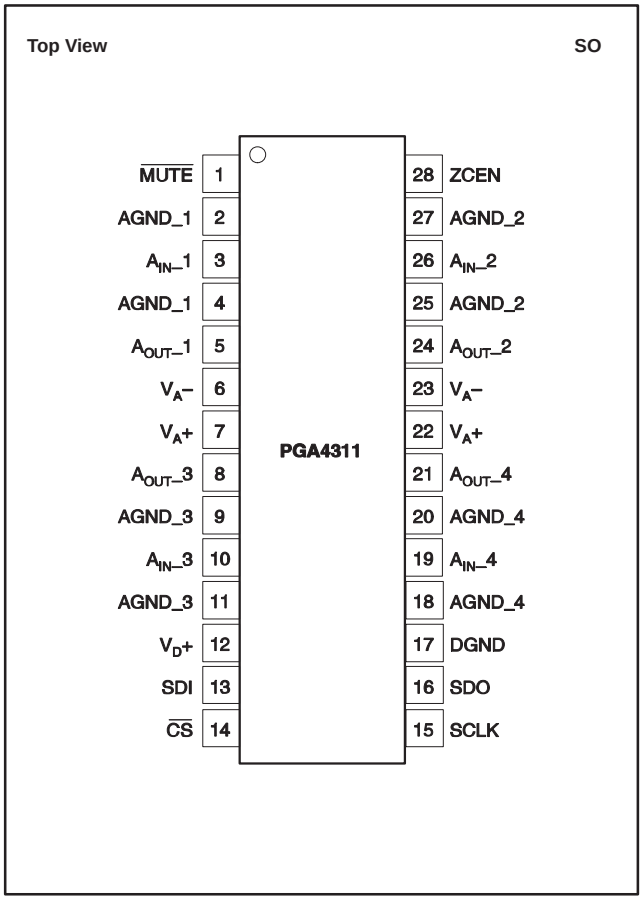
PARAMETER	CONDITIONS	PGA4311U (U−Grade)			PGA4311UA (A−Grade)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Step Size			0.5			0.5		dB
Gain Error	Gain Setting = 31.5dB		±0.05			±0.05		dB
Gain Matching			±0.05			±0.05		dB
Input Resistance			10			10		kΩ
Input Capacitance			3			3		pF
AC CHARACTERISTICS								
THD+N	V_{IN} = 2Vrms, f = 1kHz		0.0004	0.001		0.0002	0.0004	%
Dynamic Range	V_{IN} = AGND, Gain = 0dB	116	120		116	120		dB
Voltage Range, Output		(V_A−) + 1.25		(V_A+) − 1.25	(V_A−) + 1.25		(V_A+) − 1.25	V
Voltage Range, Input (without clipping)			2.5			2.5		Vrms
Output Noise	V_{IN} = AGND, Gain = 0dB		2.5	4		2.5	4	µVrms
Interchannel Crosstalk	f = 1kHz		−130			−130		dBFS
OUTPUT BUFFER								
Offset Voltage	V_{IN} = AGND, Gain = 0dB		0.25	0.5		0.25	0.5	mV
Load Capacitance Stability			100			100		pF
Short−Circuit Current			50			50		mA
Unity−Gain Bandwidth, Small Signal			10			10		MHz

ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_A+ = +5V, V_A− = −5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	CONDITIONS	PGA4311U (U−Grade)			PGA4311UA (A−Grade)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL CHARACTERISTICS								
High−Level Input Voltage, V_{IH}		+2.0		V_D+	+2.0		V_D+	V
Low−Level Input Voltage, V_{IL}		−0.3		0.8	−0.3		0.8	V
High−Level Output Voltage, V_{OH}	I_O = 200µA	(V_A+) − 1.0			(V_D+) − 1.0			V
Low−Level Output Voltage, V_{OL}	I_O = −3.2mA			0.4			0.4	V
Input Leakage Current			1	10		1	10	µA
SWITCHING CHARACTERISTICS								
Serial Clock (SCLK) Frequency	f_{SCLK}	0		6.25	0		6.25	MHz
Serial Clock (SCLK) Pulse Width LOW	t_{PH}	80			80			ns
Serial Clock (SCLK) Pulse Width HIGH	t_{PL}	80			80			ns
$\overline{\text{MUTE}}$ Pulse Width LOW	t_{MI}	2.0			2.0			ms
Input Timing								
SDI Setup Time	t_{SDS}	20			20			ns
SDI Hold Time	t_{SDH}	20			20			ns
$\overline{\text{CS}}$ Falling to SCLK Rising	t_{CSCR}	90			90			ns
SCLK Falling to $\overline{\text{CS}}$ Rising	t_{CFCS}	35			35			ns
Output Timing								
$\overline{\text{CS}}$ LOW to SDO Active	t_{CSO}			35			35	ns
SCLK Falling to SDO Data Valid	t_{CFDO}			60			60	ns
$\overline{\text{CS}}$ HIGH to SDO High Impedance	t_{CSZ}			100			100	ns
POWER SUPPLY								
Operating Voltage								
V_A+		+4.75	+5	+5.25	+4.75	+5	+5.25	V
V_A−		−4.75	−5	−5.25	−4.75	−5	−5.25	V
V_D+		+4.75	+5	+5.25	+4.75	+5	+5.25	V
Quiescent Current								
I_A+	V_A+ = +5V		17	22		17	22	mA
I_A−	V_A− = −5V		19	24		19	24	mA
I_D+	V_D+ = +5V		0.5	1.0		0.5	1.0	mA
Power−Supply Rejection Ratio PSRR (250Hz)			100			100		dB
TEMPERATURE RANGE								
Operating Range		−40		+85	−40		+85	°C
Storage Range		−65		+150	−65		+150	°C

PIN CONFIGURATION



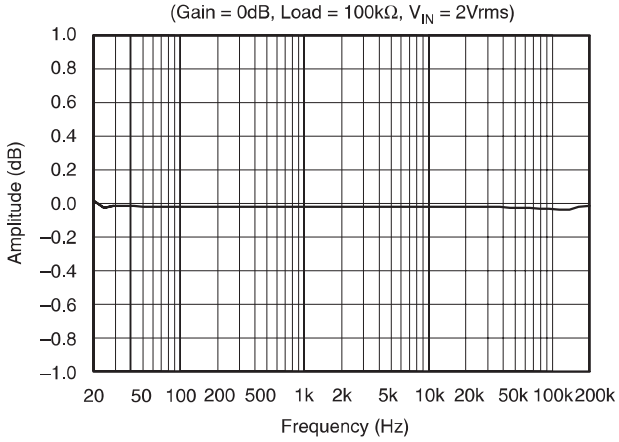
PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	$\overline{\text{MUTE}}$	Mute Control Input (Active LOW)
2	AGND_1	Analog Ground, Channel 1
3	A_{IN}_1	Analog Input, Channel 1
4	AGND_1	Analog Ground, Channel 1
5	A_{OUT}_1	Analog Output, Channel 1
6	V_A−	Analog Power Supply, −5V
7	V_A+	Analog Power Supply, +5V
8	A_{OUT}_3	Analog Output, Channel 3
9	AGND_3	Analog Ground, Channel 3
10	A_{IN}_3	Analog Input, Channel 3
11	AGND_3	Analog Ground, Channel 3
12	V_D+	Digital Power Supply, +5V
13	SDI	Serial Data Input
14	$\overline{\text{CS}}$	Chip Select Input
15	SCLK	Serial Clock Input
16	SDO	Serial Data Output
17	DGND	Digital Ground
18	AGND_4	Analog Ground, Channel 4
19	A_{IN}_4	Analog Input, Channel 4
20	AGND_4	Analog Ground, Channel 4
21	A_{OUT}_4	Analog Output, Channel 4
22	V_A+	Analog Power Supply, +5V
23	V_A−	Analog Power Supply, −5V
24	A_{OUT}_2	Analog Output, Channel 2
25	AGND_2	Analog Ground, Channel 2
26	A_{IN}_2	Analog Input, Channel 2
27	AGND_2	Analog Ground, Channel 2
28	ZCEN	Zero Crossing Enable (Active HIGH)

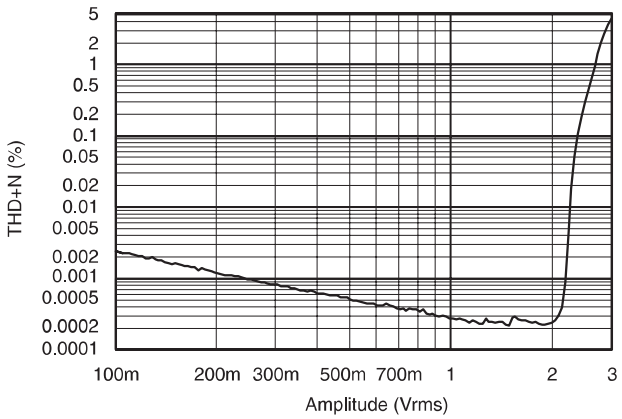
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_A+ = +5V, V_A− = −5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.
(NOTE: All plots taken with PGA4311 A−Grade.)

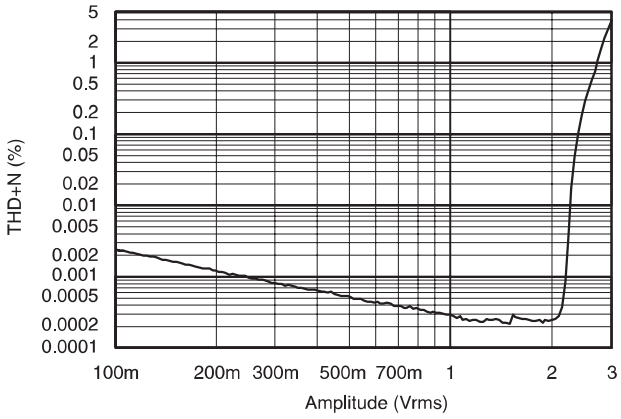
AMPLITUDE vs FREQUENCY
(Gain = 0dB, Load = 100kΩ, V_{IN} = 2Vrms)



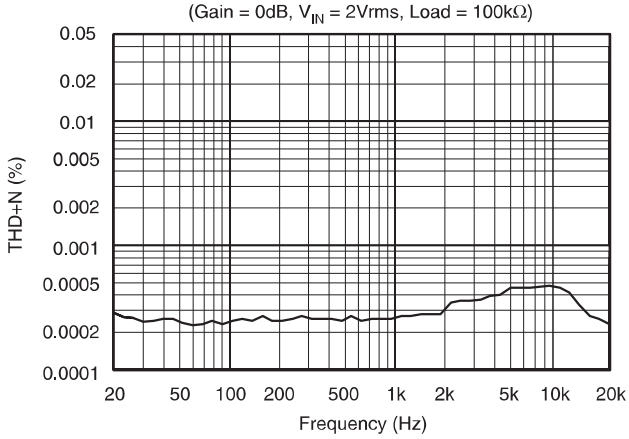
THD+N vs AMPLITUDE
(Gain = 0dB, Freq = 1kHz, Load = 100kΩ)



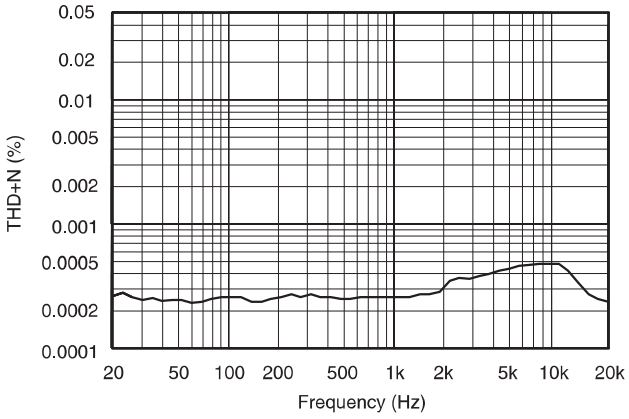
THD+N vs AMPLITUDE
(Gain = 0dB, Freq = 1kHz, Load = 600Ω)



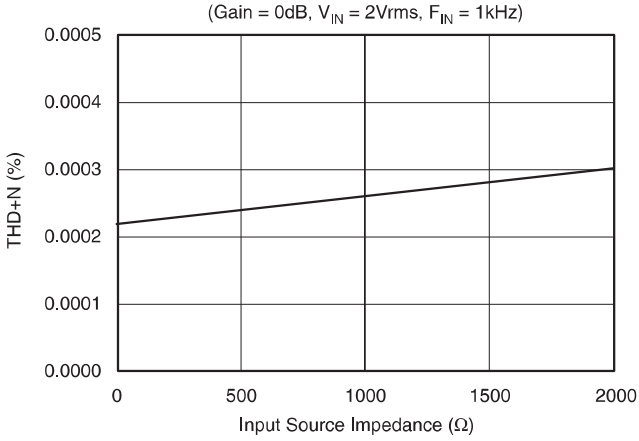
THD+N vs FREQUENCY
(Gain = 0dB, V_{IN} = 2Vrms, Load = 100kΩ)



THD+N vs FREQUENCY
(Gain = 0dB, V_{IN} = 2Vrms, Load = 600Ω)

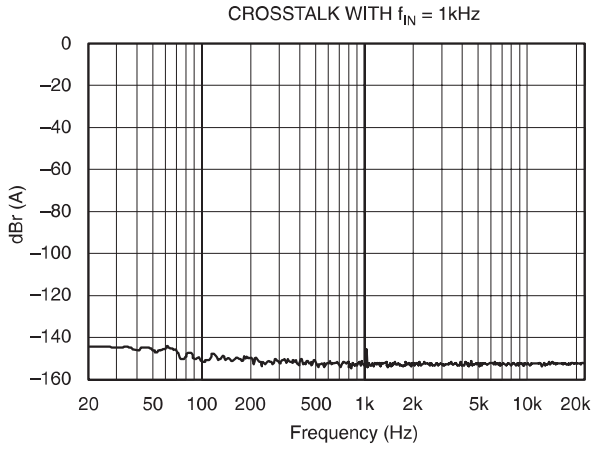


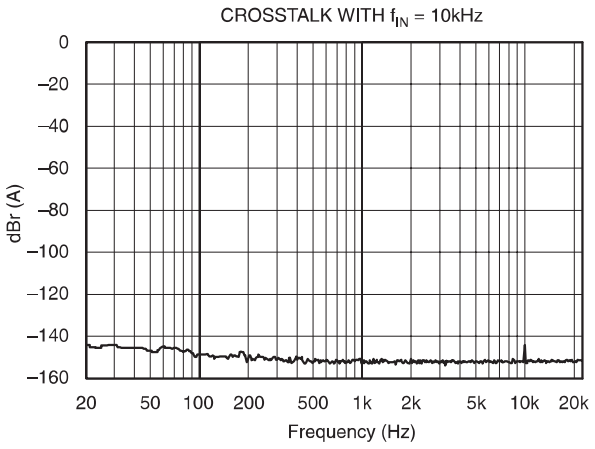
THD+N vs INPUT SOURCE IMPEDANCE
(Gain = 0dB, V_{IN} = 2Vrms, F_{IN} = 1kHz)

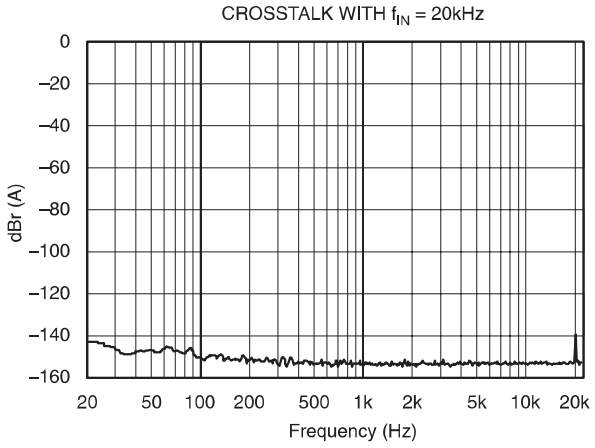


TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_A+ = +5V, V_A− = −5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.
(NOTE: All plots taken with PGA4311 A−Grade.)







GENERAL DESCRIPTION

The PGA4311 is a four-channel audio volume control. It may be used in a wide array of professional and consumer audio equipment. The PGA4311 is fabricated in a sub-micron CMOS process.

The heart of the PGA4311 is a resistor network, an analog switch array, and a high-performance op amp stage. The switches are used to select taps in the resistor network that, in turn, determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers. See Figure 1 for a functional block diagram of the PGA4311.

POWER−UP STATE

On power up, “power-up reset” is activated for about 100ms during which the circuit is in hardware $\overline{\text{MUTE}}$ state and all internal flip-flops are reset. At the end of this period, the offset calibration is initiated without any external signals. Once this has been completed, the gain byte value for all channels are set to 00_{HEX}, or the software $\overline{\text{MUTE}}$ condition. The gain will remain at this setting until the host controller programs new settings for for each channel via the serial control port.

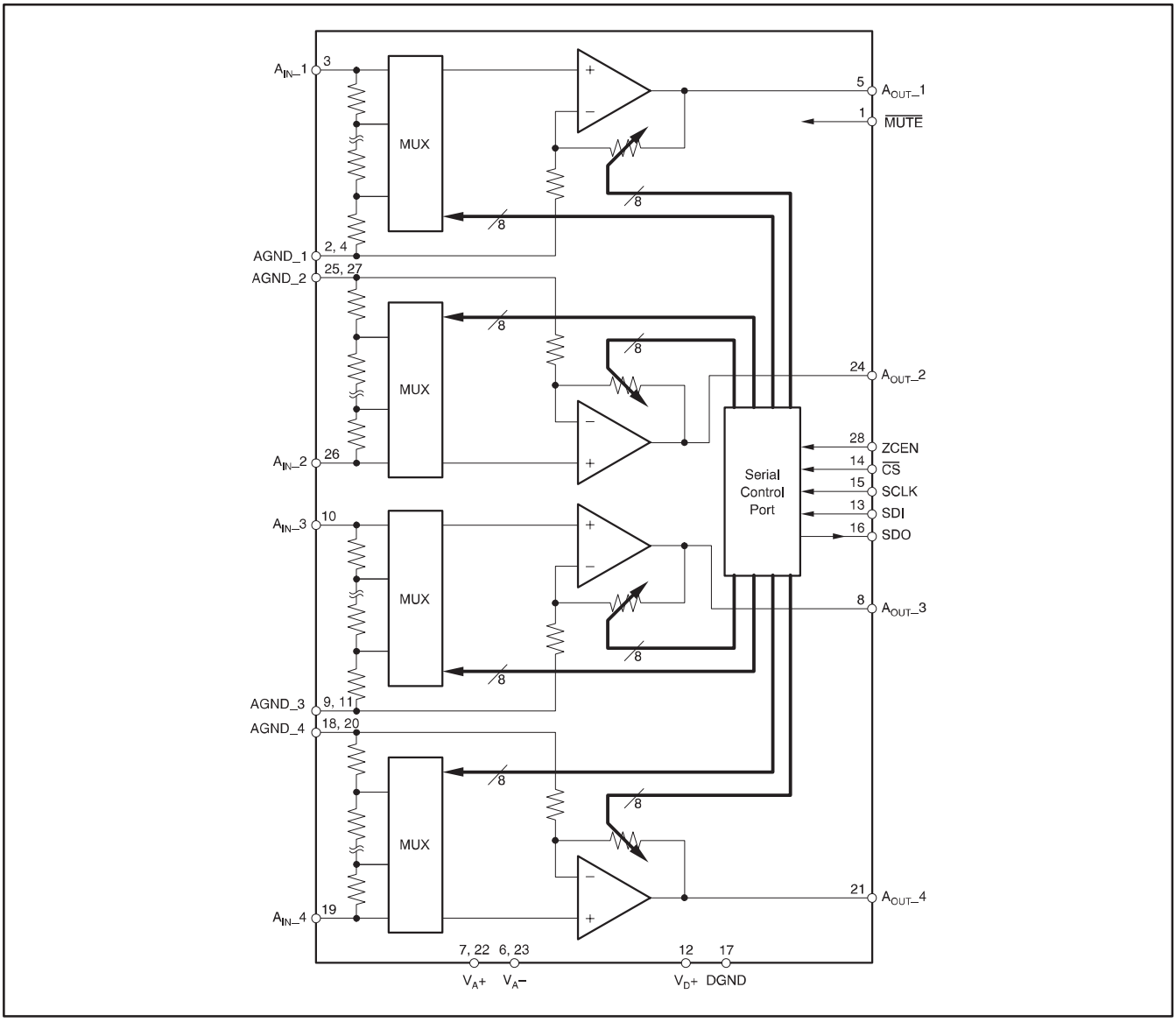


Figure 1. PGA4311 Block Diagram.

If during normal operation the power supply voltage drops below ±3.2V, the circuit enters a hardware $\overline{\text{MUTE}}$ state. A power-up sequence will be initiated if the power-supply voltage returns to greater than ±3.2V.

ANALOG INPUTS AND OUTPUTS

The PGA4311 includes four independent channels. Each channel has a corresponding input and output pin. The input and output pins are unbalanced, and referenced to analog ground.

The input and output pins may swing within 1.25V of the analog power supplies, V_A+ and V_A−. Given V_A+ = +5V and V_A− = −5V, the maximum input or output voltage range is 7.5Vp-p.

For optimal performance, it is best to drive the PGA4311 with a low source impedance. A source impedance of 600Ω or less is recommended. Source impedances up to 2kΩ will cause minimal degradation of THD+N. Please refer to the “THD+N vs Source Impedance” plot in the Typical Characteristics section of the datasheet.

SERIAL CONTROL PORT

The serial control port is utilized to program the gain settings for the PGA4311. The serial control port includes three input pins and one output pin. The inputs include $\overline{CS}$ (pin 14), SDI (pin 13), and SCLK (pin 15). The sole output pin is SDO (pin 16).

The $\overline{CS}$ pin functions as the chip select input. Data may be written to the PGA4311 only when $\overline{CS}$ is LOW. SDI is the serial data input pin. Control data is provided as a 32-bit word at the SDI pin, 8 bits each for each channel gain setting.

Data is formatted as MSB first, straight binary code. SCLK is the serial clock input. Data is clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and is used when daisy-chaining multiple PGA4311 devices. Daisy-chain operation is described in detail later in this section. SDO is a tri-state output, and assumes a high impedance state when $\overline{CS}$ is HIGH. Data appears at SDO on the falling edge of SCLK.

The protocol for the serial control port is shown in Figure 2. See Figure 3 for detailed timing specifications for the serial control port.

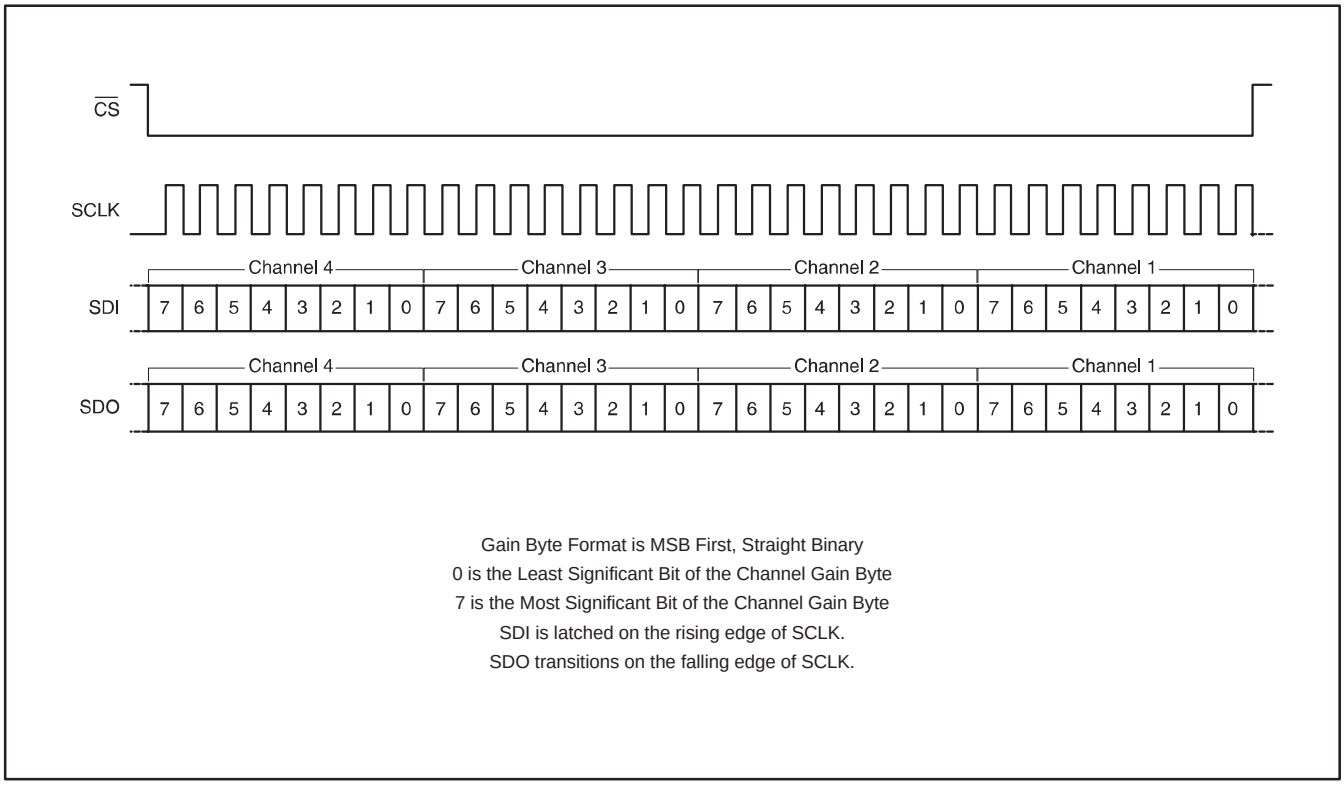


Figure 2. Serial Interface Protocol.

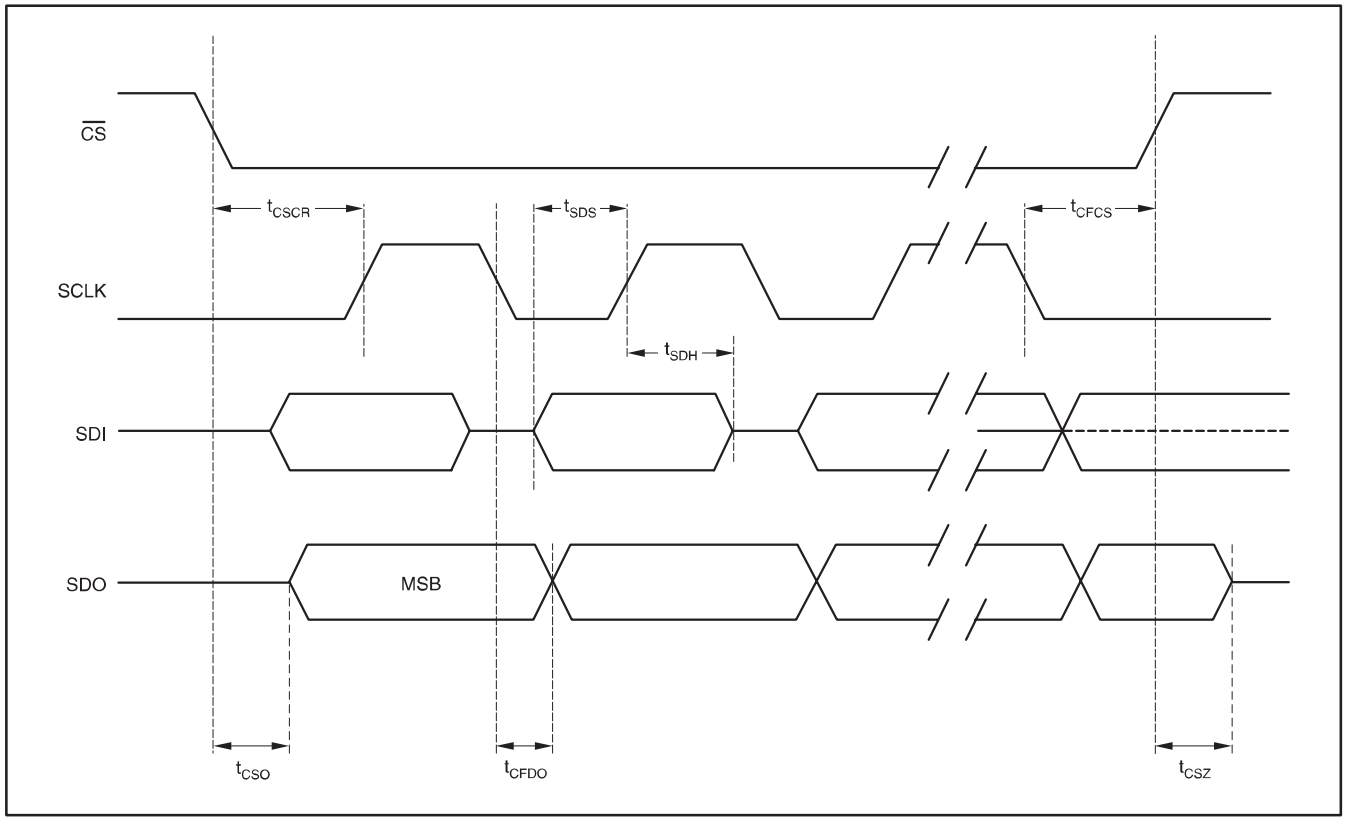


Figure 3. Serial Interface Timing Requirements.

GAIN SETTINGS

The gain for each channel is set by its corresponding 8-bit code, [7:0] (see Figure 2). The gain code data is straight binary format. If we let N equal the decimal equivalent of [7:0], then the following relationships exist for the gain settings:

For N = 0:

Mute Condition. The input multiplexer is connected to analog ground.

For N = 1 to 255:

Gain (dB) = 31.5 − [0.5 w (255 − N)]

This results in a gain range of +31.5dB (with N = 255) to −95.5dB (with N = 1).

Changes in gain setting may be made with or without zero crossing detection. The operation of the zero crossing detector and timeout circuitry is discussed later in this data sheet.

DAISY-CHAINING MULTIPLE PGA4311 DEVICES

In order to reduce the number of control signals required to support multiple PGA4311 devices on a printed circuit board, the serial control port supports daisy-chaining of multiple PGA4311 devices. Figure 4 shows the connection requirements for daisy-chain operation. This arrangement allows a 3-wire serial interface to control many PGA4311 devices.

As shown in Figure 4, the SDO pin from device #1 is connected to the SDI input of device #2, and is repeated for additional devices. This in turn forms a large shift register, in which gain data may be written for all PGA4311s connected to the serial bus. The length of the shift register is 32 • N bits, where N is equal to the number of PGA4311 devices included in the chain. The $\overline{CS}$ input must remain LOW for 32 • N SCLK periods, where N is the number of devices connected in the chain, in order to allow enough SCLK cycles to load all devices.

ZERO CROSSING DETECTION

The PGA4311 includes a zero crossing detection function that can provide for noise-free level transitions. The concept is to change gain settings on a zero crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input. When ZCEN is LOW, zero crossing detection is disabled. When ZCEN is HIGH, zero crossing detection will be enabled.

The zero crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting will not be implemented until either positive slope zero crossing is detected or a time-out period of 16ms has elapsed. In the case of a time-out, the new gain setting takes effect with no attempt to minimize audible artifacts.

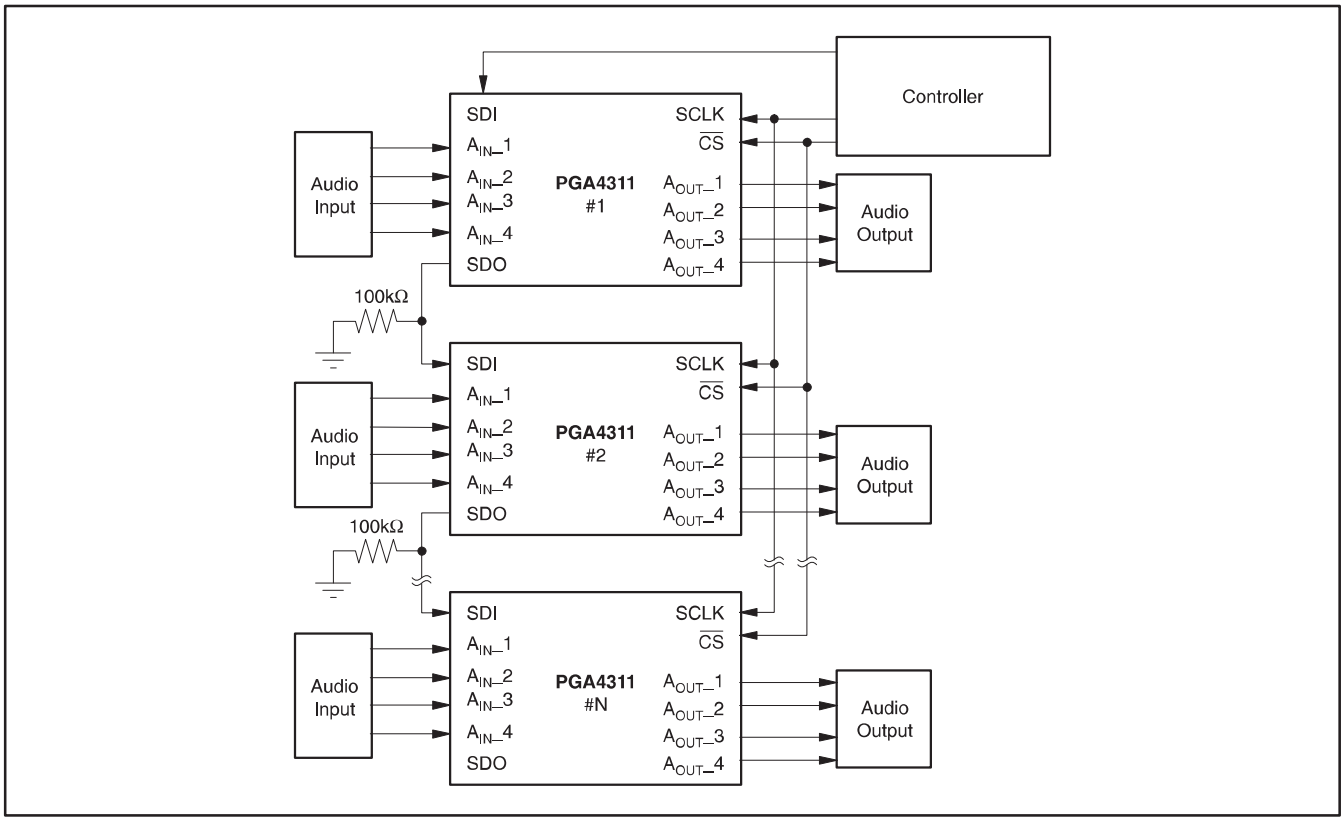


Figure 4. Daisy-Chaining Multiple PGA4311 Devices.

$\overline{\text{MUTE}}$ FUNCTION

Muting can be achieved by either hardware or software control. Hardware muting is accomplished via the $\overline{\text{MUTE}}$ input, and software muting by loading all zeroes into the volume control register.

$\overline{\text{MUTE}}$ disconnects the internal buffer amplifiers from the output pins and terminates the outputs with 10kΩ resistors to ground. The mute is activated with a zero crossing detection (independent of the zero cross enable status) or an 16ms time-out to eliminate any audible “clicks” or “pops”. $\overline{\text{MUTE}}$ also initiates an internal offset calibration.

A software mute is implemented by loading all zeroes into the volume control register. The internal amplifier is set to unity gain with the amplifier input connected to AGND.

APPLICATIONS INFORMATION

This section includes additional information that is pertinent to designing the PGA4311 into an end application.

RECOMMENDED CONNECTION DIAGRAM

Figure 5 depicts the recommended connections for the PGA4311. Power-supply bypass capacitors should be placed as close to the PGA4311 package as physically possible.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

It is recommended that the ground planes for the digital and analog sections of the PCB be separate from one another. The planes should be connected at a single point. See Figure 6 for the recommended PCB floor plan for the PGA4311.

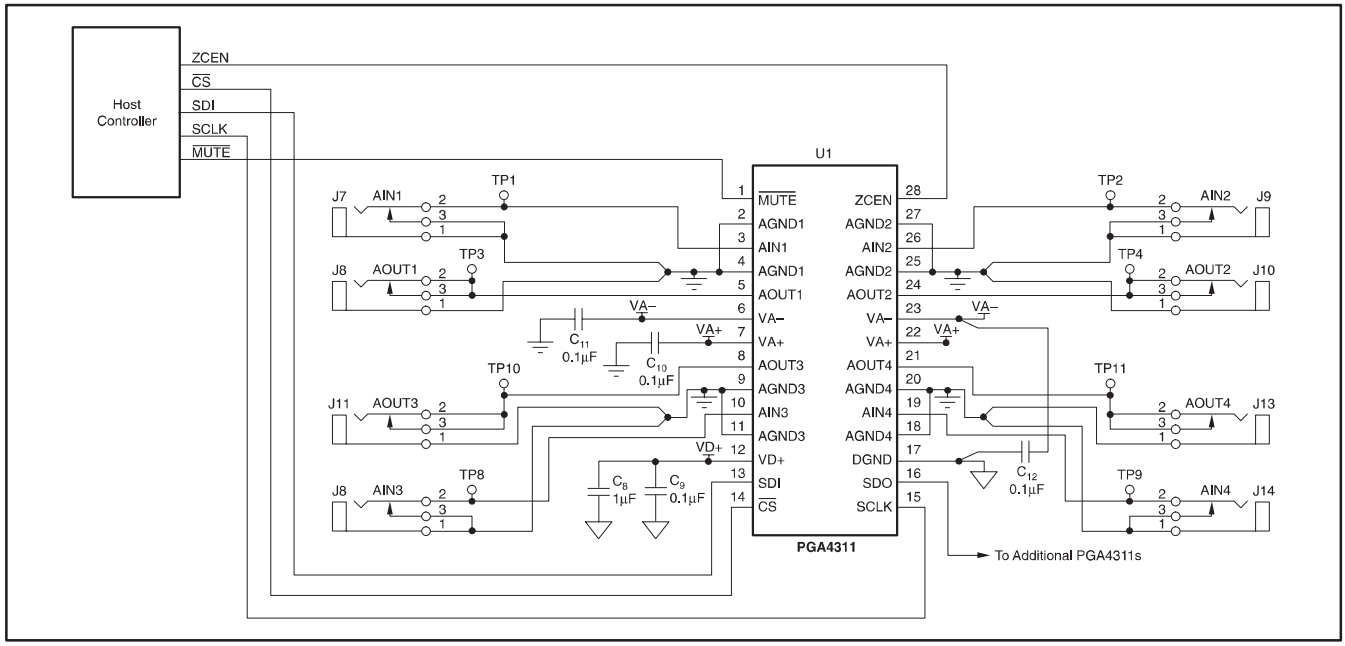


Figure 5. Recommended Connection Diagram.

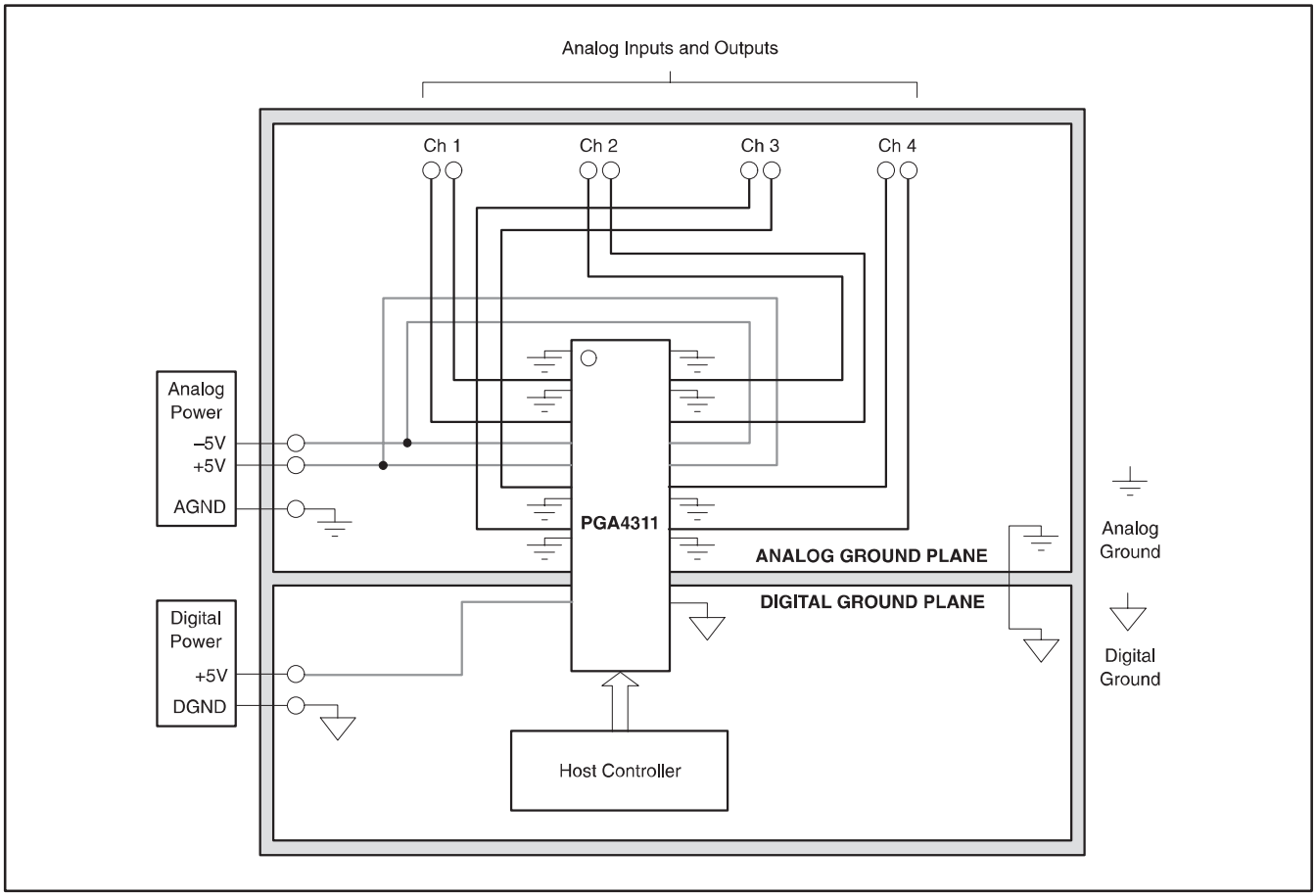


Figure 6. Typical PCB Layout Floor Plan.

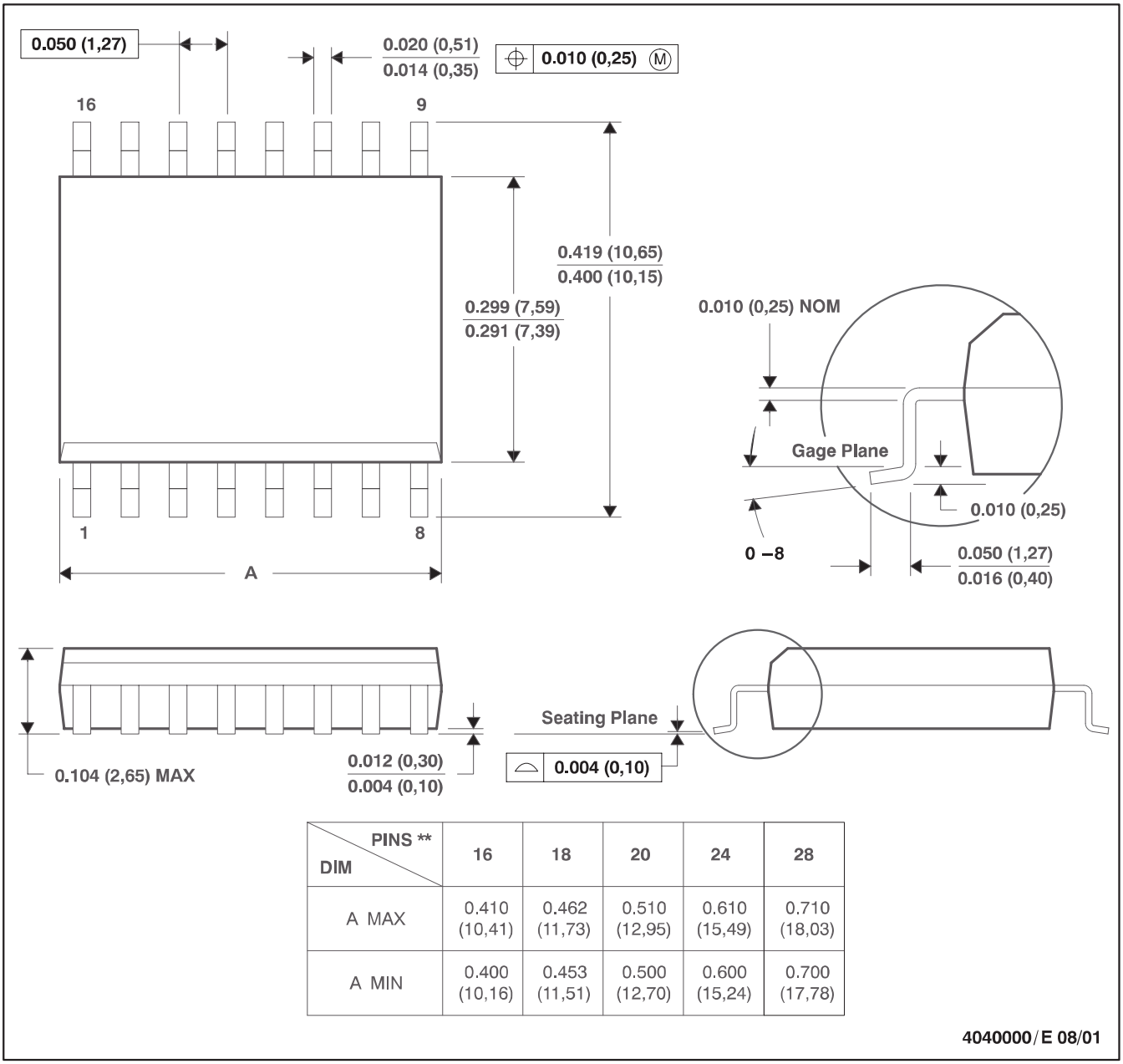
PACKAGE DRAWING

MSOI003E – JANUARY 1995 – REVISED SEPTEMBER 2001

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PGA4311U	ACTIVE	SOIC	DW	28	28	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA4311U/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA4311U/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA4311U2	PREVIEW	SOIC	DW	28	1	TBD	Call TI	Call TI
PGA4311UA	ACTIVE	SOIC	DW	28	28	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA4311UA/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA4311UA/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA4311UA1	PREVIEW	SOIC	DW	28	1	TBD	Call TI	Call TI
PGA4311UAG4	ACTIVE	SOIC	DW	28	28	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA4311UG4	ACTIVE	SOIC	DW	28	28	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

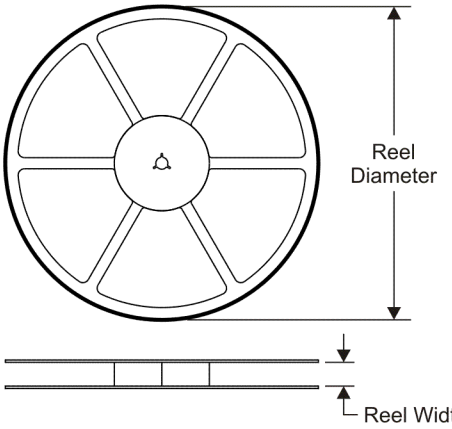
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

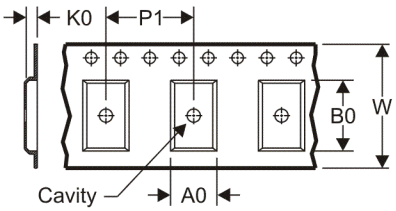
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

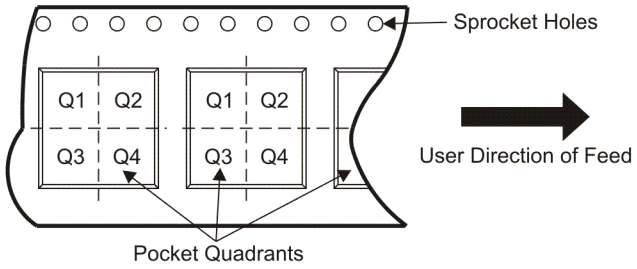


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

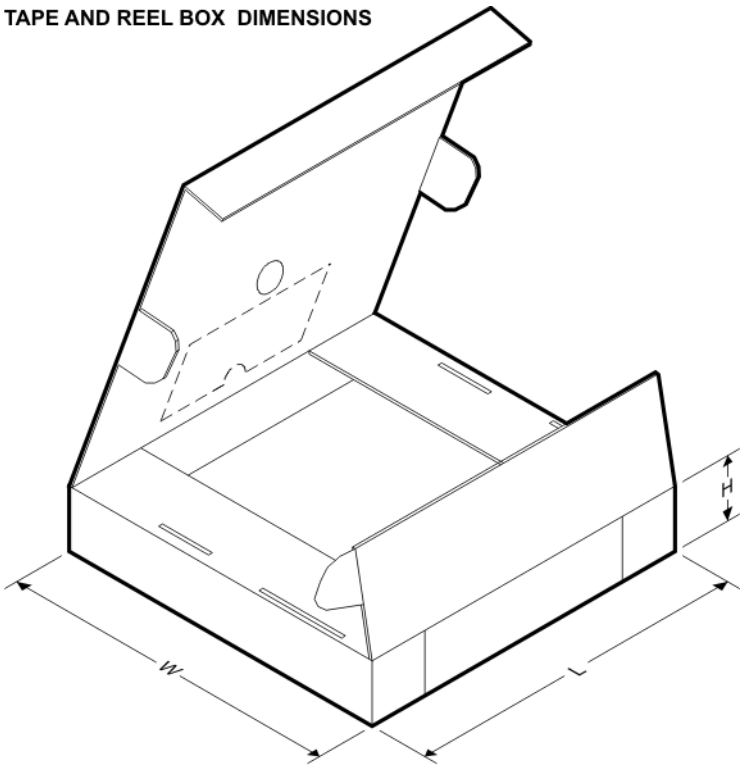
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA4311U/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
PGA4311UA/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA4311U/1K	SOIC	DW	28	1000	346.0	346.0	49.0
PGA4311UA/1K	SOIC	DW	28	1000	346.0	346.0	49.0

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