

PHB/PHD101NQ03LT

TrenchMOS™ logic level FET

Rev. 02 — 25 February 2003

Product data

1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHB101NQ03LT in SOT404 (D²-PAK)

PHD101NQ03LT in SOT428 (D-PAK).

2. Features

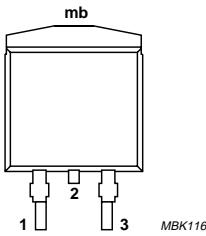
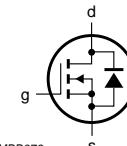
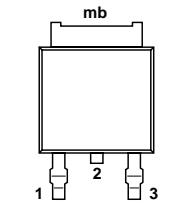
- Low gate charge
- Low on-state resistance.

3. Applications

- Optimized as a control FET in DC to DC convertors

4. Pinning information

Table 1: Pinning - SOT404, SOT428 simplified outline and symbol

| Pin | Description | Simplified outline | Symbol |
|-----|--|--|---|
| 1 | gate (g) | | |
| 2 | drain (d) | [1] | |
| 3 | source (s) | | |
| mb | mounting base, connected to drain (d) |  MBK116 |  MBB076 |
| | |  Top view MBK091 | |
| | | SOT404 (D²-PAK) | SOT428 (D-PAK) |

[1] It is not possible to make connection to pin 2 of the SOT404 and SOT428 packages.



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5. Quick reference data

Table 2: Quick reference data

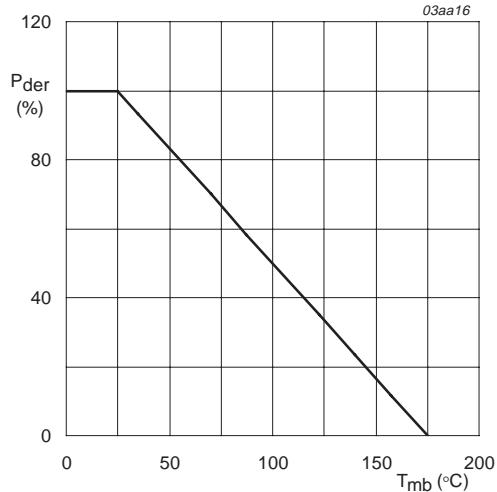
| Symbol | Parameter | Conditions | Typ | Max | Unit |
|------------|----------------------------------|--|-----|-----|------------------|
| V_{DS} | drain-source voltage (DC) | $25 \leq T_j \leq 175 \text{ }^\circ\text{C}$ | - | 30 | V |
| I_D | drain current (DC) | $T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V}$ | - | 75 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25 \text{ }^\circ\text{C}$ | - | 166 | W |
| T_j | junction temperature | | - | 175 | $^\circ\text{C}$ |
| R_{DSon} | drain-source on-state resistance | $T_j = 25 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}$ | 4.5 | 5.5 | $\text{m}\Omega$ |
| | | $T_j = 25 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}$ | 5.8 | 7.0 | $\text{m}\Omega$ |

6. Limiting values

Table 3: Limiting values

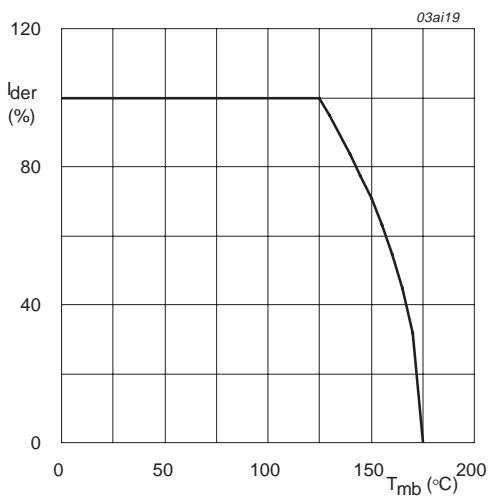
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|---|-----|----------|------------------|
| V_{DS} | drain-source voltage (DC) | $25 \leq T_j \leq 175 \text{ }^\circ\text{C}$ | - | 30 | V |
| V_{DGR} | drain-gate voltage (DC) | $25 \leq T_j \leq 175 \text{ }^\circ\text{C}; R_{GS} = 20 \text{ k}\Omega$ | - | 30 | V |
| V_{GS} | gate-source voltage (DC) | | - | ± 20 | V |
| V_{GSM} | gate-source voltage | $t_p \leq 50 \mu\text{s}; \text{ pulsed; duty cycle 25\%}; T_j \leq 150 \text{ }^\circ\text{C}$ | - | ± 25 | V |
| I_D | drain current (DC) | $T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V}; \text{Figure 2 and 3}$ | - | 75 | A |
| | | $T_{mb} = 100 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V}; \text{Figure 2}$ | - | 75 | A |
| I_{DM} | peak drain current | $T_{mb} = 25 \text{ }^\circ\text{C}; \text{ pulsed; } t_p \leq 10 \mu\text{s}; \text{Figure 3}$ | - | 240 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25 \text{ }^\circ\text{C}; \text{Figure 1}$ | - | 166 | W |
| T_{stg} | storage temperature | | -55 | +175 | $^\circ\text{C}$ |
| T_j | junction temperature | | -55 | +175 | $^\circ\text{C}$ |
| Source-drain diode | | | | | |
| I_S | source (diode forward) current (DC) | $T_{mb} = 25 \text{ }^\circ\text{C}$ | - | 75 | A |
| I_{SM} | peak source (diode forward) current | $T_{mb} = 25 \text{ }^\circ\text{C}; \text{ pulsed; } t_p \leq 10 \mu\text{s}$ | - | 240 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D = 43 \text{ A}$; $t_p = 0.19 \text{ ms}$; $V_{DD} \leq 15 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; starting $T_j = 25 \text{ }^\circ\text{C}$ | - | 185 | mJ |



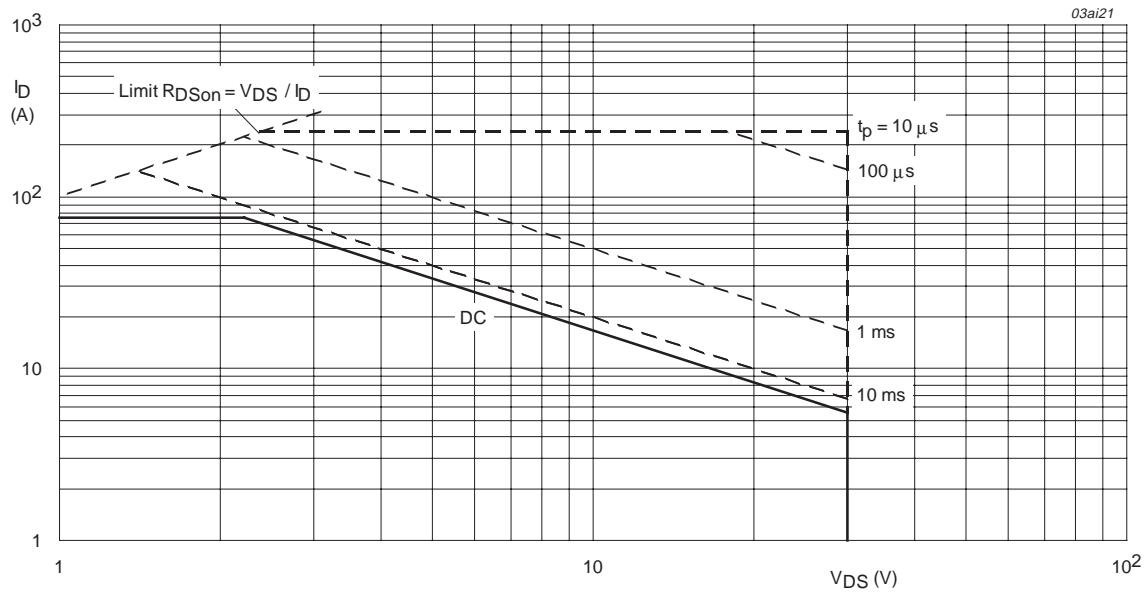
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}C)} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10V$.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---|---|-----|-----|-----|------|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 0.9 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | | | | | |
| | SOT428 | mounted on a PCB; SOT428 minimum footprint; vertical in still air | - | 75 | - | K/W |
| | SOT404 and SOT428 | mounted on a PCB; SOT404 minimum footprint; vertical in still air | - | 50 | - | K/W |

7.1 Transient thermal impedance

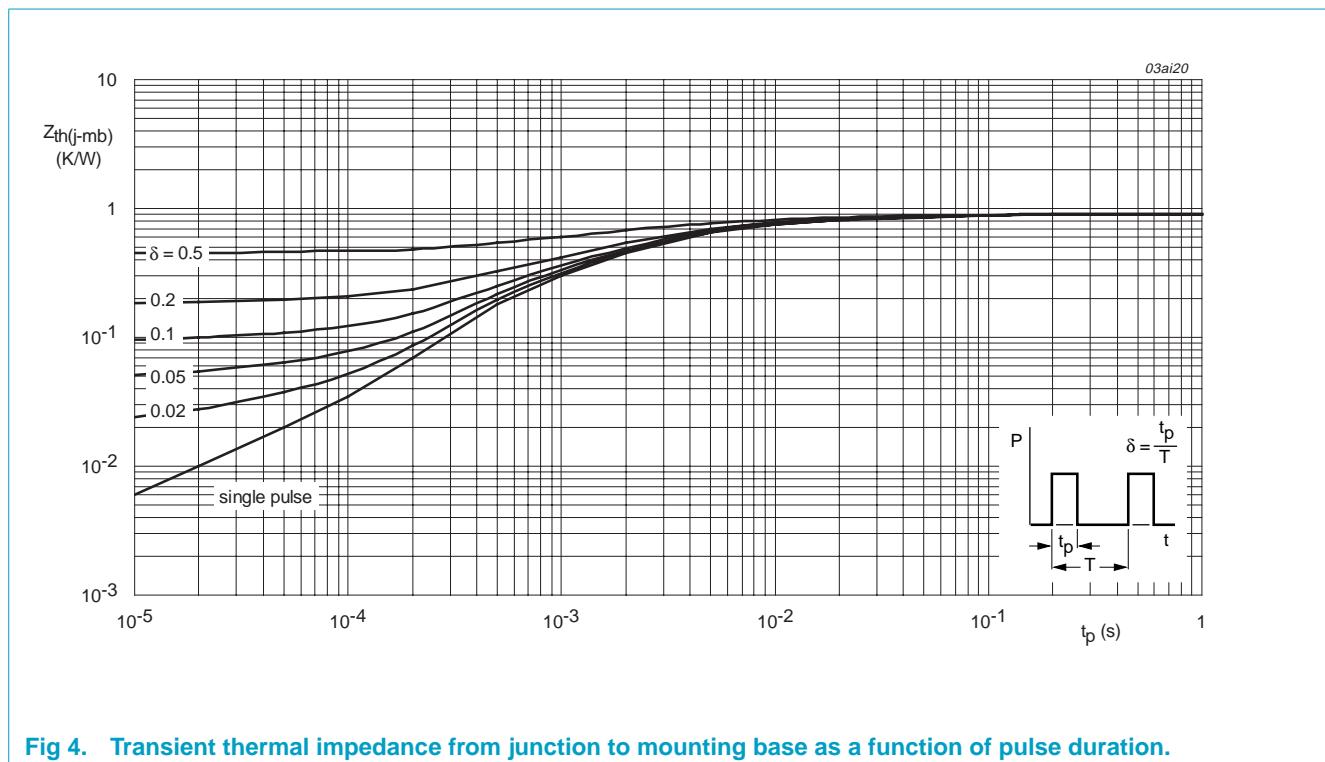


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics $T_j = 25^\circ\text{C}$ unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--------------------------------------|---|-----|------|------|------------------|
| Static characteristics | | | | | | |
| $V_{(\text{BR})\text{DSS}}$ | drain-source breakdown voltage | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}$ | | | | |
| | | $T_j = 25^\circ\text{C}$ | 30 | - | - | V |
| | | $T_j = -55^\circ\text{C}$ | 27 | - | - | V |
| $V_{GS(\text{th})}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$; Figure 9 | | | | |
| | | $T_j = 25^\circ\text{C}$ | 1 | 1.9 | 2.5 | V |
| | | $T_j = 175^\circ\text{C}$ | 0.6 | - | - | V |
| | | $T_j = -55^\circ\text{C}$ | - | - | 2.9 | V |
| I_{DSS} | drain-source leakage current | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}$ | | | | |
| | | $T_j = 25^\circ\text{C}$ | - | 0.05 | 1 | μA |
| | | $T_j = 175^\circ\text{C}$ | - | - | 500 | μA |
| I_{GSS} | gate-source leakage current | $V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$ | - | 10 | 100 | nA |
| $R_{DS\text{on}}$ | drain-source on-state resistance | $V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}$; Figure 7 and 8 | | | | |
| | | $T_j = 25^\circ\text{C}$ | - | 5.8 | 7 | $\text{m}\Omega$ |
| | | $T_j = 175^\circ\text{C}$ | - | 10.5 | 12.6 | $\text{m}\Omega$ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}$; Figure 7 | | | | |
| | | $T_j = 25^\circ\text{C}$ | - | 4.5 | 5.5 | $\text{m}\Omega$ |
| Dynamic characteristics | | | | | | |
| $Q_{g(\text{tot})}$ | total gate charge | $I_D = 50 \text{ A}; V_{DD} = 15 \text{ V}; V_{GS} = 5 \text{ V}$; Figure 13 | - | 23 | - | nC |
| Q_{gs} | gate-source charge | | - | 10.5 | - | nC |
| Q_{gd} | gate-drain (Miller) charge | | - | 8 | - | nC |
| C_{iss} | input capacitance | $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$; Figure 11 | - | 2180 | - | pF |
| C_{oss} | output capacitance | | - | 600 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 225 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD} = 15 \text{ V}; I_D = 25 \text{ A}; V_{GS} = 4.5 \text{ V}$ | - | 23 | - | ns |
| t_r | rise time | $R_G = 5.6 \Omega$; resistive load | - | 90 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 37 | - | ns |
| t_f | fall time | | - | 33 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain (diode forward) voltage | $I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}$; Figure 12 | - | 0.85 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$ | - | 37 | - | ns |
| Q_r | recovered charge | | - | 33 | - | nC |

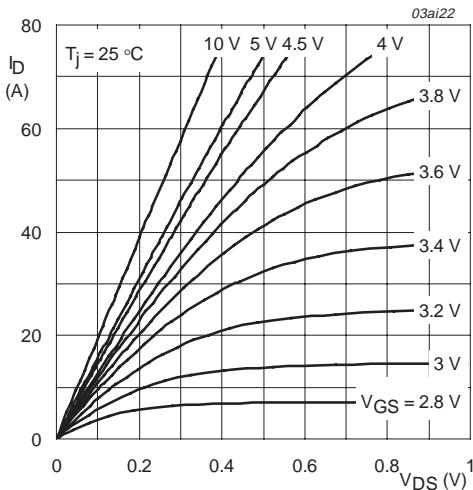


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.

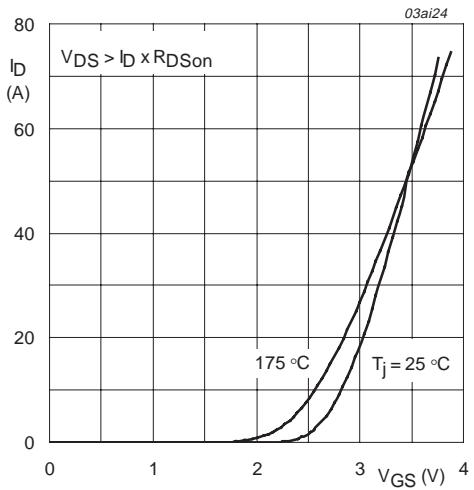


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.

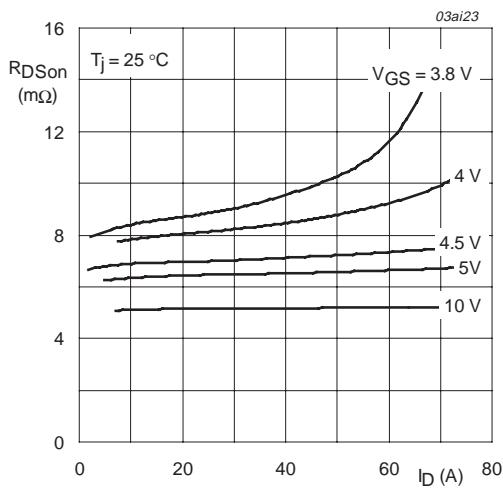


Fig 7. Drain-source on-state resistance as a function of drain current; typical values.

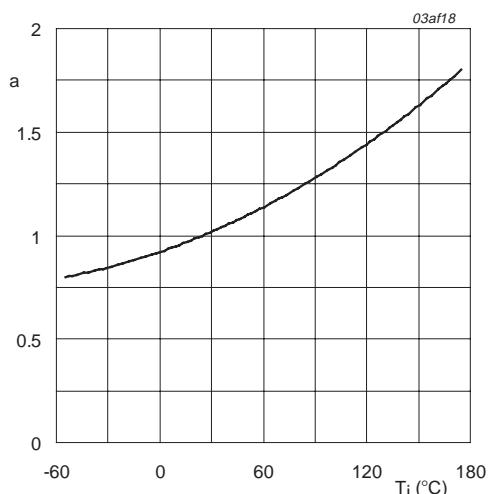
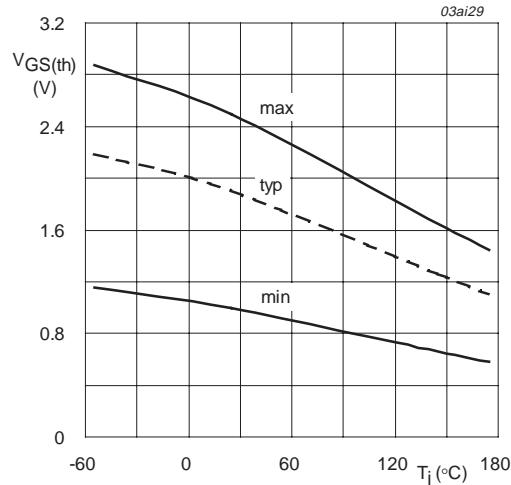
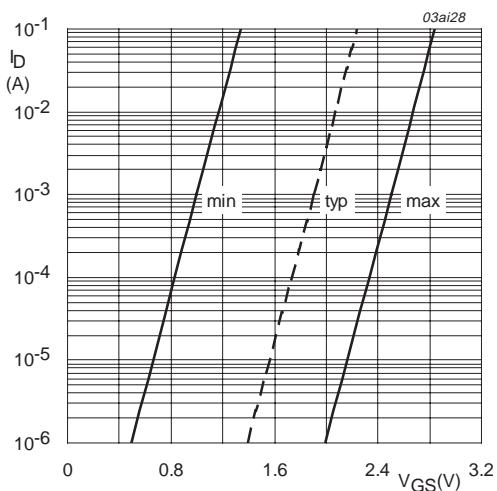


Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



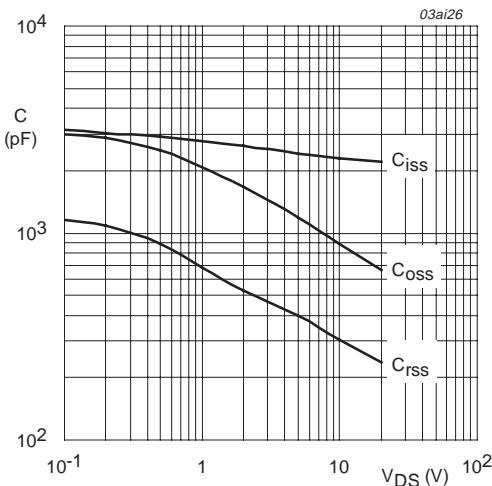
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



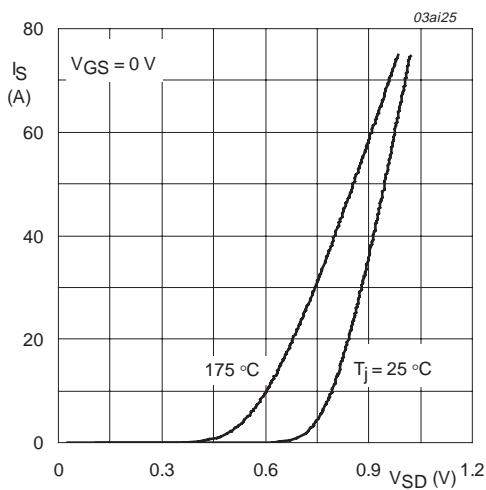
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



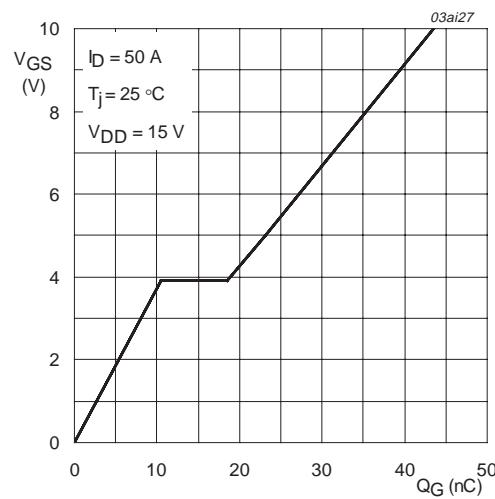
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 175°C ; $V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



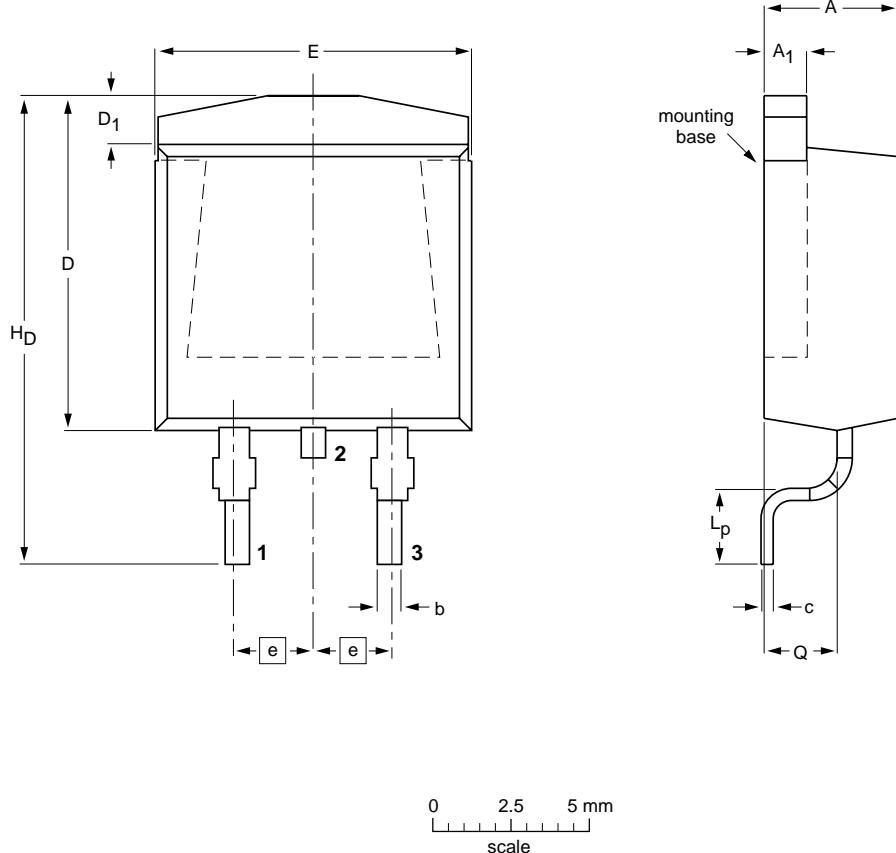
$I_D = 50 \text{ A}; V_{DD} = 15 \text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ | b | c | D max. | D ₁ | E | e | L _p | H _D | Q |
|------|--------------|----------------|--------------|--------------|--------|----------------|---------------|------|----------------|----------------|--------------|
| mm | 4.50 4.10 | 1.40 1.27 | 0.85 0.60 | 0.64 0.46 | 11 | 1.60 1.20 | 10.30 9.70 | 2.54 | 2.90 2.10 | 15.80 14.80 | 2.60 2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT404 | | | | | | 99-06-25 01-02-12 |

Fig 14. SOT404 (D²-PAK)

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

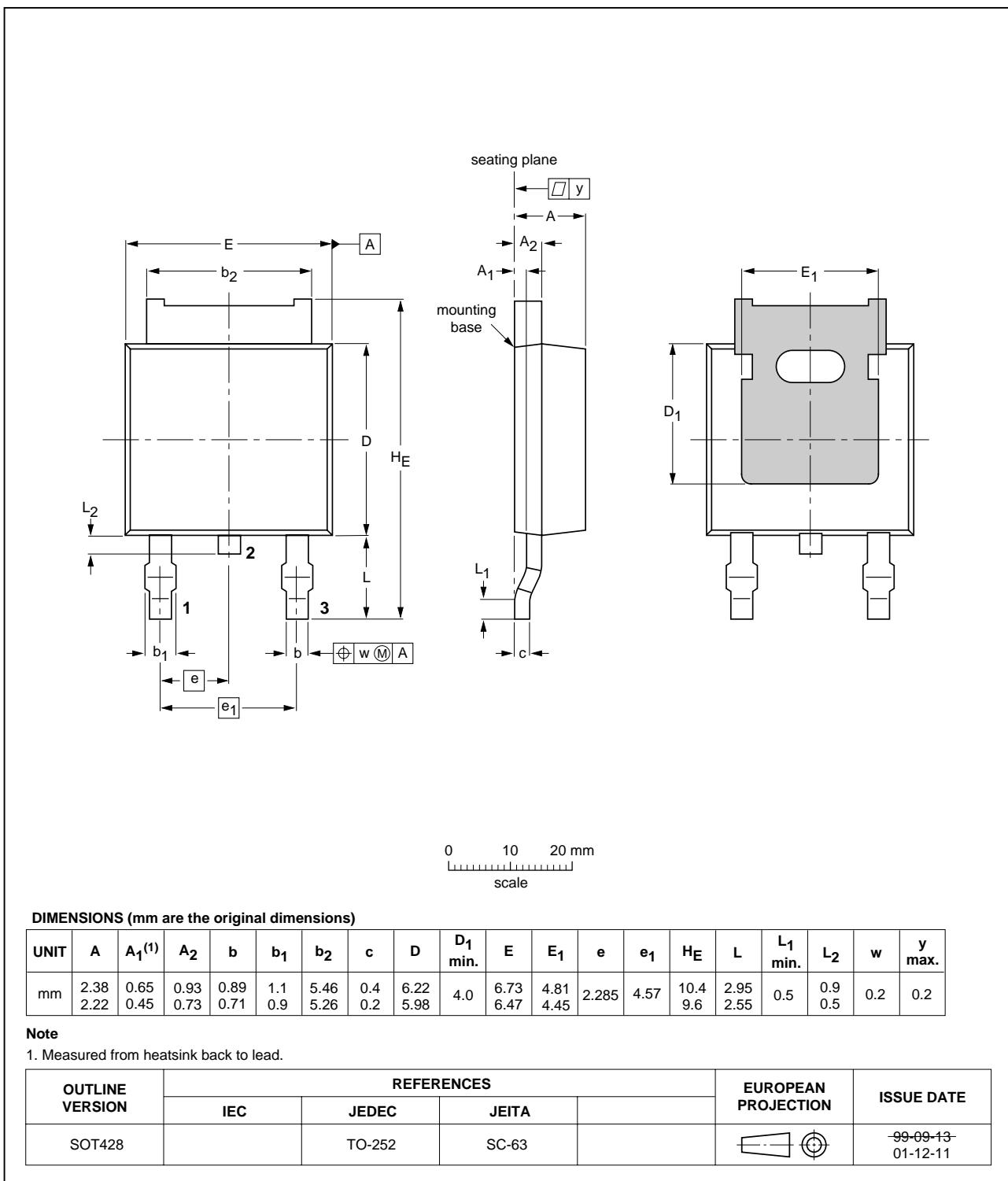


Fig 15. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

| Rev | Date | CPCN | Description |
|-----|----------|------|---|
| 02 | 20030225 | - | Product data (9397 750 10929) Modifications: <ul style="list-style-type: none">• Removal of PHP101NQ03LT (Now in separate data sheet).• Section 7 “Thermal characteristics” Clarification of thermal resistance table.• Graphics updated to latest standard. |
| 01 | 20020220 | - | Product data (9397 750 09307); initial version |

11. Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2][3]} | Definition |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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