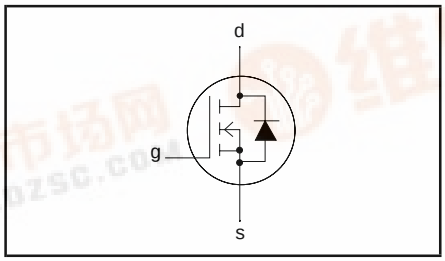
# N-channel TrenchMOS™ transistor Logic level FET

# PHB11N03LT, PHD11N03LT

## FEATURES

- **'Trench'** technology
- Low on-state resistance
- Fast switching
- Logic level compatible

## SYMBOL




## QUICK REFERENCE DATA

$V_{DSS}$ = 30 V

$I_D$ = 10.5 A

$R_{DS(ON)} \leq 150$ mΩ ($V_{GS}$ = 5 V)

$R_{DS(ON)} \leq 130$ mΩ ($V_{GS}$ = 10 V)

## GENERAL DESCRIPTION

N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using '**trench**' technology.

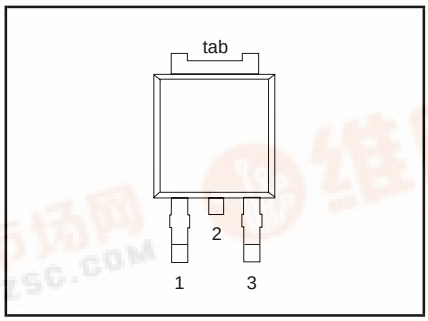
**Applications:-**
- d.c. to d.c. converters
- switched mode power supplies

The PHB11N03LT is supplied in the SOT404 ($D^2$PAK) surface mounting package.
The PHD11N03LT is supplied in the SOT428 (DPAK) surface mounting package.

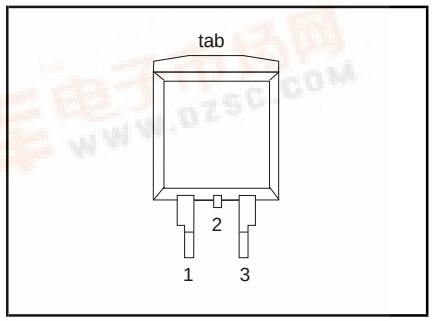
## PINNING

| PIN | DESCRIPTION |
|---|---|
| 1 | gate |
| 2 | drain [1] |
| 3 | source |
| tab | drain |

## SOT428 (DPAK)




## SOT404 ($D^2$PAK)




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-source voltage | $T_j$ = 25 ˚C to 175˚C | - | 30 | V |
| $V_{DGR}$ | Drain-gate voltage | $T_j$ = 25 ˚C to 175˚C; $R_{GS}$ = 20 kΩ | - | 30 | V |
| $V_{GS}$ | Gate-source voltage | | - | ± 15 | V |
| $V_{GSM}$ | Pulsed gate-source voltage | | - | ± 20 | V |
| $I_D$ | Continuous drain current | $T_{mb}$ = 25 ˚C | - | 10.3 | A |
| | | $T_{mb}$ = 100 ˚C | - | 7.3 | A |
| $I_{DM}$ | Pulsed drain current | $T_{mb}$ = 25 ˚C | - | 41 | A |
| $P_D$ | Total power dissipation | $T_{mb}$ = 25 ˚C | - | 33 | W |
| $T_j$, $T_{stg}$ | Operating junction and storage temperature | | - 55 | 175 | ˚C |

1 It is not possible to make contact to pin 2 of the SOT404 or SOT428 package

## AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $E_{AS}$ | Non-repetitive avalanche energy | Unclamped inductive load, $I_{AS}$ = 3.3 A; $t_p$ = 220 μs; $T_j$ prior to avalanche = 25˚C; $V_{DD} \leq$ 15 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; refer to fig:15 | - | 25 | mJ |
| $I_{AS}$ | Peak non-repetitive avalanche current | | - | 10.3 | A |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | 4.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | SOT428 and SOT404 package, pcb mounted, minimum footprint | 50 | - | K/W |

## ELECTRICAL CHARACTERISTICS

$T_j$= 25˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 0.25 mA; | 30 | - | - | V |
| | | $T_j$ = -55˚C | 26 | - | - | V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$; $I_D$ = 1 mA | 1.0 | 1.5 | 2.0 | V |
| | | $T_j$ = 175˚C | 0.5 | - | - | V |
| | | $T_j$ = -55˚C | - | - | 2.3 | V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 5.5 A | - | 100 | 130 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 5.5 A | - | 120 | 150 | mΩ |
| | | $T_j$ = 175˚C | - | 250 | 315 | mΩ |
| $g_{fs}$ | Forward transconductance | $V_{DS}$ = 25 V; $I_D$ = 5.5 A | 4 | 7 | - | S |
| $I_{GSS}$ | Gate source leakage current | $V_{GS}$ = ±5 V; $V_{DS}$ = 0 V | - | 10 | 100 | nA |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; | - | 0.05 | 10 | μA |
| | | $T_j$ = 175˚C | - | - | 500 | μA |
| $Q_{g(tot)}$ | Total gate charge | $I_D$ = 10 A; $V_{DD}$ = 15 V; $V_{GS}$ = 5 V | - | 3.8 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 1.2 | - | nC |
| $Q_{gd}$ | Gate-drain (Miller) charge | | - | 1.7 | - | nC |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD}$ = 30 V; $R_D$ = 2.7 Ω; | - | 6 | 16 | ns |
| $t_r$ | Turn-on rise time | $R_G$ = 10 Ω; $V_{GS}$ = 5 V | - | 64 | 80 | ns |
| $t_{d\ off}$ | Turn-off delay time | Resistive load | - | 20 | 30 | ns |
| $t_f$ | Turn-off fall time | | - | 26 | 40 | ns |
| $L_d$ | Internal drain inductance | Measured from tab to centre of die | - | 3.5 | - | nH |
| $L_d$ | Internal drain inductance | Measured from drain lead to centre of die (SOT78 package only) | - | 4.5 | - | nH |
| $L_s$ | Internal source inductance | Measured from source lead to source bond pad | - | 7.5 | - | nH |
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz | - | 250 | 330 | pF |
| $C_{oss}$ | Output capacitance | | - | 55 | 75 | pF |
| $C_{rss}$ | Feedback capacitance | | - | 42 | 55 | pF |

## REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j$ = 25˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous source current (body diode) | | - | - | 10.3 | A |
| $I_{SM}$ | Pulsed source current (body diode) | | - | - | 41 | A |
| $V_{SD}$ | Diode forward voltage | $I_F$ = 10 A; $V_{GS}$ = 0 V | - | 1.15 | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_F$ = 10 A; -d$I_F$/dt = 100 A/µs; | - | 35 | - | ns |
| $Q_{rr}$ | Reverse recovery charge | $V_{GS}$ = 0 V; $V_R$ = 30 V | - | 55 | - | nC |

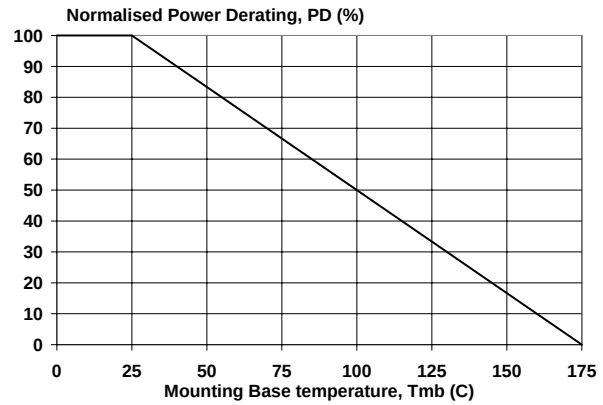



*Fig.1. Normalised power dissipation.*
*PD% = 100·$P_D$/$P_{D\ 25\ ^\circ C}$ = f($T_{mb}$)*

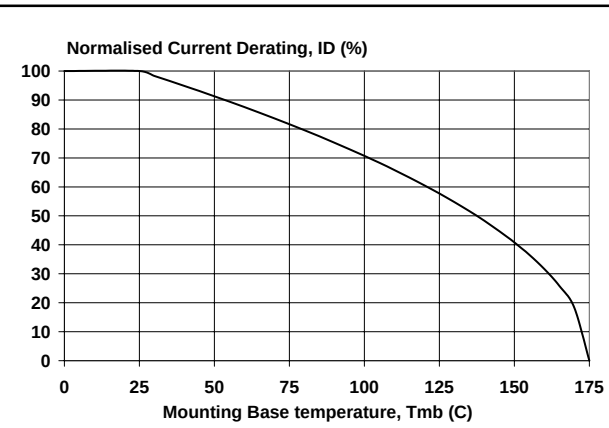



*Fig.2. Normalised continuous drain current.*
*ID% = 100·$I_D$/$I_{D\ 25\ ^\circ C}$ = f($T_{mb}$); conditions: $V_{GS} \geq 5$ V*

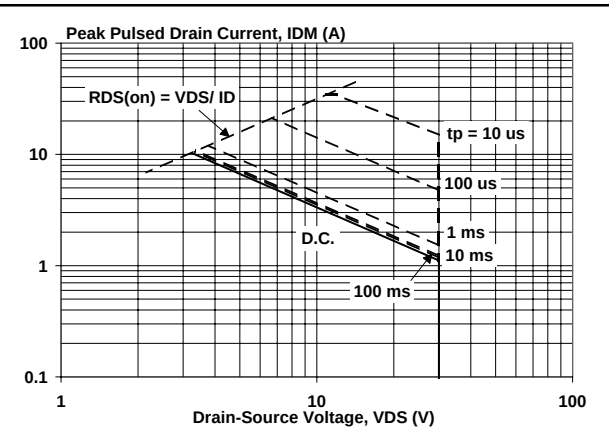



*Fig.3. Safe operating area. $T_{mb}$ = 25 ˚C*
*$I_D$ & $I_{DM}$ = f($V_{DS}$); $I_{DM}$ single pulse; parameter $t_p$*

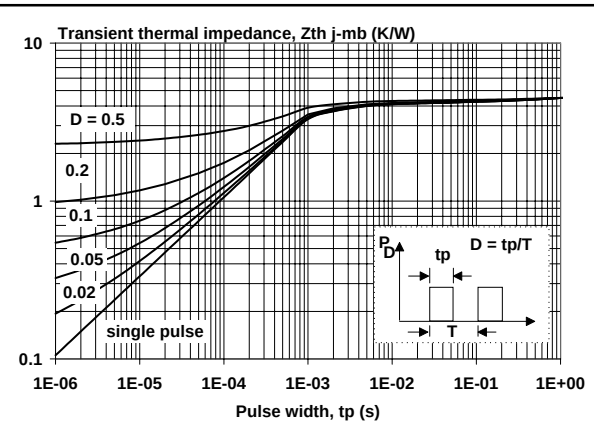



*Fig.4. Transient thermal impedance.*
*$Z_{th\ j\text{-}mb}$ = f(t); parameter D = $t_p$/T*

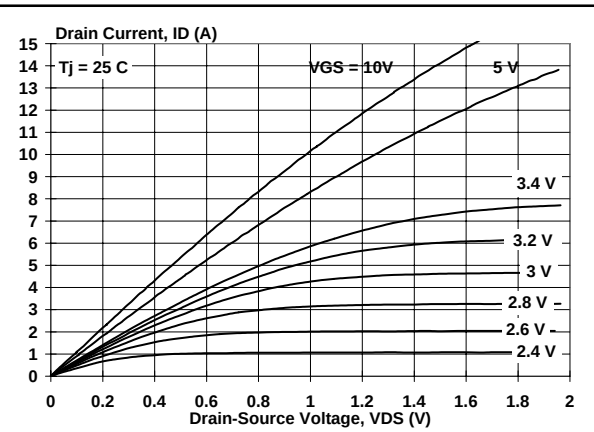



*Fig.5. Typical output characteristics, $T_j$ = 25 ˚C.*
*$I_D$ = f($V_{DS}$)*

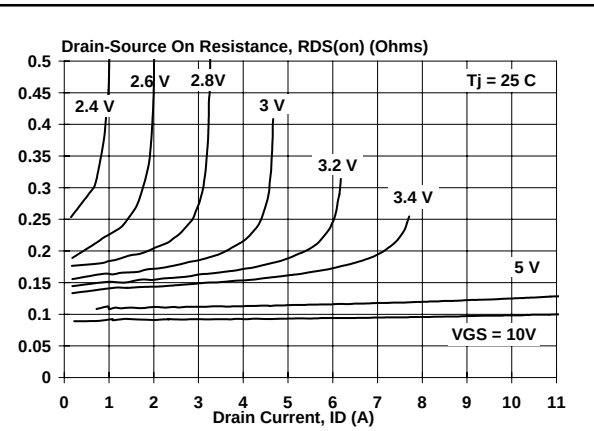



*Fig.6. Typical on-state resistance, $T_j$ = 25 ˚C.*
*$R_{DS(ON)}$ = f($I_D$)*

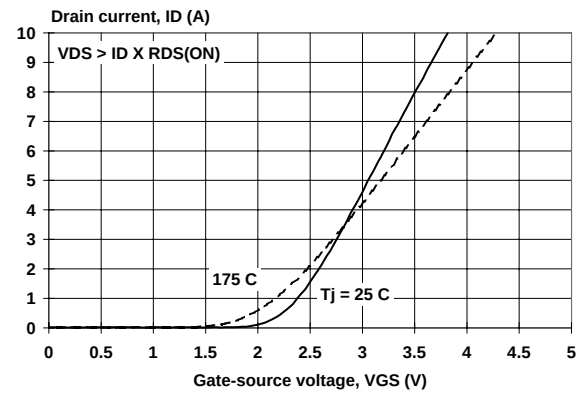



*Fig.7. Typical transfer characteristics.*
*$I_D = f(V_{GS})$*

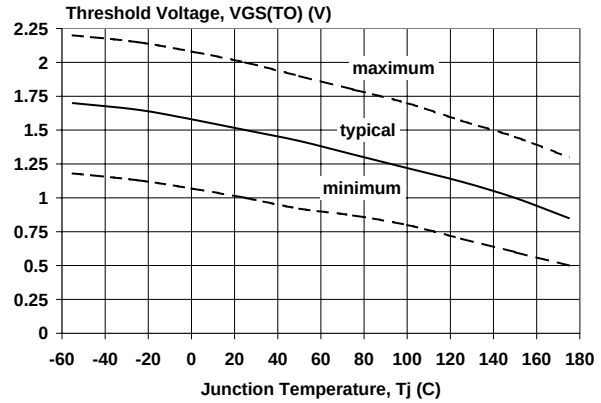



*Fig.10. Gate threshold voltage.*
*$V_{GS(TO)} = f(T_j)$; conditions: $I_D$ = 1 mA; $V_{DS} = V_{GS}$*

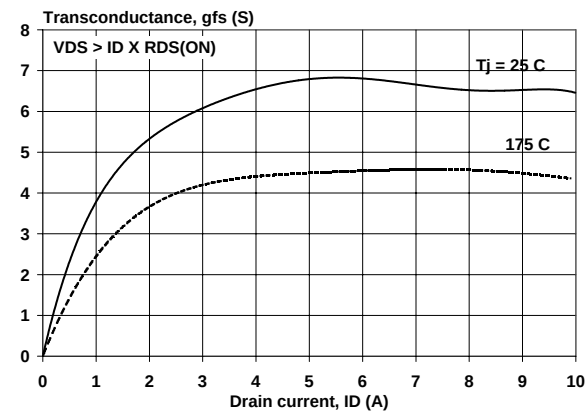



*Fig.8. Typical transconductance, $T_j$ = 25 ˚C.*
*$g_{fs} = f(I_D)$*

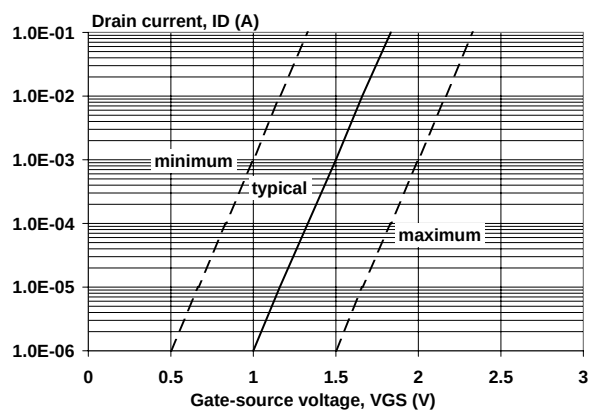



*Fig.11. Sub-threshold drain current.*
*$I_D = f(V_{GS})$; conditions: $T_j$ = 25 ˚C; $V_{DS} = V_{GS}$*

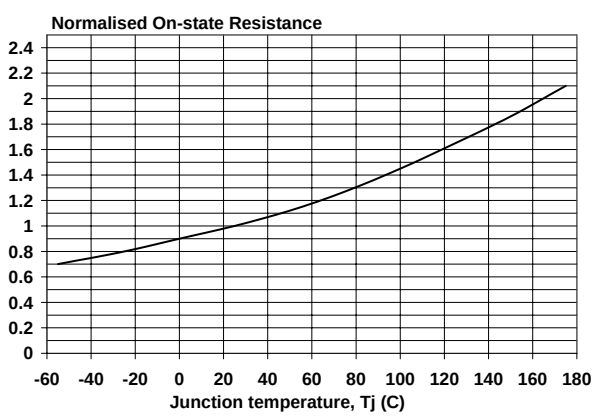



*Fig.9. Normalised drain-source on-state resistance.*
*$R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$*

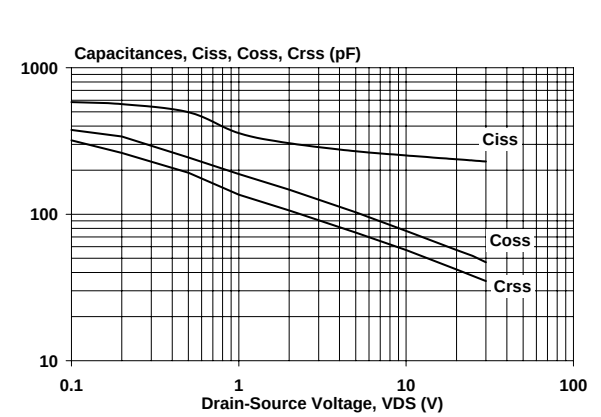



*Fig.12. Typical capacitances, $C_{iss}$, $C_{oss}$, $C_{rss}$.*
*$C = f(V_{DS})$; conditions: $V_{GS}$ = 0 V; f = 1 MHz*

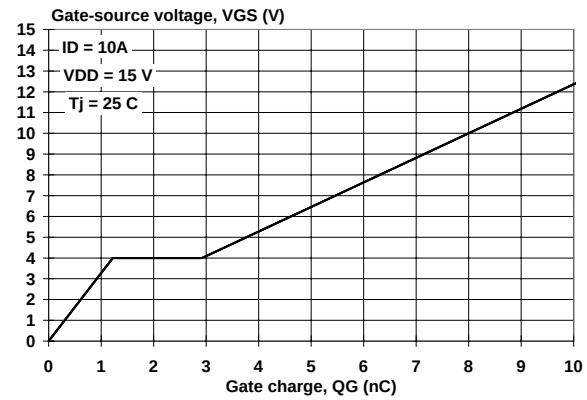



*Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$*

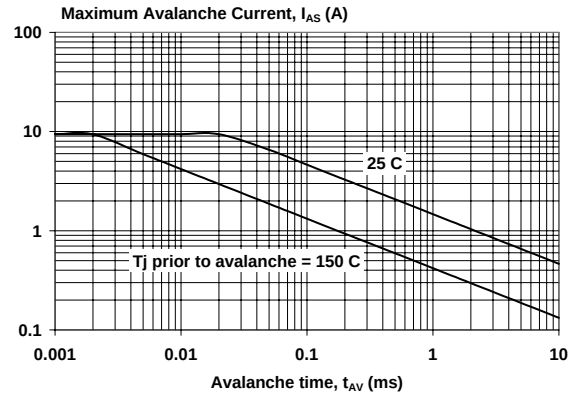



*Fig.15. Maximum permissible non-repetitive avalanche current ($I_{AS}$) versus avalanche time ($t_{AV}$); unclamped inductive load*

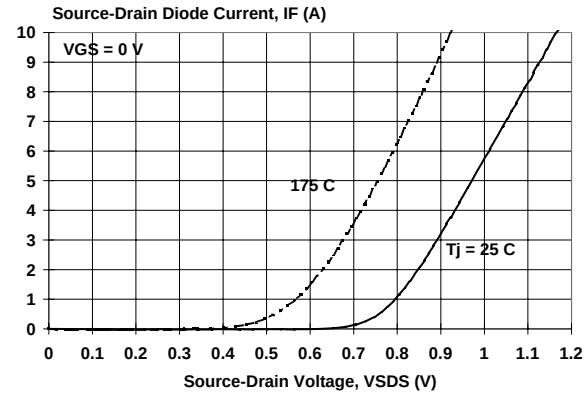
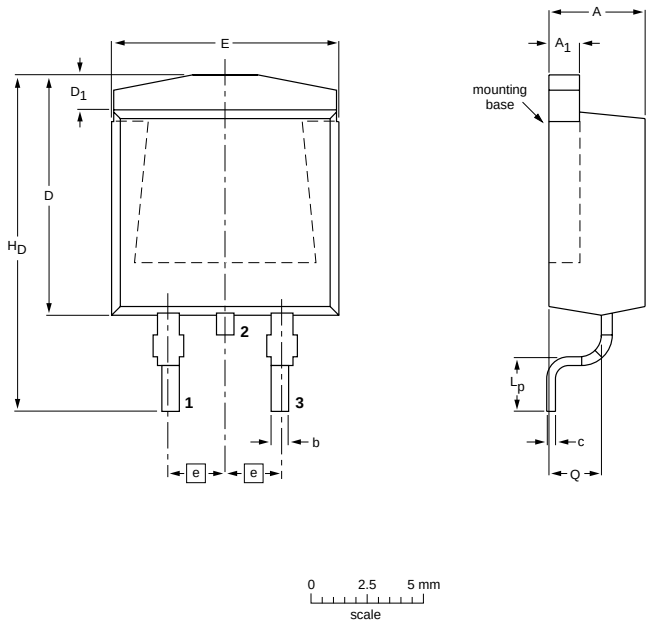



*Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter $T_j$*

## MECHANICAL DATA

**Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads (one lead cropped)** **SOT404**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | c | D max. | $D_1$ | E | e | $L_p$ | $H_D$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.50<br>4.10 | 1.40<br>1.27 | 0.85<br>0.60 | 0.64<br>0.46 | 11 | 1.60<br>1.20 | 10.30<br>9.70 | 2.54 | 2.90<br>2.10 | 15.40<br>14.80 | 2.60<br>2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT404 | | | | | | ~~98-12-14~~<br>99-06-25 |

*Fig.16. SOT404 surface mounting package. Centre pin connected to mounting base.*

**Notes**

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

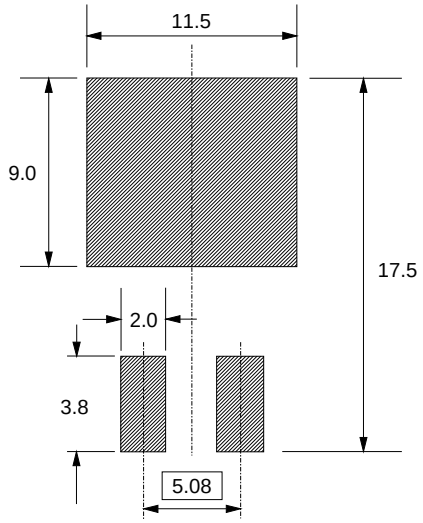
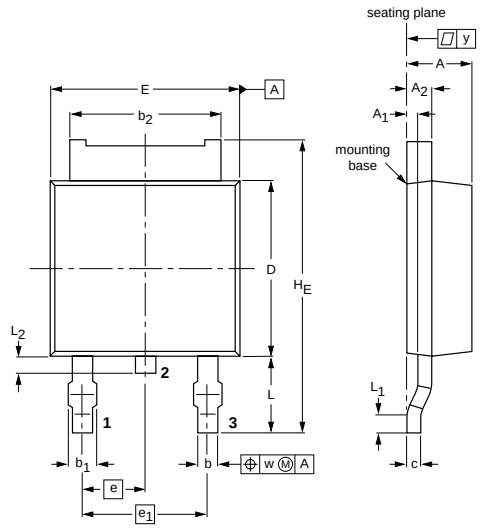



*Fig.17. SOT404 : soldering pattern for surface mounting.*

## MECHANICAL DATA

**Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)** **SOT428**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ (1) | $A_2$ | b | $b_1$ max. | $b_2$ | c | D max. | $D_1$ max. | E max. | $E_1$ min. | e | $e_1$ | $H_E$ max. | L | $L_1$ min. | $L_2$ | w | y max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.38<br>2.22 | 0.65<br>0.45 | 0.89<br>0.71 | 0.89<br>0.71 | 1.1<br>0.9 | 5.36<br>5.26 | 0.4<br>0.2 | 6.22<br>5.98 | 4.81<br>4.45 | 6.73<br>6.47 | 4.0 | 2.285 | 4.57 | 10.4<br>9.6 | 2.95<br>2.55 | 0.5 | 0.7<br>0.5 | 0.2 | 0.2 |

**Note**

1. Measured from heatsink back to lead.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT428 | | | | | | 98-04-07 |

*Fig.18. SOT428 surface mounting package. Centre pin connected to mounting base.*

**Notes**

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

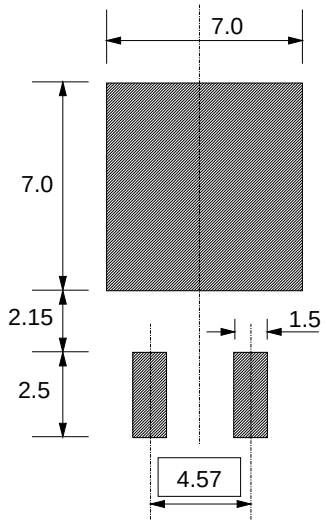



*Fig.19. SOT428 : soldering pattern for surface mounting.*

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |
|  | |
|  | |
|  | |

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.