

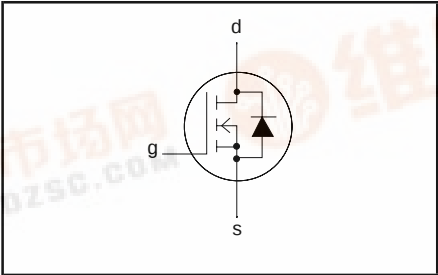
**PowerMOS transistors
Avalanche energy rated**

PHP2N50E, PHB2N50E, PHD2N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$$V_{DSS} = 500 \text{ V}$$

$$I_D = 2 \text{ A}$$

$$R_{DS(ON)} \leq 5 \Omega$$

GENERAL DESCRIPTION

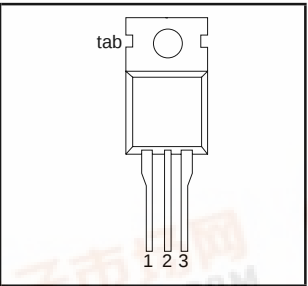
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP2N50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB2N50E is supplied in the SOT404 surface mounting package.
The PHD2N50E is supplied in the SOT428 surface mounting package.

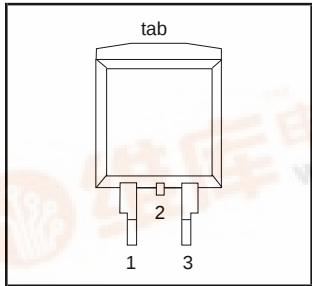
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

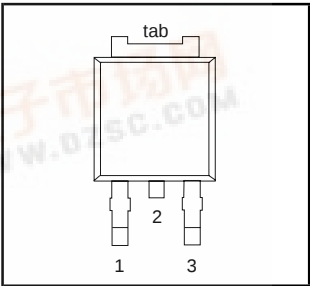
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 20 \text{ k}\Omega$	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	2	A
		$T_{mb} = 100^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	1.3	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	8	A
P_D	Total dissipation	$T_{mb} = 25^\circ\text{C}$	-	50	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	$^\circ\text{C}$

¹ It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.



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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 1.26$ A; $t_p = 0.2$ ms; T_j prior to avalanche = 25°C; $V_{DD} \leq 50$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; refer to fig:17	-	82	mJ
E_{AR}	Repetitive avalanche energy ²	$I_{AR} = 2$ A; $t_p = 2.5$ μs; T_j prior to avalanche = 25°C; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; refer to fig:18	-	3.3	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

² pulse width and repetition rate limited by T_j max.

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ELECTRICAL CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	500	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	$V_{GS} = 10\text{ V}; I_D = 1\text{ A}$	-	3.1	5	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	$V_{DS} = 30\text{ V}; I_D = 1\text{ A}$	0.5	1.3	-	S
I_{DSS}	Drain-source leakage current	$V_{DS} = 500\text{ V}; V_{GS} = 0\text{ V}$	-	1	25	μA
		$V_{DS} = 400\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	30	250	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30\text{ V}; V_{DS} = 0\text{ V}$	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 2\text{ A}; V_{DD} = 400\text{ V}; V_{GS} = 10\text{ V}$	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	15	nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}; R_D = 120\text{ }\Omega;$	-	10	-	ns
t_r	Turn-on rise time	$R_G = 24\text{ }\Omega$	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Turn-off fall time		-	20	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	236	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Feedback capacitance		-	22	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	-	2	A
I_{SM}	Pulsed source current (body diode)	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	-	8	A
V_{SD}	Diode forward voltage	$I_S = 2\text{ A}; V_{GS} = 0\text{ V}$	-	-	1.2	V
t_{rr}	Reverse recovery time	$I_S = 2\text{ A}; V_{GS} = 0\text{ V}; dI/dt = 100\text{ A}/\mu\text{s}$	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	2.1	-	μC

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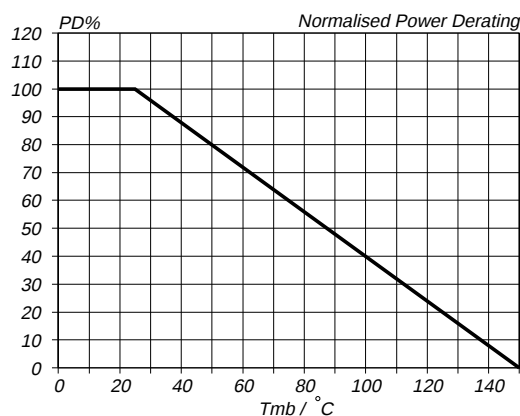


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ\text{C}} = f(T_{mb})$

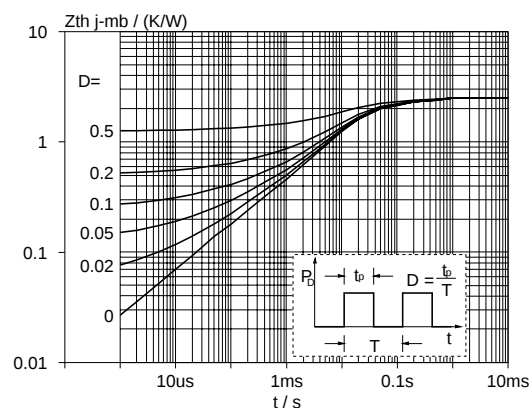


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t)$; parameter $D = t_p / T$

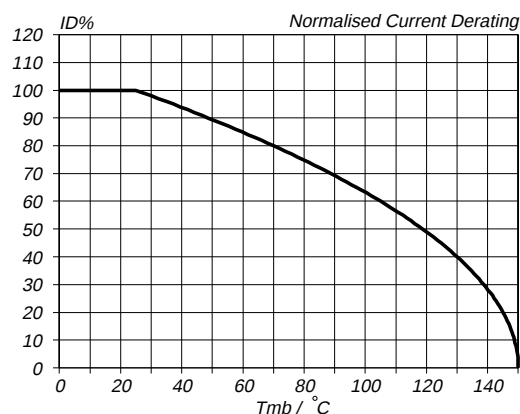


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ\text{C}} = f(T_{mb})$; conditions: $V_{GS} \geq 10\text{ V}$

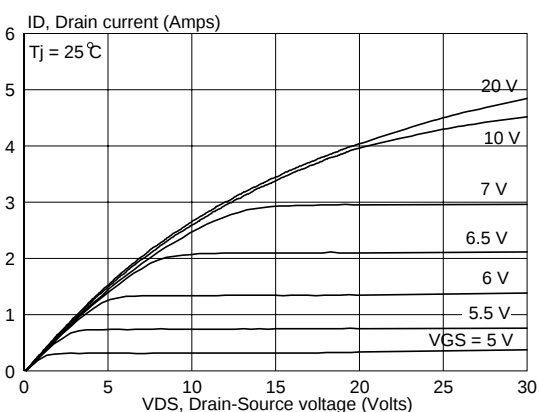


Fig.5. Typical output characteristics.
 $I_D = f(V_{DS})$; parameter V_{GS}

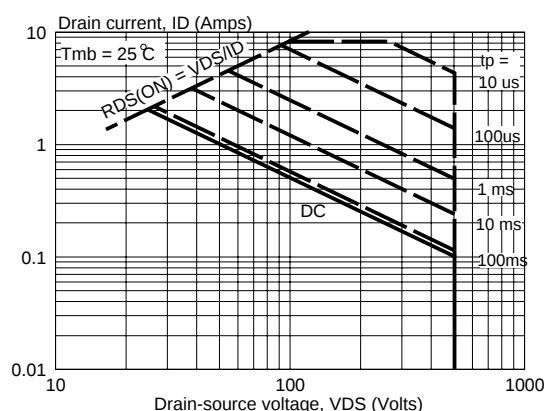


Fig.3. Safe operating area. $T_{mb} = 25^\circ\text{C}$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

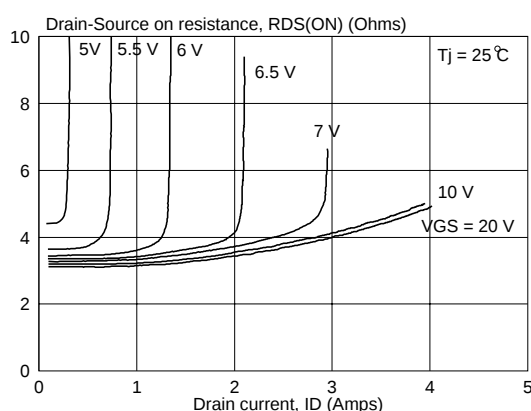


Fig.6. Typical on-state resistance.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

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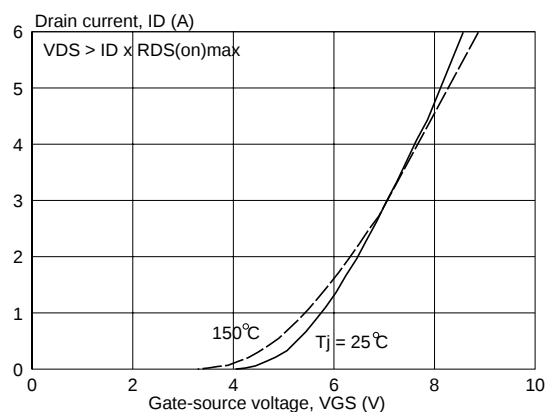


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; parameter T_j

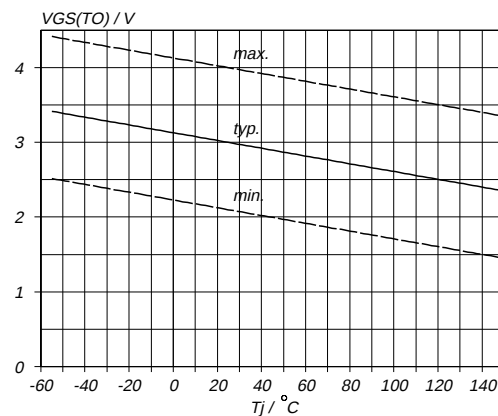


Fig. 10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25 \text{ mA}$; $V_{DS} = V_{GS}$

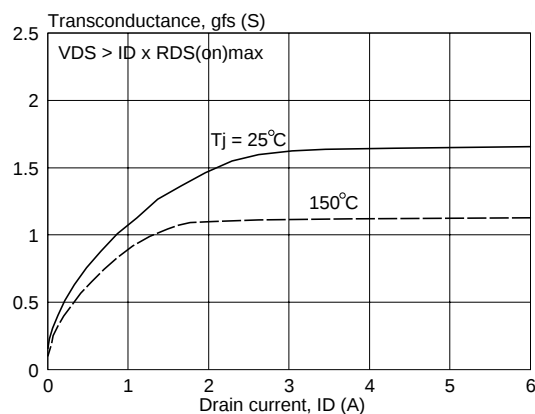


Fig. 8. Typical transconductance.
 $g_{fs} = f(I_D)$; parameter T_j

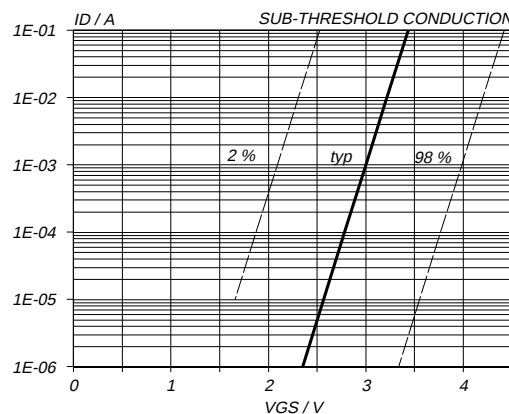


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

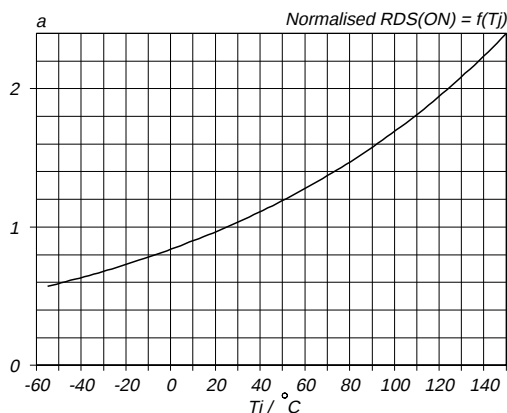


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)} / R_{DS(ON)25^\circ\text{C}} = f(T_j)$; $I_D = 1 \text{ A}$; $V_{GS} = 10 \text{ V}$

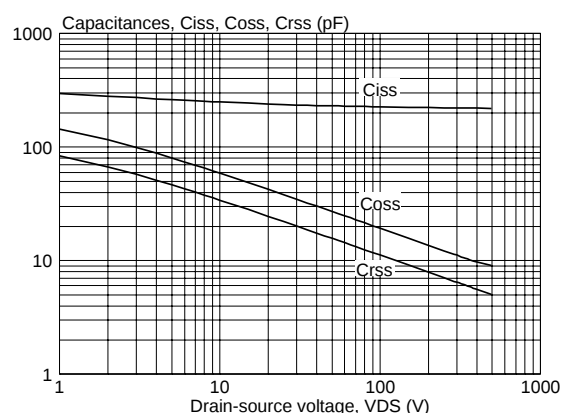


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

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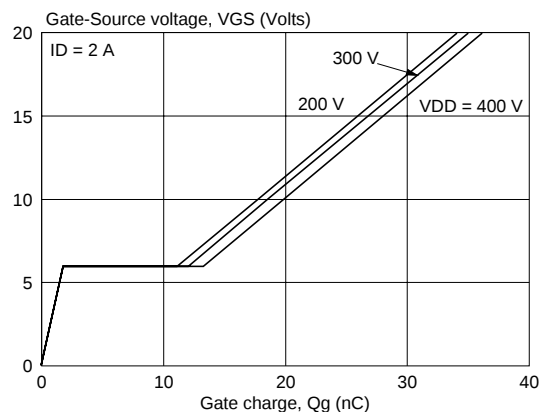


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; parameter V_{DS}

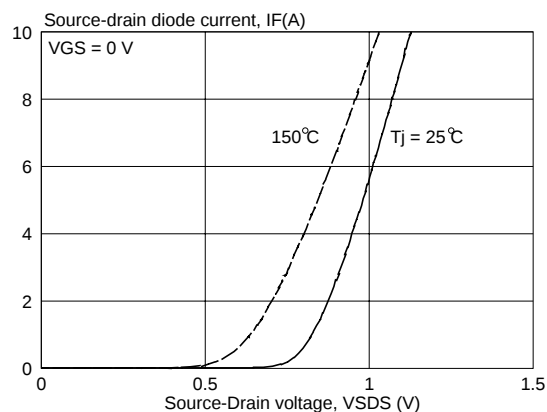


Fig.16. Source-Drain diode characteristic.
 $I_F = f(V_{SDS})$; parameter T_J

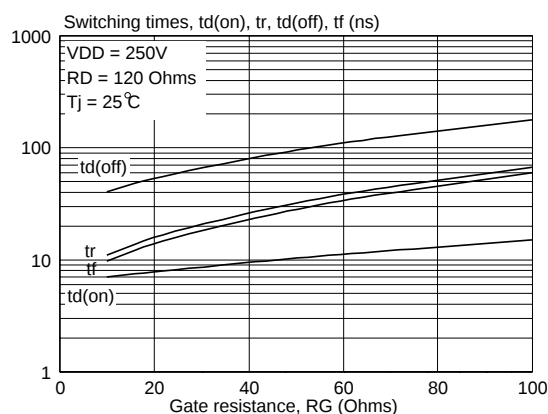


Fig.14. Typical switching times; $t_{d(on)}$, t_r , $t_{d(off)}$, $t_f = f(R_G)$

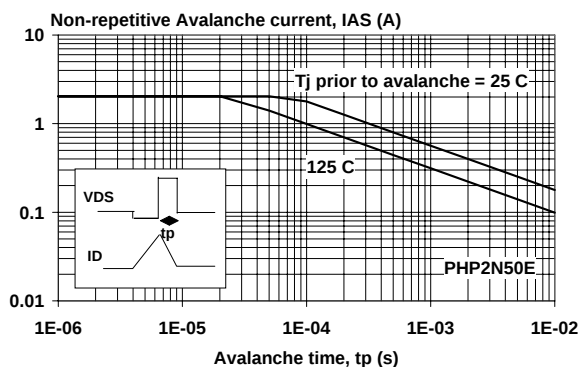


Fig.17. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

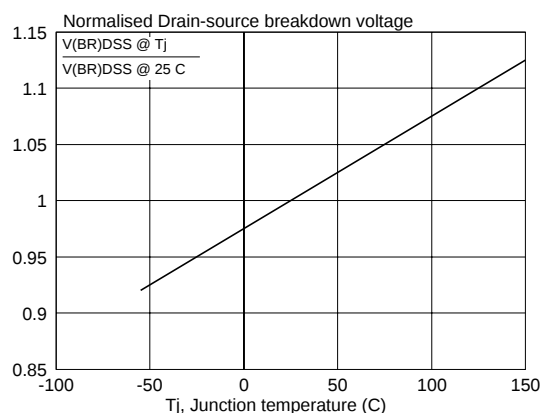


Fig.15. Normalised drain-source breakdown voltage;
 $V_{(BR)DSS} / V_{(BR)DSS\ 25\ ^\circ C} = f(T_J)$

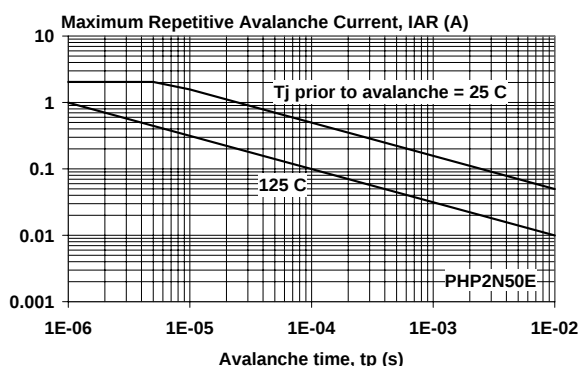


Fig.18. Maximum permissible repetitive avalanche current (I_{AR}) versus avalanche time (t_p)

PHP2N50E, PHB2N50E, PHD2N50E

Net Mass: 2 g

Fig.19. SOT78 (TO220AB); pin 2 connected to mounting base.

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

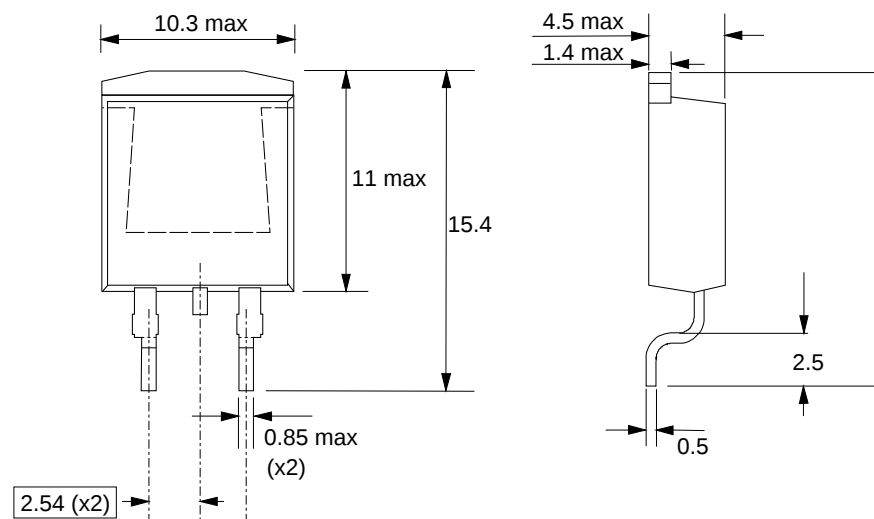


Fig.20. SOT404 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

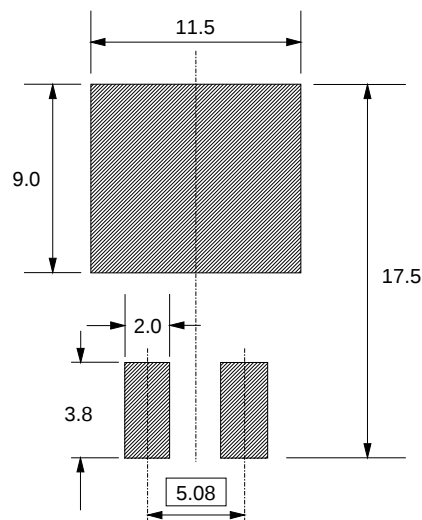


Fig.21. SOT404 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

PHP2N50E, PHB2N50E, PHD2N50E

Dimensions in mm : Net Mass: 1.4 g

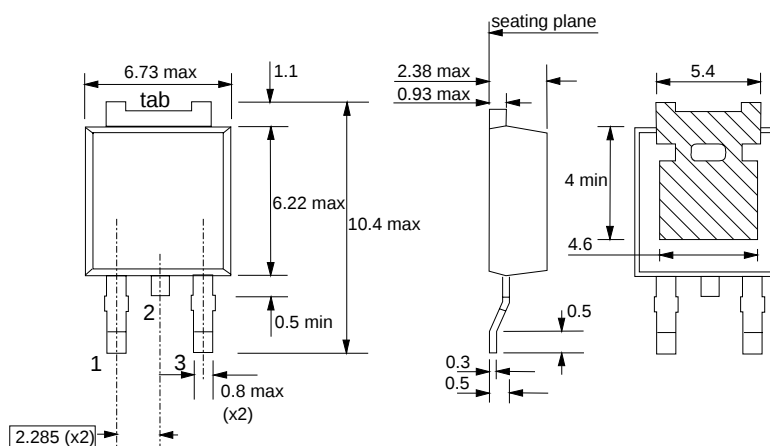


Fig.22. SOT428 : centre pin connected to mounting base.

Dimensions in mm

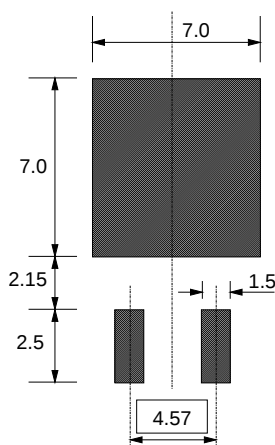


Fig.23. SOT428 : soldering pattern for surface mounting.

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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