

PHP/PHB33NQ20T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 8 November 2004

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low on-state resistance
- Low thermal resistance
- Fast switching
- Low gate charge.

1.3 Applications

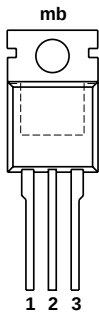
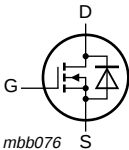
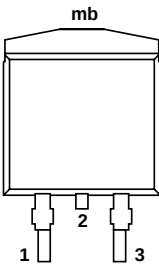
- DC-to-DC primary side switching.

1.4 Quick reference data

- $V_{DS} \leq 200\text{ V}$
- $I_D \leq 32.7\text{ A}$
- $R_{DS(on)} \leq 77\text{ m}\Omega$
- $Q_{gd} = 9.6\text{ nC (typ.)}$

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1	gate		
2	drain ^[1]		
3	source		
mb	mounting base; connected to drain		
		SOT78 (TO-220AB)	SOT404 (D²-PAK)

[1] It is not possible to make a connection to pin 2 of the SOT404 package.

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PHP33NQ20T	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 lead TO-220AB	SOT78
PHB33NQ20T	D ² -PAK	Plastic single-ended surface mounted package (D ² -PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage (DC)	25 °C ≤ T _j ≤ 175 °C	-	200	V
V _{DGR}	drain-gate voltage (DC)	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	200	V
V _{GS}	gate-source voltage (DC)		-	±20	V
I _D	drain current (DC)	T _{mb} = 25 °C; V _{GS} = 10 V; Figure 2 and 3	-	32.7	A
		T _{mb} = 100 °C; V _{GS} = 10 V; Figure 2	-	23.1	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Figure 3	-	65.4	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Figure 1	-	230	W
T _{stg}	storage temperature		-55	+175	°C
T _j	junction temperature		-55	+175	°C
Source-drain diode					
I _S	source (diode forward) current (DC)	T _{mb} = 25 °C	-	32.7	A
I _{SM}	peak source (diode forward) current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs	-	65.4	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	unclamped inductive load; I _D = 10.4 A; t _p = 0.14 ms; V _{DD} ≤ 200 V; R _{GS} = 50 Ω; V _{GS} = 10 V; starting at T _j = 25 °C	-	190	mJ

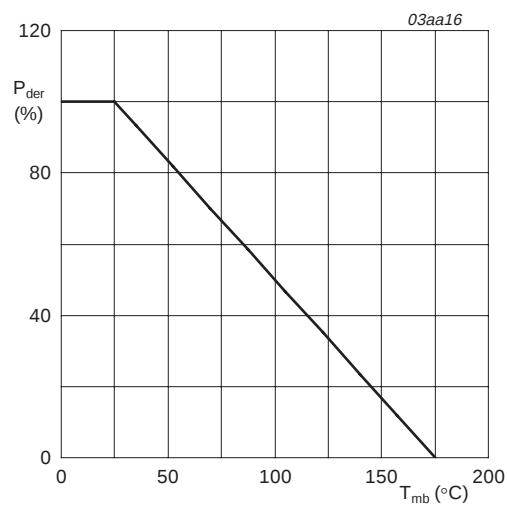


Fig 1. Normalized total power dissipation as a function of mounting base temperature.

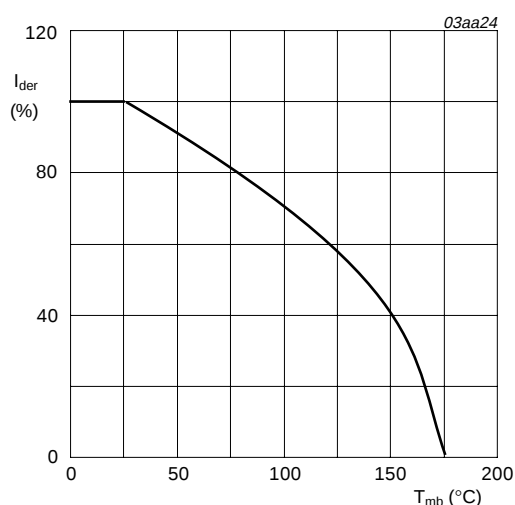


Fig 2. Normalized continuous drain current as a function of mounting base temperature.

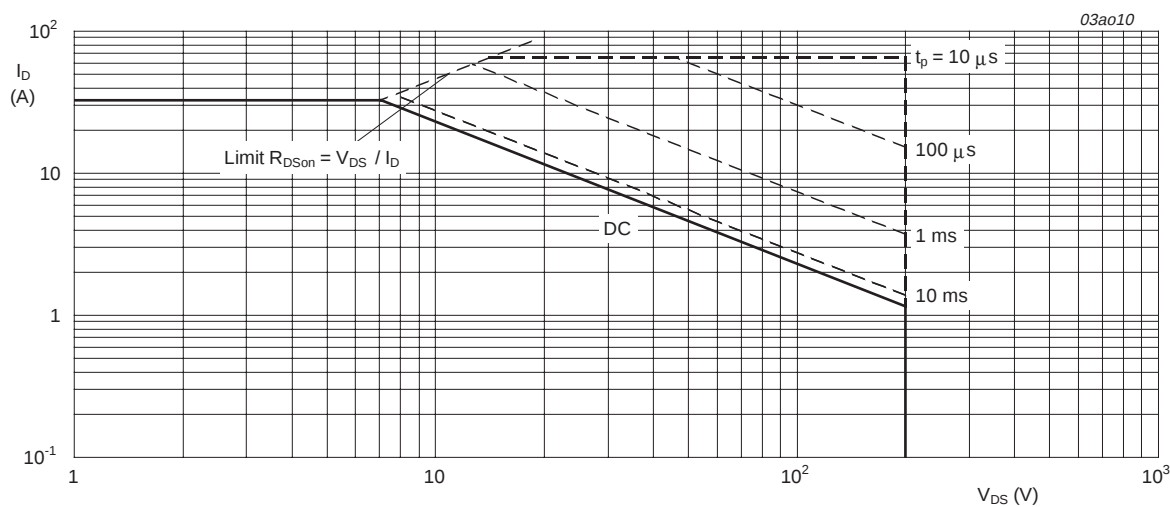


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.65	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in free air	-	60	-	K/W
	SOT404	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W

5.1 Transient thermal impedance

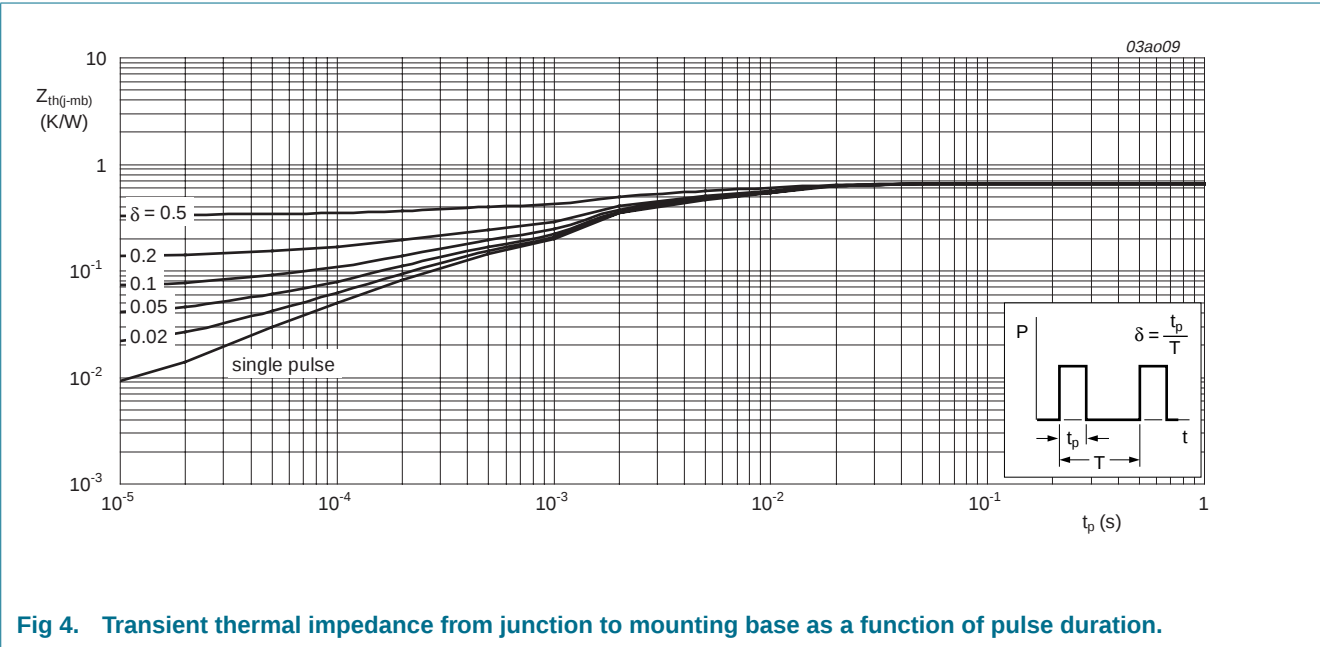
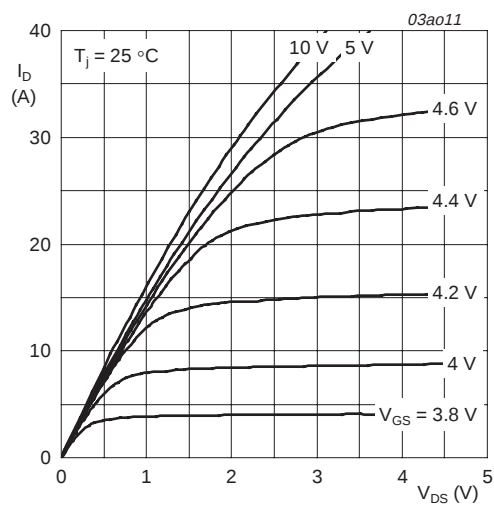


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

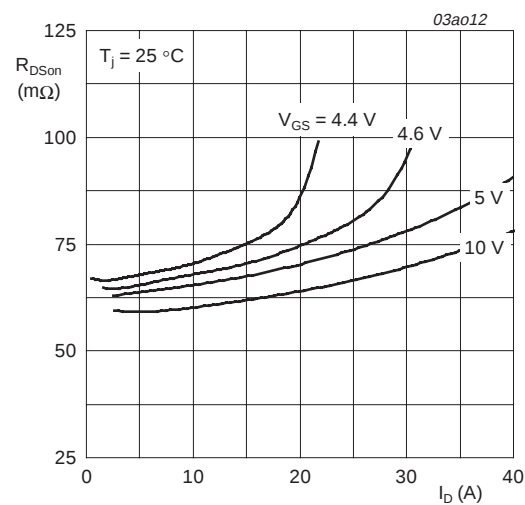
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	200	-	-	V
		$T_j = -55\text{ °C}$	180	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 and 10				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 160\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; Figure 6 and 8				
		$T_j = 25\text{ °C}$	-	65	77	m Ω
		$T_j = 175\text{ °C}$	-	182	215	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 100\text{ V}$; $V_{GS} = 10\text{ V}$; Figure 11	-	32.2	-	nC
Q_{gs}	gate-source charge		-	6.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	9.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 13	-	1870	-	pF
C_{oss}	output capacitance		-	230	-	pF
C_{rss}	reverse transfer capacitance		-	70	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 100\text{ V}$; $R_L = 4\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 6\text{ }\Omega$	-	12	-	ns
t_r	rise time		-	35	-	ns
$t_{d(off)}$	turn-off delay time		-	43	-	ns
t_f	fall time		-	45	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.87	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	150	-	ns
Q_r	recovered charge		-	645	-	nC



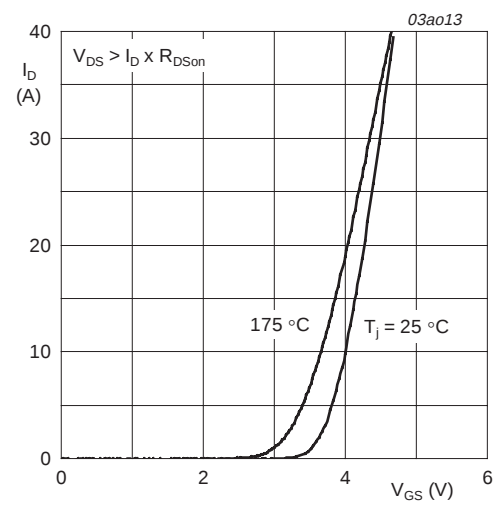
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



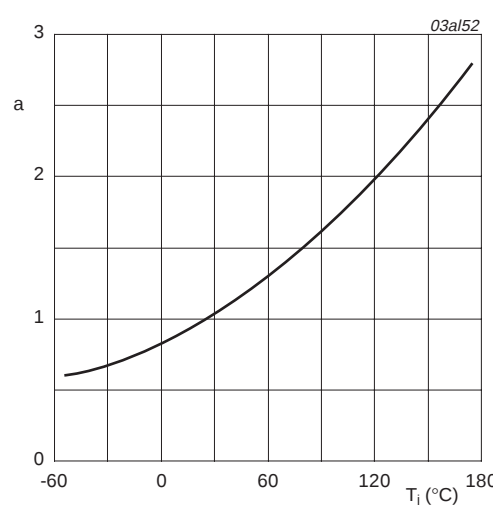
$T_j = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



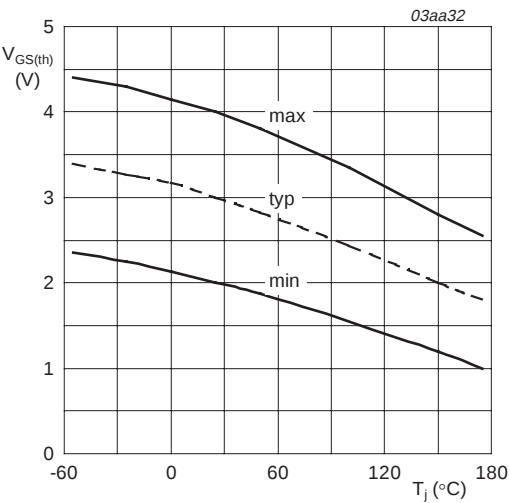
$T_j = 25^\circ\text{C}$ and 175°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



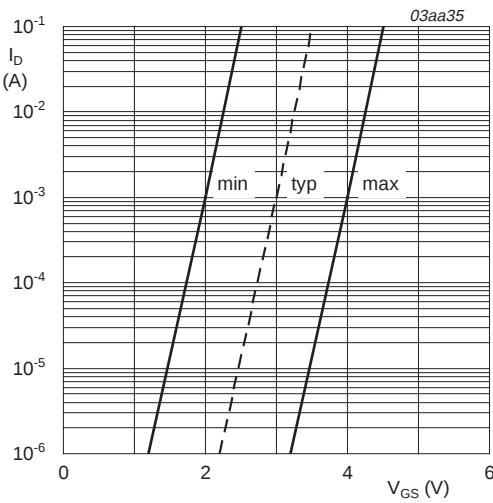
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



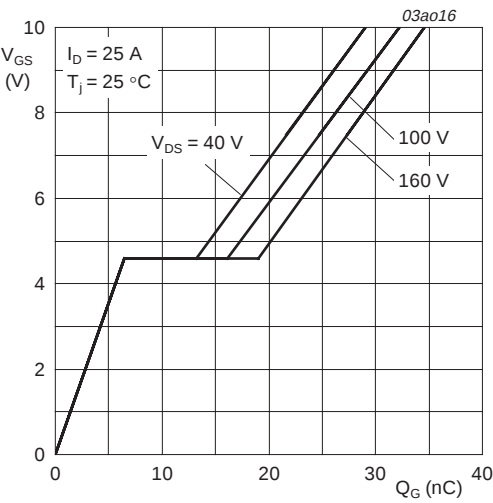
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



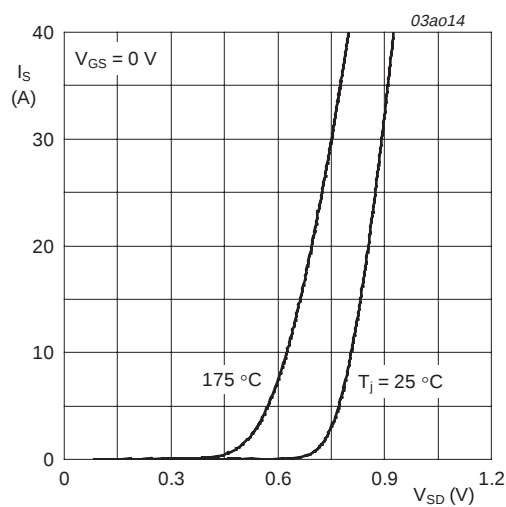
$T_j = 25\text{ °C}$; $V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



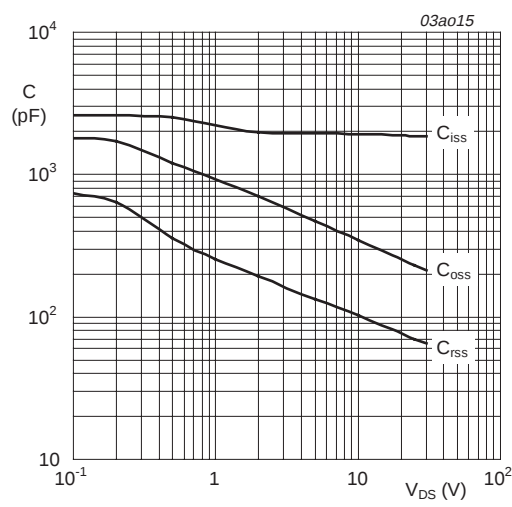
$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}, 100\text{ V}$ and 160 V

Fig 11. Gate-source voltage as a function of gate charge; typical values.



$T_j = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB SOT78

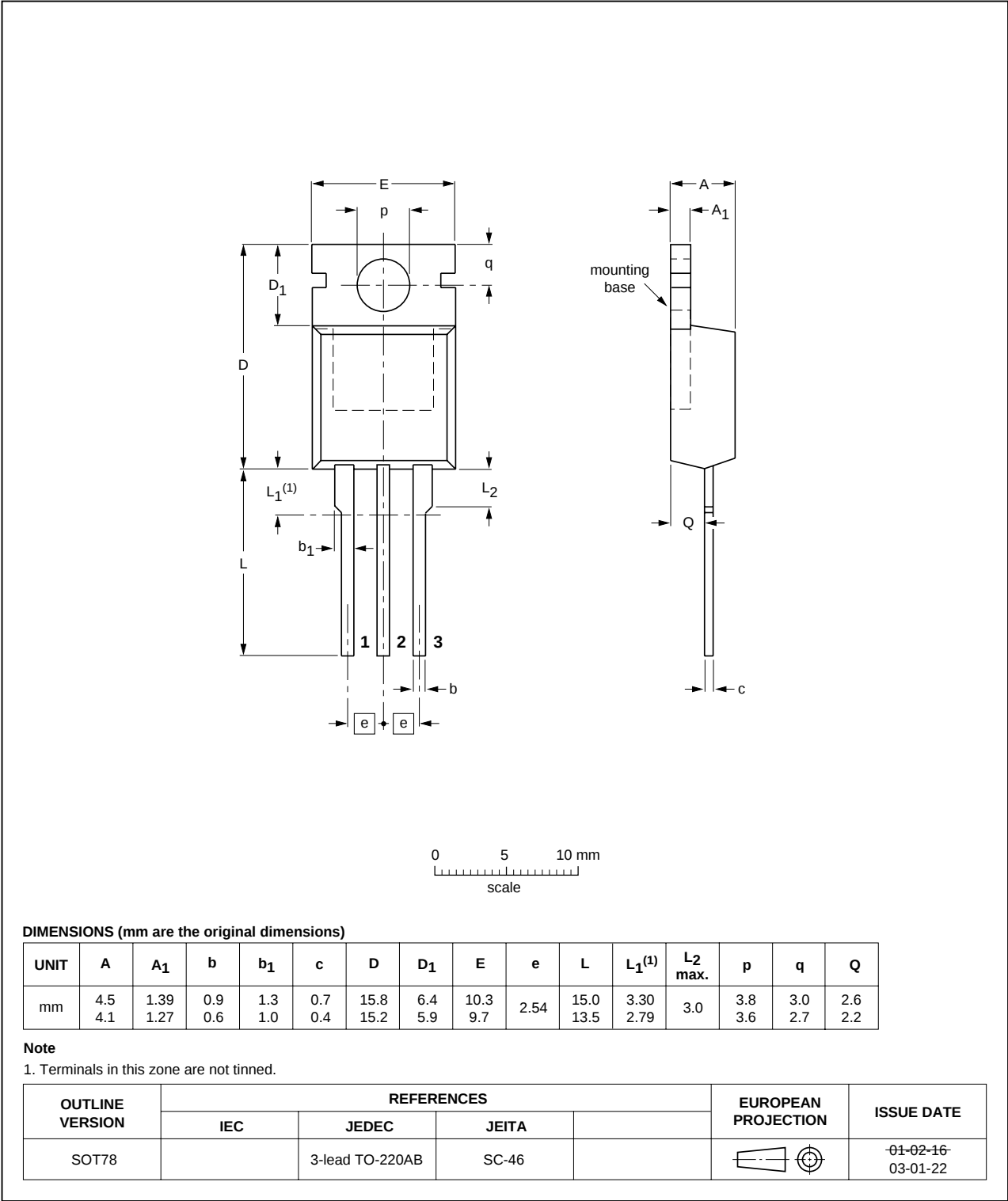
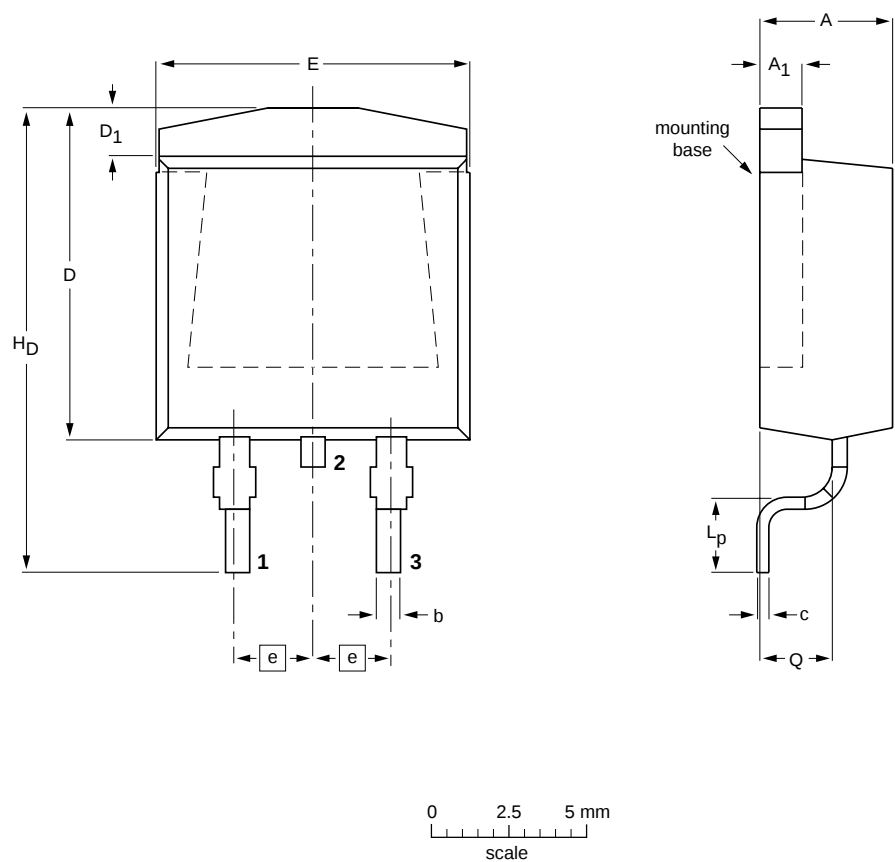


Fig 14. SOT78 (TO-220AB) package outline.

Plastic single-ended surface mounted package (D²-PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						01-02-12 04-10-13

Fig 15. SOT404 (D²-PAK) package outline.



8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PHP_PHB33NQ20T_1	20041108	Product data sheet	-	9397 750 14003	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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