

Philips Semiconductors

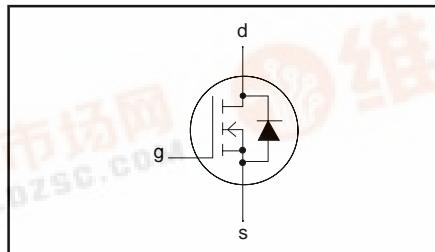
Product specification

N-channel TrenchMOS<sup>TM</sup> transistorPHP34NQ10T, PHB34NQ10T  
PHD34NQ10T

## FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

## SYMBOL



## QUICK REFERENCE DATA

 $V_{DSS} = 100 \text{ V}$  $I_D = 35 \text{ A}$  $R_{DS(ON)} \leq 40 \text{ m}\Omega$ 

## GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope using 'trench' technology.

## Applications:-

- d.c. to d.c. converters
- switched mode power supplies

The PHP34NQ10T is supplied in the SOT78 (TO220AB) conventional leaded package.

The PHB34NQ10T is supplied in the SOT404 (D<sup>2</sup>PAK) surface mounting package.

The PHD34NQ10T is supplied in the SOT428 (DPAK) surface mounting package.

## PINNING

## SOT78 (TO220AB)

SOT404 (D<sup>2</sup>PAK)

## SOT428 (DPAK)

PIN	DESCRIPTION	SOT78 (TO220AB)	SOT404 (D <sup>2</sup> PAK)	SOT428 (DPAK)
1	gate			
2	drain <sup>1</sup>			
3	source			
tab	drain			

## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DSS}$	Drain-source voltage	$T_j = 25 \text{ }^\circ\text{C to } 175 \text{ }^\circ\text{C}$	-	100	V
$V_{DGR}$	Drain-gate voltage	$T_j = 25 \text{ }^\circ\text{C to } 175 \text{ }^\circ\text{C}; R_{GS} = 20 \text{ k}\Omega$	-	100	V
$V_{GS}$	Gate-source voltage		-	$\pm 20$	V
$I_D$	Continuous drain current	$T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V}$	-	35	A
$I_{DM}$	Pulsed drain current	$T_{mb} = 100 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V}$	-	25	A
$P_D$	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	140	A
$T_j, T_{stg}$	Operating junction and storage temperature	$T_{mb} = 25 \text{ }^\circ\text{C}$	-55	175	$^\circ\text{C}$

<sup>1</sup> It is not possible to make connection to pin:2 of the SOT404 or SOT428 packages.

## N-channel TrenchMOS™ transistor

PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T**AVALANCHE ENERGY LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E <sub>AS</sub>	Non-repetitive avalanche energy	Unclamped inductive load, I <sub>AS</sub> = 26 A; t <sub>p</sub> = 100 µs; T <sub>j</sub> prior to avalanche = 25°C; V <sub>DD</sub> ≤ 25 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; refer to fig:15	-	170	mJ
I <sub>AS</sub>	Peak non-repetitive avalanche current		-	35	A

**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R <sub>th j-mb</sub>	Thermal resistance junction to mounting base		-	-	1.1	K/W
R <sub>th j-a</sub>	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 & SOT428 packages, pcb mounted, minimum footprint	-	60	-	K/W
			-	50	-	K/W

**ELECTRICAL CHARACTERISTICS**T<sub>j</sub>=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.25 mA;	100	-	-	V
V <sub>GS(TO)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA	89	-	-	V
V <sub>DS(ON)</sub>	Drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 17 A	2	3	4	V
I <sub>GSS</sub>	Gate source leakage current	V <sub>GS</sub> = ± 10 V; V <sub>DS</sub> = 0 V	1	-	-	V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V	-	35	40	mΩ
			-	-	108	mΩ
Q <sub>g(tot)</sub>	Total gate charge	I <sub>D</sub> = 34 A; V <sub>DD</sub> = 80 V; V <sub>GS</sub> = 10 V	-	10	100	nA
Q <sub>gs</sub>	Gate-source charge		-	0.05	10	µA
Q <sub>gd</sub>	Gate-drain (Miller) charge		-	-	500	µA
t <sub>d on</sub>	Turn-on delay time	V <sub>DD</sub> = 50 V; R <sub>D</sub> = 1.5 Ω;	-	12	-	ns
t <sub>r</sub>	Turn-on rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 5.6 Ω	-	55	-	ns
t <sub>d off</sub>	Turn-off delay time	Resistive load	-	48	-	ns
t <sub>f</sub>	Turn-off fall time		-	38	-	ns
L <sub>d</sub>	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L <sub>d</sub>	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L <sub>s</sub>	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz	-	1704	-	pF
C <sub>oss</sub>	Output capacitance		-	227	-	pF
C <sub>rss</sub>	Feedback capacitance		-	140	-	pF

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PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_s$	Continuous source current (body diode)		-	-	35	A
$I_{SM}$	Pulsed source current (body diode)		-	-	140	A
$V_{SD}$	Diode forward voltage	$I_F = 17 \text{ A}; V_{GS} = 0 \text{ V}$	-	0.85	1.2	V
$t_{rr}$ $Q_{rr}$	Reverse recovery time Reverse recovery charge	$I_F = 17 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s};$ $V_{GS} = 0 \text{ V}; V_R = 25 \text{ V}$	-	76 0.24	-	ns $\mu\text{C}$

## N-channel TrenchMOS™ transistor

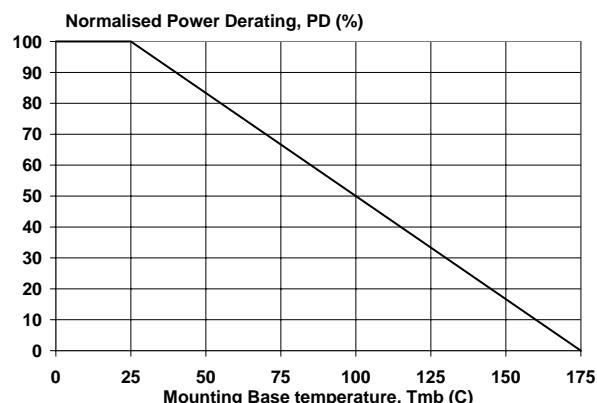
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PHD34NQ10T

Fig.1. Normalised power dissipation.  
 $PD\% = 100 \cdot P_D / P_{D, 25^\circ C} = f(T_{mb})$

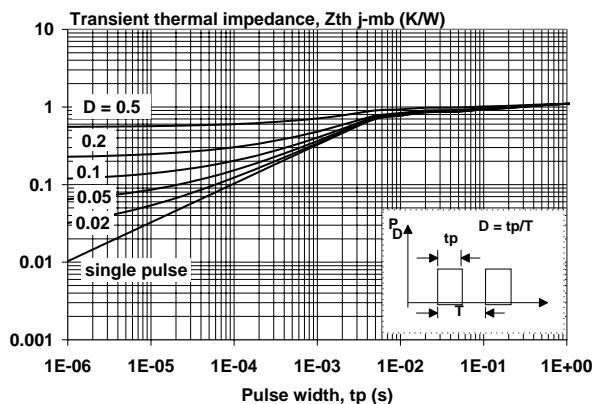


Fig.4. Transient thermal impedance.  
 $Z_{th j-mb} = f(t_p); \text{parameter } D = t_p/T$

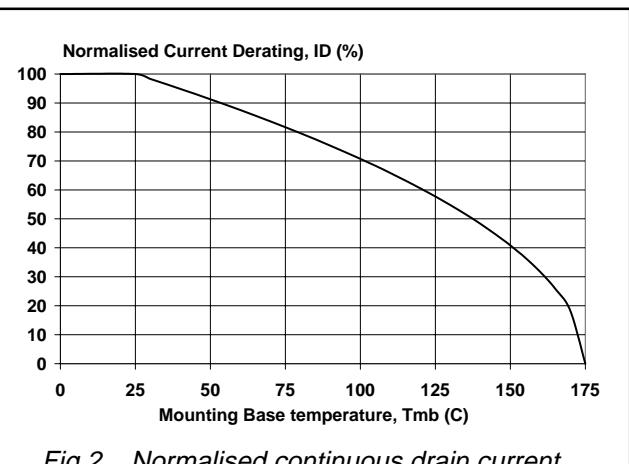


Fig.2. Normalised continuous drain current.  
 $ID\% = 100 \cdot I_D / I_{D, 25^\circ C} = f(T_{mb}); V_{GS} \geq 10 V$

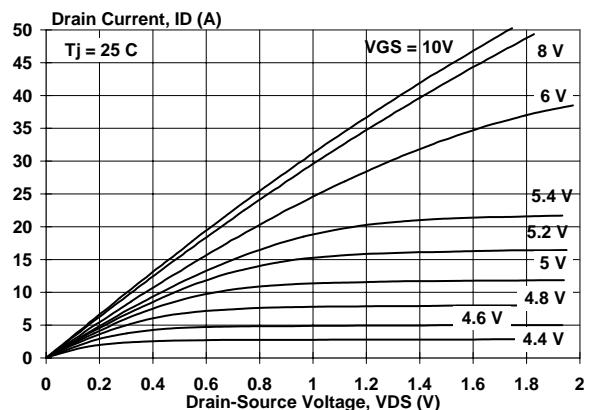


Fig.5. Typical output characteristics,  $T_j = 25^\circ C$ .  
 $I_D = f(V_{DS})$

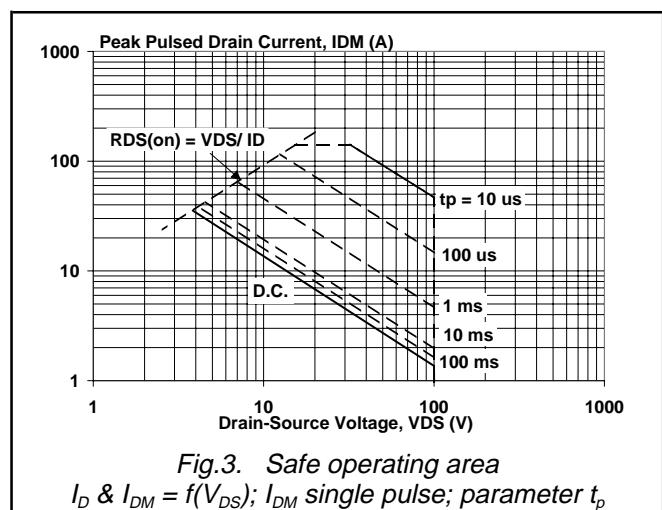


Fig.3. Safe operating area  
 $I_D \& I_{DM} = f(V_{DS}); I_{DM}$  single pulse; parameter  $t_p$

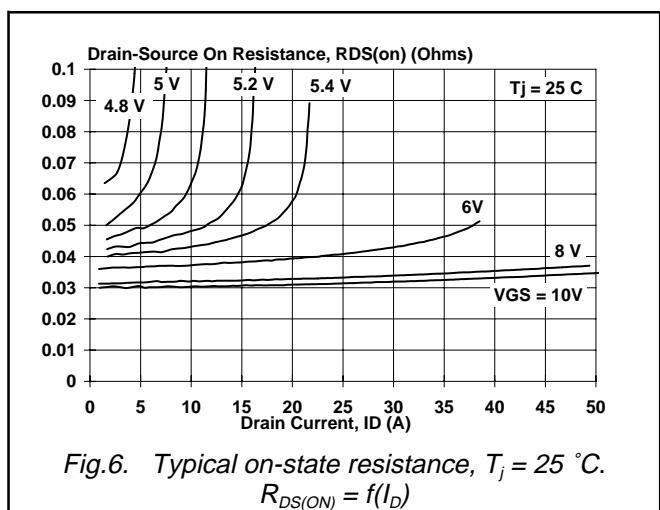


Fig.6. Typical on-state resistance,  $T_j = 25^\circ C$ .  
 $R_{DS(ON)} = f(I_D)$

## N-channel TrenchMOS™ transistor

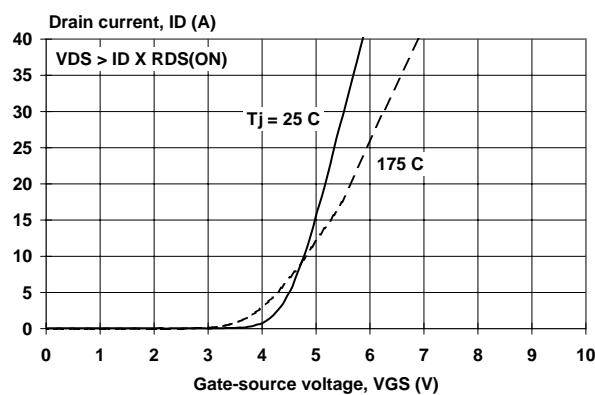
PHP34NQ10T, PHB34NQ10T  
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Fig.7. Typical transfer characteristics.  
 $I_D = f(V_{GS})$

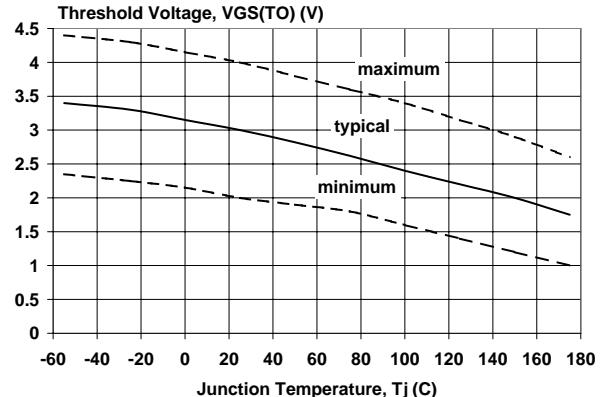


Fig.10. Gate threshold voltage.  
 $V_{GS(TO)} = f(T_j)$ ; conditions:  $I_D = 1 \text{ mA}$ ;  $V_{DS} = V_{GS}$

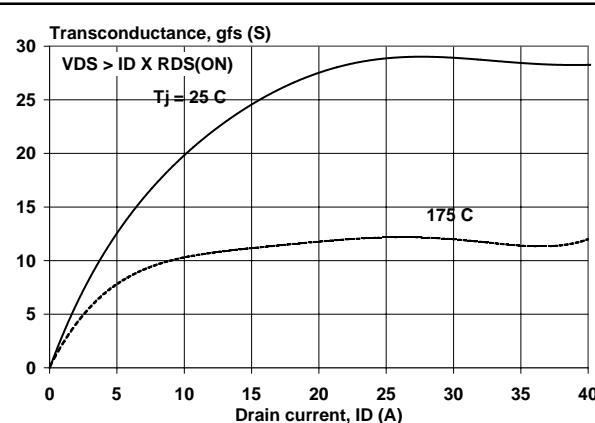


Fig.8. Typical transconductance,  $T_j = 25^\circ\text{C}$ .  
 $g_{fs} = f(I_D)$

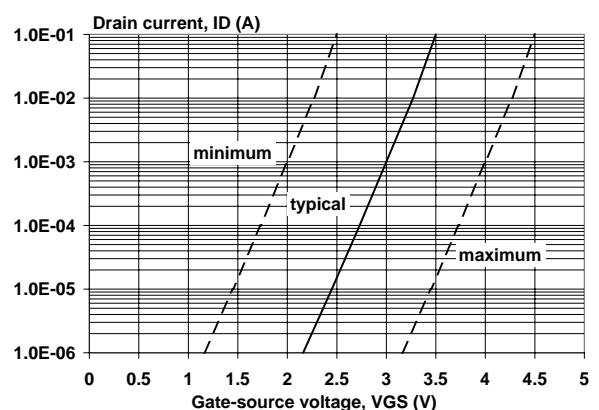


Fig.11. Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_j = 25^\circ\text{C}$ ;  $V_{DS} = V_{GS}$

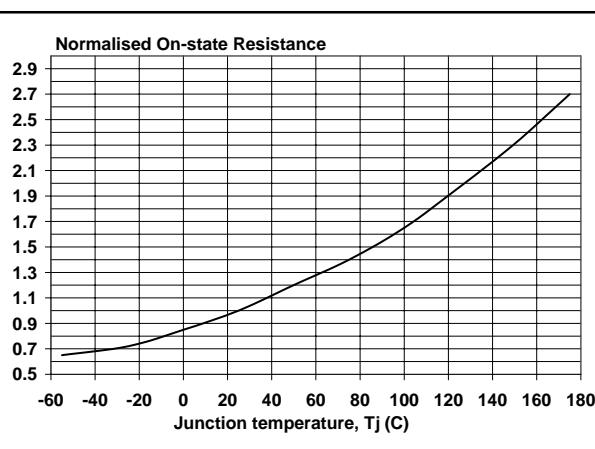


Fig.9. Normalised drain-source on-state resistance.  
 $R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_j)$

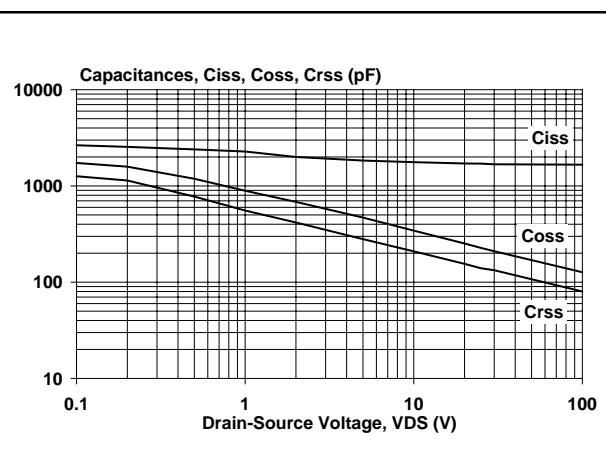


Fig.12. Typical capacitances,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ .  
 $C = f(V_{DS})$ ; conditions:  $V_{GS} = 0 \text{ V}$ ;  $f = 1 \text{ MHz}$

## N-channel TrenchMOS™ transistor

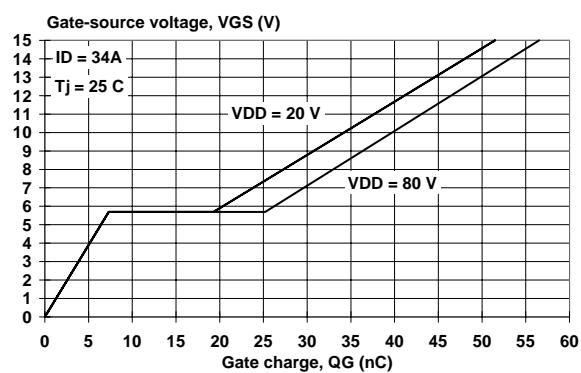
PHP34NQ10T, PHB34NQ10T  
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Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$

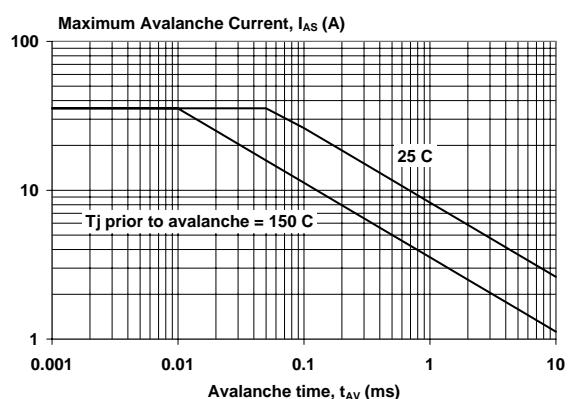


Fig.15. Maximum permissible non-repetitive avalanche current ( $I_{AS}$ ) versus avalanche time ( $t_{AV}$ ); unclamped inductive load

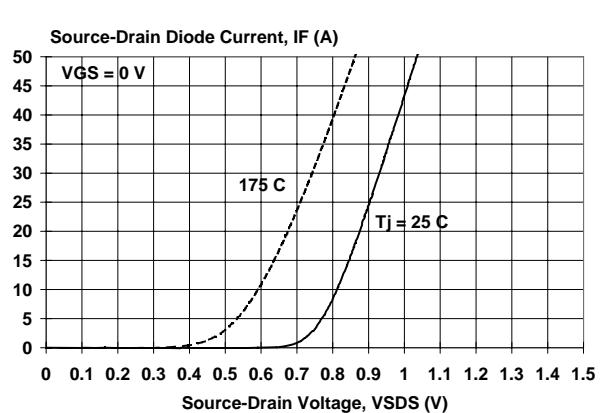


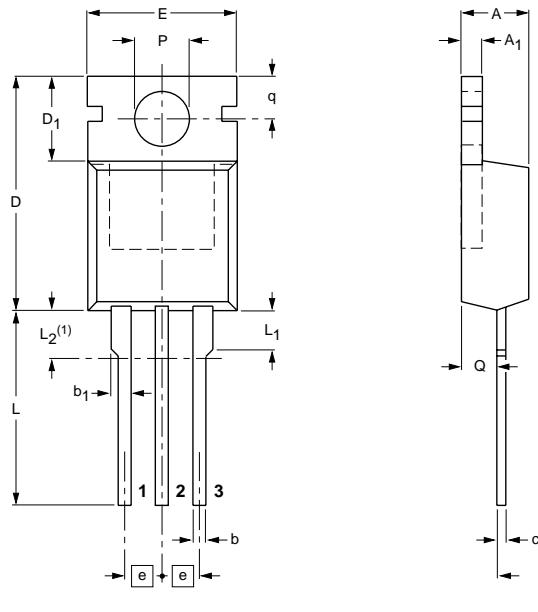
Fig.14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ; parameter  $T_j$

## N-channel TrenchMOS™ transistor

PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T

## MECHANICAL DATA

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220 SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

## Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220				97-06-11

Fig. 16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

## Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

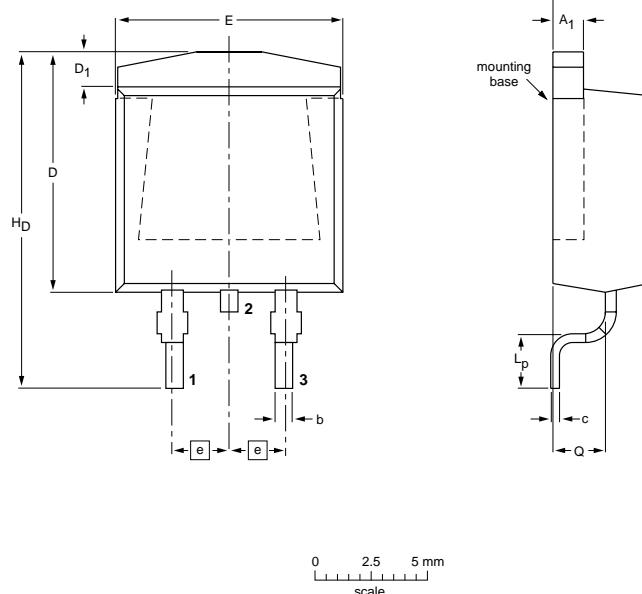
## N-channel TrenchMOS™ transistor

PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T

## MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D <sub>max.</sub>	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.40 14.80	2.60 2.20

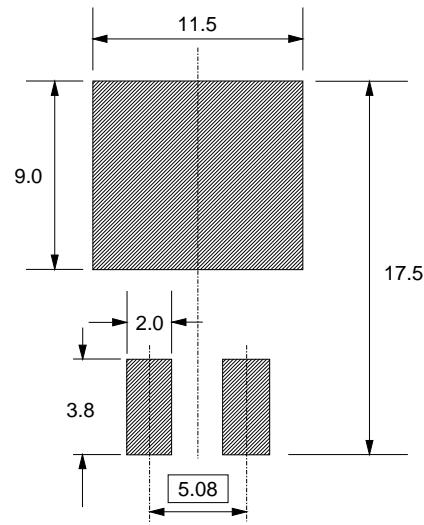
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						-98-12-14- 99-06-25

Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

## Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T**MOUNTING INSTRUCTIONS***Dimensions in mm**Fig.18. SOT404 : soldering pattern for surface mounting.*

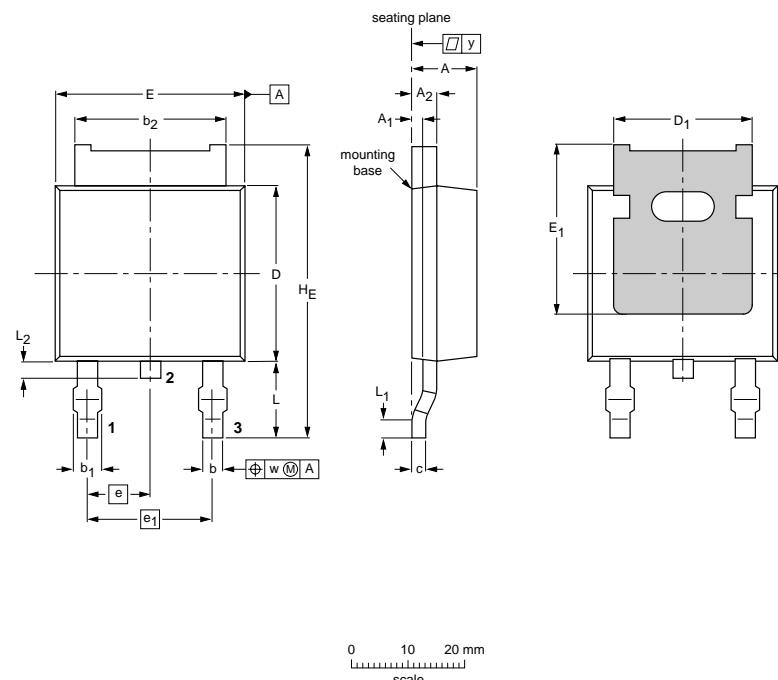
## N-channel TrenchMOS™ transistor

PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T

## MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads  
(one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub> <sup>(1)</sup>	A <sub>2</sub>	b	b <sub>1</sub> max.	b <sub>2</sub>	c	D max.	D <sub>1</sub> max.	E max.	E <sub>1</sub> min.	e	e <sub>1</sub>	H <sub>E</sub> max.	L	L <sub>1</sub> min.	L <sub>2</sub>	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0 4.57	2.285 4.57	10.4 9.6	2.95 2.55	0.5 0.5	0.7 0.5	0.2 0.2	0.2 0.2	

## Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428						98-04-07

Fig.19. SOT428 surface mounting package. Centre pin connected to mounting base.

## Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

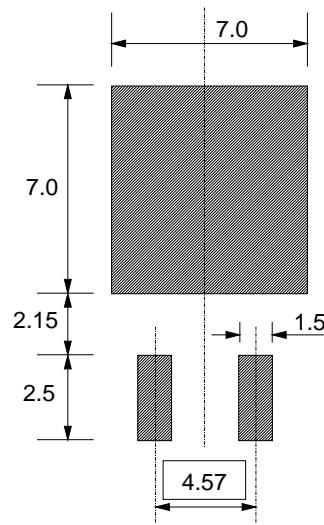
PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T**MOUNTING INSTRUCTIONS***Dimensions in mm*

Fig.20. SOT428 : soldering pattern for surface mounting.

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N-channel TrenchMOS™ transistor

PHP34NQ10T, PHB34NQ10T  
PHD34NQ10T

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## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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