

Philips Semiconductors

Product specification

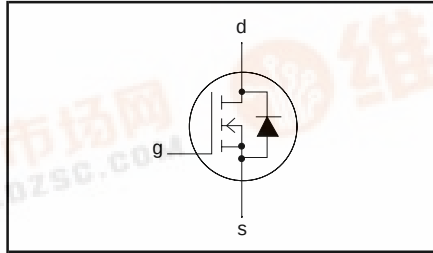
N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$$V_{DSS} = 100 \text{ V}$$

$$I_D = 47 \text{ A}$$

$$R_{DS(ON)} \leq 25 \text{ m}\Omega$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope using 'trench' technology.

Applications:-

- d.c. to d.c. converters
- switched mode power supplies

The PHP45NQ10T is supplied in the SOT78 (TO220AB) conventional leaded package.

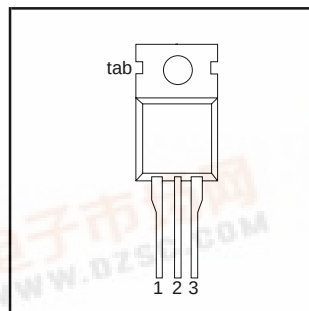
The PHB45NQ10T is supplied in the SOT404 (D²PAK) surface mounting package.

The PHW45NQ10T is supplied in the SOT429 (TO247) conventional leaded package.

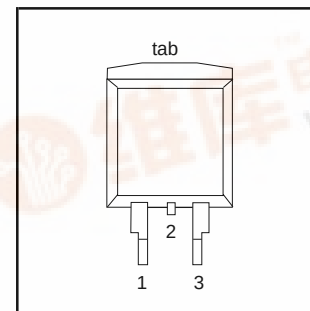
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

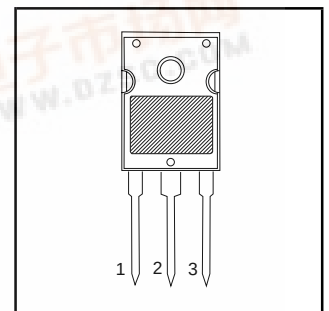
SOT78 (TO220AB)



SOT404 (D²PAK)



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 175°C	-	100	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 20 \text{ k}\Omega$	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	47	A
		$T_{mb} = 100^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	33	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	188	A
P_D	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	150	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin 2 of the SOT404 package.

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 40$ A; $t_p = 100$ μ s; T_j prior to avalanche = 25°C; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig:15	-	260	mJ
I_{AS}	Non-repetitive avalanche current		-	47	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	SOT78 package, in free air SOT429 package, in free air SOT404 package, pcb mounted, minimum footprint	-	-	1	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	60	-	K/W
			-	45	-	K/W
			-	50	-	K/W

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$	100 89	-	-	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2 1 -	3 - -	4 - 6	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A $T_j = 175^\circ\text{C}$	- -	22 -	25 68	m Ω m Ω
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10$ V; $V_{DS} = 0$ V	-	0.02	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100$ V; $V_{GS} = 0$ V; $T_j = 175^\circ\text{C}$	-	0.05 -	10 500	μ A μ A
$Q_{g(tot)}$	Total gate charge	$I_D = 45$ A; $V_{DD} = 80$ V; $V_{GS} = 10$ V	-	61	-	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	25	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 50$ V; $R_D = 1.8$ Ω ; $V_{GS} = 10$ V; $R_G = 5.6$ Ω Resistive load	-	18	-	ns
t_r	Turn-on rise time		-	72	-	ns
$t_{d\ off}$	Turn-off delay time		-	69	-	ns
t_f	Turn-off fall time		-	58	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 and SOT429 packages)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	2600	-	pF
C_{oss}	Output capacitance		-	340	-	pF
C_{rss}	Feedback capacitance		-	195	-	pF

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)	I _F = 25 A; V _{GS} = 0 V	-	-	47	A
I _{SM}	Pulsed source current (body diode)		-	-	188	A
V _{SD}	Diode forward voltage		-	0.87	1.2	V
t _{rr}	Reverse recovery time	I _F = 20 A; -dI _F /dt = 100 A/μs; V _{GS} = 0 V; V _R = 25 V	-	82	-	ns
Q _{rr}	Reverse recovery charge		-	0.26	-	μC

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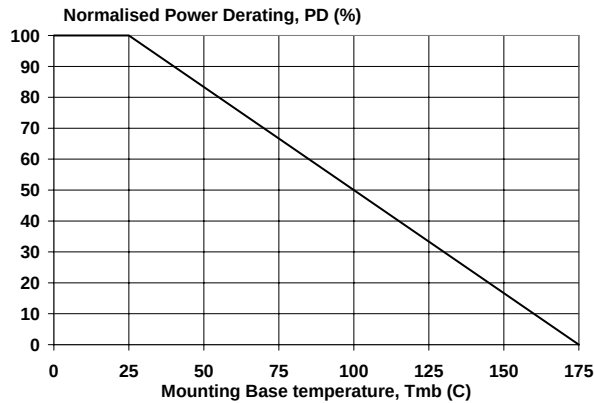
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PHW45NQ10T

Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25^\circ\text{C}} = f(T_{mb})$

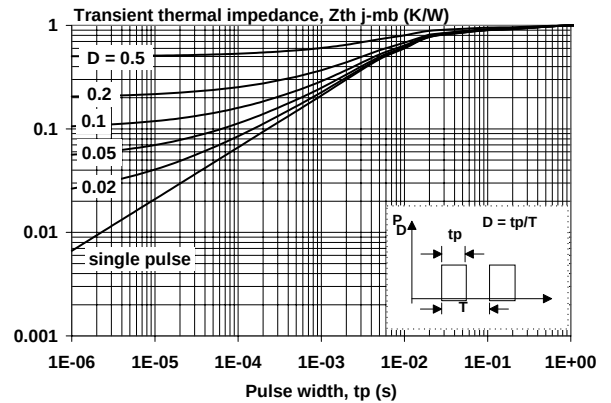


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t); \text{ parameter } D = t_p/T$

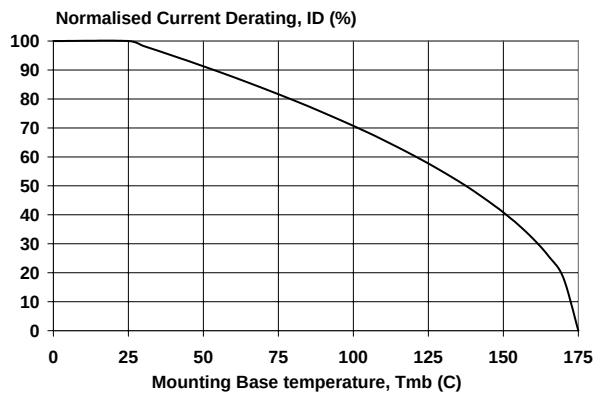


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25^\circ\text{C}} = f(T_{mb}); V_{GS} \geq 10\text{ V}$

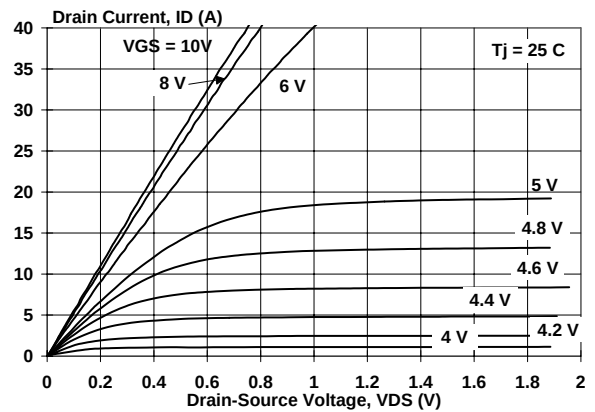


Fig.5. Typical output characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$

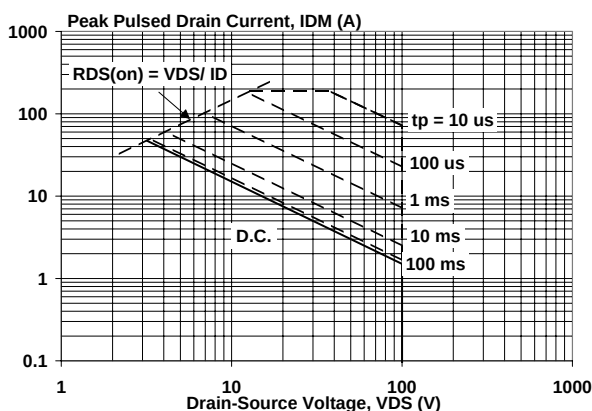


Fig.3. Safe operating area
 $I_D \text{ \& } I_{DM} = f(V_{DS}); I_{DM} \text{ single pulse; parameter } t_p$

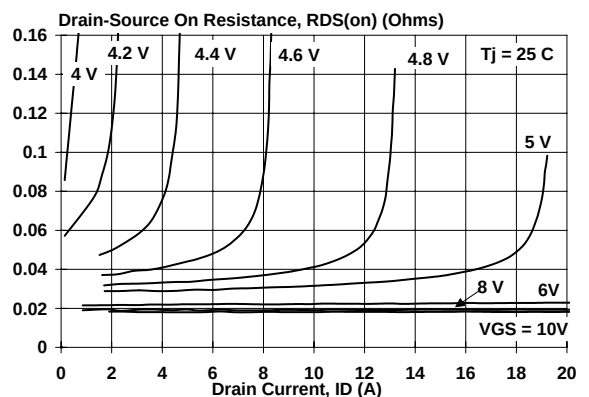
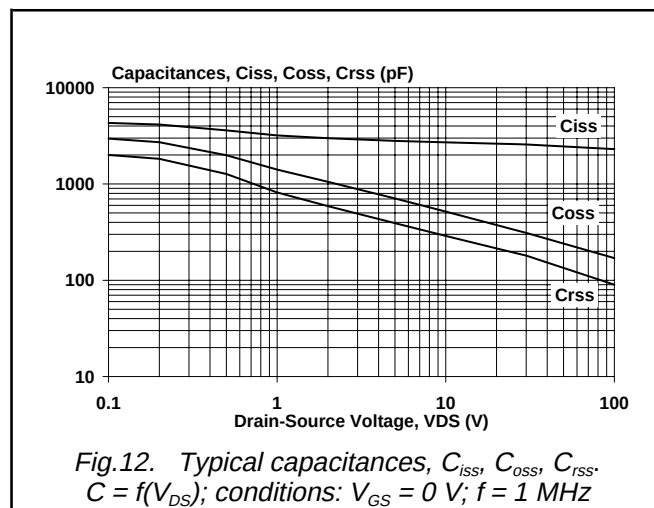
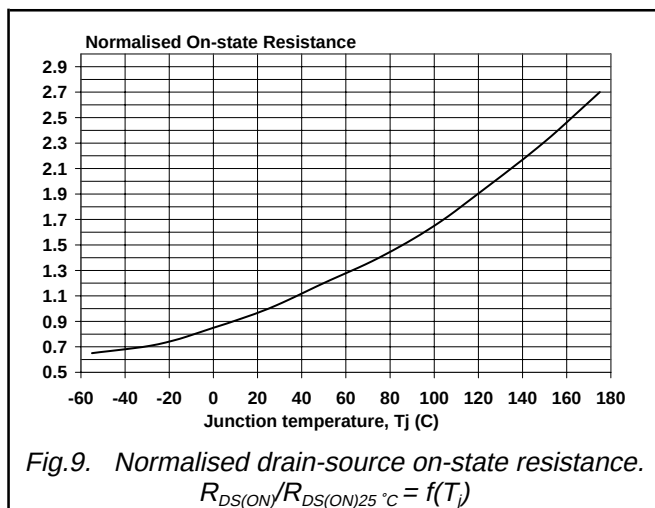
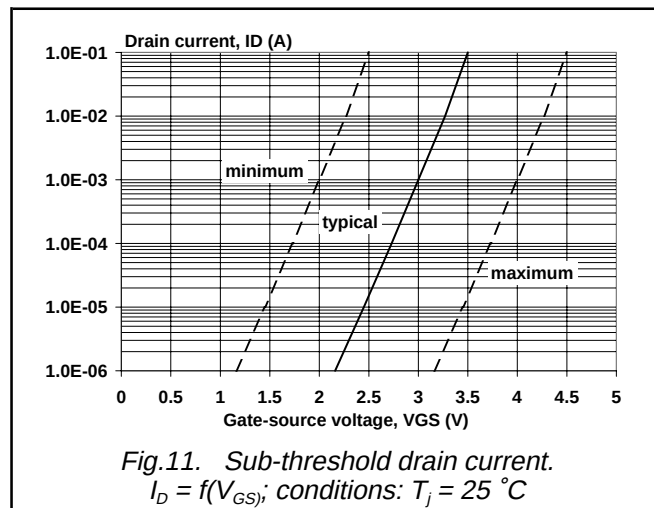
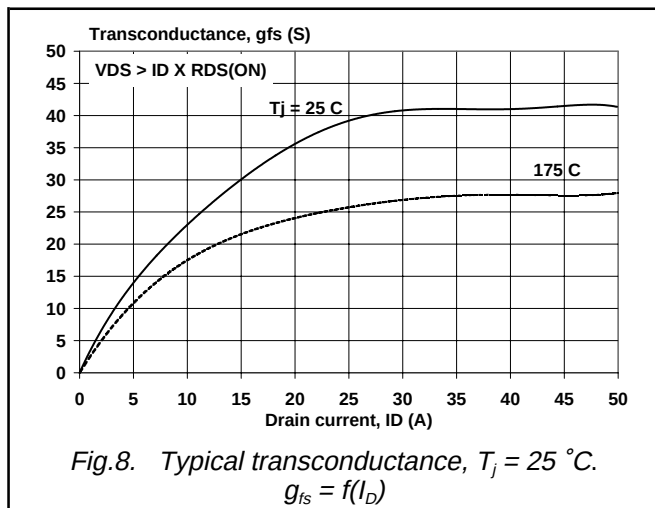
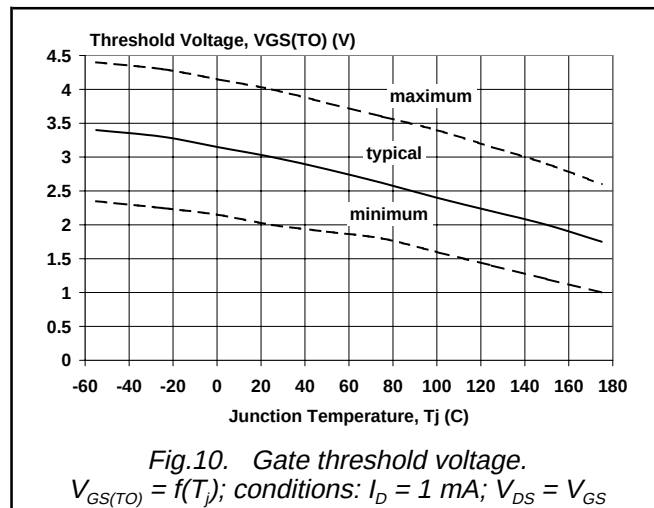
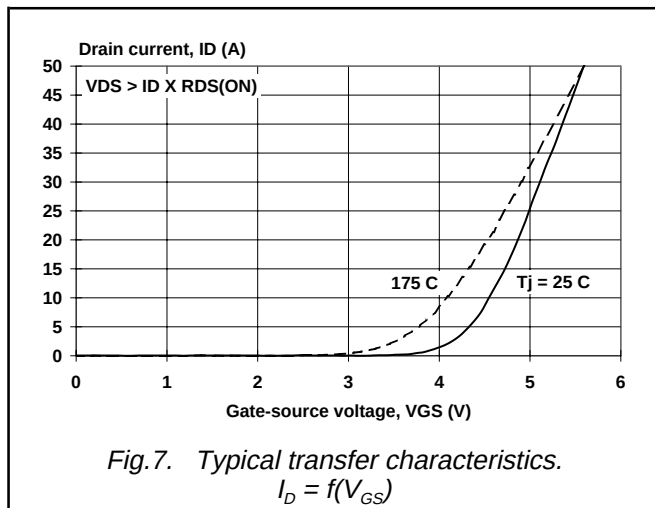


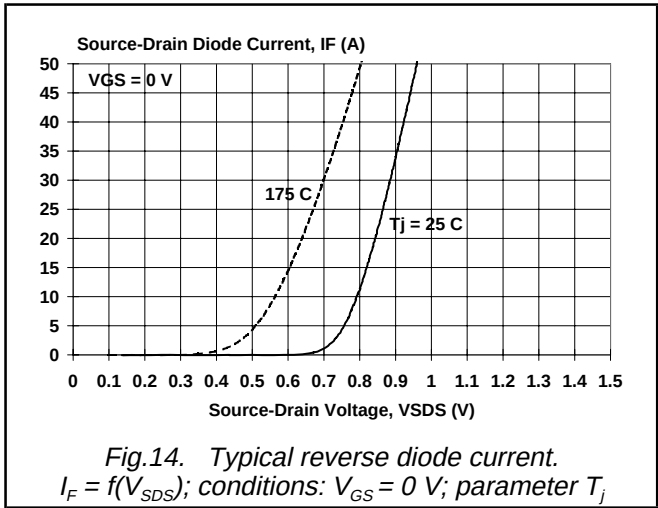
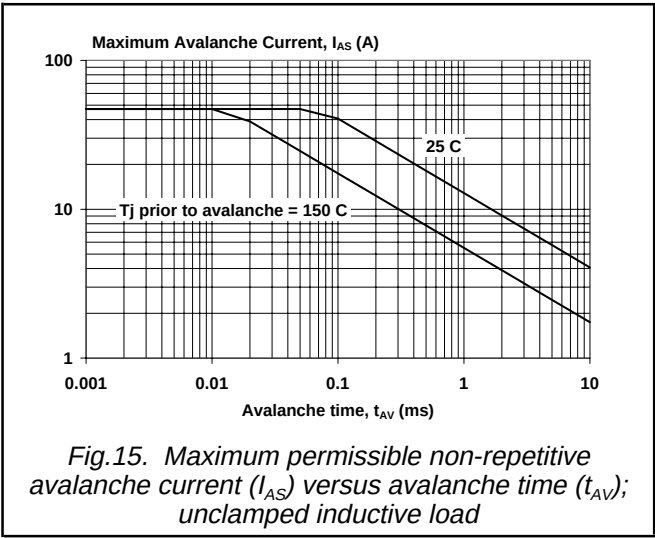
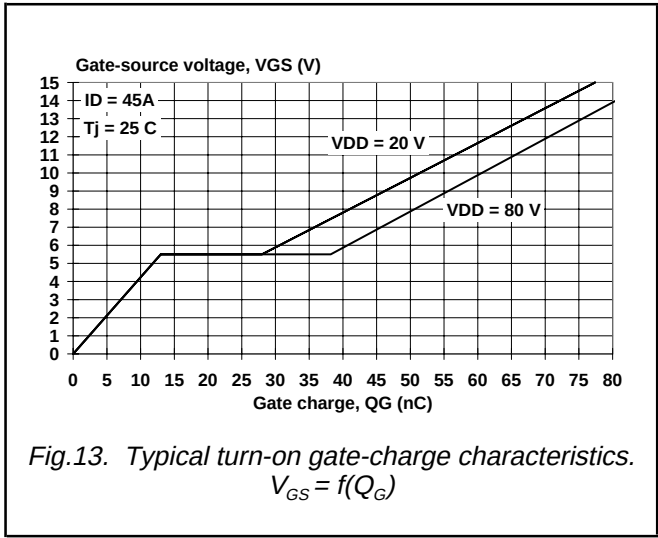
Fig.6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(on)} = f(I_D)$

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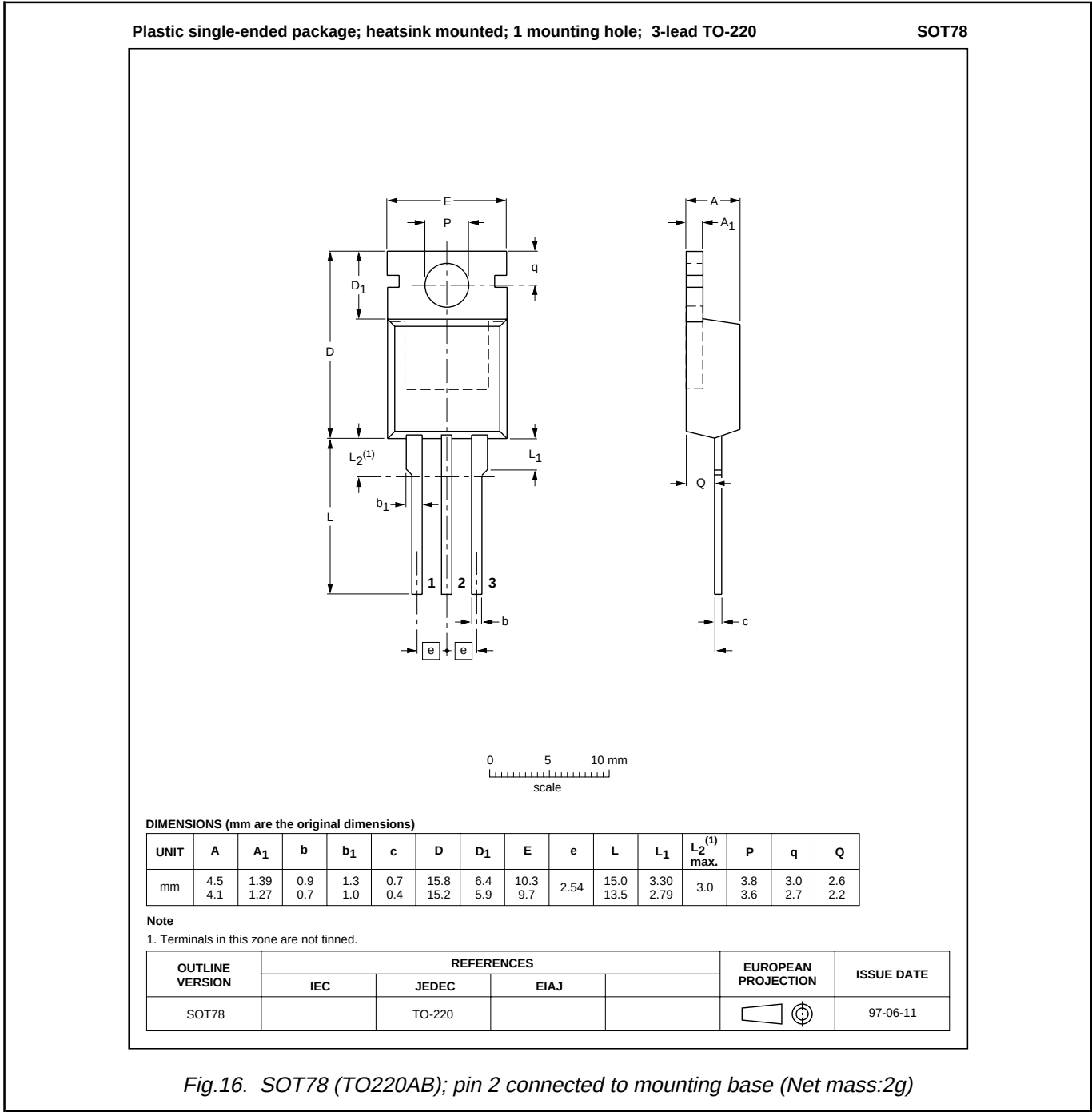
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PHW45NQ10T



N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
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MECHANICAL DATA



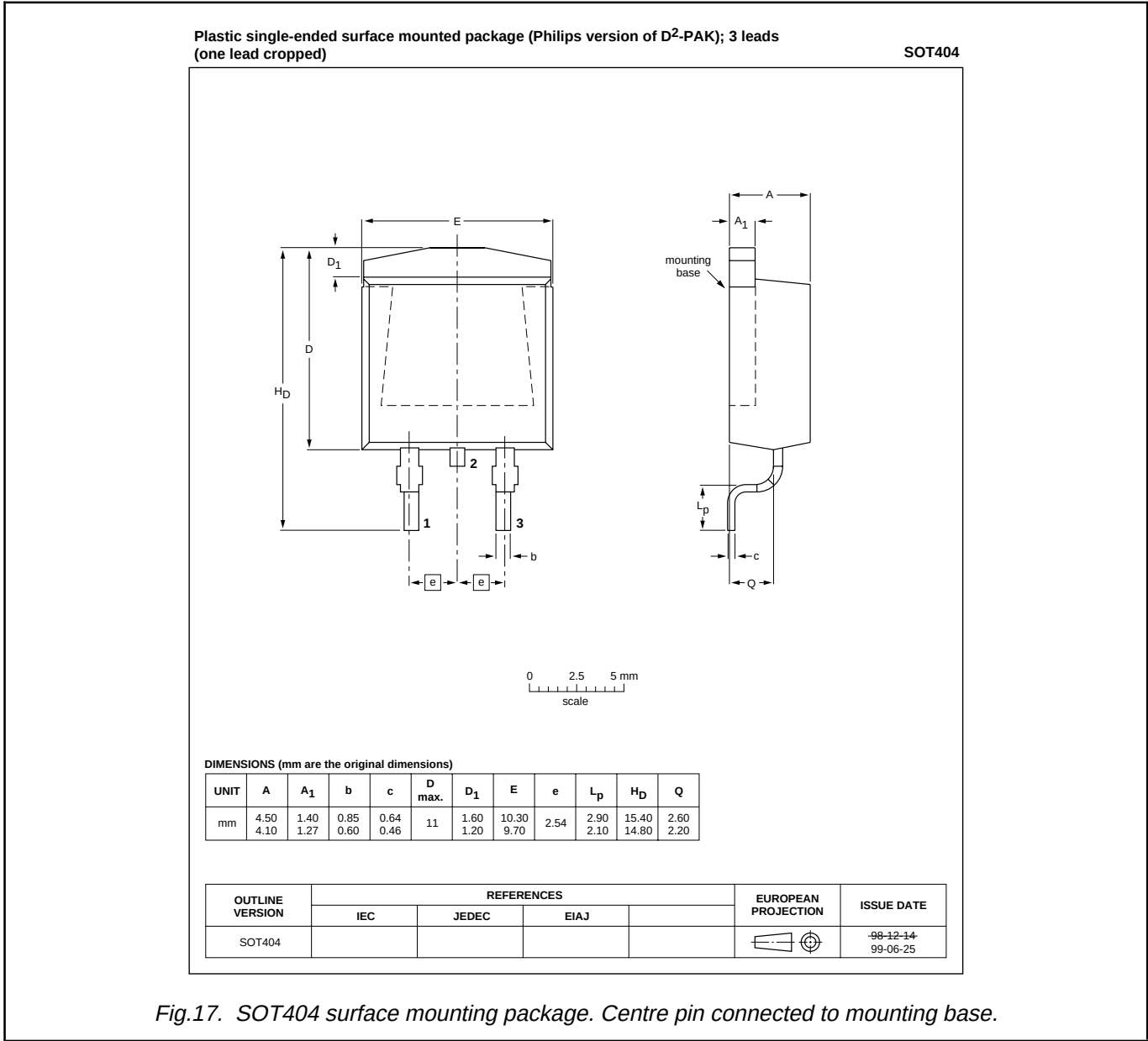
Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

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PHW45NQ10T

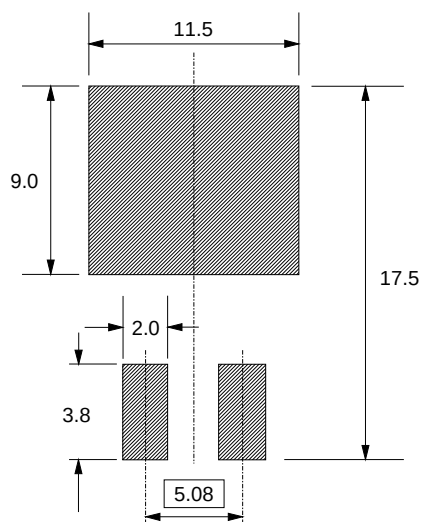
MECHANICAL DATA



Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

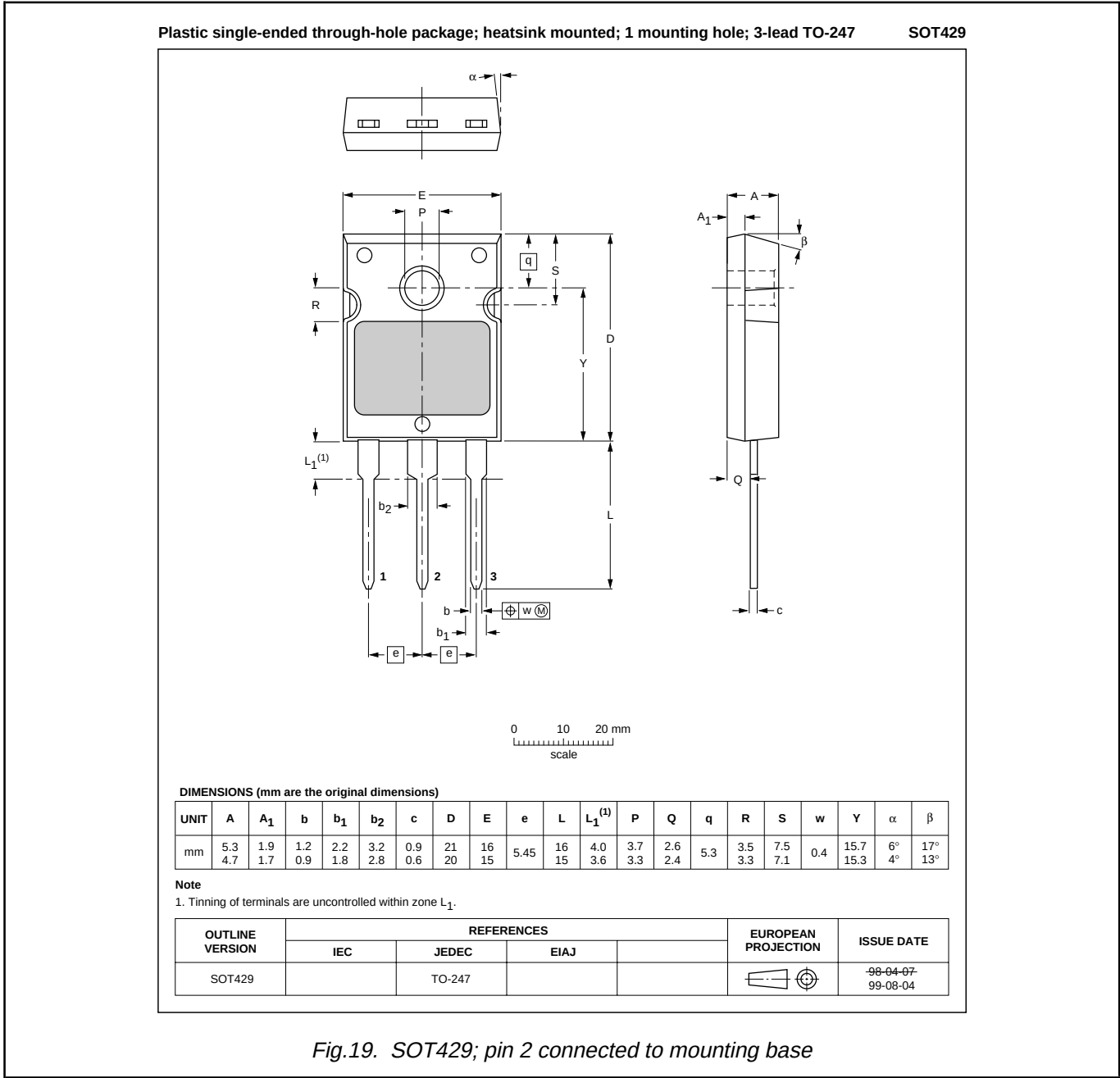
N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T**MOUNTING INSTRUCTIONS***Dimensions in mm**Fig.18. SOT404 : soldering pattern for surface mounting.*

N-channel TrenchMOS™ transistor

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PHW45NQ10T

MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT429 envelope.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOSTM transistorPHB45NQ10T, PHP45NQ10T
PHW45NQ10T

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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