

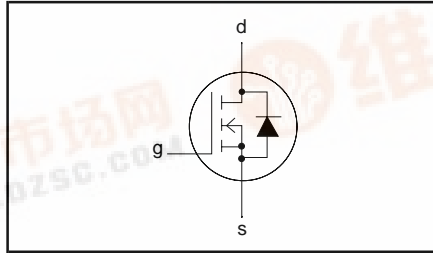
N-channel TrenchMOS™ transistor

**PHP9NQ20T, PHB9NQ20T
PHD9NQ20T**

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 200\text{ V}$
$I_D = 8.7\text{ A}$
$R_{DS(ON)} \leq 400\text{ m}\Omega$

GENERAL DESCRIPTION

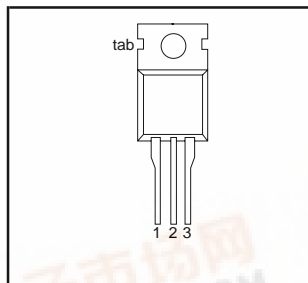
N-channel, enhancement mode field-effect power transistor using **Trench** technology, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP9NQ20T is supplied in the SOT78 (TO220AB) conventional leaded package
 The PHB9NQ20T is supplied in the SOT404 (D²PAK) surface mounting package
 The PHD9NQ20T is supplied in the SOT428 (DPAK) surface mounting package

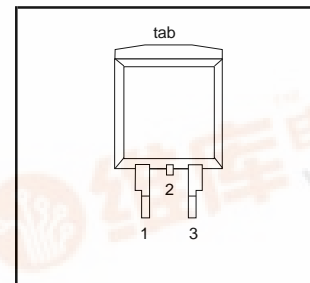
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

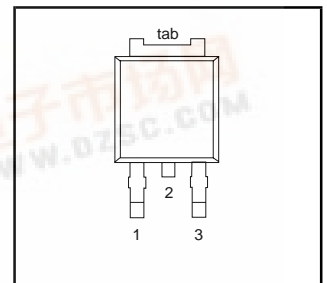
SOT78 (TO220AB)



SOT404 (D²PAK)



SOT428 (DPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$	-	200	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	200	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	8.7	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	6.2	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	35	A
P_D	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	88	W
T_j, T_{stg}	Operating junction and storage temperature		-55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin:2 of the SOT404 or SOT428 packages.



TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 7.2A$; $t_p = 100 \mu s$; T_j prior to avalanche = $25^\circ C$; $V_{DD} \leq 25 V$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 V$; refer to fig;15	-	93	mJ
I_{AS}	Peak non-repetitive avalanche current		-	8.7	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.7	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 & SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V$; $I_D = 0.25 mA$; $T_j = -55^\circ C$	200 178	-	-	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1 mA$	2	3	4	V
		$T_j = 175^\circ C$	1	-	-	V
		$T_j = -55^\circ C$	-	-	6	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 4.5 A$	-	300	400	m Ω
		$T_j = 175^\circ C$	-	-	1.16	Ω
g_{fs}	Forward transconductance	$V_{DS} = 25 V$; $I_D = 4.5 A$	3.8	6	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10 V$; $V_{DS} = 0 V$	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200 V$; $V_{GS} = 0 V$	-	0.05	10	μA
		$T_j = 175^\circ C$	-	-	500	μA
$Q_{g(tot)}$	Total gate charge	$I_D = 9 A$; $V_{DD} = 160 V$; $V_{GS} = 10 V$	-	24	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 100 V$; $R_D = 10 \Omega$;	-	8	-	ns
t_r	Turn-on rise time	$V_{GS} = 10 V$; $R_G = 5.6 \Omega$	-	19	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	25	-	ns
t_f	Turn-off fall time		-	15	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0 V$; $V_{DS} = 25 V$; $f = 1 MHz$	-	959	-	pF
C_{oss}	Output capacitance		-	93	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

TrenchMOS™ transistor

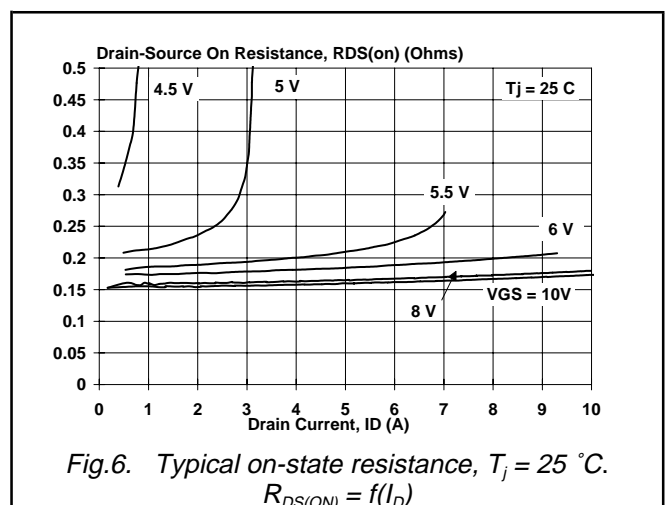
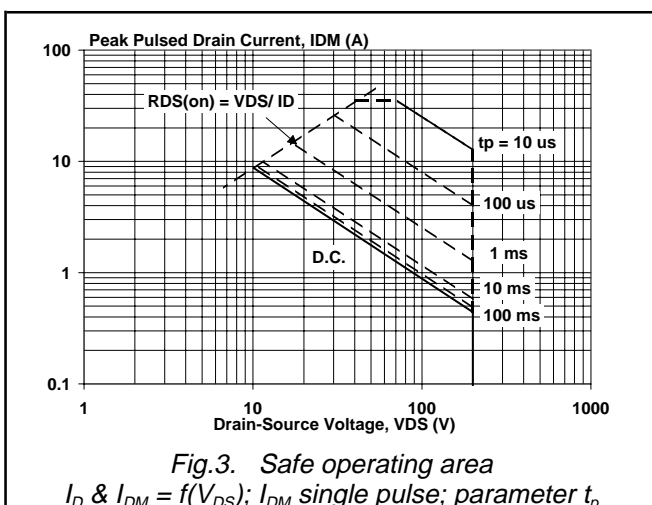
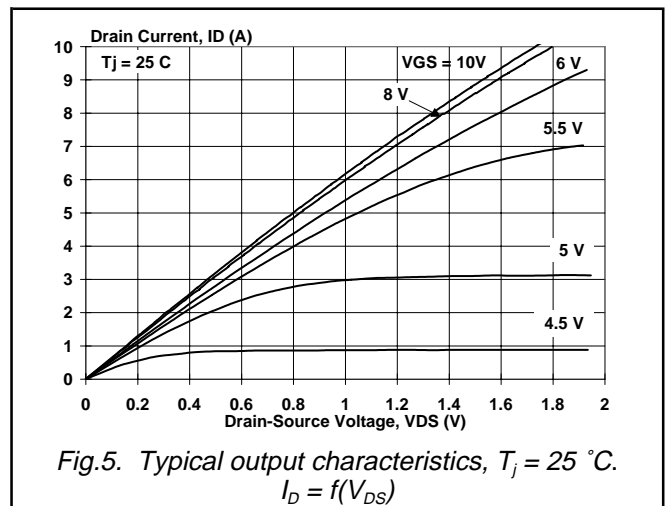
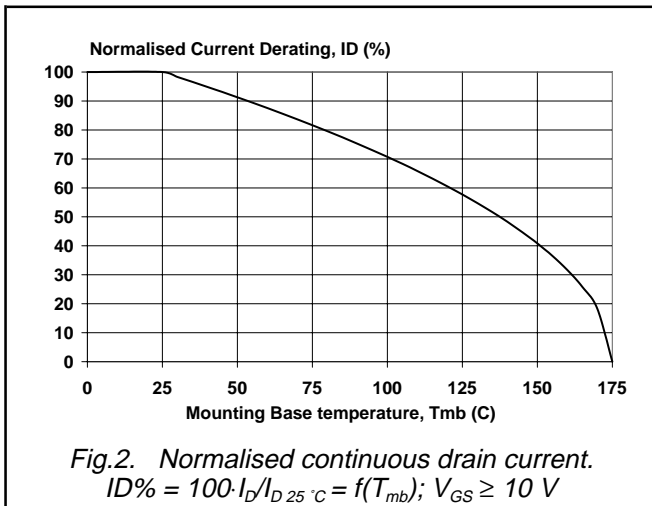
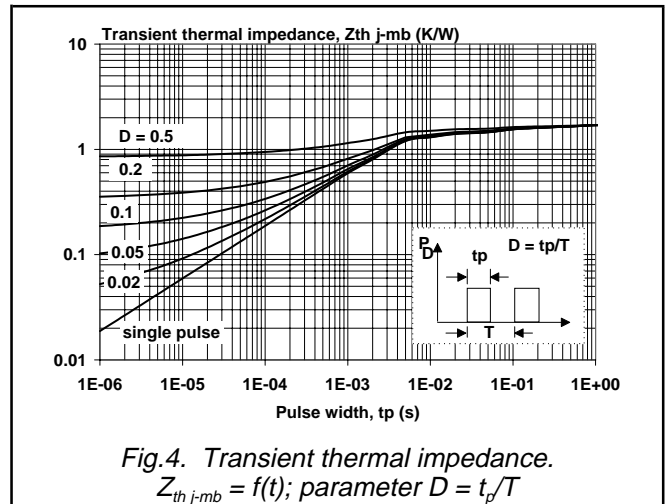
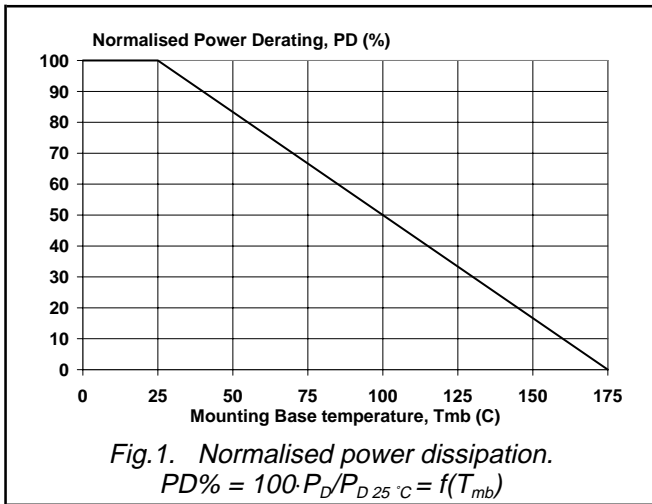
PHP9NQ20T, PHB9NQ20T

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	9	A
I_{SM}	Pulsed source current (body diode)		-	-	36	A
V_{SD}	Diode forward voltage	$I_F = 9\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.2	V
t_{rr}	Reverse recovery time	$I_F = 9\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	92	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = -10\text{ V}; V_R = 25\text{ V}$	-	0.5	-	μC

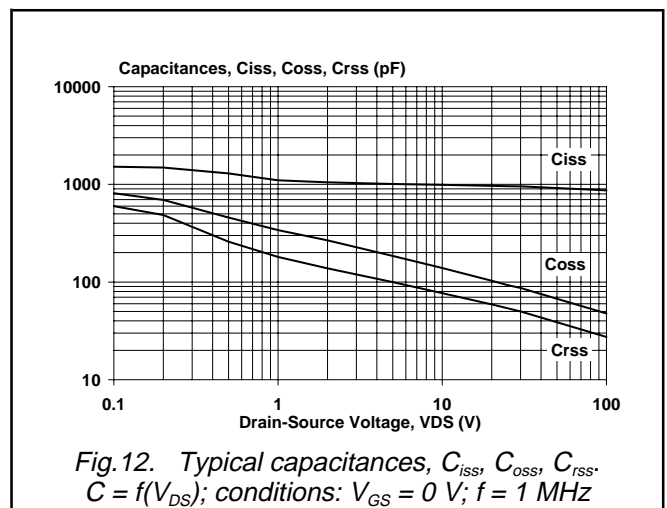
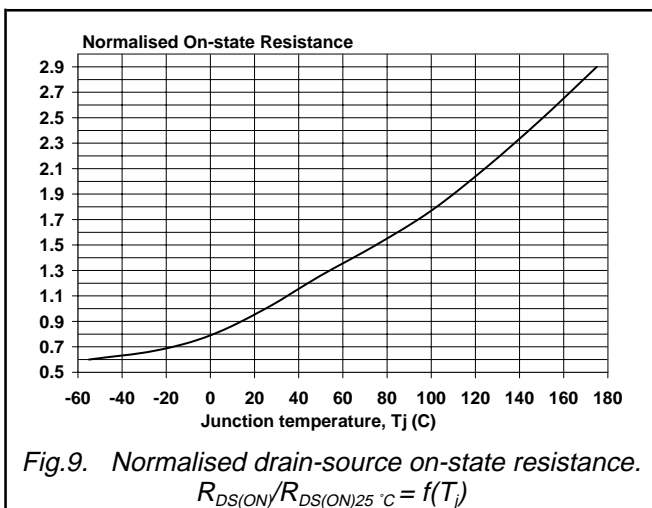
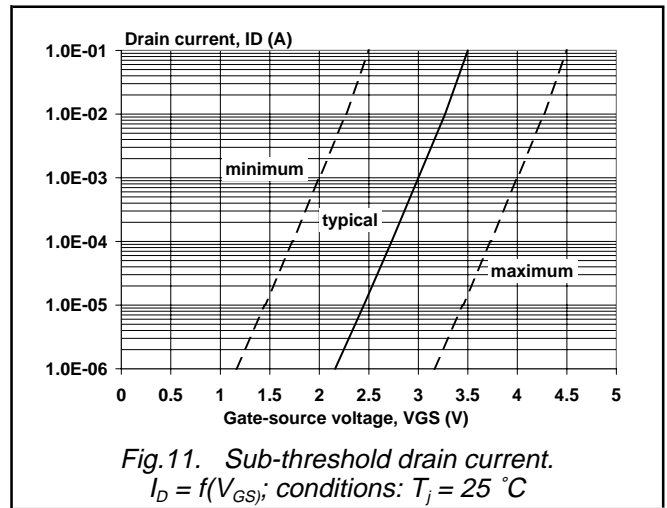
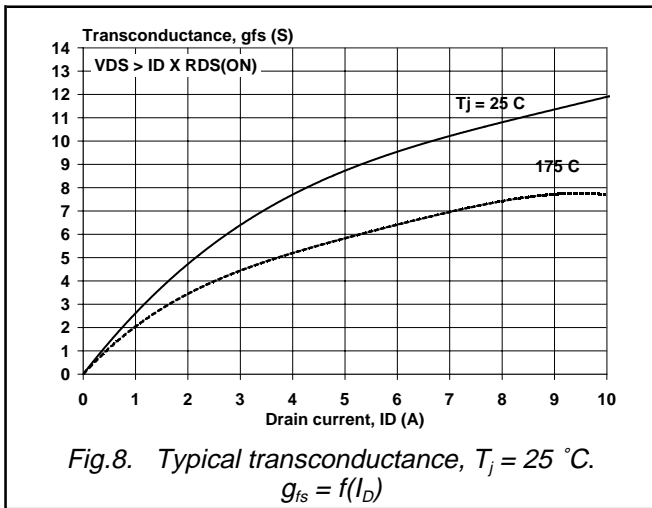
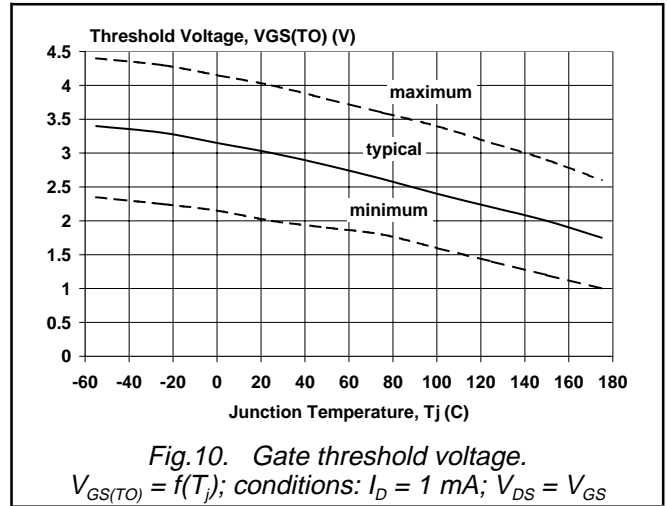
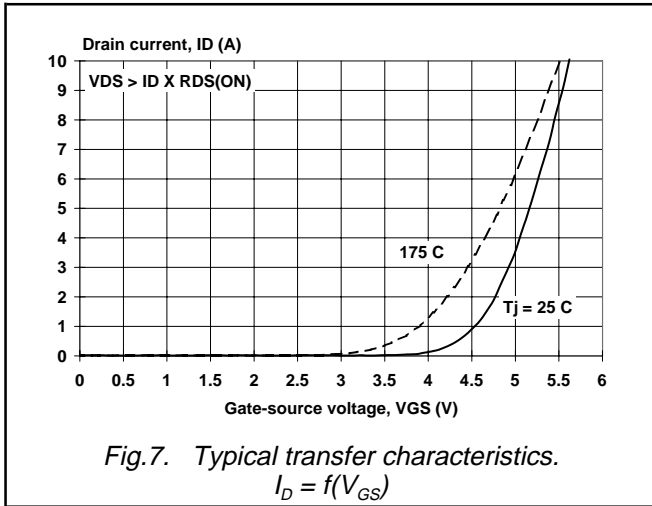
TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T



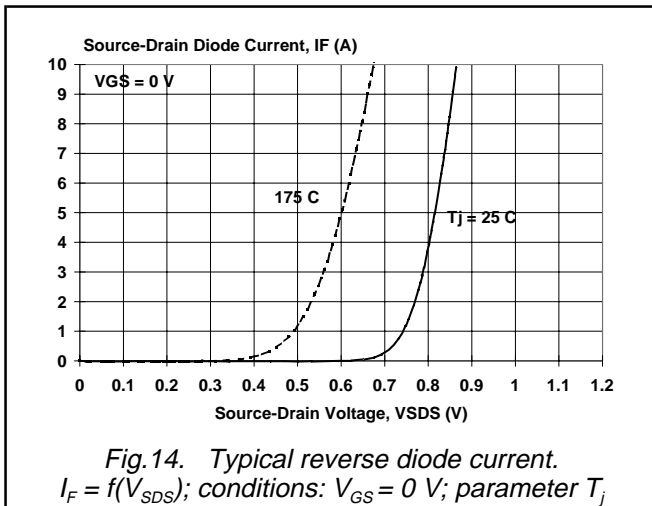
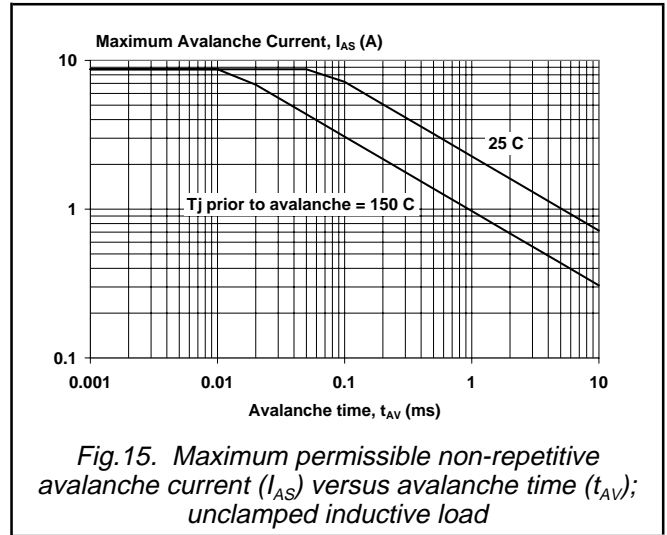
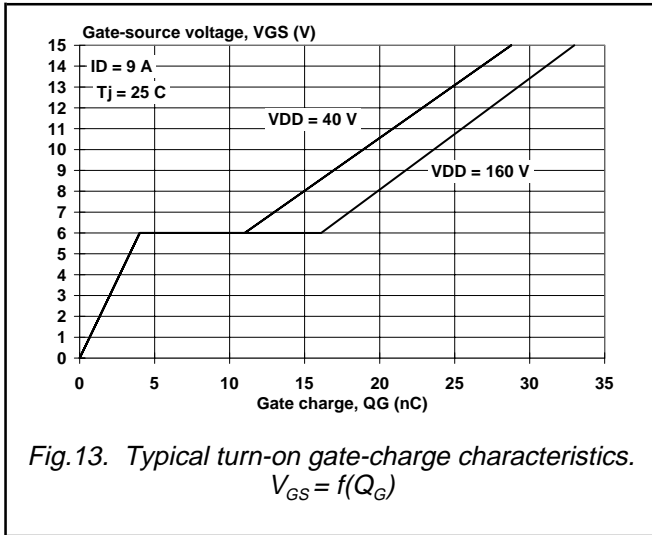
TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T



TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T



TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T

MECHANICAL DATA

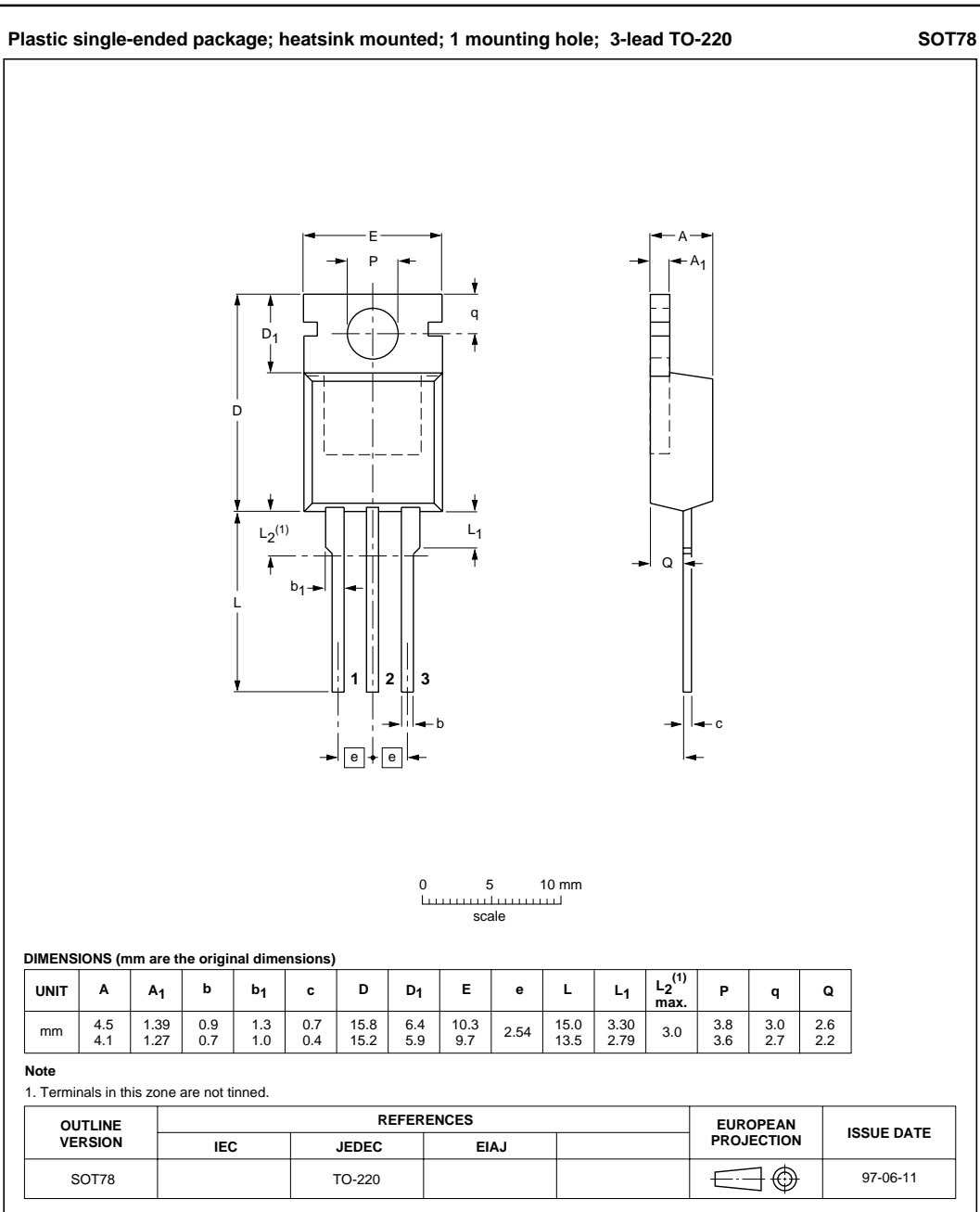


Fig.16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T

MECHANICAL DATA

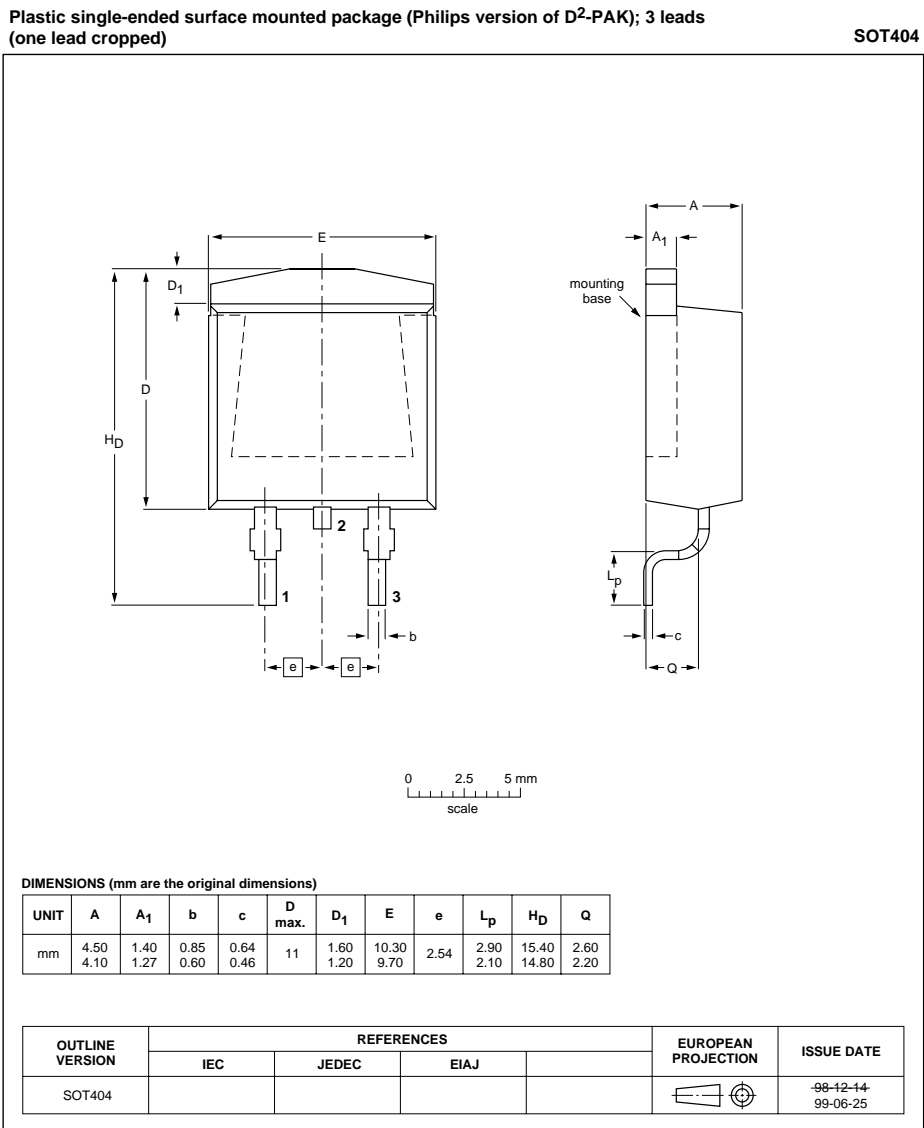


Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T

MOUNTING INSTRUCTIONS

Dimensions in mm

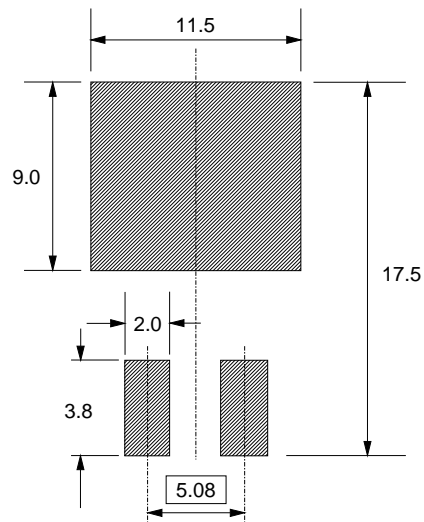


Fig.18. SOT404 : soldering pattern for surface mounting.

TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T

MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

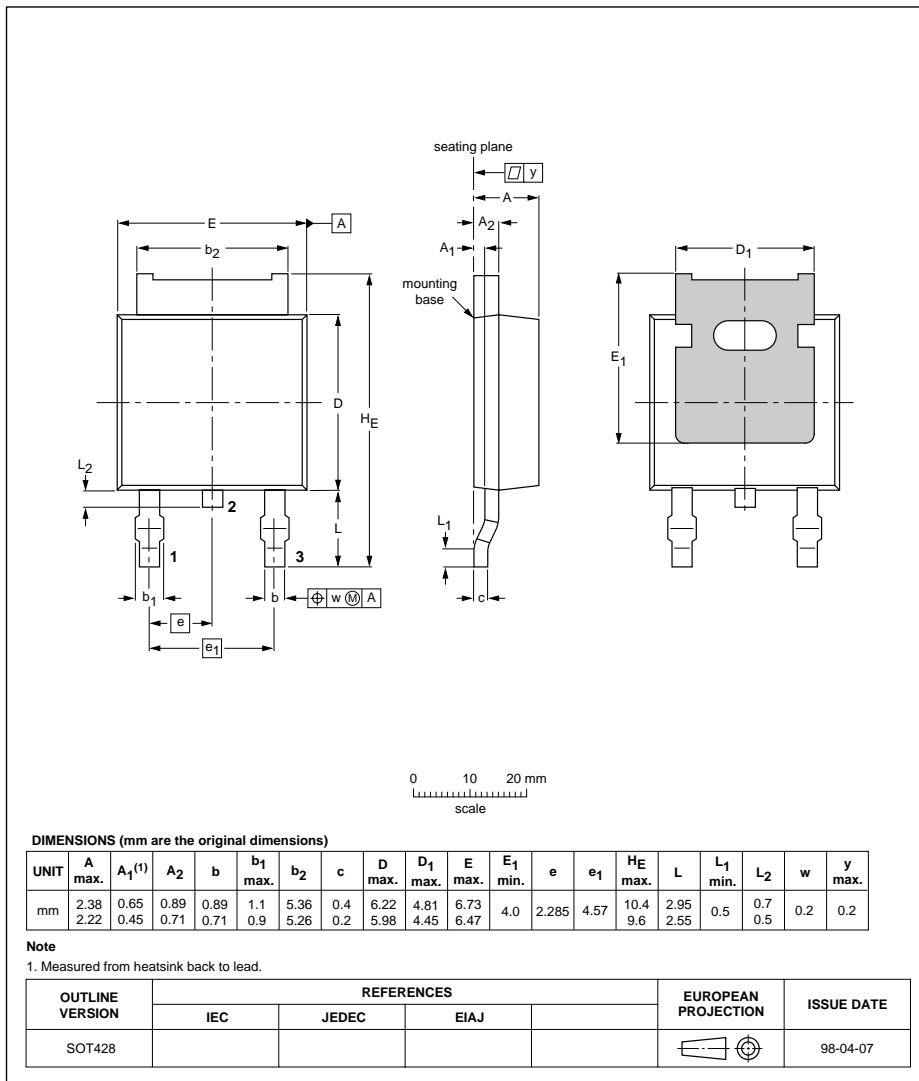


Fig. 19. SOT428 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T

MOUNTING INSTRUCTIONS

Dimensions in mm

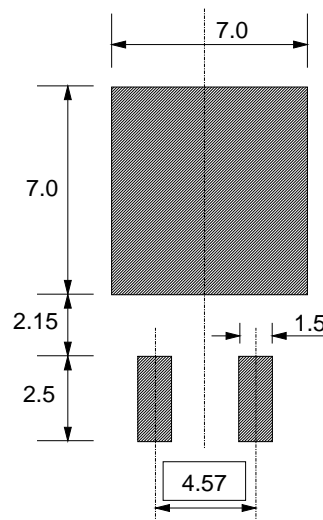


Fig.20. SOT428 : soldering pattern for surface mounting.

TrenchMOS™ transistor

PHP9NQ20T, PHB9NQ20T

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1999	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.