

DISCRETE SEMICONDUCTORS

DATA SHEET

PHN205

Dual N-channel enhancement
mode
MOS transistor

Product specification

1997 Oct 22

Supersedes data of 1997 Jun 18

File under Discrete Semiconductors, SC13b

Dual N-channel enhancement mode MOS transistor

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FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

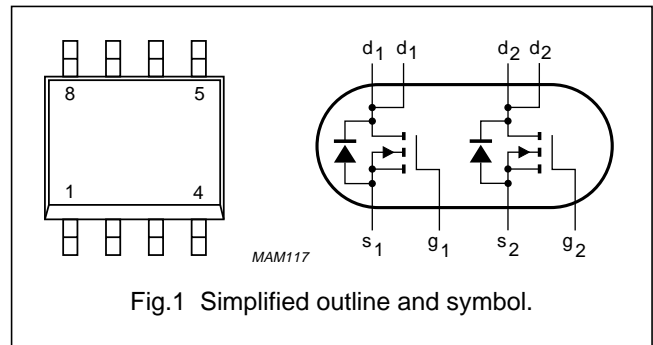
DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s ₁	source 1
2	g ₁	gate 1
3	s ₂	source 2
4	g ₂	gate 2
5	d ₂	drain 2
6	d ₂	drain 2
7	d ₁	drain 1
8	d ₁	drain 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V _{DS}	drain-source voltage (DC)		–	30	V
V _{SD}	source-drain diode forward voltage	I _S = 1.25 A	–	1	V
V _{GS}	gate-source voltage (DC)		–	±20	V
V _{GSth}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS}	1	2.8	V
I _D	drain current (DC)	T _s = 80 °C	–	6.4	A
R _{DSon}	drain-source on-state resistance	I _D = 3.2 A; V _{GS} = 10 V	–	50	mΩ
P _{tot}	total power dissipation	T _s = 80 °C	–	3.5	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
I_D	drain current (DC)	$T_s = 80\text{ }^\circ\text{C}$; note 1	–	6.4	A
I_{DM}	peak drain current	note 2	–	25	A
P_{tot}	total power dissipation	$T_s = 80\text{ }^\circ\text{C}$; note 3	–	3.5	W
		$T_{amb} = 25\text{ }^\circ\text{C}$; note 4	–	2.6	W
		$T_{amb} = 25\text{ }^\circ\text{C}$; note 5	–	1.1	W
		$T_{amb} = 25\text{ }^\circ\text{C}$; note 6	–	1.5	W
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	operating junction temperature		–65	+150	$^\circ\text{C}$
Source-drain diode					
I_S	source current (DC)	$T_s = 80\text{ }^\circ\text{C}$	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

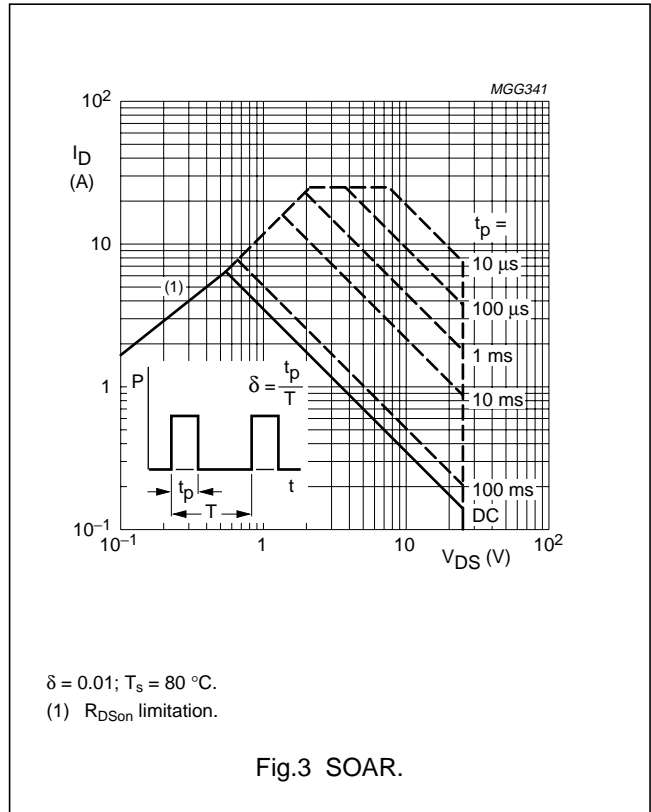
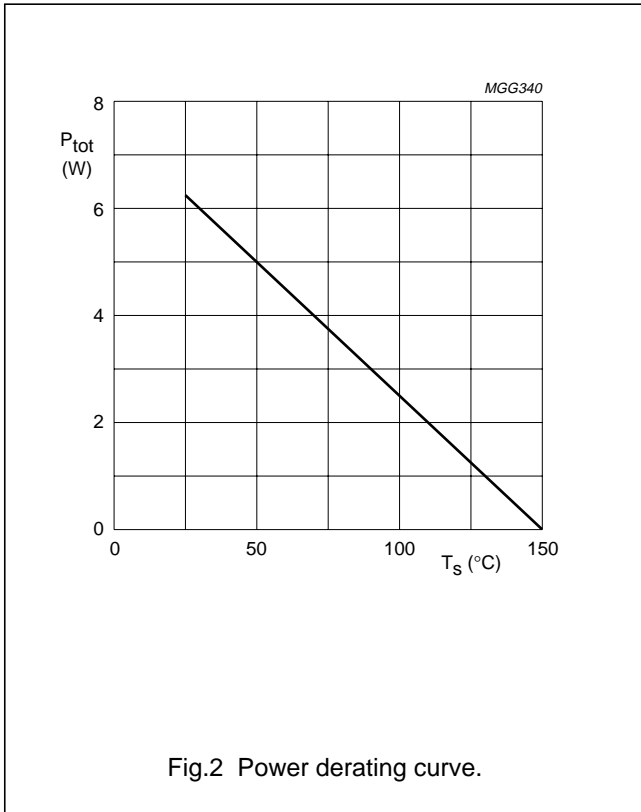
- T_s is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
- Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.
- Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.
- Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	20	K/W

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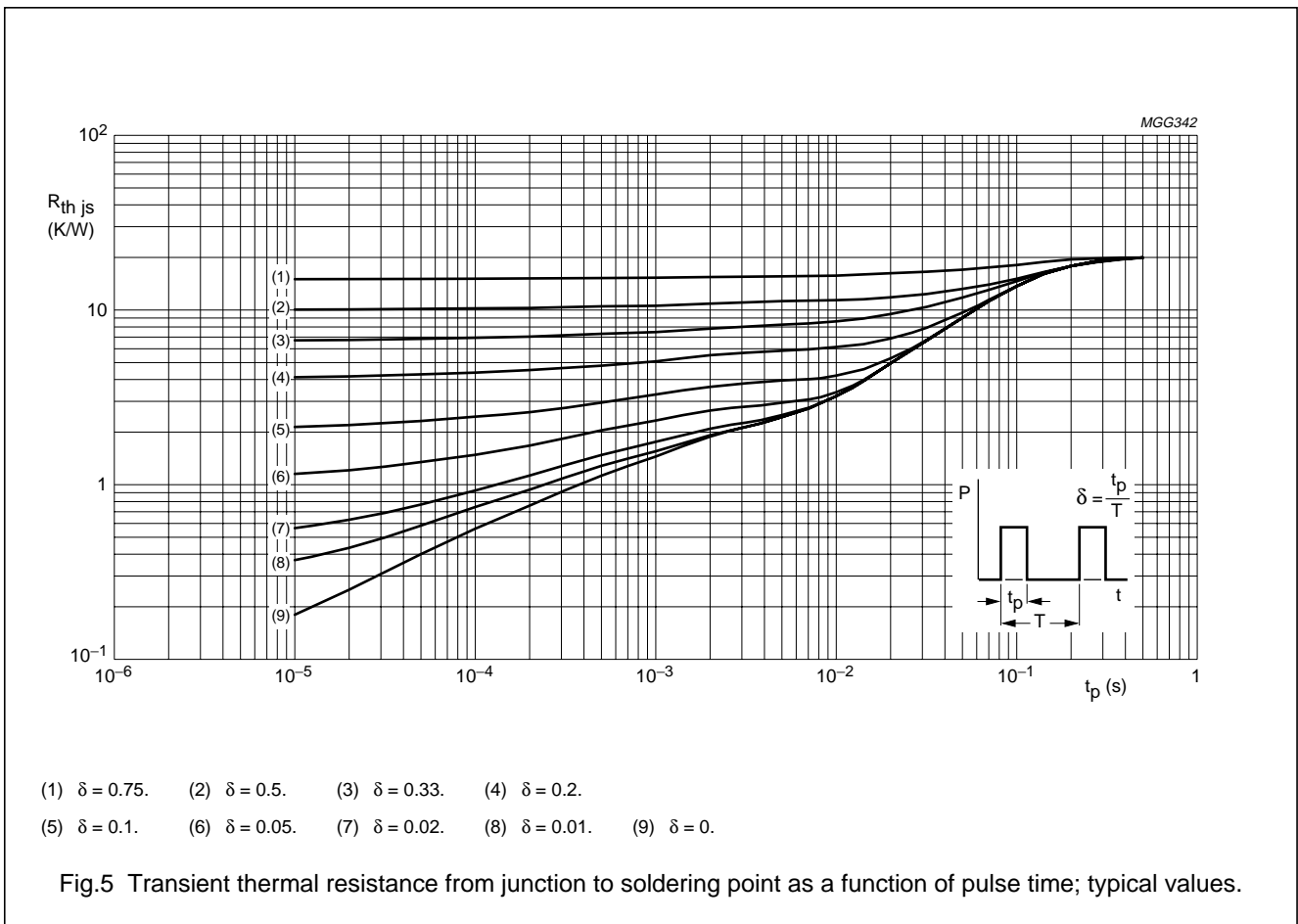
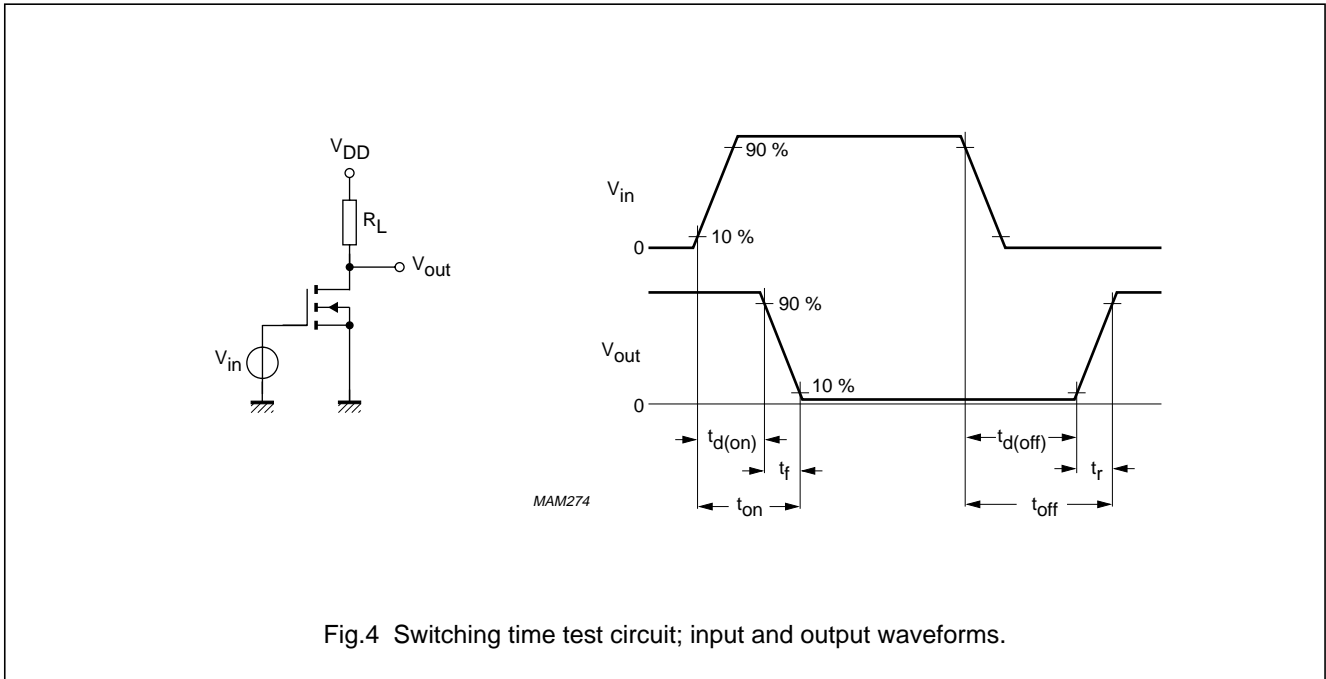
CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 10\ \mu\text{A}$	30	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = 1\ \text{mA}$	1	–	2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 24\ \text{V}$	–	–	100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}; I_D = 1.6\ \text{A}$	–	–	0.1	Ω
		$V_{GS} = 10\ \text{V}; I_D = 3.2\ \text{A}$	–	–	0.05	Ω
C_{iss}	input capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	450	–	pF
C_{oss}	output capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	200	–	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	100	–	pF
Q_G	total gate charge	$V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 3.2\ \text{A}$	–	15	–	nC
Q_{GS}	gate-source charge	$V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 3.2\ \text{A}$	–	1	–	nC
Q_{GD}	gate-drain charge	$V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 3.2\ \text{A}$	–	5	–	nC
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0\ \text{to}\ 10\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_{gen} = 6\ \Omega; \text{see Fig.4}$	–	7	–	ns
t_f	fall time	$V_{GS} = 0\ \text{to}\ 10\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_{gen} = 6\ \Omega; \text{see Fig.4}$	–	8	–	ns
t_{on}	turn-on switching time	$V_{GS} = 0\ \text{to}\ 10\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_{gen} = 6\ \Omega; \text{see Fig.4}$	–	15	–	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = 10\ \text{to}\ 0\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_{gen} = 6\ \Omega; \text{see Fig.4}$	–	20	–	ns
t_r	rise time	$V_{GS} = 10\ \text{to}\ 0\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_{gen} = 6\ \Omega; \text{see Fig.4}$	–	12	–	ns
t_{off}	turn-off switching time	$V_{GS} = 10\ \text{to}\ 0\ \text{V}; V_{DD} = 15\ \text{V};$ $I_D = 1\ \text{A}; R_{gen} = 6\ \Omega; \text{see Fig.4}$	–	32	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0; I_S = 1.25\ \text{A}$	–	–	1	V
t_{rr}	reverse recovery time	$I_S = 1.25\ \text{A}; di/dt = -100\ \text{A}/\mu\text{s}$	–	45	–	ns

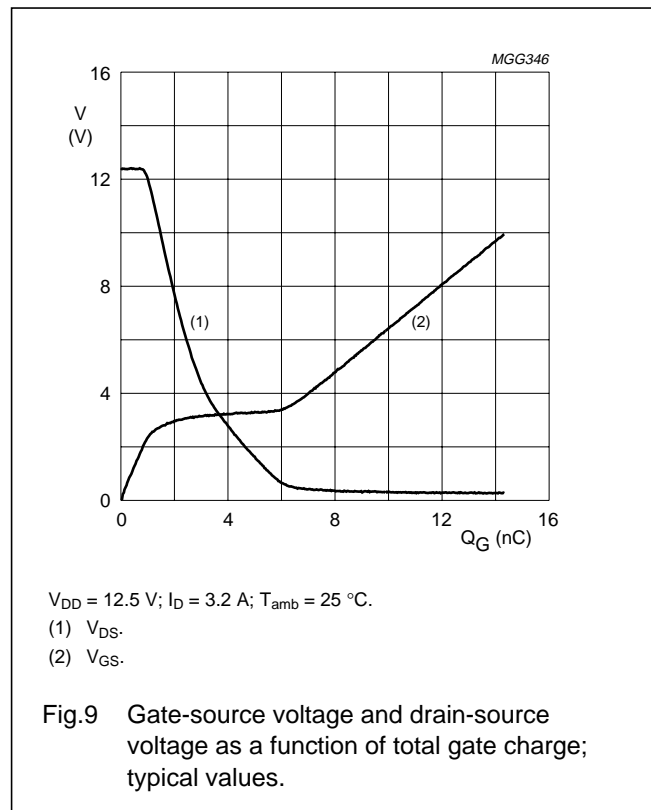
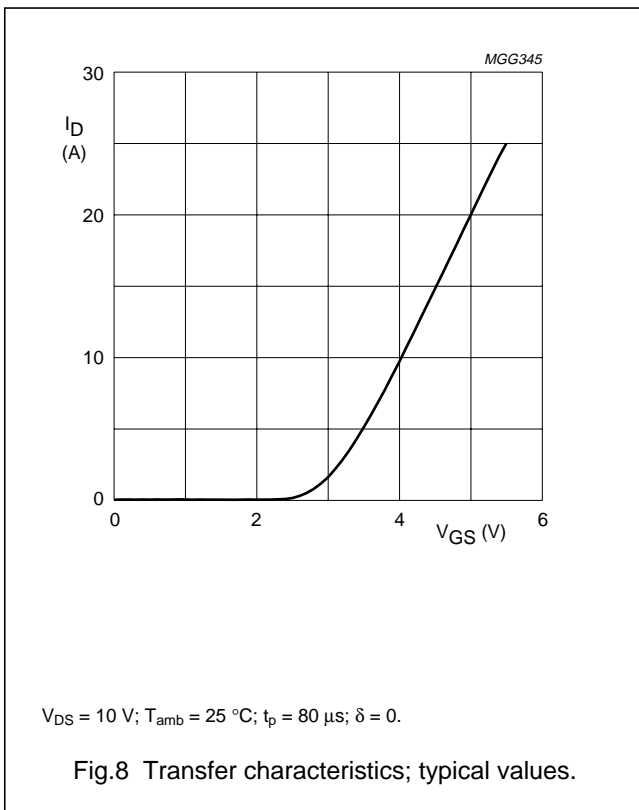
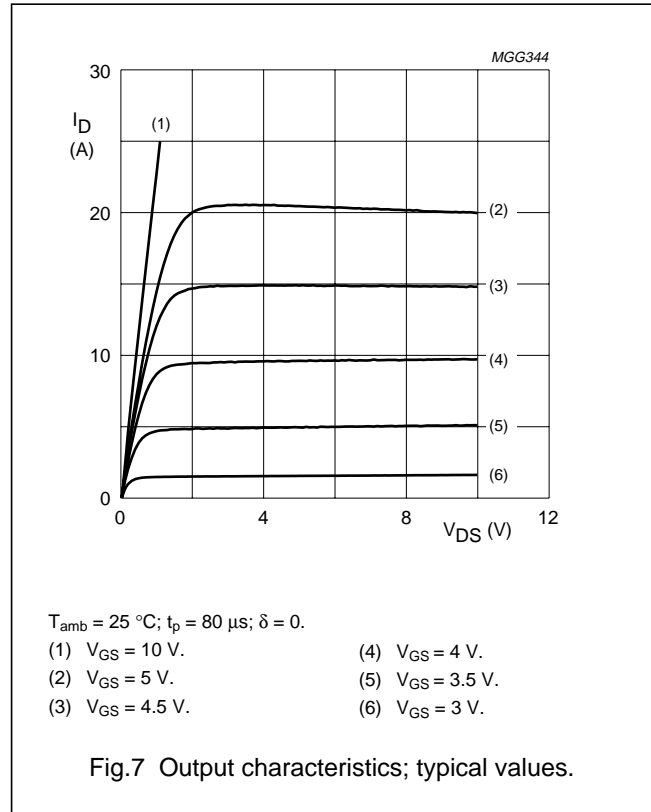
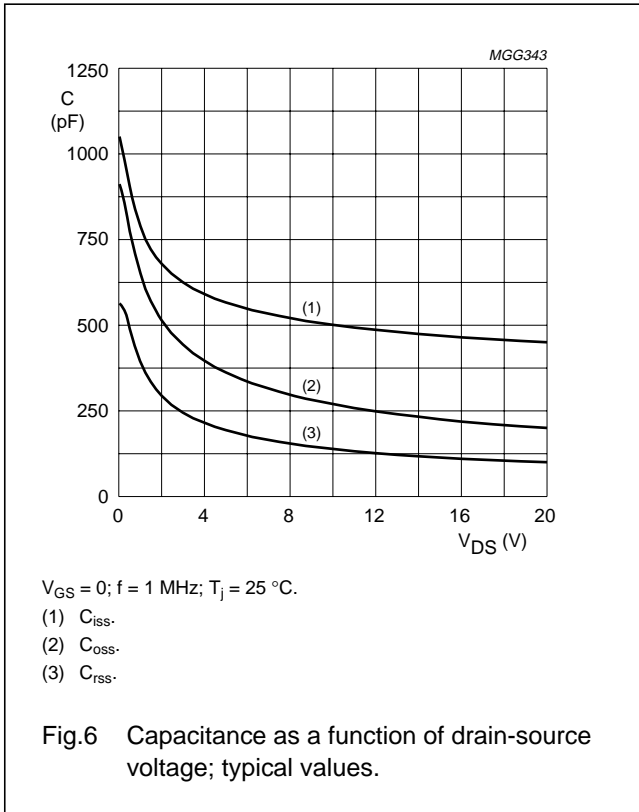
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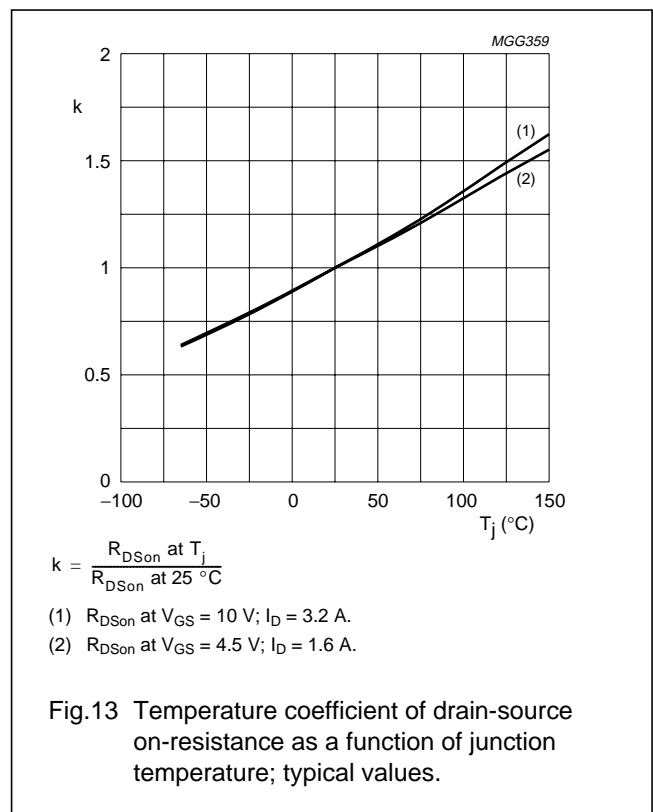
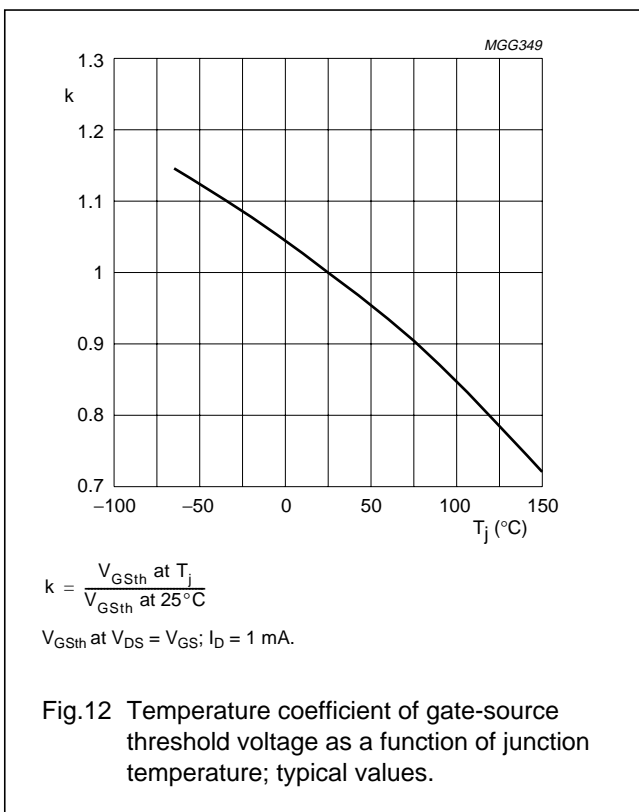
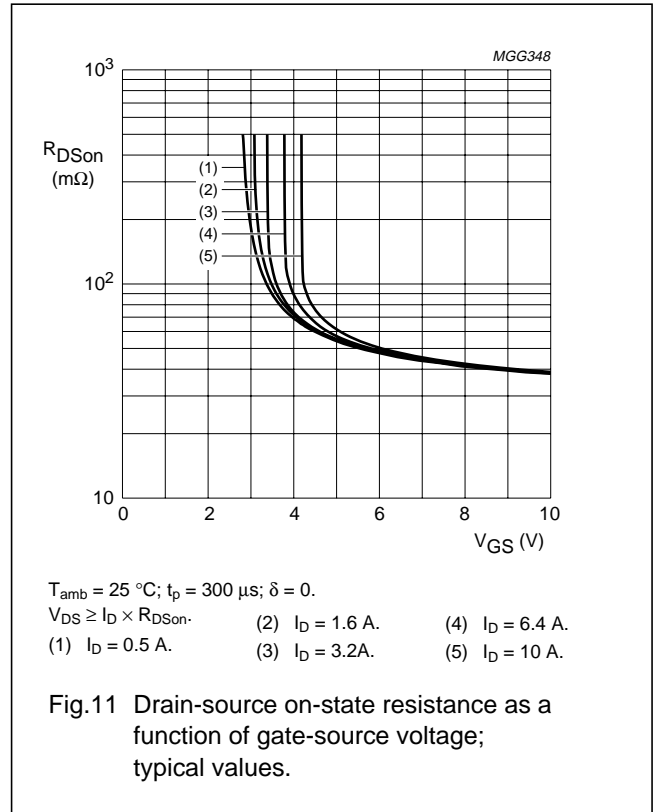
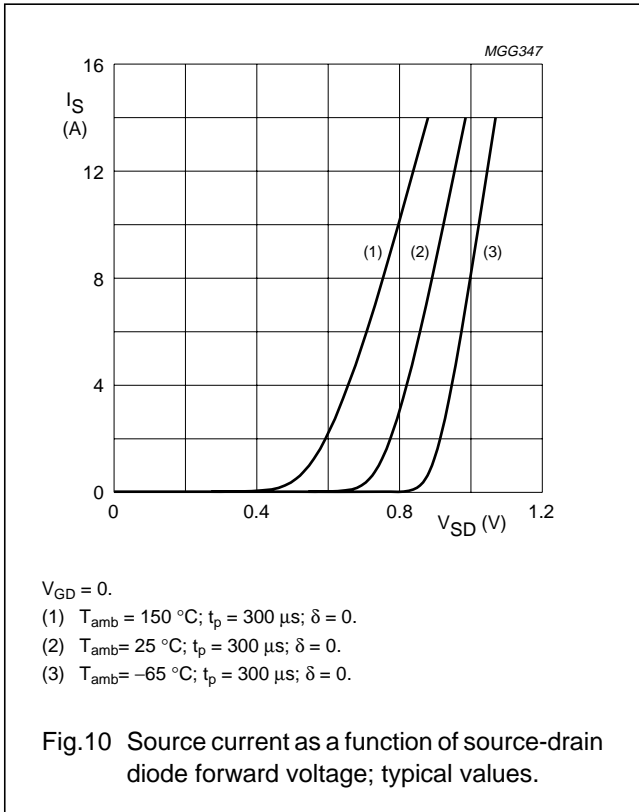
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Dual N-channel enhancement mode MOS transistor

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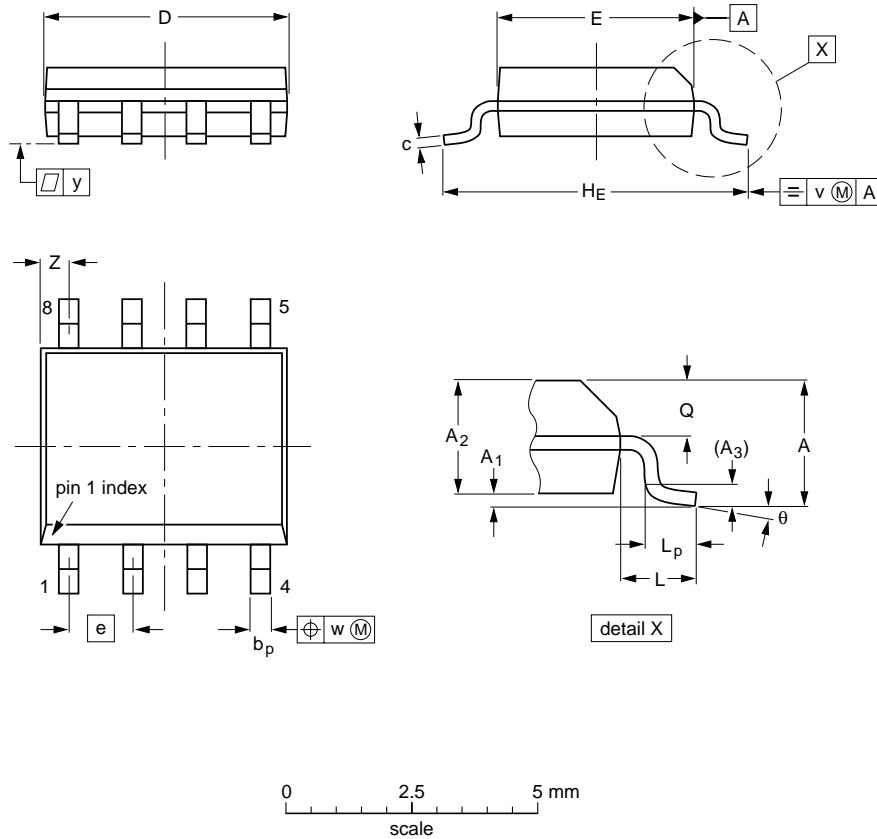
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PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT96-1	076E03S	MS-012AA			95-02-04 97-05-22

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

137107/00/03/pp12

Date of release: 1997 Oct 22

Document order number: 9397 750 02978

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