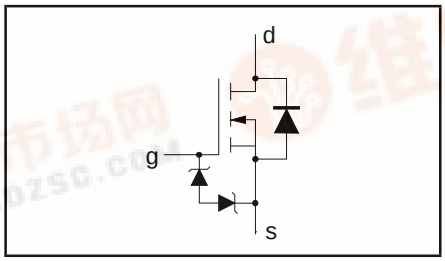
TrenchMOS™ transistor Logic level FET

PHT6N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Surface mounting package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 5.9 A

$R_{DS(ON)} \leq 30\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 28\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

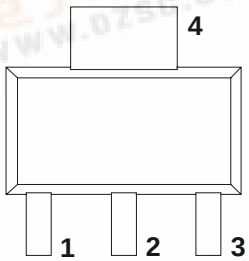
N-channel enhancement mode logic level field-effect power transistor using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHT6N03LT is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT223



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	30	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{amb} = 25 ˚C; V_{GS} = 10 V	-	5.9	A
		T_{amb} = 100 ˚C; V_{GS} = 10 V	-	4.1	A
I_{DM}	Pulsed drain current		-	23.6	A
P_D	Total power dissipation	T_{amb} = 25 ˚C	-	1.8	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	˚C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	mounted on any pcb	-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	mounted on test pcb of fig:17	-	70	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = 1 mA	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 3.2 A	-	24	30	mΩ
		V_{GS} = 10 V; I_D = 3.2 A	-	18	28	mΩ
		V_{GS} = 5 V; I_D = 3.2 A; T_j = 150˚C	-	-	51	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.9 A	8	14	-	S
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 150˚C	-	-	10	µA
$Q_{g(tot)}$	Total gate charge	I_D = 5.9 A; V_{DD} = 24 V; V_{GS} = 5 V	-	24	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	11	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 5.9 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	5.9	A
I_{SM}	Pulsed source current (body diode)		-	-	10	A
V_{SD}	Diode forward voltage	I_F = 5.9 A; V_{GS} = 0 V	-	0.75	1.2	V
t_{rr}	Reverse recovery time	I_F = 5.9 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 5.9 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 ˚C	-	60	mJ

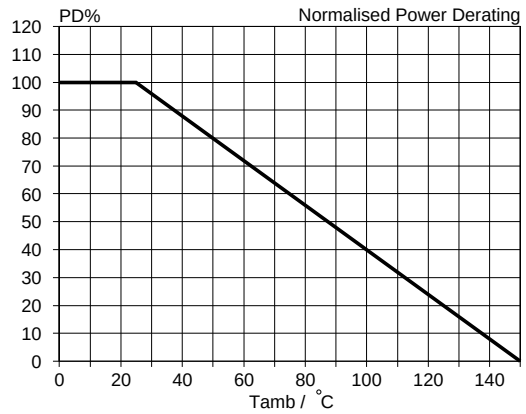


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{amb})

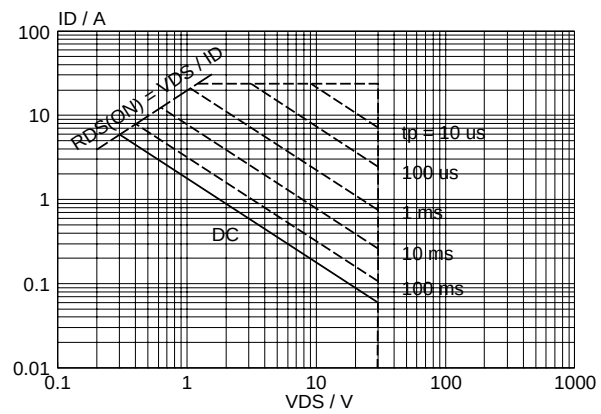


Fig.3. Safe operating area. T_{amb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

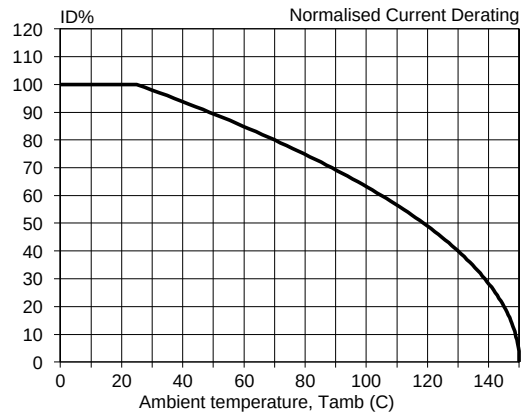


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{amb}); conditions: $V_{GS} \geq$ 5 V

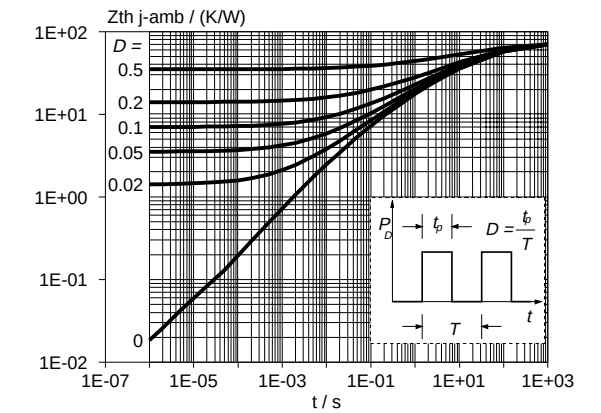


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

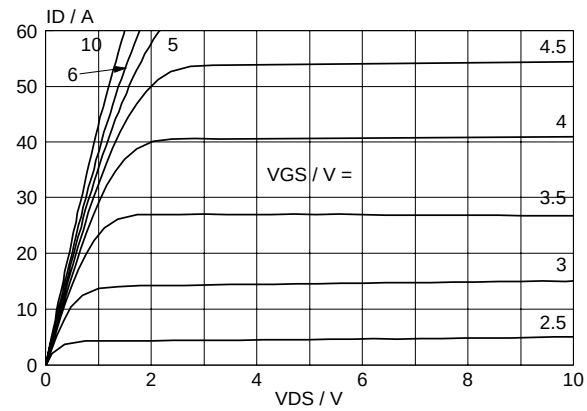


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

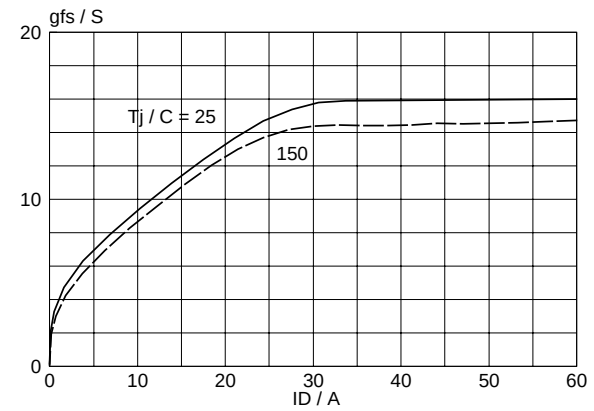


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

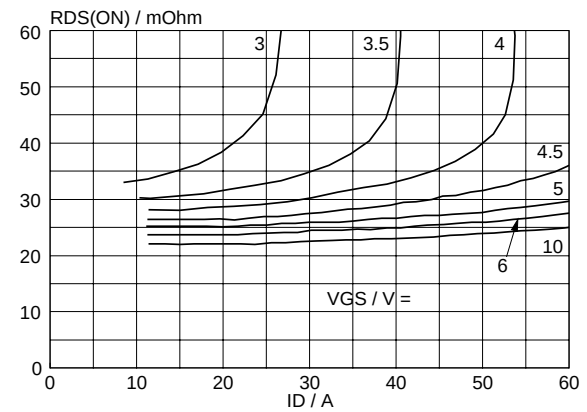


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

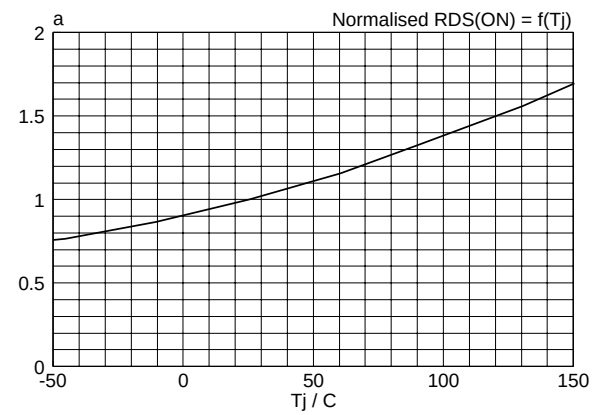


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.2 A; V_{GS} = 5 V

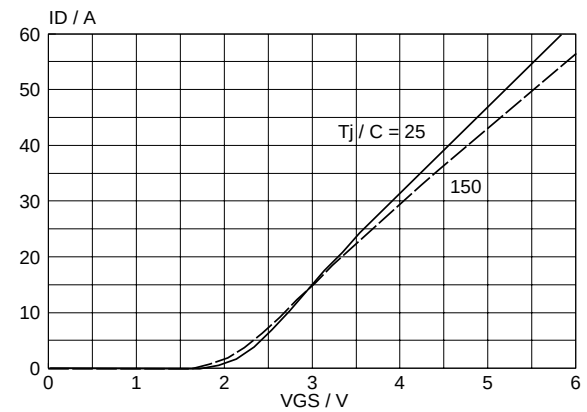


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

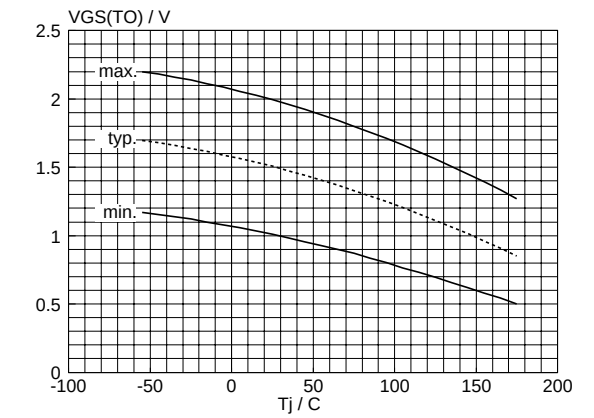


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

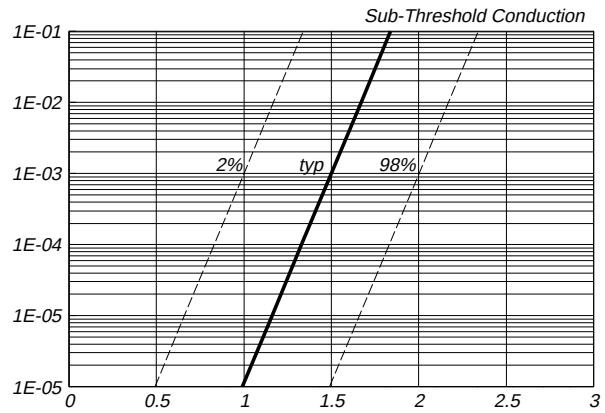


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

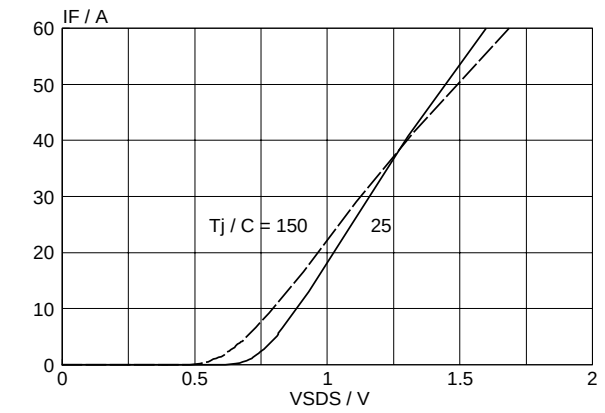


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

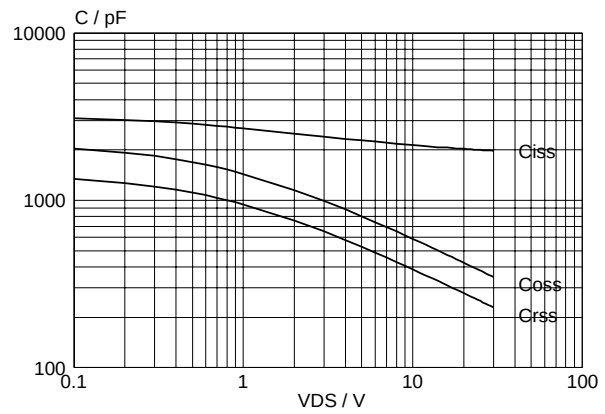


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

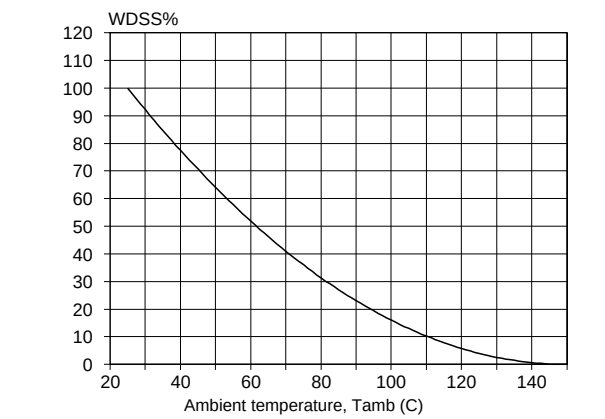


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = $f(T_{amb})$; conditions: I_D = 5.9 A

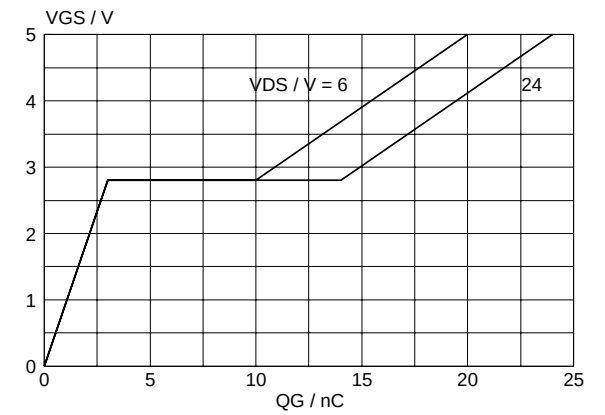


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 5.9 A; parameter V_{DS}

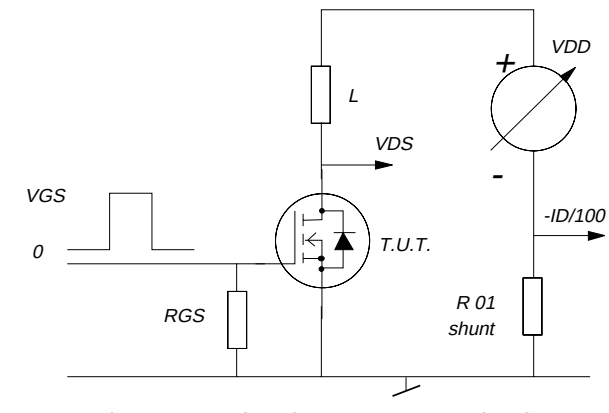


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PRINTED CIRCUIT BOARD

Dimensions in mm.

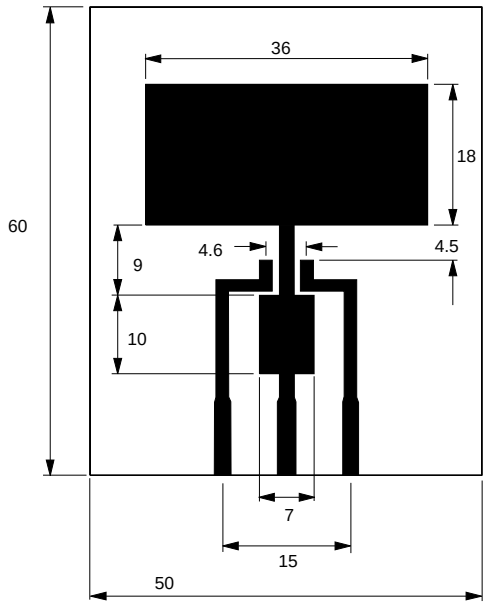


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).