PowerMOS transistor
Isolated version of PHP4N40E

PHX2N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

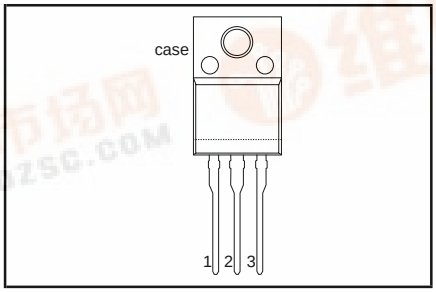
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	2.4	A
P_{tot}	Total power dissipation	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.8	Ω

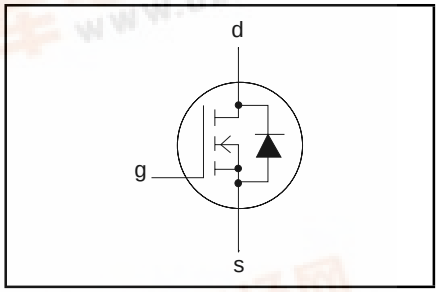
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 ˚C	-	2.4	A
		T_{hs} = 100 ˚C	-	1.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 ˚C	-	9.6	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 ˚C	-	2.4	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 ˚C	-	9.6	A
P_{tot}	Total power dissipation	T_{hs} = 25 ˚C	-	25	W
T_{stg}	Storage temperature		-55	150	˚C
T_j	Junction temperature		-	150	˚C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 4.2 A ; $V_{DD} \le$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25˚C prior to surge	-	190	mJ
		T_j = 100˚C prior to surge	-	35	mJ
W_{DSR} [1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 4.2 A ; $V_{DD} \le$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \le$ 150 ˚C	-	5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 ˚C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 ˚C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.1 A	-	1.5	1.8	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 4.2 A ;V_{GS} = 0 V	-	1.2	1.6	V

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 2.1 A	1.7	2.0	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Feedback capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	- - -	360 60 25	500 80 60	pF pF pF
$Q_{g(tot)}$ Q_{gs} Q_{gd}	Total gate charge Gate to source charge Gate to drain (Miller) charge	V_{GS} = 10 V; I_D = 4.2 A; V_{DS} = 320 V	- - -	19 2 10	- - -	nC nC nC
$t_{d\ on}$ t_r $t_{d\ off}$ t_f	Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time	V_{DD} = 30 V; I_D = 2.5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{GEN} = 50 Ω	- - - -	15 40 50 30	20 60 65 40	ns ns ns ns
t_{rr} Q_{rr}	Source-drain diode reverse recovery time Source-drain diode reverse recovery charge	I_F = 4.2 A; -dI_F/dt = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	- -	300 2.5	- -	ns µC
L_d L_s	Internal drain inductance Internal source inductance	Measured from drain lead 6 mm from package to centre of die Measured from source lead 6 mm from package to source bond pad	- -	4.5 7.5	- -	nH nH

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

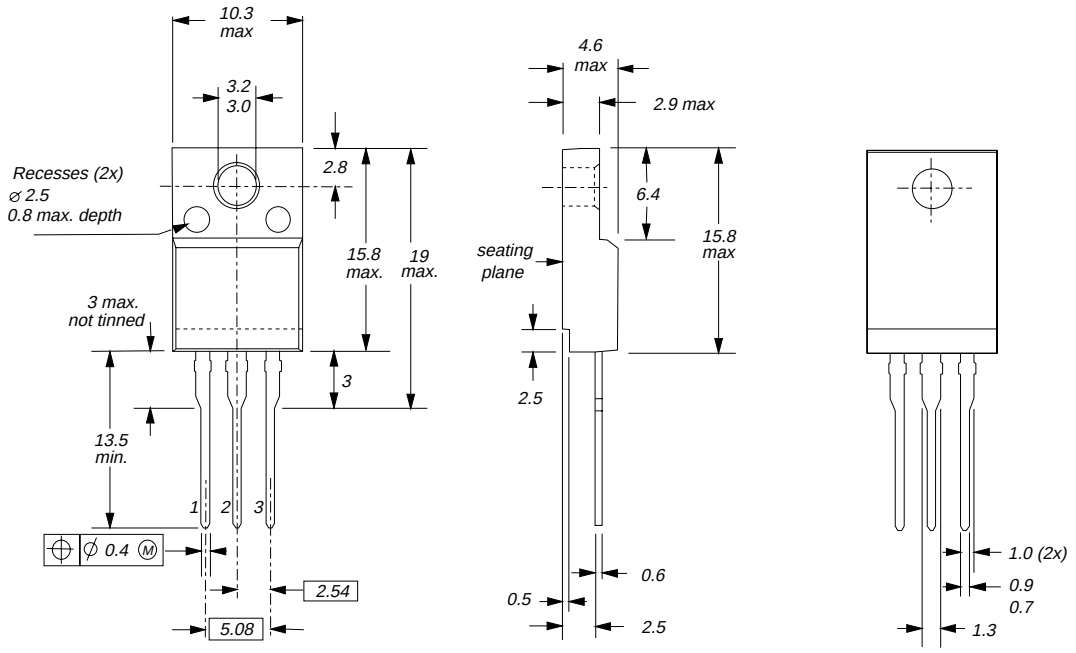


Fig.1. SOT186A; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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