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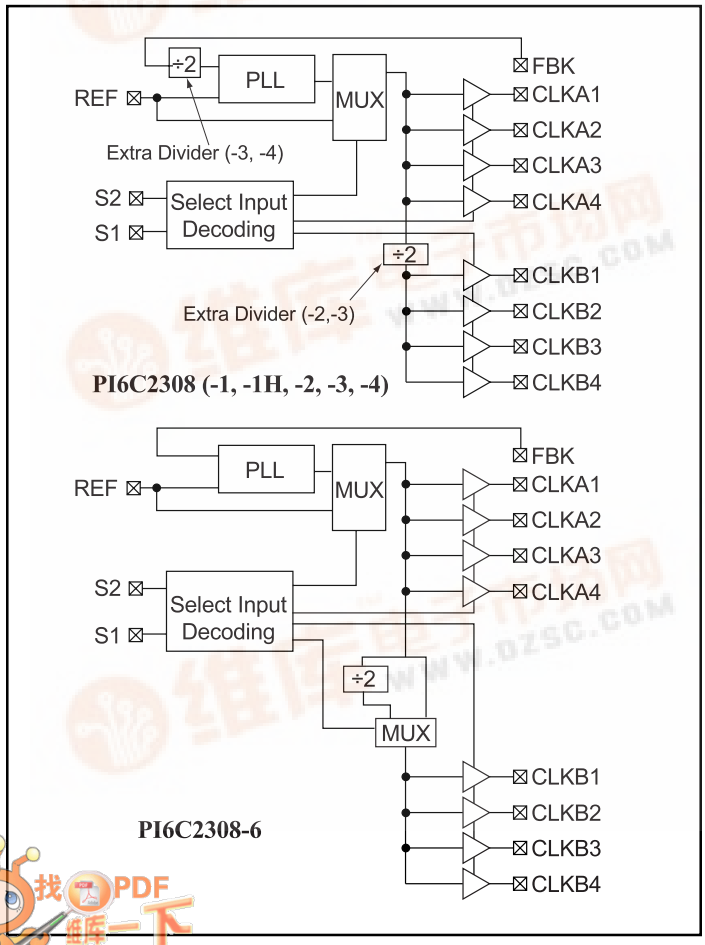
PI6C2308

3.3V Zero-Delay Buffer

Product Features

- 10 MHz to 134 MHz operating range
- Zero input-output propagation delay, adjustable by external capacitive load on FBK input
- Multiple configurations, see "Available PI6C2308 Configurations" table
- Input to output delay, less than 200ps
- Multiple low skew outputs
  - Output-output skew less than 200ps
  - Device-device skew less than 600ps
  - Two banks of four outputs, Hi-Z by two select inputs
- Low Jitter, less than 200ps
- 3.3V operation
- Space-saving Packages:
  16-pin, 150-mil SOIC package (W16) (-1, -1H, -2, -3, -4, -6)
  16-pin TSSOP package (L16) (-1, -1H)
- Available in industrial and commercial temperatures

Block Diagrams



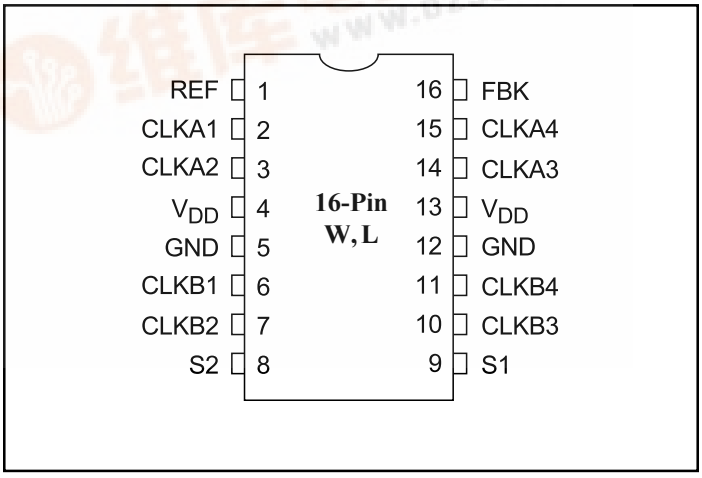
Functional Description

Providing two banks of four outputs, the PI6C2308 is a 3.3V zero-delay buffer designed to distribute clock signals in applications including PC, workstation, datacom, telecom, and high-performance systems. Each bank of four outputs can be controlled by the select inputs as shown in the Select Input Decoding Table.

The PI6C2308 provides 8 copies of a clock signal that has 200ps phase error compared to a reference clock. The skew between the output clock signals for PI6C2308 is less than 200ps. When there are no rising edges on the REF input, the PI6C2308 enters a power down state. In this mode, the PLL is off and all outputs are Hi-Z. This results in less than 12µA of current draw. The Select Input Decoding Table shows additional examples when the PLL shuts down. The PI6C2308 configuration table shows all available devices.

The base part, PI6C2308-1, provides output clocks in sync with a reference clock. With faster rise and fall times, the PI6C2308-1H is the high drive version of the PI6C2308-1. Depending on which output drives the feedback pin, PI6C2308-2 provides 2X and 1X clock signals on each output bank. The PI6C2308-3 allows the user to obtain 4X and 2X frequencies on the outputs. The PI6C2308-4 provides 2X clock signals on all outputs. PI6C2308 (-1, -2, -3, -4) allows bank B to be Hi-Z when all output clocks are not required. The PI6C2308-6 allows bank B to switch from Reference clock to half of the frequency of Reference clock using the control inputs S1 and S2 if Bank A is connected to feedback FBK. In addition, using the control inputs S1 and S2, the PI6C2308-6 allows bank A to switch from Reference clock to 2X the frequency of Reference clock if Bank B is connected to feedback FBK. For testing purposes, the select inputs connect the input clock directly to outputs.

Pin Configuration PI6C2308 (–1, –1H, –2, –3, –4, –6)



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Select Input Decoding for PI6C2308 (-1, -1H, -2, -3, -4)

S2	S1	CLKA [1-4]	CLKB [1-4]	Output Source	PLL Shutdown
0	0	Hi-Z	Hi-Z	PLL	Y
0	1	Driven	Hi-Z	PLL	N
1	0	Driven	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

Select Input Decoding for PI6C2308-6

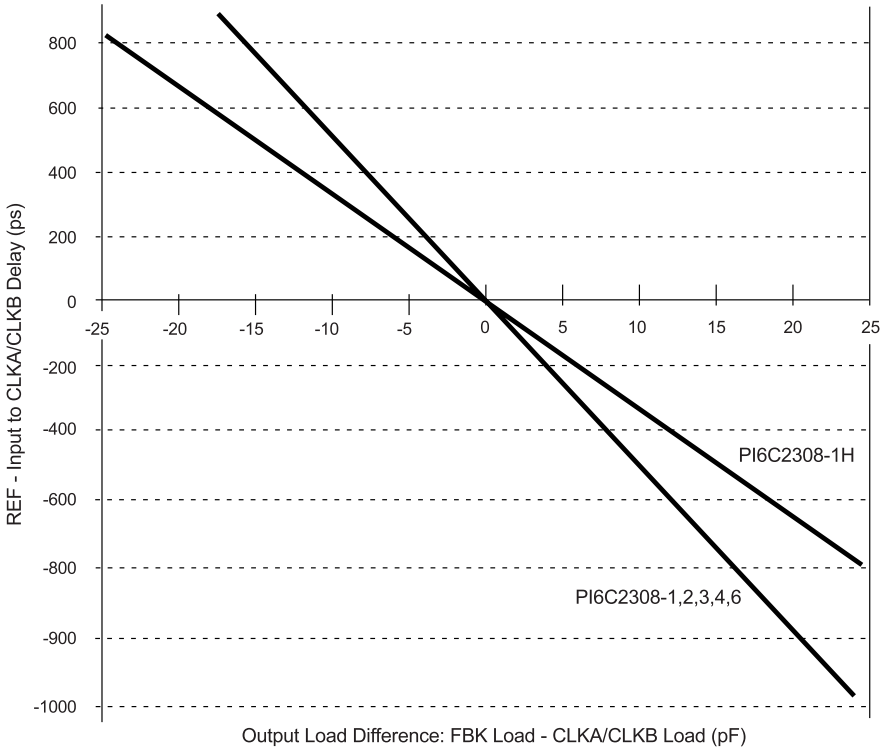
S2	S1	CLKA [1-4]	CLKB [1-4]	Output Source	PLL Shutdown
0	0	Hi-Z	Hi-Z	PLL	Y
0	1	Driven = Reference	Driven = Reference/2	Reference	Y
1	0	Driven = PLL	Driven = PLL	PLL	N
1	1	Driven = PLL	Driven = PLL/2	PLL	N

Available PI6C2308 Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
PI6C2308-1	Bank A or Bank B	Reference	Reference
PI6C2308-1H	Bank A or Bank B	Reference	Reference
PI6C2308-2	Bank A	Reference	Reference/2
PI6C2308-2	Bank B	2X Reference	Reference
PI6C2308-3	Bank A	2X Reference	Reference
PI6C2308-3	Bank B	4X Reference	2X Reference
PI6C2308-4	Bank A or Bank B	2X Reference	2X Reference
PI6C2308-6	Bank A	Reference	Reference or Reference/2
PI6C2308-6	Bank B	Reference or 2X Reference	Reference

Zero Delay and Skew Control

REF. Input to CLKA/CLKB Delay vs. Difference in Loading between FBK pin and CLKA/CLKB pins



To close the feedback loop of the PI6C2308, the FBK pin can be driven from any of the 8 available output pins. The output driving the FBK pin will be driving a total load of 7pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. This is shown in the graph above.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

Maximum Ratings

Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage (Except REF)	–0.5V to V_{DD}+0.5V
DC Input Voltage REF	–0.5 to 7V
Storage Temperature	–65ºC to +150ºC
Maximum Soldering Temperature (10 seconds)	260ºC
Junction Temperature	150ºC
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000V

Operating Conditions

(Over operating range, T_A = 0ºC to +70°C, V_{CC} = 3.3V ±0.3V)

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient)	0	70	ºC
C_L	Load Capacitance	—	30	pF
C_{IN}	Input Capacitance	—	7	

Pin Description

Pin	Signal	Description
1	REF(1)	Input reference frequency, 5V tolerant input, allows spread spectrum clock input
2	CLKA1(2)	Clock output, Bank A
3	CLKA2(2)	Clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1(2)	Clock output, Bank B
7	CLKB2(2)	Clock output, Bank B
8	S2(3)	Select input, bit 2
9	S1(3)	Select input, bit 1
10	CLKB3(2)	Clock output, Bank B
11	CLKB4(2)	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V, supply
14	CLKA3(2)	Clock output, Bank A
15	CLKA4(2)	Clock output, Bank A
16	FBK	PLL feedback input

Electrical Characteristics for Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage(4)	—	—	0.8	V
V_{IH}	Input HIGH Voltage(4)	—	2.0	—	
I_{IL}	Input LOW Current	V_{IN} = 0V	—	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	—	100	
V_{OL}	Output LOW Voltage(5)	I_{OL} = 8mA (–1, –2, –3,–4, –6) I_{OL} = 12mA (-1H)	—	0.4	V
V_{OH}	Output HIGH Voltage(5)	I_{OH} = –8mA (–1, –2, –3,–4, –6) I_{OH} = –12mA (-1H)	2.4	—	
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz	—	12	µA
I_{DD}	Supply Current	Unloaded outputs, 66.66 MHz, Select inputs at V_{DD} or GND	—	39	mA
I_{DD}	Supply Current	Unloaded outputs 100 MHz Select Inputs @ V_{DD} or GND	—	54	

Switching Characteristics[5] for Commercial Temperature Device

Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
t_1	Output Frequency	15pF to 30pF load	10		134	MHz
t_2	Duty Cycle[5] = $t_2 \div t_1$ (2308-1H)	Measured at 1.4V, for high drive output	45	50	55	%
	Duty Cycle = $t_2 \div t_1$ (2308-1, -2, -3, -4, -6)	Measured at 1.4V, for normal drive output	40	50	60	
t_3	Rise Time[4] @30pF	Measured between 0.8V and 2.0V			2.2	ns
	Rise Time[4] @15pF				1.5	
	Rise Time[4] @30pF (–1H)				1.5	
t_4	Fall Time[4] @30pF				2.2	
	Fall Time[4] @15pF				1.5	
	Fall Time[4] @30pF (–1H)				1.25	
t_5	Output to Output Skew[4] on same bank (2308–1,–1H,–2,–3,–4,–6)	All outputs equally loaded, $V_{DD}/2$			200	ps
	Output Bank A to Output Bank B Skew[4]) (2308–1,–1H,–4)	All outputs equally loaded, $V_{DD}/2$			200	
	Output Bank A to Output Bank B Skew[4]) (2308–2,–3,–6)	All outputs equally loaded, $V_{DD}/2$			400	
t_6 (Phase Error)	Input to Output Delay, REF Rising Edge to FBK Rising Edge[4]	Measured at $V_{DD}/2$		0	±200	
t_7	Device to Device Skew[4]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	600	
t_8	Output Slew Rate[4]	Measured between 0.8V and 2.0V on -1H device using Test Circuit #2	1			V/ns
t_J	Cycle-to-Cycle Jitter[4] (2308–1,–1H,–4)	Measured at 66.67 MHz, loaded 30pF outputs			200	ps
		Measured at 133 MHz, loaded 15pF outputs			100	
t_J	Cycle-to-Cycle Jitter[4] (2308–2,–3,–6)	Measured at 66.6 MHz, loaded 30pF outputs			400	
t_{LOCK}	PLL Lock Time[4]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.
4. REF and FBK inputs have a threshhold voltage of $V_{DD}/2$.
5. For definition of t_{1-8}, see Switching Waveforms on page 8.

Operating Conditions for Industrial Temperature Devices

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz		15	
C_{IN}	Input Capacitance		7	

Electrical Characteristics For Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	
V_{OL}	Output LOW Voltage(4)	I_{OL} = 8mA (–1,–2,–3,–4,–6) I_{OL} = 12mA (–1H)		0.4	V
V_{OH}	Output HIGH Voltage(4)	I_{OL} = 8mA (–1,–2,–3,–4,–6) I_{OL} = 12mA (–1H)	2.4		
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	µA
I_{DD}	Supply Current	Unloaded outputs, 100 MHz, Select inputs at V_{DD} or GND		54.0	mA
				70.0 (–1H)	
		Unloaded outputs, 66 MHz, REF, except (–1H)		39.0	
		Unloaded outputs, 33 MHz, REF, except (–1H)		20.0	

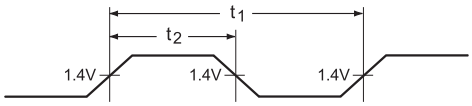
Switching Characteristics for Industrial Temperature Devices[5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Units
t_1	Output Frequency	30pF load, All devices	10		100	MHz
		20pF load, –1H devices			134	
		15pF load, –1,–2,–3,–4,–6 devices			134	
t_2	Duty Cycle[4] = $t_2 \div t_1$ (–1,–2,–3,–4,–6)	Measured at 1.4V, F_{OUT} <66.66MHz 30pF load	40.0	50.0	60.0	%
		Measured at 1.4V, F_{OUT} <133 MHz 15pF load				
		Measured at 1.4V, F_{OUT} <45 MHz 15pF load	45.0		55.0	
	Duty Cycle[4] = $t_2 \div t_1$ (–1H)	Measured at 1.4V, F_{OUT} <66.66MHz 30pF load	45.0			
		Measured at 1.4V, F_{OUT} <133 MHz 15pF load	40.0		60.0	
		Measured at 1.4V, F_{OUT} <45MHz 30pF load	45.0		55.0	
t_3	Rise Time[4] (–1,–2,–3,–4)	Measured between 0.8V and 2.0V, 30pF load			2.2	ns
		Measured between 0.8V and 2.0V, 15pF load			1.50	
	Rise Time[4] (–1H)	Measured between 0.8V and 2.0V, 30pF load			1.50	
t_4	Fall Time[4] (–1,–2,–3,–4)	Measured between 0.8V and 2.0V, 30pF load			2.50	
		Measured between 0.8V and 2.0V, 15pF load			1.50	
	Fall Time[4] (–1H)	Measured between 0.8V and 2.0V, 30pF load			1.25	
t_5	Output to Output Skew on same Bank (–1,–2,–3,–4,–6)[4]	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–1,–1H,– 4)					
	Output Bank A to Output Bank B Skew (–2,– 3,–6)				400	
t_6	Delay, REF Rising Edge to FBK Rising Edge[4]	Measured at $V_{DD}/2$		0	±200	
t_7	Device to Device Skew[4]	Measured at $V_{DD}/2$ MHz, on the FBK pins of devices			600	
t_8	Output Slew Rate[4]	Measured twx 0.8V & 2.0V on 1H,–5 device using Test Crt #2	1			V/ns
t_J	Cycle to Cycle Jitter[4], (–1,– 1H,– 4)	Measured at 66.67 MHz, loaded outputs, 30pF Load			200	ps
		Measured at 133 MHz, loaded outputs, 15pF Load			100	
	Cycle to Cycle Jitter[4], (–2,–3,–6)	Measured at 66.67 MHz, loaded outputs, 30pF Load			400	
t_{LOCK}	PLL Lock Time[4]	Stable power supply, valid clocks presented on REF & FBK pins			1.0	ms

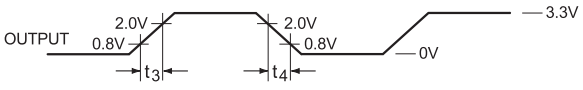
Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.
4. REF and FBK inputs have a threshhold voltage of $V_{DD}/2$.
5. For definition of $t_{1\text{-}8}$, see Switching Waveforms on page 8.

Switching Waveforms

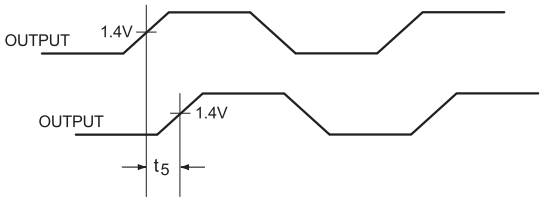
Duty Cycle Timing



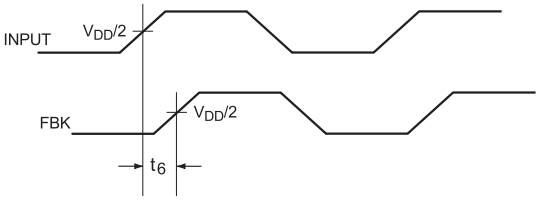
All Outputs Rise/Fall Time



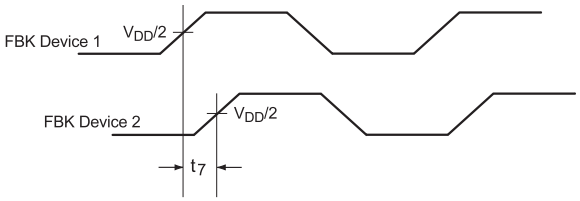
Output-Output Skew



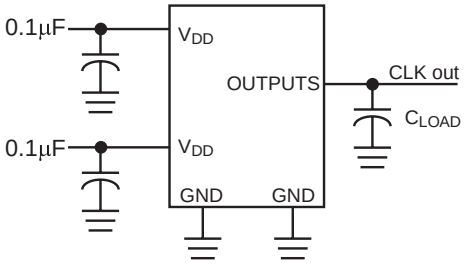
Input-Output Propagation Delay



Device-Device Skew

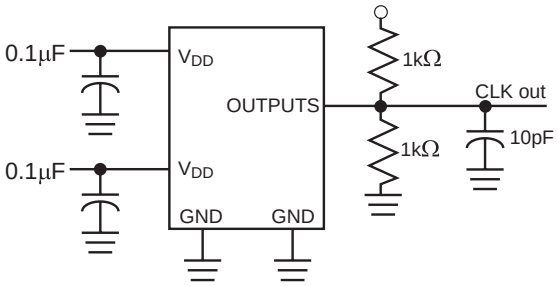


Test Circuit #1



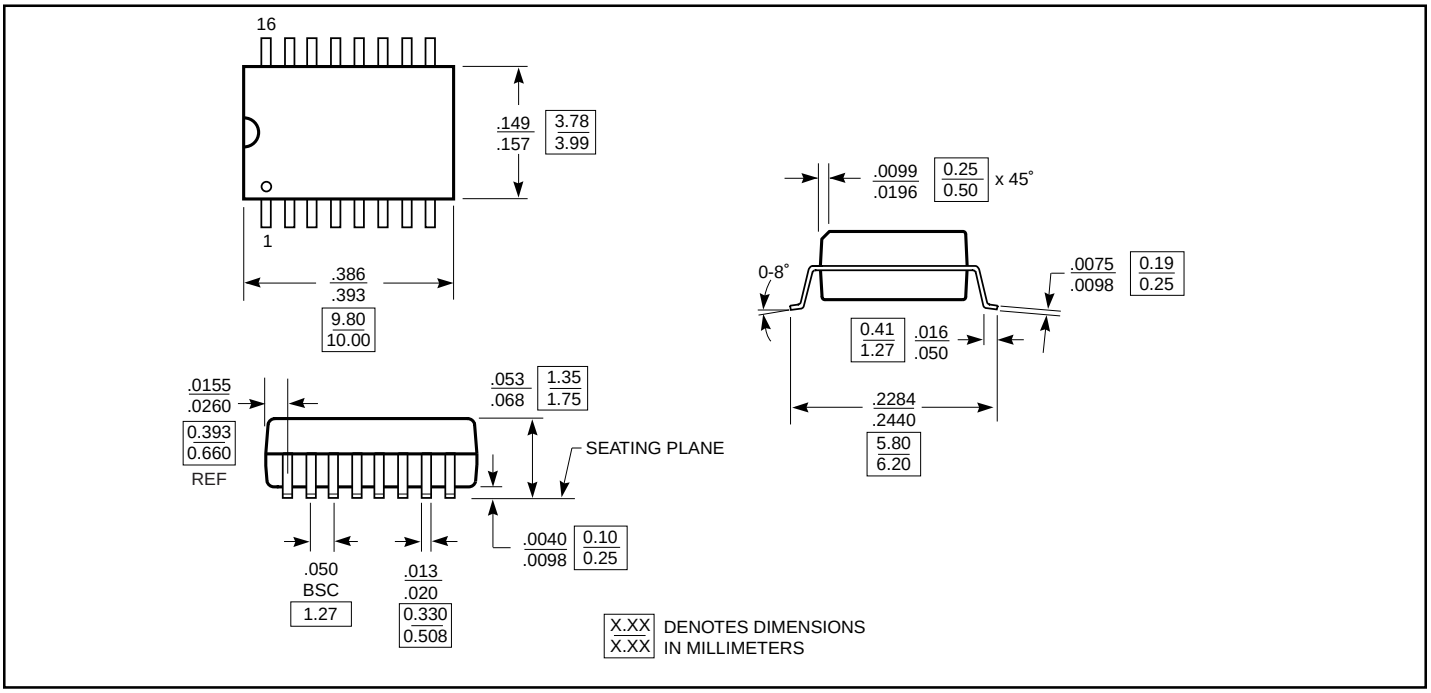
Test Circuit for all parameters except t_8

Test Circuit #2

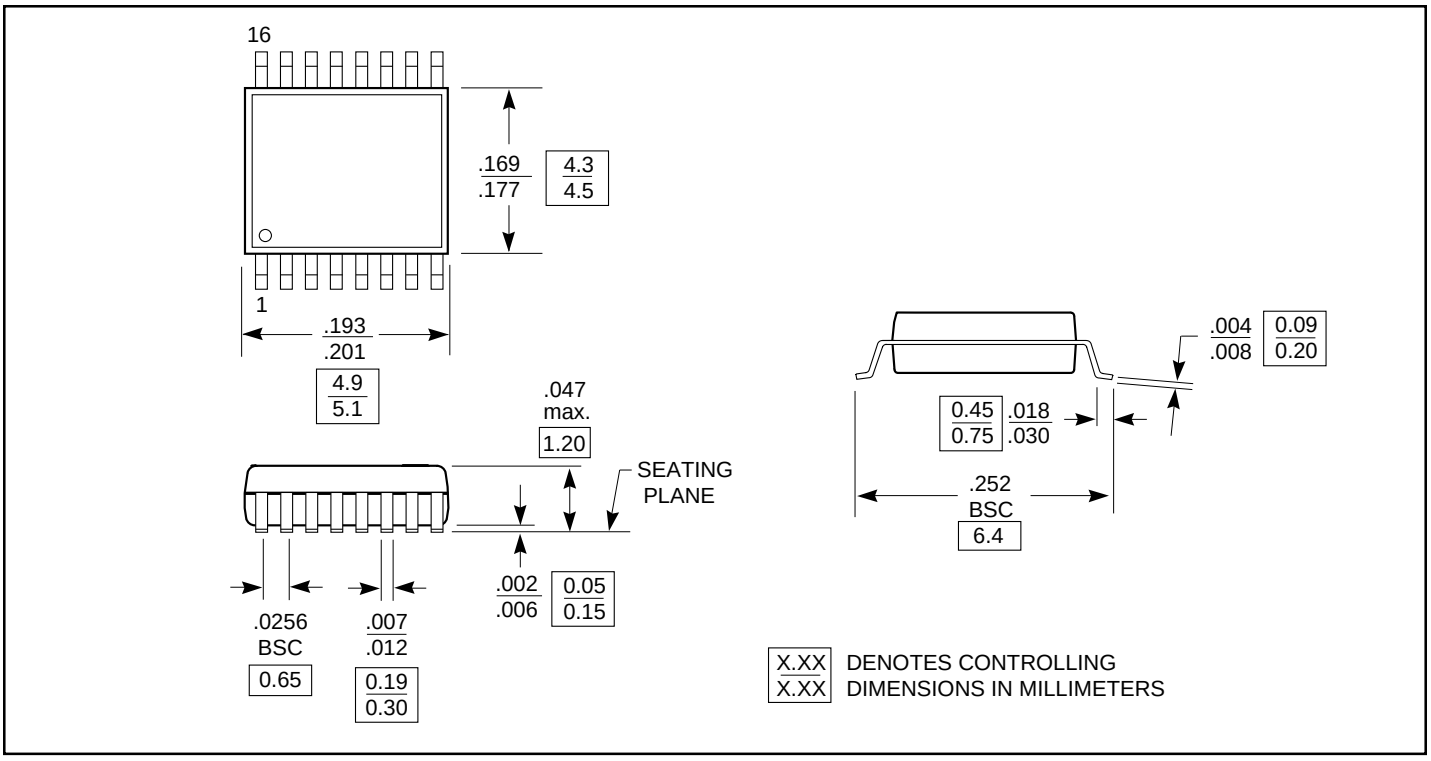


Test Circuit for t_8 ,Output slew rate on -1H device

16-Pin SOIC (W)



16-Pin TSSOP (L)



Note: Controlling dimensions in millimeters. Ref: JEDEC MS - 012 AC

Ordering Information (Commercial Temperature Device)

Ordering Code	Package Name	Package Type	Operating Range
PI6C2308-1W	W16	16-pin 150-mil SOIC	Commercial
PI6C2308-1HW			
PI6C2308-2W			
PI6C2308-3W			
PI6C2308-4W			
PI6C2308-6W			
PI6C2308-1L	L16	16-pin TSSOP	
PI6C2308-1HL			

Ordering Information (Industrial Temperature Device)

Ordering Code	Package Name	Package Type	Operating Range
PI6C2308-1WI	W16	16-pin 150-mil SOIC	Industrial
PI6C2308-1HWI			
PI6C2308-2WI			
PI6C2308-3WI			
PI6C2308-4WI			
PI6C2308-6WI			
PI6C2308-1LI	L16	16-pin TSSOP	
PI6C2308-1HLI			