



PI6C2502A

Phase-Locked Loop Clock Driver

Product Features

- High-Performance Phase-Locked-Loop Clock Distribution for Networking,
- Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ± 75 ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Wide range of Clock Frequencies 80 to 134 MHz
- Package: Plastic 8-pin SOIC Package (W)

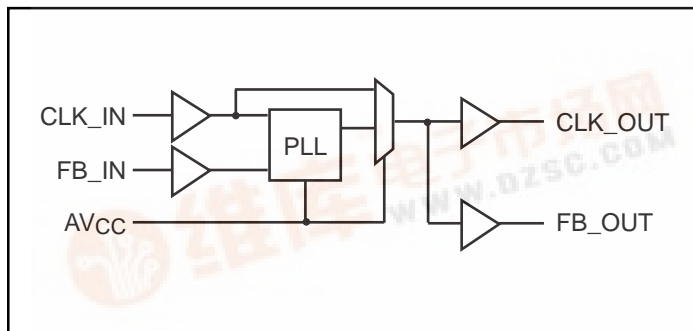
Product Description

The PI6C2502A features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero.

Application

If a system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers such as PI6C2509Q, and PI6C2510Q, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends the use of a zero-delay buffer and an eighteen output non-zero-delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

Logic Block Diagram



Product Pin Configuration

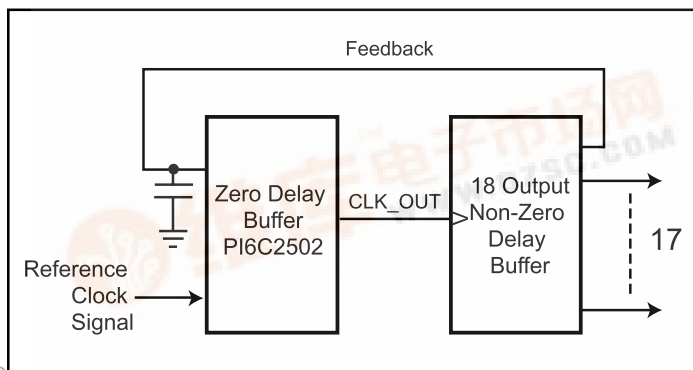
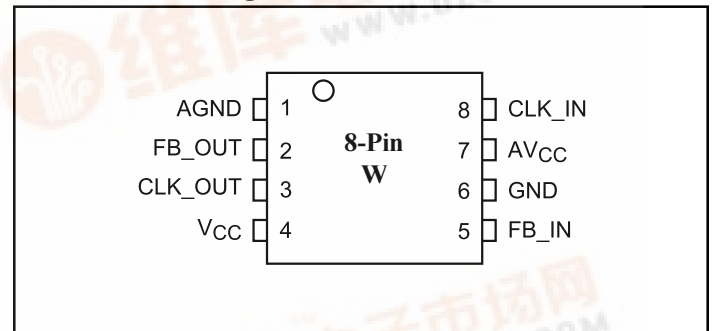


Figure 1. This Combination Provides Zero-Delay Between the Reference Clocks Signal and 17 Outputs.



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Pin Functions

| Pin Name | Pin Number | Type | Description |
|------------------|------------|--------|---|
| CLK_IN | 8 | I | Reference Clock input. CLK_IN allows spread spectrum clock input. |
| FB_IN | 5 | I | Feedback input. FB_IN provides the feedback signal to the internal PLL. |
| FB_OUT | 2 | O | Feedback output FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs CLK_OUT. |
| CLK_OUT | 3 | O | Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor. |
| AV _{CC} | 7 | Power | Analog power supply. AV _{CC} can be also used to bypass the PLL for test purposes. When AV _{CC} is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs. |
| AGND | 1 | Ground | Analog ground. AGND provides the ground reference for the analog circuitry. |
| V _{CC} | 4 | Power | Power supply. |
| GND | 6 | Ground | Ground. |

DC Specifications (Absolute maximum ratings over operating free-air temperature range)

| Symbol | Parameter | Min. | Max. | Units |
|-------------------|---|------|-----------------------|-------|
| V _I | Input voltage range | -0.5 | V _{CC} + 0.5 | V |
| V _O | Output voltage range | | | |
| V _{I_DC} | DC input voltage | | 3.8 | |
| I _{O_DC} | DC output current | | 100 | mA |
| Power | Maximum power dissipation at T _A = 55°C in still air | | 1.0 | W |
| T _{STG} | Storage temperature | -65 | 150 | °C |

Note:

Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

| Parameter | Test Conditions | V _{CC} | Min. | Typ. | Max. | Units |
|-----------------|--|-----------------|------|------|------|-------|
| I _{CC} | V _I = V _{CC} or GND; I _O = 0 ⁽¹⁾ Standby Current | 3.6V | | | 10 | μA |
| C _I | V _I = V _{CC} or GND | 3.3V | | 4 | | pF |
| C _O | V _O = V _{CC} or GND | | | 6 | | |

Note:

1. Continuous Output Current



Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units |
|-----------------|--------------------------------|------|-----------------|-------|
| V _{CC} | Supply voltage | 3.0 | 3.6 | V |
| V _{IH} | High level input voltage | 2.0 | | |
| V _{IL} | Low level input voltage | | 0.8 | |
| V _I | Input voltage | 0 | V _{CC} | |
| T _A | Operating free-air temperature | 0 | 70 | °C |

Electrical Characteristics (Over Recommended Operating Free-Air Temperature Range)

Pull Up/Down Currents of PI6C2502A, V_{CC} = 3.0V)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|-----------------|-------------------|--------------------------|------|-------|-------|
| I _{OH} | Pull-up current | V _{out} = 2.4V | | -13.6 | mA |
| | Pull-up current | V _{out} = 2.0V | | -22 | |
| I _{OL} | Pull-down current | V _{out} = 0.8V | 19 | | |
| | Pull-down current | V _{out} = 0.55V | 13 | | |

AC Specifications

(Timing requirements over recommended ranges of supply voltage and operating free-air temperature)

| Symbol | Parameter | Min. | Max. | Units |
|------------------|-----------------------------------|------|------|-------|
| F _{CLK} | Clock frequency PI6C2502A | 80 | 134 | MHz |
| D _{CYI} | Input clock duty cycle | 40 | 60 | % |
| | Stabilization Time after power up | | 1 | ms |

Switching Characteristics

(Over recommended ranges of supply voltage and operating free-air temperature, CL = 30pF)

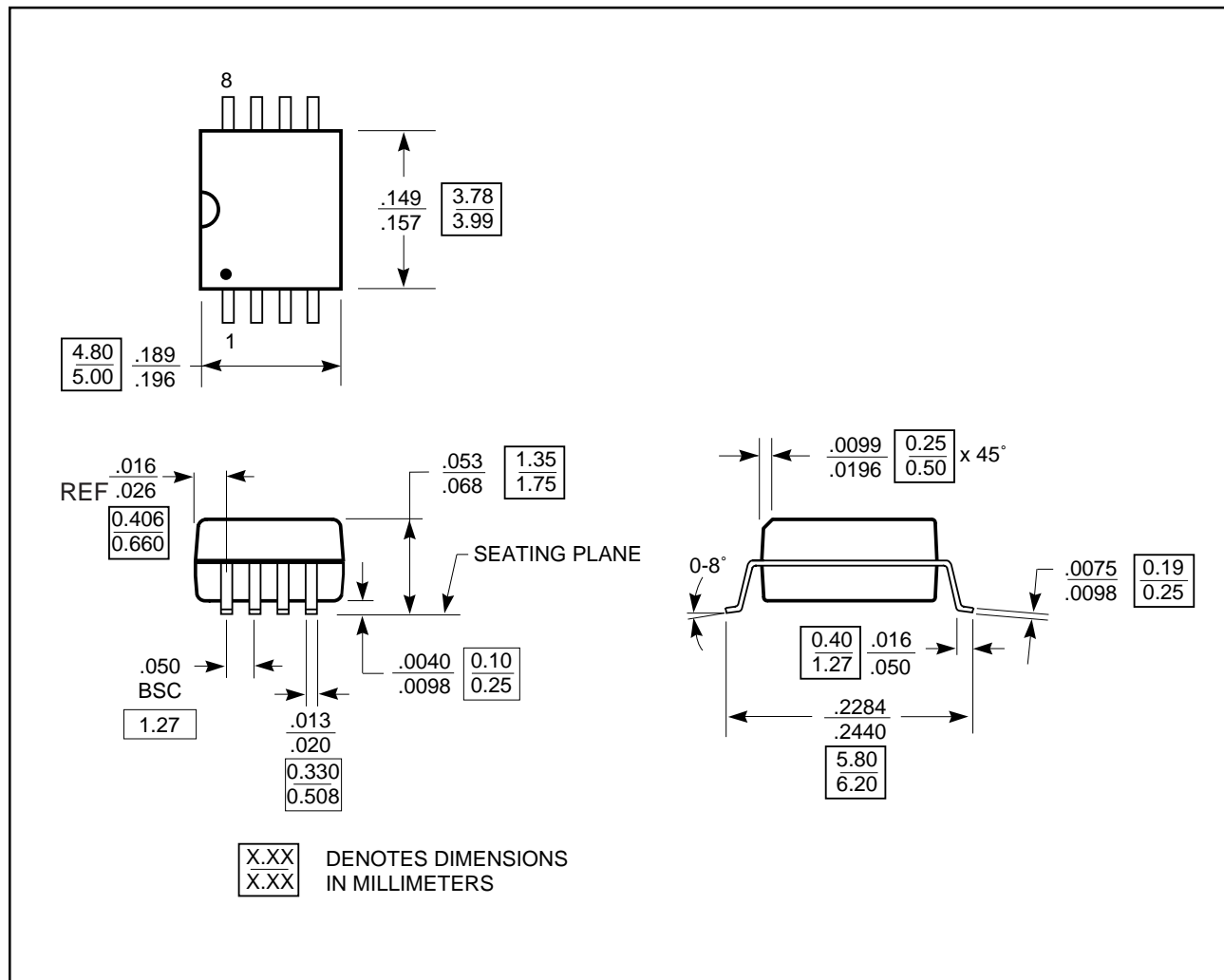
| Parameter | From (Input) | To (Output) | V _{CC} = 3.3V ±0.3V, 0-70°C | | | Units |
|--|-------------------------|-------------|--------------------------------------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| t _{phase error without jitter} | CLK_IN↑ at 100 & 66 MHz | FB_IN↑ | -150 | | +150 | ps |
| Jitter, cycle-to-cycle | At 100 & 66 MHz | CLK_OUT | -75 | | +75 | |
| Duty cycle | | | 45 | | 55 | % |
| t _r , rise-time, 0.4V to 2.0V | | | | 1.0 | | ns |
| t _f , fall-time, 2.0V to 0.4V | | | | 1.1 | | |

Note:

These switching parameters are guaranteed by design.

Package Mechanical Information

Plastic 8-pin SOIC Package



Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|---------------|--------------|--------------------|-----------------|
| PI6C2502AW | W8 | 8-pin 150-mil SOIC | Commercial |