PERICOM®

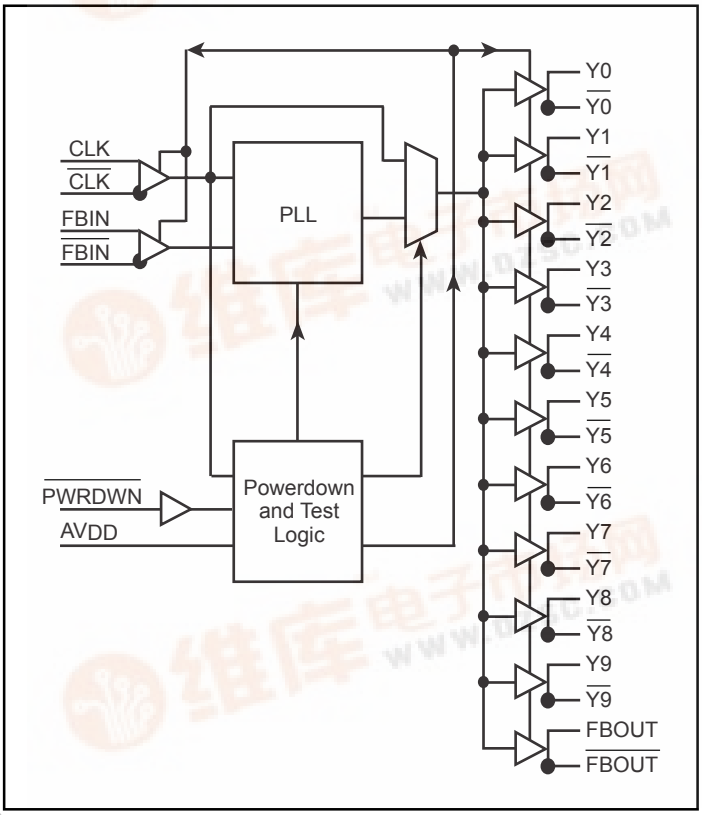
PI6CVF857

1:10 PLL Clock Driver for 2.5V DDR-SDRAM Memory

Product Features

- Operating Frequency up to 220 MHz for PC3200 Registered DIMM applications
- Distributes one differential clock input pair to ten differential clock output pairs
- Inputs (CLK, $\overline{CLK}$) and (FBIN, $\overline{FBIN}$)
- Input $\overline{PWRDWN}$: LVCMOS
- Outputs (Yx, $\overline{Yx}$), (FBOUT, $\overline{FBOUT}$)
- External feedback pins (FBIN, $\overline{FBIN}$) are used to synchronize the outputs to the clock input
- Operates at 2.5V for PC1600, PC2100, PC2700, and 2.6V for PC3200
- Packaging (Pb-free & Green available, select packages):
  - 48-pin TSSOP
  - 40-pin TQFN
  - 56-ball VFBGA

Block Diagram



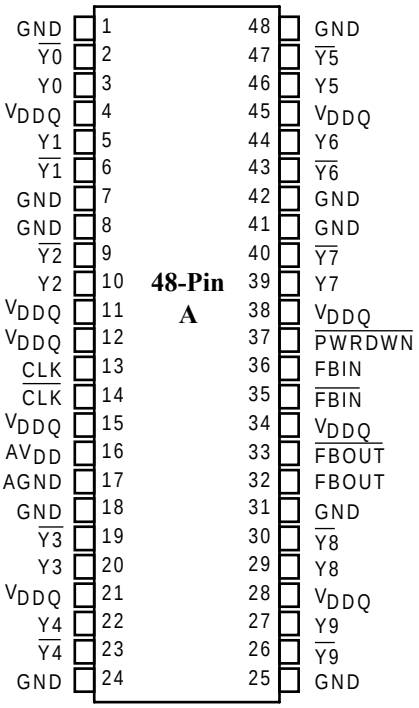
Product Description

PI6CVF857 PLL clock device is developed for registered DDR DIMM applications. The device is a zero-delay buffer that distributes a differential clock input pair (CLK, $\overline{CLK}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{Y[0:9]}$), and one differential pair feedback clock outputs (FBOUT, $\overline{FBOUT}$) . The clock outputs are controlled by the input clocks (CLK, $\overline{CLK}$), the feedback clocks (FBIN, $\overline{FBIN}$), the 2.5V LVCMOS input ($\overline{PWRDWN}$), and the Analog Power input (AV_{DD}). When input $\overline{PWRDWN}$ is low while power is applied, the input receivers are disabled, the PLL is turned off, and the differential clock outputs are 3-stated. When the AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes.

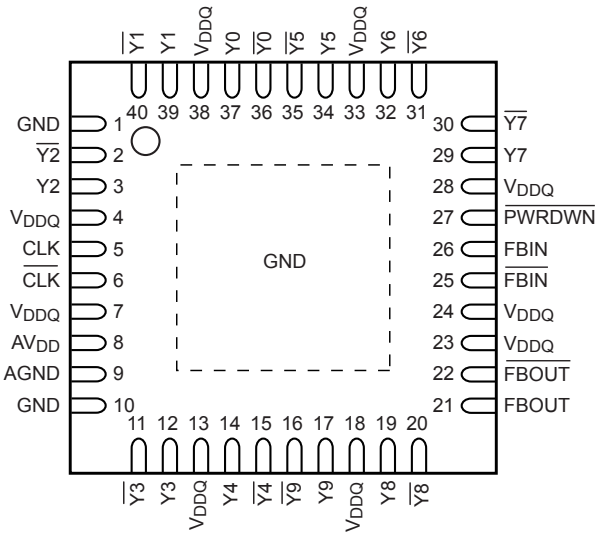
When the input frequency falls below a suggested detection frequency that is below the operating frequency of the PLL, the device will enter a low power mode. An input frequency detection circuit will detect the low frequency condition and perform the same low power features as when the $\overline{PWRDWN}$ input is low.

The PLL in the PI6CVF857 clock driver uses the input clocks (CLK, $\overline{CLK}$) and the feedback clocks (FBIN, $\overline{FBIN}$) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], $\overline{Y[0:9]}$). The PI6CVF857 is also able to track Spread Spectrum Clocking for reduced EMI.

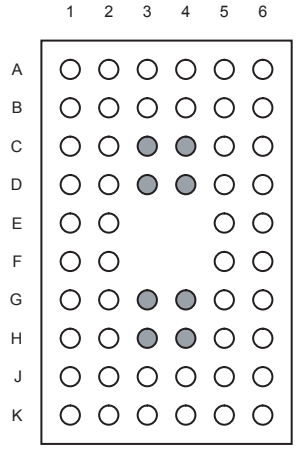
Pin Configuration TSSOP (A)



Pin Configuration QFN (ZD)



Ball Configuration VFBGA (NF)



NO CONNECT on C3, C4, D3, D4, G3, G4, H3 and H4

Ball Configuration

	1	2	3	4	5	6
A	Y0	$\overline{Y0}$	GND	GND	$\overline{Y5}$	Y5
B	$\overline{Y1}$	Y1	VDDQ	VDDQ	Y6	$\overline{Y6}$
C	GND	GND	NC	NC	GND	GND
D	Y2	$\overline{Y2}$	NC	NC	$\overline{Y7}$	Y7
E	VDDQ	VDDQ	NB	NB	VDDQ	$\overline{PWRDWN}$
F	CLK	$\overline{CLK}$	NB	NB	$\overline{FBIN}$	FBIN
G	VDDQ	AVDD	NC	NC	$\overline{FBOUT}$	VDDQ
H	AGND	GND	NC	NC	GND	FBOUT
J	$\overline{Y3}$	Y3	VDDQ	VDDQ	Y8	$\overline{Y8}$
K	Y4	$\overline{Y4}$	GND	GND	$\overline{Y9}$	Y9

Notes:
NC = No Contact
NB = No Ball

Pinout Table

Pin Name	Description
CLK $\overline{CLK}$	Reference Clock input
Yx	Clock outputs.
$\overline{Yx}$	Complement Clock outputs.
FBOUT $\overline{FBOUT}$	Feedback output, and Complement Feedback Output
FBIN $\overline{FBIN}$	Feedback Input, and Complement Feedback Input
$\overline{PWRDWN}$	Power down and output disable for all Yx and $\overline{Yx}$ outputs. When $\overline{PWRDWN}$ = 0, the part is powered down and the differential clock outputs are disabled to a - state. When $\overline{PWRDWN}$ = 1, all differential clock outputs are enabled and run at the same frequency as CLK.
V_{DDQ}	Power Supply for I/O.
AV_{DD}	Analog /core power supply. AV_{DD} can be used to bypass the PLL for testing purposes. When AV_{DD} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	Analog/core ground. Provides the ground reference for the analog/core circuitry
GND	Ground

Function Table

Inputs				Outputs				PLL
AV_{DD}	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
X	L	L	H	Z	Z	Z	Z	off
X	L	H	L	Z	Z	Z	Z	off
Nominal(2)	H	L	H	L	H	L	H	on
Nominal(2)	H	H	L	H	L	H	L	on
Nominal(2)	X	< 20 MHz (1)		Z	Z	Z	Z	off

Notes:
1. For testing and power saving purposes, PI6CVF857 will power down if the frequency of the reference inputs CLK, $\overline{CLK}$ is well below the operating frequency range. The maximum power down clock frequency is below 20 MHz. For example, PI6CVF857 will be powered down when the CLK,$\overline{CLK}$ stop running.
2. AV_{DD} Nominal is 2.5V for PC1600, PC2100, and PC2700. AV_{DD} Nominal is 2.6V for PC3200.

Z = High impedance
X = Don't care

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_{DDQ}, AV_{DD}	I/O supply voltage range and analog/core supply voltage range	– 0.5	3.6	V
V_I	Input voltage range	– 0.5	V_{DDQ} +0.5	
V_O	Output voltage range	– 0.5		
I_{IK}	Input Clamp Current	– 50	50	mA
I_{OK}	Output Clamp Current	– 50	50	
I_O	Continuous output Current	– 50	50	
$I_{O(PWR)}$	Continuous current through each AV_{DD}, V_{DDQ}, or GND	– 100	100	
Tstg	Storage temperature	– 65	150	°C
$\varnothing_{JA}$	Junction to ambient thermal (package A)		104	°C/w
$\varnothing_{JC}$	Junction to case thermal (package A)		38	°C/w

Note: Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Specifications

Recommended Operating Conditions

Symbol	Parameter		Min.	Nom.	Max.	Units
AV_{DD}	Analog/core supply voltage		V_{DDQ} – 0.12	V_{DDQ}	2.7	V
V_{DDQ}	Output supply voltage	PC1600 - PC2700	2.3	2.5	2.7	
		PC3200	2.5	2.6	2.7	
V_{IL}	Low-level input voltage for $\overline{PWRDWN}$ pin		–0.3		0.7	
V_{IH}	High-level input voltage for $\overline{PWRDWN}$ pin		1.7		V_{DDQ} +0.3	
I_{OH}	High-level output current		–		12	mA
I_{OL}	Low-level output current		–		–12	
V_{IX}	Input differential-pair crossing voltage		(V_{DDQ}/2) –0.2		(V_{DDQ}/2) +0.2	V
V_{IN}	Input voltage level		–0.3		V_{DDQ} +0.3	
V_{ID}	Input differential voltage between CLK and $\overline{CLK}$	DC	0.36		V_{DDQ} +0.6	
		AC	0.7		V_{DDQ} +0.6	
T_A	Operating free air temperature		–40		85	°C

Timing Requirements for PC1600 ~ PC2700 (Over recommended operating free-air temperature)

Symbol	Description	AV_{DD}, V_{DDQ} = 2.5V ±0.2V		Units
		Min.	Max.	
f_{CK}	Operating clock frequency(1,2)	60	170	MHz
	Application clock frequency(3)	95	170	
t_{DC}	Input clock duty cycle	40	60	%
t_{STAB}	PLL stabilization time after powerup		100	µs

Notes:
1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which the clock is not required to meet the other timing parameters. (Used for low-speed debug).
3. Application clock frequency indicates a range over which the PLL meets all of the timing parameters.

Electrical Characteristics for PC1600 ~ PC2700 (Over recommended operating free-air temperature)

Parameter		Test Conditions	A_{VDD}, V_{DDQ}	Min.	Typ.	Max.	Units
V_{IK}	All inputs	I_I = –18mA	2.3V			–1.2	V
V_{OH}	High output voltage	I_{OH} = –100µA	2.3 to 2.7V	V_{DDQ}– 0.1			
		I_{OH} = –12mA	2.3V	1.7			
V_{OL}	Low output voltage	I_{OL} = 100µA	2.3 to 2.7V			0.1	
		I_{OL} = 12mA	2.3V			0.6	
I_I	CLK, FBIN	V_I = V_{DDQ} or GND	2.7V			±10	µA
	$\overline{PWRDWN}$	V_I = V_{DDQ} or GND	2.7V				
I_{DDPD}	Static supply current I_{DDQ} + I_{ADD}	CLK & $\overline{CLK}$ = 0 MHz, $\overline{PWRDWN}$ = Low				200	
I_{DDQ}	Dynamic supply current of V_{DDQ}	CLK & $\overline{CLK}$ = 170 MHz All outputs are open	2.7V			300	mA
I_{ADD}	Dynamic supply current of AV_{DD}	CLK & $\overline{CLK}$ = 170 MHz	2.7V			12	mA
C_I	CLK and $\overline{CLK}$	V_I = V_{DDQ} or GND	2.5V	2.0		3.5	pF
	FBIN and $\overline{FBIN}$						
$C_{I(\Delta)}$	CLK and $\overline{CLK}$(5)	V_I = V_{DDQ} or GND	2.5V	–0.25		0.25	
	FBIN and $\overline{FBIN}$(5)						

Note:
4. The maximum power-down clock frequency is below 20 MHz.
5. Guaranteed by design, but not production tested.

Timing Requirements for PC3200 (Over recommended operating free-air temperature)

Symbol	Description	AV_{DD}, V_{DDQ} = 2.6V ±0.1V		Units
		Min.	Max.	
f_{CK}	Operating clock frequency(1,2)	60	220	MHz
	Application clock frequency(3)	95	220	
t_{DC}	Input clock duty cycle	40	60	%
t_{STAB}	PLL stabilization time after powerup		100	µs

Notes:
1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which the clock is not required to meet the other timing parameters. (Used for low-speed debug).
3. Application clock frequency indicates a range over which the PLL meets all of the timing parameters.

Electrical Characteristics for PC3200 (Over recommended operating free-air temperature)

Parameter		Test Conditions	A_{VDD}, V_{DDQ}	Min.	Typ.	Max.	Units
V_{IK}	All inputs	I_I = –18mA	2.5V			–1.2	V
V_{OH}	High output voltage	I_{OH} = –100µA	2.5 to 2.7V	V_{DDQ}– 0.1			
		I_{OH} = –12mA	2.5V	1.7			
V_{OL}	Low output voltage	I_{OL} = 100µA	2.5 to 2.7V			0.1	
		I_{OL} = 12mA	2.5V			0.6	
I_I	CLK, FBIN	V_I = V_{DDQ} or GND	2.7V			±10	µA
	$\overline{PWRDWN}$	V_I = V_{DDQ} or GND	2.7V				
I_{DDPD}	Static supply current I_{DDQ} + I_{ADD}	CLK & $\overline{CLK}$ = 0 MHz, $\overline{PWRDWN}$ = Low				200	
I_{DDQ}	Dynamic supply current of V_{DDQ}	CLK & $\overline{CLK}$ = 200 MHz All outputs are open	2.7V			300	mA
I_{ADD}	Dynamic supply current of AV_{DD}	CLK & $\overline{CLK}$ = 200 MHz	2.7V			12	mA
C_I	CLK and $\overline{CLK}$	V_I = V_{DDQ} or GND	2.6V	2.0		3.5	pF
	FBIN and $\overline{FBIN}$						
$C_{I(\Delta)}$	CLK and $\overline{CLK}$(5)	V_I = V_{DDQ} or GND	2.6V	–0.25		0.25	
	FBIN and $\overline{FBIN}$(5)						

Note:
4. The maximum power-down clock frequency is below 20 MHz.
5. Guaranteed by design, but not production tested.

AC Specifications for PC1600 ~ PC2700

Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)(See Figure 1 & 2)

Parameter	Description	Diagram	AV_{DD}, V_{DDQ} = 2.5V ±0.2V			Units
			Min.	Nom.	Max	
tjit(cc)	Cycle-to-cycle jitter	Figure 4	–50		50	ps
t(θ)	Static phase offset(1)	Figure 5	–50	0	50	
tsk(o)	Output clock skew	Figure 6			75	
tjit(per)	Period jitter	Figure 7	–75		75	
tjit(hper)	Half-period jitter	Figure 8	–100		100	
tsl(i)	Input clock slew rate	Figure 9	1.0		4.0	V/ns
tsl(o)	Output clock slew rate(2)	Figure 9	1.0		2.0	
V_{OX}	Output differential-pair cross-voltage		(V_{DDQ}/2) –0.1		(V_{DDQ}/2) +0.1	V
The PLL is capable of meeting all the above parameters while supporting SSC synthesizers with the following parameters						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
	PLL loop bandwidth(4)		2			MHz
	Phase angle				–0.031	degrees

Notes:

1. Static Phase offset does not include Jitter.
2. The Output Skew Rate is calculated by using the load shown in Figure 3.
3. V_{OX} specified at the DRAM clock input or the test load in Figure 2.
4. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

AC Specifications for PC3200

Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)(See Figure 1 & 2)

Parameter	Description	Diagram	AV_{DD}, V_{DDQ} = 2.6V ±0.1V			Units
			Min.	Nom.	Max	
tjit(cc)	Cycle-to-cycle jitter	Figure 4	–50		50	ps
t(θ)	Static phase offset(1)	Figure 5	–50	0	50	
tsk(o)	Output clock skew	Figure 6			75	
tjit(per)	Period jitter	Figure 7	–50		50	
tjit(hper)	Half-period jitter	Figure 8	–75		75	
tsl(i)	Input clock slew rate	Figure 9	1.0		4.0	V/ns
tsl(o)	Output clock slew rate(2)	Figure 9	1.0		2.0	
V_{OX}	Output differential-pair cross-voltage		(V_{DDQ}/2) –0.1		(V_{DDQ}/2) +0.1	V
The PLL is capable of meeting all the above parameters while supporting SSC synthesizers with the following parameters						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
	PLL loop bandwidth(4)		2			MHz
	Phase angle				–0.031	degrees

Notes:

1. Static Phase offset does not include Jitter.
2. The Output Skew Rate is calculated by using the load shown in Figure 3.
3. V_{OX} specified at the DRAM clock input or the test load in Figure 2.
4. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

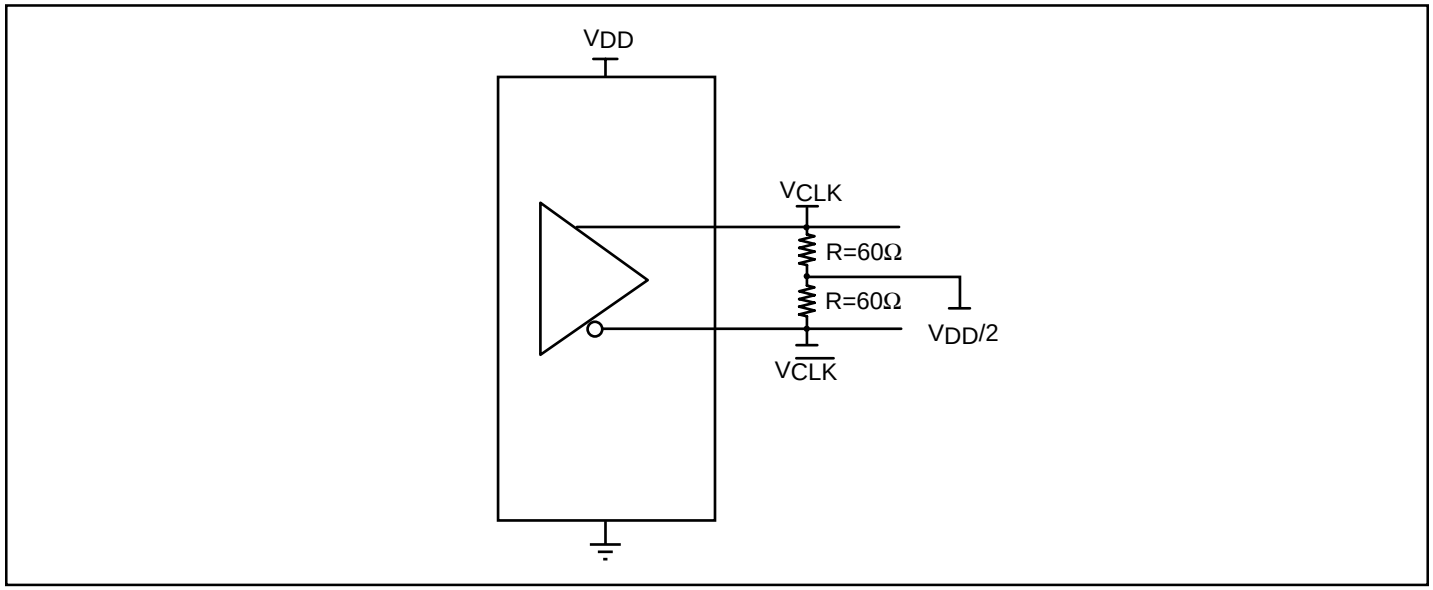


Figure 1. IBIS Model Output Load

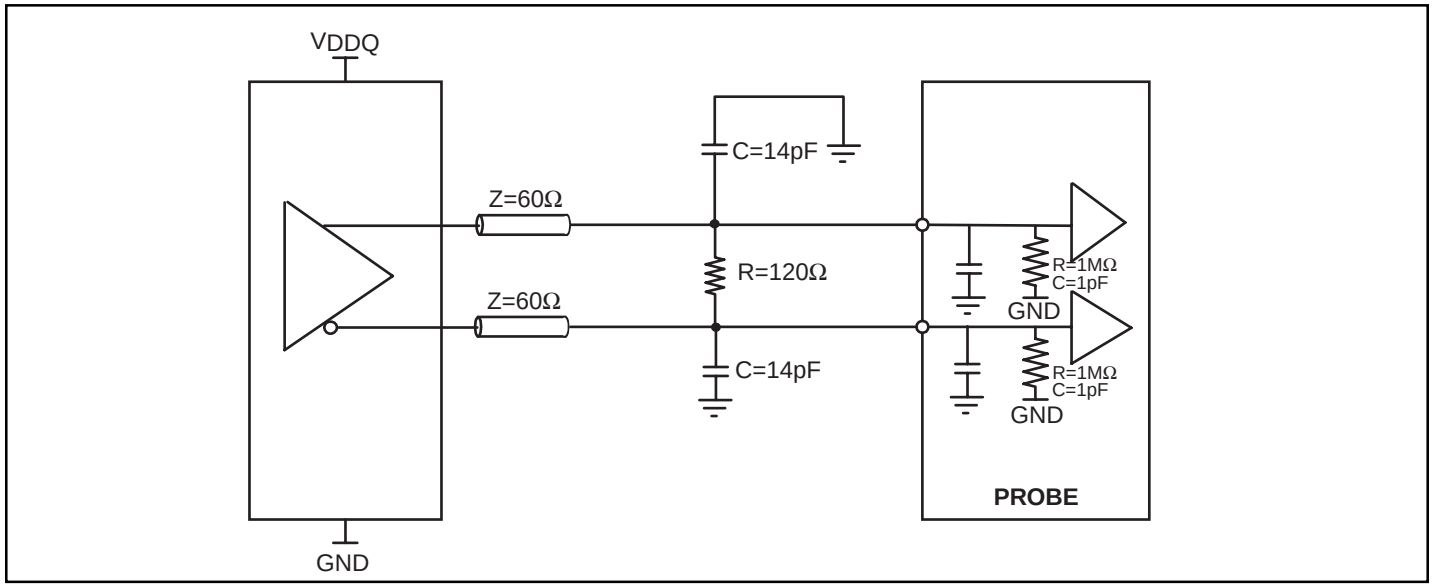


Figure 2. Output Load Test Circuit 1

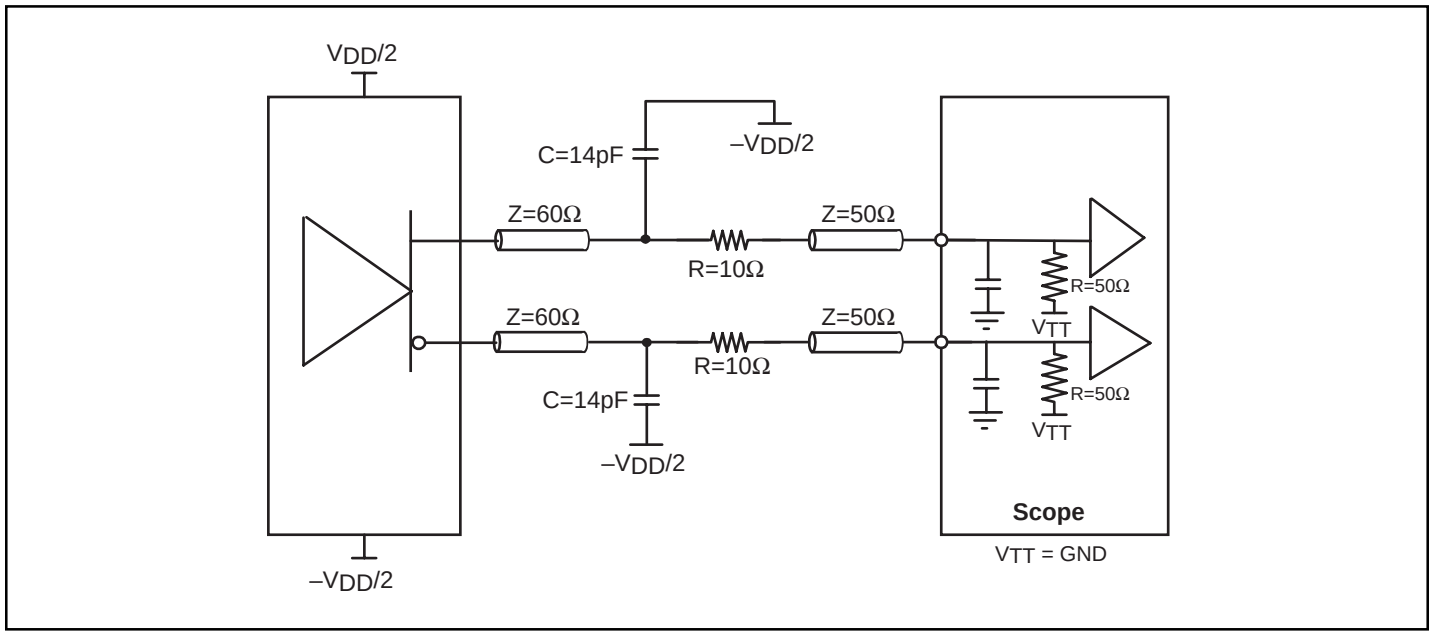


Figure 3. Output Load Test Circuit 2

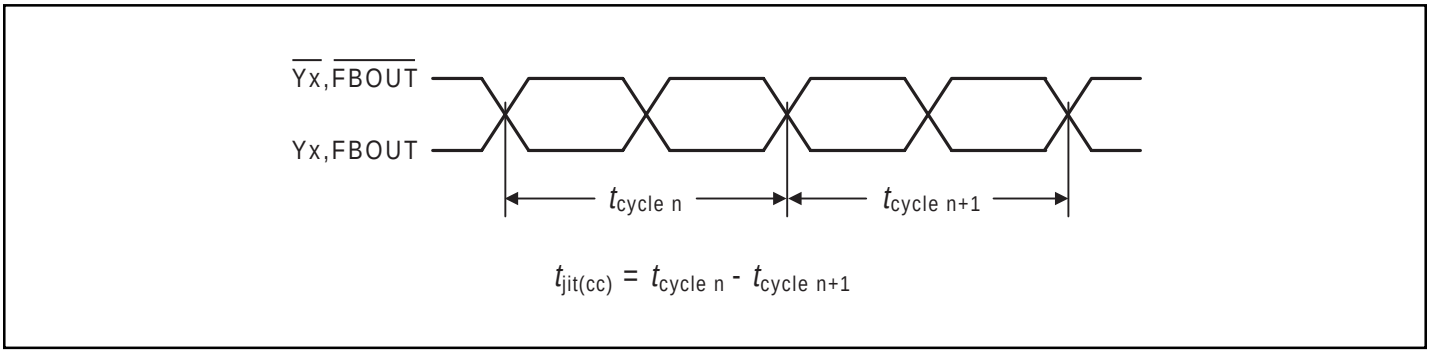


Figure 4. Cycle-to-Cycle Jitter

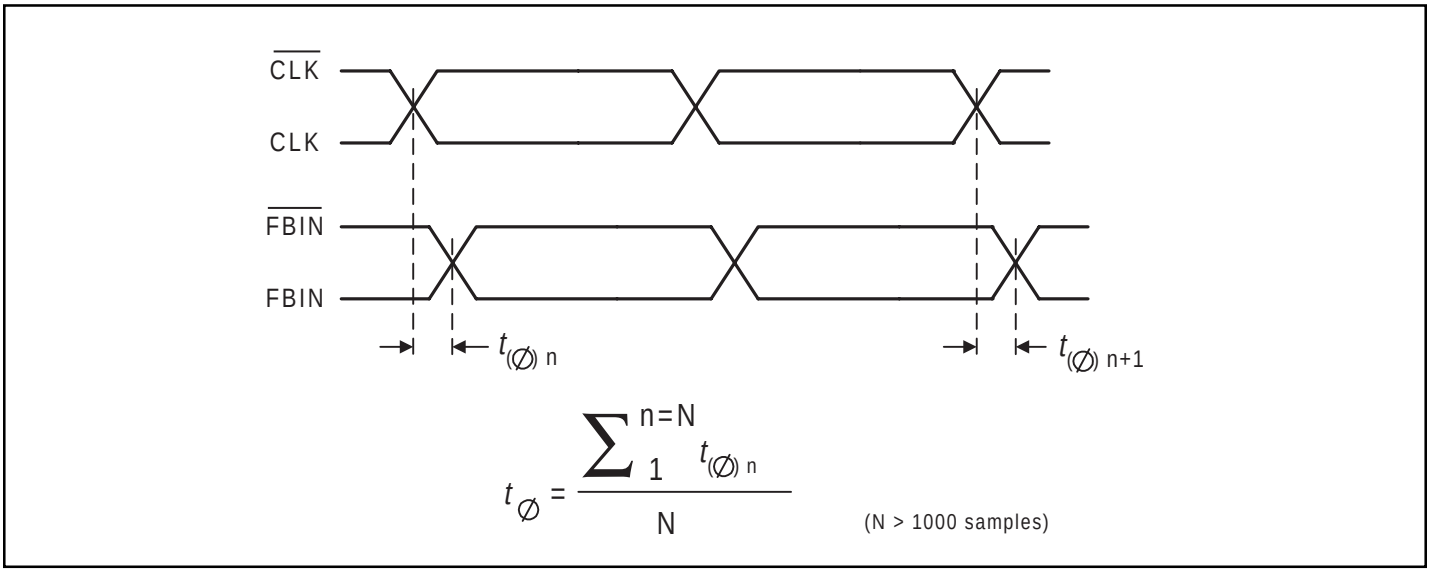


Figure 5. Static Phase Offset

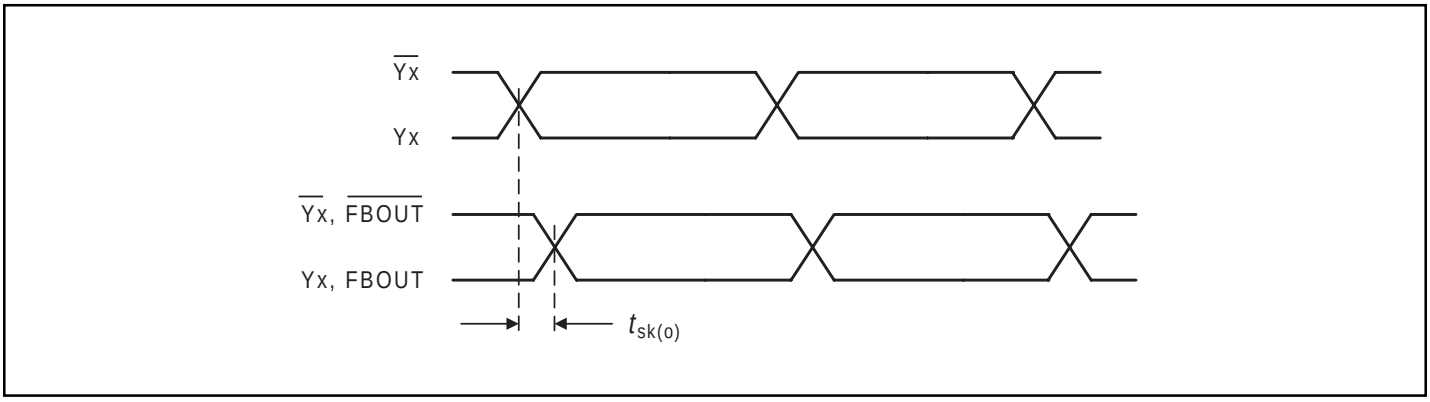
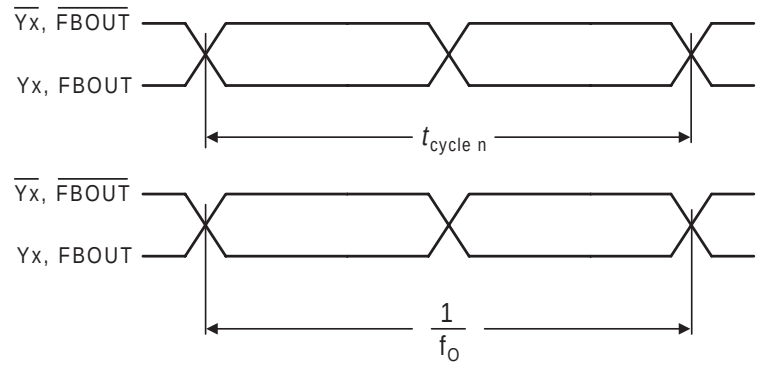


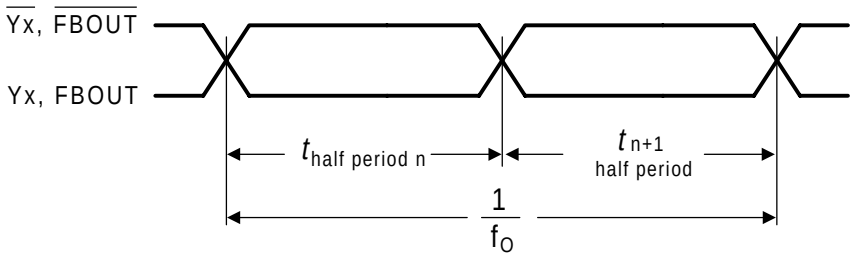
Figure 6. Output Skew



$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_O}$$

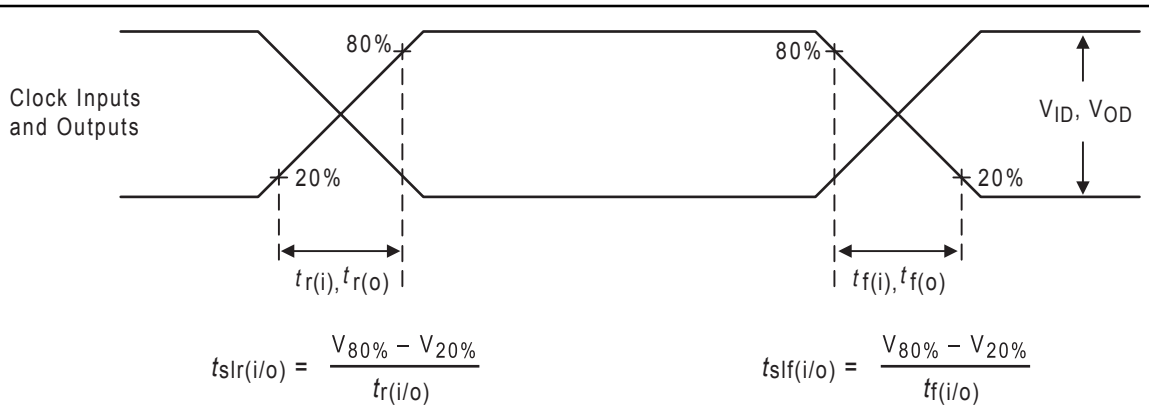
(f_O = input frequency measured at CLK, $\overline{CLK}$)

Figure 7. Period Jitter



$$t_{jit(hper)} = t_{half\ period\ n} - \frac{1}{2*f_O}$$

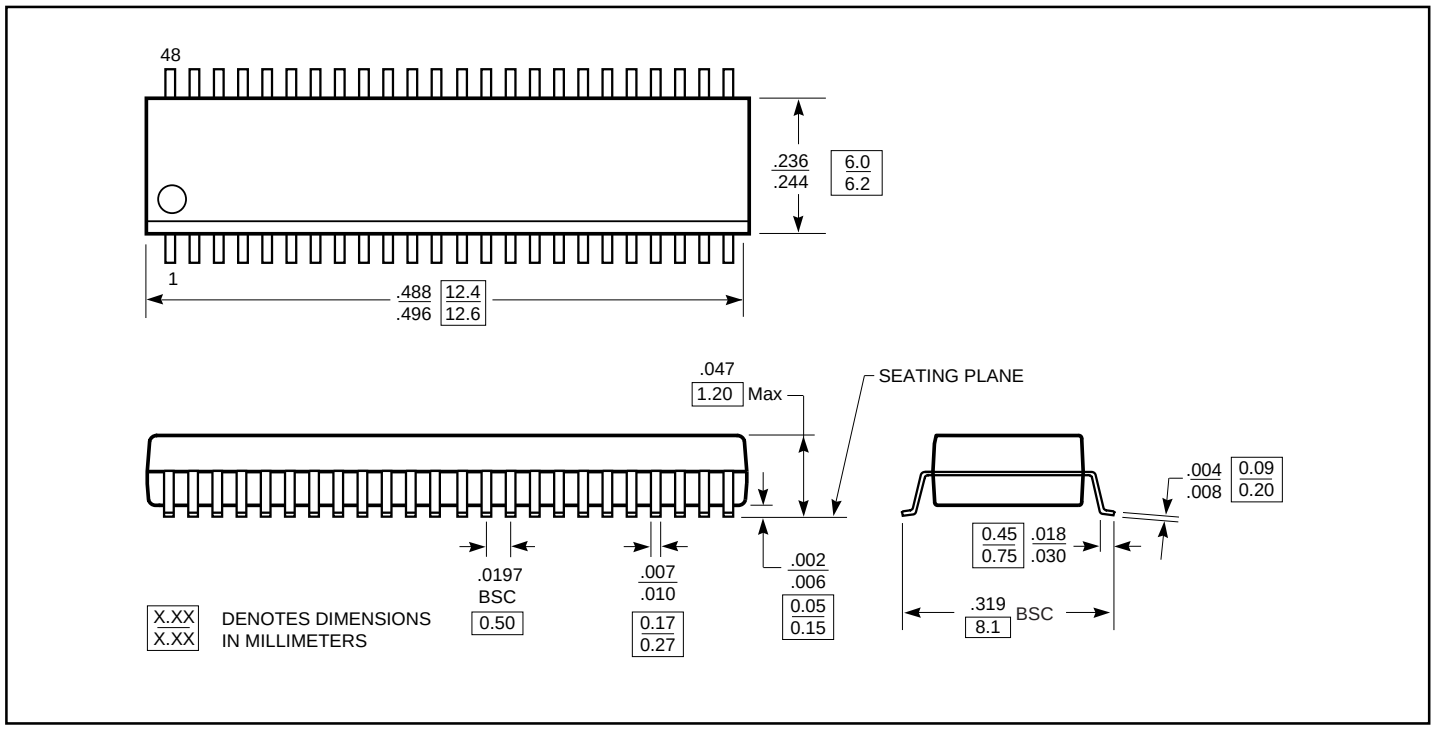
Figure 8. Half-Period Jitter



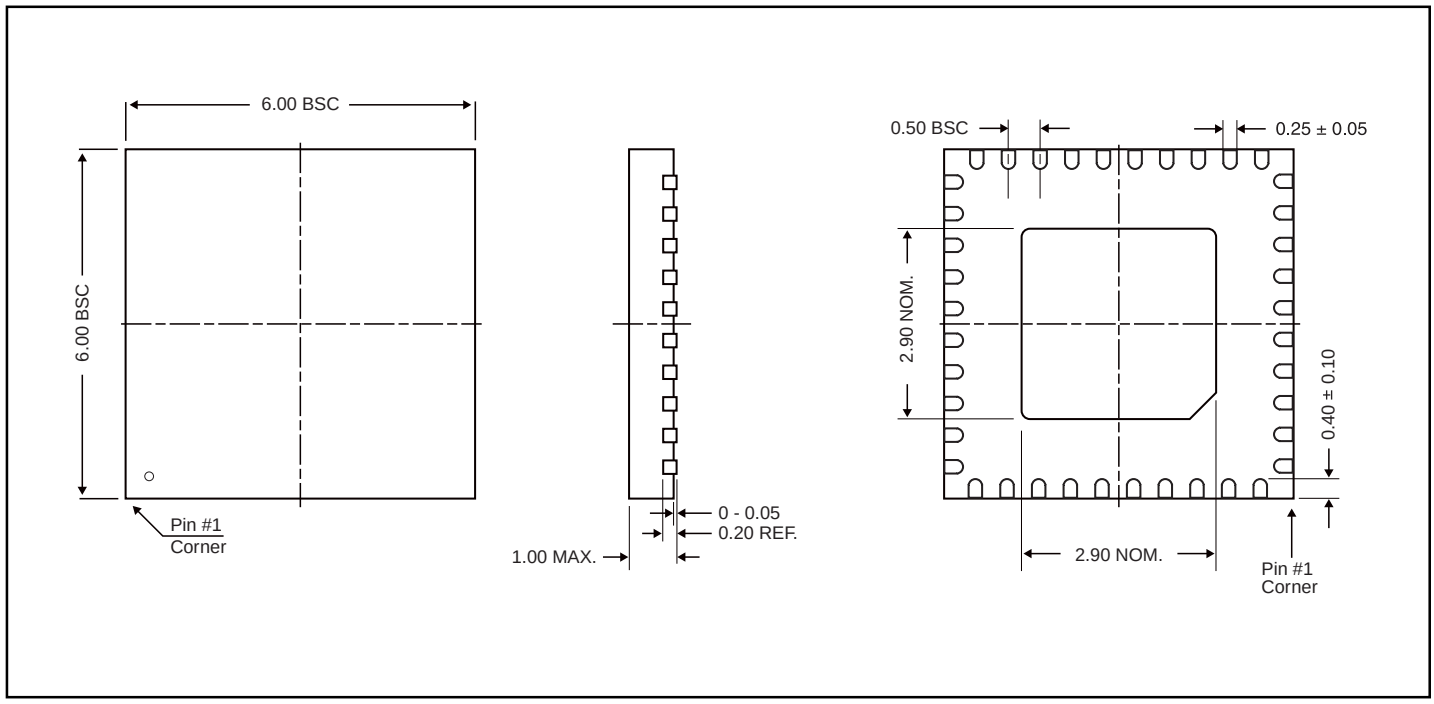
$$t_{slr(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{r(i/o)}} \qquad t_{slf(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{f(i/o)}}$$

Figure 9. Input and Output Slew Rates

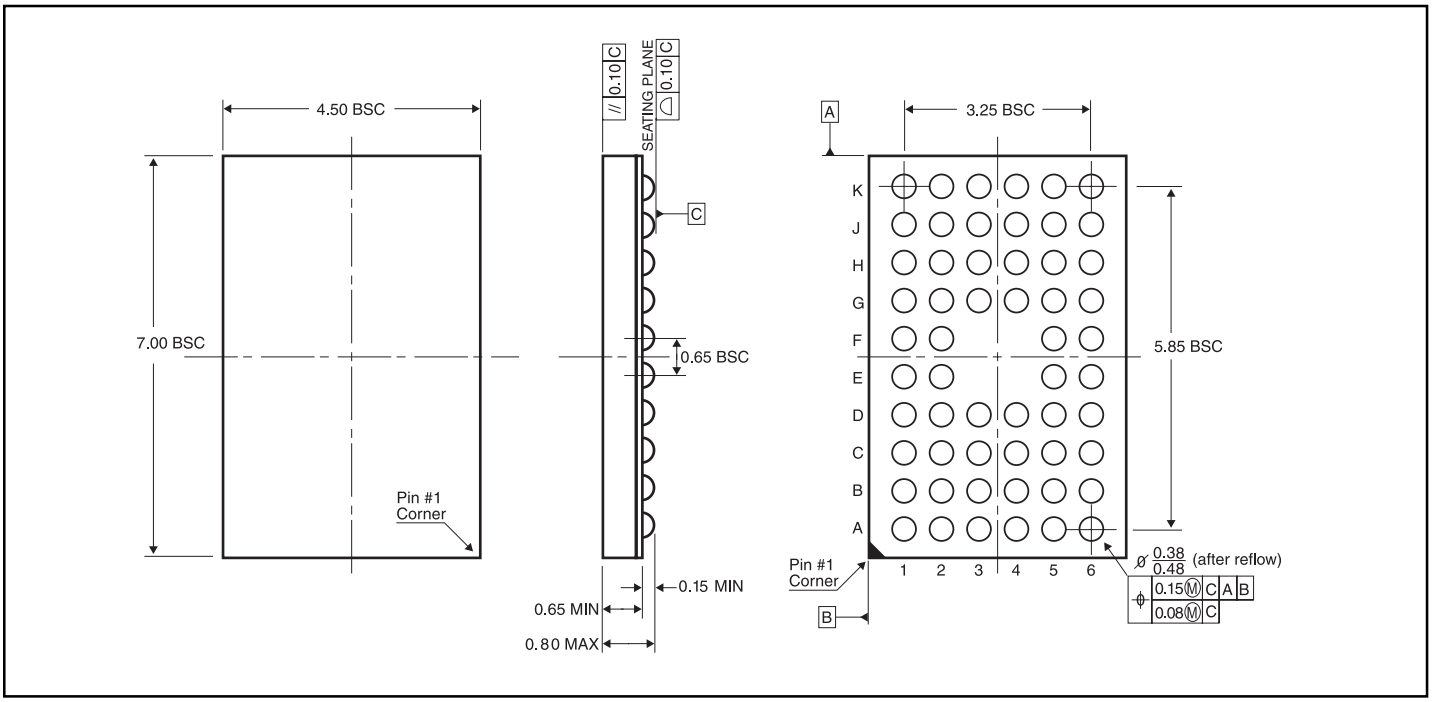
Packaging Mechanical: 48-Pin TSSOP (A)



Packaging Mechanical: 40-Contact TQFN (ZD)



Packaging Mechanical: 56-Ball VFBGA (NF)



Ordering Information

Ordering Code	Package Code	Pin Count - Package Type
PI6CVF857A	A	48-pin TSSOP
PI6CVF857AE	AE	Pb-free & Green, 48-pin TSSOP
PI6CVF857ZDE	ZDE	Pb-free & Green, 40-contact TQFN
PI6CVF857NF	NF	56-ball, VFBGA

Notes:
1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/