



## PI90LV047A/PI90LVB047A

### 3V LVDS Quad Flow-Through Differential Line Drivers

#### Features

- >500 Mbps (250 MHz) switching rates
- Flow-through pinout simplifies PCB layout
- Low Voltage Differential Signaling with output voltages of  $\pm 350\text{mV}$  into:
  - 100-ohm load (PI90LV047)
  - 50-ohm load (PI90LVB047)
- 300ps typical differential skew
- 400ps maximum differential skew
- 1.7ns maximum propagation delay
- 3.3V power supply design
- $\pm 350\text{mV}$  differential signaling
- Bus-Pin ESD protection >10kV
- Interoperable with existing 5V LVDS receivers
- High impedance on LVDS outputs on power down
- Conforms to TIA/EIA-644 LVDS Standard
- Industrial operating temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Packages (Pb-free & Green Available):
  - 16-pin SOIC (S)
  - 16-pin TSSOP (L)

#### Description

The PI90LV047A/PI90LVB047A are quad flow-through differential line drivers designed for applications requiring ultra-low power dissipation and high data rates. The devices are designed to support data rates in excess of 400 Mbps (200 MHz) using Low Voltage Differential Signaling (LVDS) technology.

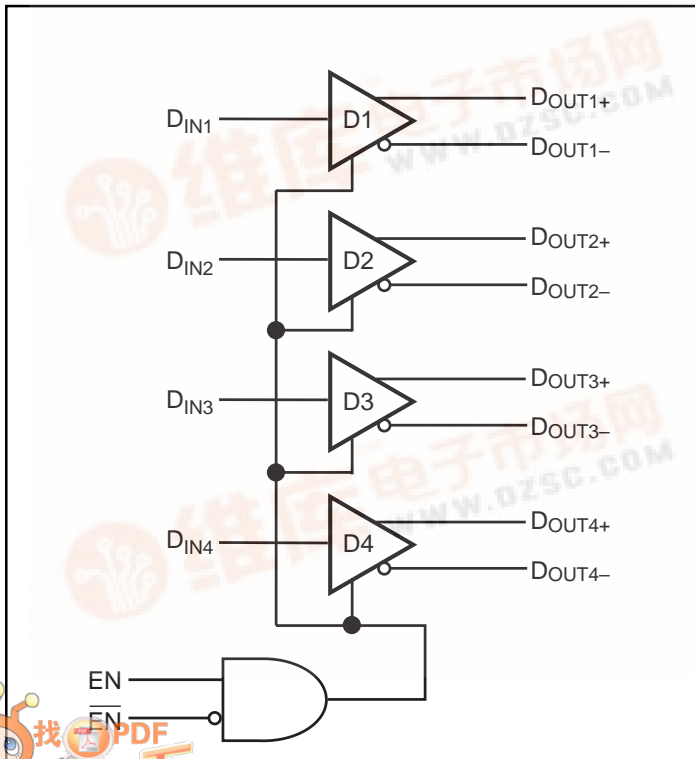
The PI90LV047A/PI90LVB047A accept low-voltage TTL/CMOS input levels and translates them to low-voltage (350 mV) differential output signals.

The PI90LVB047A doubles the output drive current to achieve Bus LVDS signaling levels with a 50-ohm load. A doubly terminated Bus LVDS line enables multipoint configurations. In addition, the driver supports a 3-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13mW typical. The devices have a flow-through pinout for easy PCB layout.

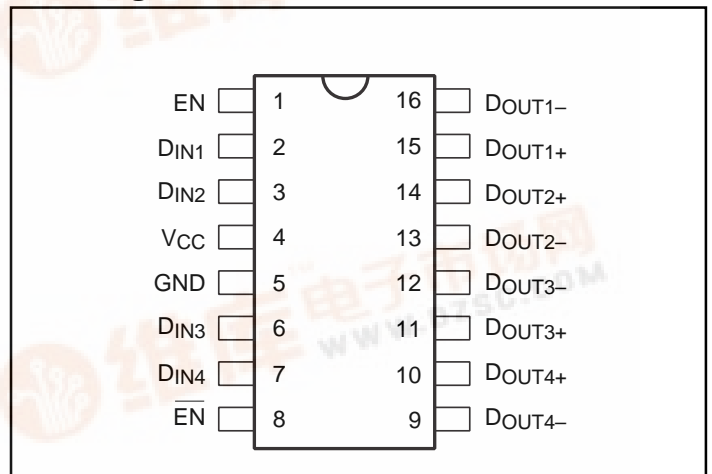
The EN and  $\overline{\text{EN}}$  inputs are banded together and control the 3-state outputs. The enables are common to all four drivers.

The intended application of these devices and signaling technique is for both point-to-point baseband (PI90LV047A) and multipoint (PI90LVB047A) data transmission over controlled impedance media.

#### Block Diagram

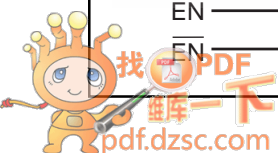


#### Pin Configuration



#### Truth Table

Enables		Input	Outputs	
EN	$\overline{\text{EN}}$	D <sub>IN</sub>	D <sub>OUT+</sub>	D <sub>OUT-</sub>
H	L or Open	L	L	H
		H	H	L
All other combinations of ENABLE inputs		X	Z	Z





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### Absolute Maximum Ratings

Supply Voltage ( $V_{CC}$ )	−0.3V to +4V
Input Voltage ( $D_{IN}$ )	−0.3V to ( $V_{CC} + 0.3V$ )
Enable Input Voltage ( $EN, \overline{EN}$ )	−0.3V to ( $V_{CC} + 0.3V$ )
Output Voltage ( $D_{OUT+}, D_{OUT-}$ )	−0.3V to +3.9V
Short Circuit Duration ( $D_{OUT+}, D_{OUT-}$ )	Continuous
Maximum Package Power Dissipation @ +25°C	
M Package	1088mW
MTC Package	866mW
Derate M Package	8.5 mW/°C above +25°C
Derate MTC Package	6.9 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C

### Lead Temperature Range

Soldering (4 seconds)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating <sup>(10)</sup>	
(HBM, 1.5kW, 100pF)	≥10kV
(EIAJ, 0W, 200pF)	≥1200V

### Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	+3.0	+3.3	+3.6	V
Operating Free Air Temperature ( $T_A$ )	−40	+25	+85	°C

### Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified<sup>(2,3,4)</sup>.

Symbol	Parameter	Test Conditions		Pin	Min.	Typ.	Max.	Units	
V <sub>OD1</sub>	Differential output voltage magnitude	R <sub>L</sub> = 100 ohms (LV047A) R <sub>L</sub> = 50 ohms (LVB047A) See Figure 1		D <sub>OUT−</sub> D <sub>OUT+</sub>	250	310	450	mV	
ΔV <sub>OD1</sub>	Change in Magnitude of V <sub>OD1</sub> for complementary output states					1	35	mV	
V <sub>OS</sub>	Offset voltage		LVxxx		1.125	1.2	1.375	V	
			LVBxxx		1.00	1.15	1.375		
ΔV <sub>OS</sub>	Change in magnitude of V <sub>OS</sub> for complementary output states					1	25	mV	
V <sub>OH</sub>	Output high voltage					1.33	1.6	V	
V <sub>OL</sub>	Output low voltage			0.90	1.02				
V <sub>IH</sub>	Input high voltage			D <sub>IN</sub> , EN, EN	2.0		V <sub>CC</sub>		
V <sub>IL</sub>	Input low voltage				GND		0.8		
I <sub>IH</sub>	Input high current	V <sub>IN</sub> = V <sub>CC</sub> or 2.5V				−20	2	+20	μA
I <sub>IL</sub>	Input low current	V <sub>IN</sub> = GND or 0.4V				−10	−2	+10	μA
V <sub>CL</sub>	Input clamp voltage	I <sub>CL</sub> = −18mA				−1.5	−0.8		V
I <sub>OS</sub>	Output short circuit current <sup>(11)</sup>	Enabled, D <sub>IN</sub> = V <sub>CC</sub> , D <sub>OUT+</sub> = 0V or D <sub>IN</sub> = GND, D <sub>OUT−</sub> = 0V	LVxxx LVBxxx	D <sub>OUT−</sub> D <sub>OUT+</sub>		−4.2	−10	mA	
						−9.0	−20		
I <sub>OSD</sub>	Differential output short circuit current <sup>(11)</sup>	Enabled, V <sub>OD</sub> = 0V	LVxxx LVBxxx			−4.2	−10	mA	
						−9.0	−20		
I <sub>OFF</sub>	Power-off leakage	V <sub>OUT</sub> = 0V or 3.6V, V <sub>CC</sub> = 0V or Open			−20	±1	+20	μA	
I <sub>OZ</sub>	Output 3-State current	EN = 0.8V and EN = 2.0V, V <sub>OUT</sub> = 0V or V <sub>CC</sub>			−10	±1	+10		
I <sub>CC</sub>	No load supply current drivers enabled	D <sub>IN</sub> = V <sub>CC</sub> or GND	LV047A LVB047A	V <sub>CC</sub>		4.0	8.0	mA	
						6.0	19.0		
I <sub>CCL</sub>	Loaded supply current drivers enabled	R <sub>L</sub> = 100 ohms, (all channels) D <sub>IN</sub> = V <sub>CC</sub> or GND (all inputs)	LV047A LVB047A			20	30		
						35	45		
I <sub>CCZ</sub>	No load supply current drivers disabled	D <sub>IN</sub> = V <sub>CC</sub> or GND, EN = GND, EN = V <sub>CC</sub>	LV047A LVB047A			2.2	8.0		
					3.0	8.0			



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## Switching Characteristics

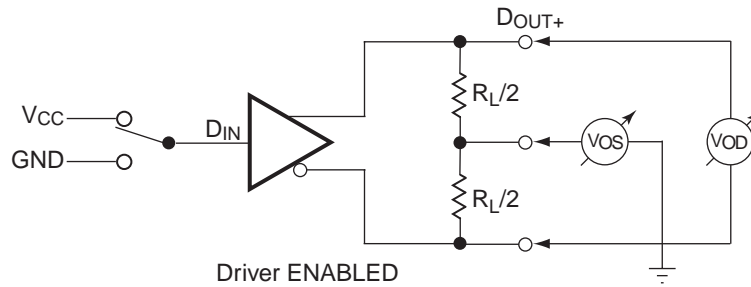
$V_{CC} = +3.3V \pm 10\%$ ,  $T_A = -40^\circ C^{(3,9,12)}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{PHLD}$	Differential Propagation Delay High to Low	$R_L = 100\text{ohms (LV047)}$ $R_L = 50\text{ohms (LVB047)}$ $C_L = 15\text{pF}$ (Figures 2 and 3)	0.5	0.8	1.9	
$t_{PLHD}$	Differential Propagation Delay Low to High		0.5	1.2	1.9	
$t_{SKD1}$	Differential Pulse Skew $t_{PHLD} - t_{PLHD}^{(5)}$		0	0.3	0.4	
$t_{SKD2}$	Channel-to-Channel Skew <sup>(6)</sup>		0	0.4	0.5	
$t_{SKD3}$	Differential Part-to-Part Skew <sup>(7)</sup>		0		1.0	
$t_{SKD4}$	Differential Part-to-Part Skew <sup>(8)</sup>		0		1.2	
$t_{TLH}$	Rise Time			0.5	1.5	
$t_{THL}$	Fall Time			0.5	1.5	
$t_{PHZ}$	Disable Time High to Z	$R_L = 100\text{ohms (LV047)}$ $R_L = 50\text{ohms (LVB047)}$ $C_L = 15\text{pF}$ (Figures 4 and 5)			5	
$t_{PLZ}$	Disable Time Low to Z				5	
$t_{PZH}$	Enable Time Z to High				7	
$t_{PZL}$	Enable Time Z to Low				7	
$f_{MAX}$	Maximum Operating Frequency <sup>(14)</sup>					MHz

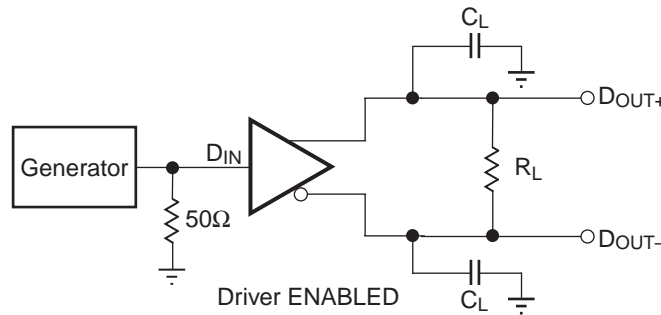
### Notes

- “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except:  $V_{OD1}$  and  $\Delta V_{OD1}$ .
- All typicals are given for:  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ .
- The PI90LV047A is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90 ohms to 110 ohms).
- $t_{SKD1} |t_{PHLD} - t_{PLHD}|$  is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- $t_{SKD2}$  is the Differential Channel-to-Channel Skew of any event on the same device.
- $t_{SKD3}$ , Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ C$  of each other within the operating temperature range.
- $t_{SKD4}$ , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as  $|Max - Min|$  differential propagation delay.
- Generator waveform for all tests unless otherwise specified:  $f = 1 \text{ MHz}$ ,  $Z_O = 50 \text{ ohms}$ ,  $t_r \leq 1 \text{ ns}$ , and  $t_f \leq 1 \text{ ns}$ .
- ESD Ratings:  
 HBM (1.5 kohms, 100pF)  $\geq 10\text{kV}$   
 EIAJ (0 ohm, 200pF)  $\geq 1200\text{V}$
- Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only.
- $C_L$  includes probe and jig capacitance.
- All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.
- $f_{MAX}$  generator input conditions:  $t_r = t_f < 1\text{ns}$  (0% to 100%), 50% duty cycle, 0V to 3V.  
 Output Criteria: duty cycle = 45%/55%,  $V_{OD} > 250\text{mV}$ , all channels switching.

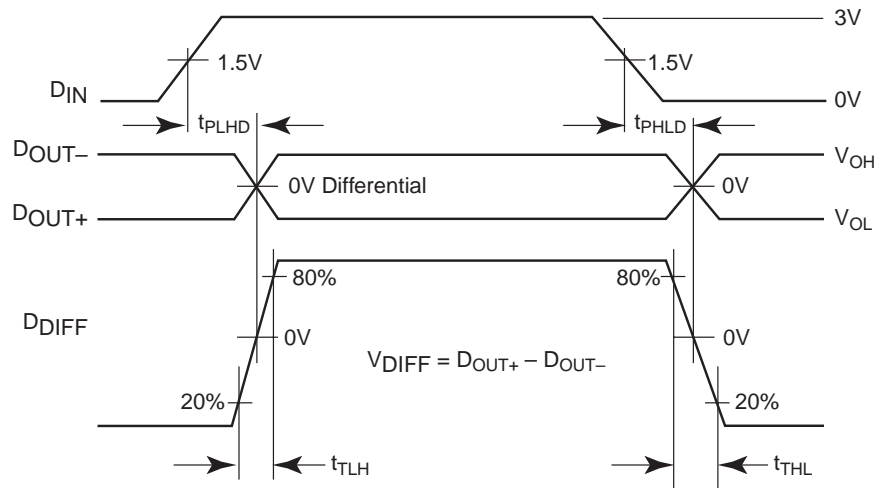
## Parameter Measurement Information



**Figure 1. Driver  $V_{OD}$  and  $V_{OS}$  Test Circuit**



**Figure 2. Driver Propagation Delay & Transition Time Test Circuit**



**Figure 3. Driver Propagation Delay and Transition Time Waveforms**

The schematic diagram illustrates a 1/4 PI90LV047A differential line driver circuit. A Generator is connected to the EN pin through a 50Ω resistor. The VCC pin is connected to a +1.2V supply, and the GND pin is connected to ground. The D<sub>IN</sub> pin is connected to the D input of a differential driver. The EN pin is connected to the EN input of a differential driver. The output of the driver is connected to the D<sub>OUT</sub> pins, which are terminated with 50Ω resistors to ground. The output signals are labeled D<sub>OUT</sub>+ and D<sub>OUT</sub>-.

The timing diagram illustrates the relationship between the Enable (EN) signal and the DAC outputs (DOUT+ and DOUT-). The EN signal is shown as a square wave between 0V and 3V. The DOUT+ and DOUT- signals are shown as square waves between 0V and 3V. The diagram includes the following labels and parameters:

- EN When  $\overline{EN} = \text{GND or OPEN}$** : This label is associated with the first EN signal trace, which is active-low.
- $\overline{EN}$  When  $EN = V_{CC}$** : This label is associated with the second EN signal trace, which is active-low.
- $D_{OUT+}$  When  $D_{IN} = V_{CC}$** : This label is associated with the top output signal trace.
- $D_{OUT-}$  When  $D_{IN} = \text{GND}$** : This label is associated with the bottom output signal trace.
- $D_{OUT+}$  When  $D_{IN} = \text{GND}$** : This label is associated with the top output signal trace during its low state.
- $D_{OUT-}$  When  $D_{IN} = V_{CC}$** : This label is associated with the bottom output signal trace during its high state.
- Parameters:**
  - $t_{PHZ}$ : Propagation delay from EN falling to DOUT+ rising.
  - $t_{PZH}$ : Propagation delay from EN rising to DOUT+ falling.
  - $t_{PLZ}$ : Propagation delay from EN falling to DOUT- rising.
  - $t_{PZL}$ : Propagation delay from EN rising to DOUT- falling.

Enable

Data Input

1/4 PI90LV047A

Any LVDS Receiver

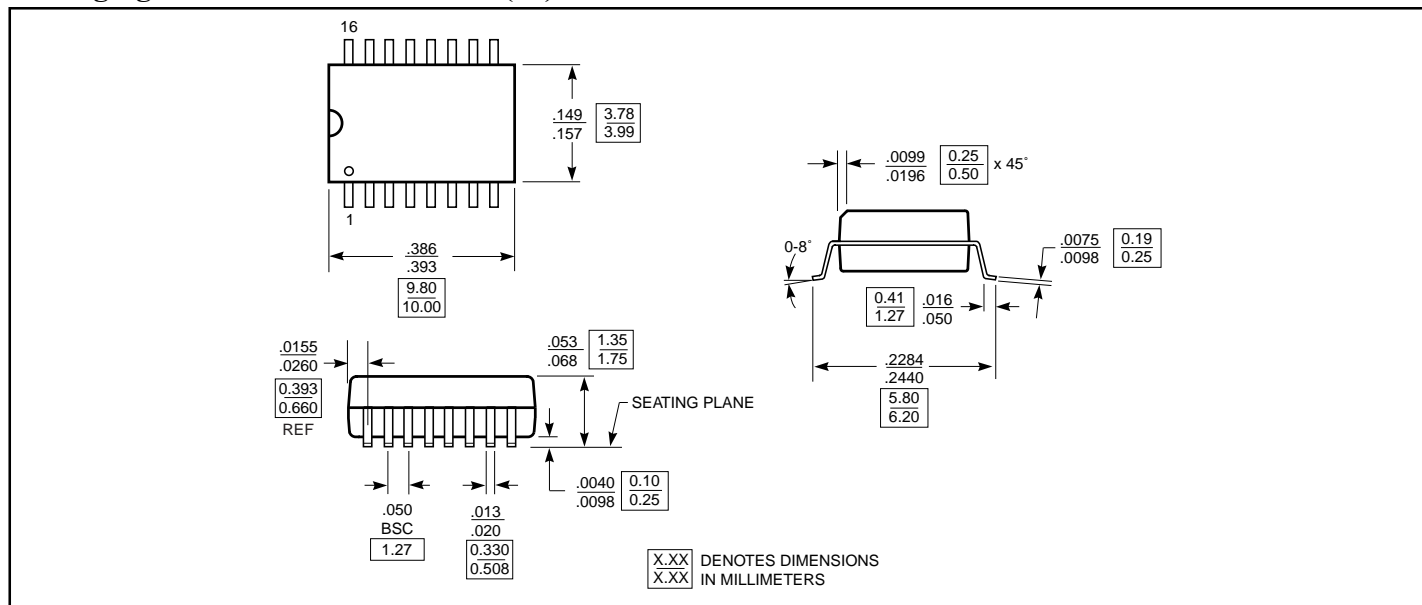
Data Output

### Figure 6. Point-to-Point Application

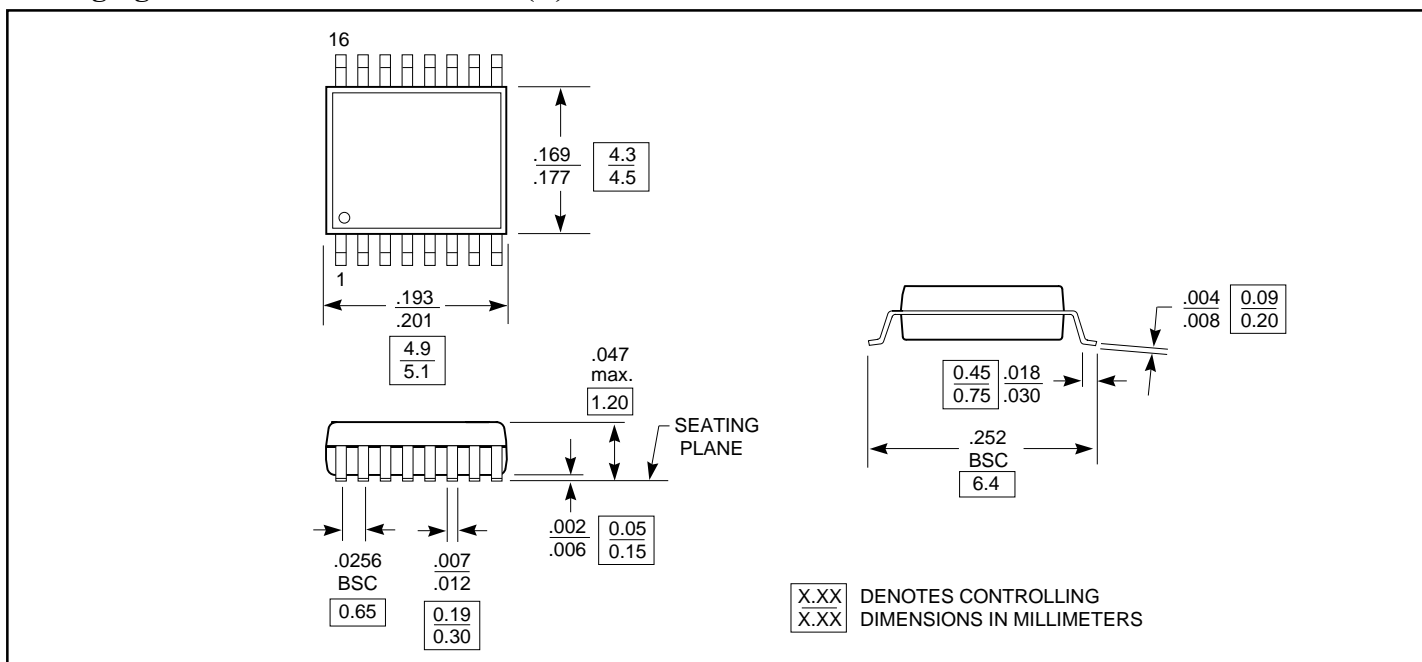


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**Packaging Mechanical: 16-Pin SOIC (W)**



**Packaging Mechanical: 16-Pin TSSOP (L)**





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**Ordering Information**

Ordering Code	Package Code	Package Type
PI90LV047AW	W	16-pin SOIC
PI90LV047AWE	W	Pb-free & Green, 16-pin SOIC
PI90LV047AL	L	16-pin TSSOP
PI90LV047ALE	L	Pb-free & Green, 16-pin TSSOP
PI90LVB047AW	W	16-pin SOIC
PI90LVB047AWE	W	Pb-free & Green, 16-pin SOIC
PI90LVB047AL	L	16-pin TSSOP
PI90LVB047ALE	L	Pb-free & Green, 16-pin TSSOP

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. X = Tape and reel