PIC18F24J10/25J10/44J10/45J10 Rev. A2 Silicon Errata

The PIC18F24J10/25J10/44J10/45J10 Rev. A2 parts you have received conform functionally to the Device Data Sheet (DS39682**A**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F24J10/25J10/44J10/45J10 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F24J10/25J10/44J10/45J10 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F24J10	0001 1101 000	0001
PIC18LF24J10	0001 1101 010	0001
PIC18F25J10	0001 1100 000	0001
PIC18LF25J10	0001 1100 010	0001
PIC18F44J10	0001 1101 001	0001
PIC18LF44J10	0001 1101 011	0001
PIC18F45J10	0001 1100 001	0001
PIC18LF45J10	0001 1100 011	0001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Timer1

In 16-Bit Asynchronous Counter mode or 16-Bit Asynchronous Oscillator mode, the TMR1H buffer does not update when TMR1L is read. This issue only affects reading the TMR1H registers. The timers increment and set the interrupt flags as expected. The Timer registers can also be written as expected.

Work around

Use 8-bit mode by clearing the RD16 (T1CON<7>) bit or use the synchronization option by clearing T1SYNC (T1CON<2>).

2. Module: EUSART

In asynchronous duplex communication, the reception can get corrupted if any bit of the TXSTA register is modified during a reception.

Work around

The CSRC (TXSTA<7>) bit should not be set. Though this is a "don't care" bit in Asynchronous mode, make sure that this bit is not set.

3. Module: EUSART

In Synchronous mode, EUSART baud rates using SPBRG values of '0' and '1' may not function correctly.

Work around

Use another baud rate configuration to generate the desired baud rate.

4. Module: EUSART

After the last received byte has been read from the EUSART receive buffer, RCREG, the value is no longer valid for subsequent read operations. The RCREG register should only be read once for each byte received.

Work around

After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREG, poll the RCIDL (BAUDCON<6>) bit for a low-to-high transition, or use the EUSART Receive Interrupt Flag, RCIF (PIR1<5>).

5. Module: EUSART

In 9-Bit Asynchronous, Full-Duplex, Receive mode, received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after RCIDL (BAUDCON<6>) is set.

Work around

Only write to TX9D when a reception is not in progress (RCIDL = 1). No interrupt is associated with RCIDL, therefore, it must be polled in software to determine when TX9D can be updated.

6. Module: MSSP

In SPI mode, the Buffer Full flag bit, BF (SSPxSTAT<0>), the Write Collision Detect bit, WCOL (SSPxCON1<7>), and the Receive Overflow Indicator bit, SSPOV (SSPxCON1<6>), are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPxCON1 register).

For example, if SSPxBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPxBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPxBUF is read (thus clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

7. Module: MSSP (I^2C™ Mode)

It has been observed that following a Power-on Reset, I^2C mode may not initialize properly by just configuring the SCLx and SDAx pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I^2C operation:

1. Configure the SCLx and SDAx pins as outputs by clearing their corresponding TRIS bits.
2. Force SCLx and SDAx low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCLx and SDAx as inputs by setting their TRIS bits.

Once this is done, use the SSPxCON1 and SSPxCON2 registers to configure the proper I^2C mode as before .

8. Module: Core (Program Memory Space)

Writes to program memory address 300000h, that are not blocked, can cause the program memory at different locations to be corrupted.

Work around

Do not write to address 300000h. If you wish to modify the contents of the Configuration registers, then modify the Configuration Words located at the end of the user memory (7FF4h for PIC18FX5J10 devices and 3FF4h for PIC18FX4J10 devices) and issue a Reset command. This will reload the Configuration registers with the new configuration setting.

9. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer, TXREG, are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREG is written to;
- the baud rate counter overflows (at the end of the bit period); and
- a Stop bit is being transmitted (shifted out of TSR).

Work around

If possible, do not use the module's double-buffer capability. Instead, load the TXREG register when the TRMT bit (TXSTA<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, then load TXREG immediately after TXIF is set or wait 1-bit time after TXIF is set. Both solutions prevent writing TXREG while a Stop bit is transmitted. Note that TXIF is set at the beginning of the Stop bit transmission.

If transmission is intermittent, then do the following:

- Wait for the TRMT bit to be set before loading TXREG.
- Alternatively, use a free timer resource to time the baud period. Set up the timer to overflow at the end of the Stop bit, then start the timer when you load the TXREG. Do not load the TXREG when timer is about to overflow.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (04/2006)

First revision of this document. Includes silicon issues 1 (Timer1), 2-5 (EUSART), 6 (MSSP), 7 (MSSP – I^2C Mode), 8 (Core – Program Memory Space) and 9 (EUSART).

Rev B Document (05/2006)

Updated silicon issue 9 (EUSART).

NOTES:

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