DATA SHEET

PLC18V8Z

Zero standby power
CMOS versatile PAL devices

Product specification
Replaces data sheet PLC18V8Z35/PLC18V8ZI of Dec 19 1995,
and data sheet PLC18V8Z25/PLC18V8ZI of Dec 19, 1995

1997 Aug 08

Philips
Semiconductors

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Zero standby power CMOS versatile PAL devices

PLC18V8Z

DESCRIPTION

The PLC18V8Z is a universal PAL® device featuring high performance and virtually zero-standby power for power sensitive applications. They are reliable, user-configurable substitutes for discrete TTL/CMOS logic. While compatible with TTL and HCT logic, the PLC18V8Z can also replace HC logic over the V_{CC} range of 4.5 to 5.5V.

The PLC18V8Z is a two-level logic element comprised of 10 inputs, 74 AND gates (product terms) and 8 output Macro cells.

Each output features an “Output Macro Cell” which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the PLC18V8Z is capable of emulating all common 20-pin PAL devices to reduce documentation, inventory, and manufacturing costs.

A power-up reset function and a Register Preload function have been incorporated in the PLC18V8Z architecture to facilitate state machine design and testing.

With a standby current of less than 100µA and active power consumption of 1.5mA/MHz, the PLC18V8Z is ideally suited for power sensitive applications in battery operated/backed portable instruments and computers.

The PLC18V8Z is also processed to industrial requirements for operation over an extended temperature range of -40°C to +85°C and supply voltage of 4.5V to 5.5V.

Ordering information can be found on the following page.

FEATURES

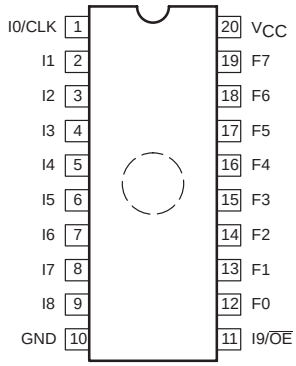
- 20-pin Universal Programmable Array Logic
- Virtually Zero-Standby-power
  - 20µA (typical)
- Available in DIP, PLCC, SOL (Small Outline), SSOP (Shrink Small Outline), and TSSOP (Thin Shrink Small Outline) packages
- Functional replacement for Series 20 PAL devices
  - I_{OL} = 24mA
- Up to 18 inputs and 8 input/output macro cells
- Programmable output polarity
- Power-up reset on all registers
- Register Preload capability
- Synchronous Preset/Asynchronous Reset
- Security fuse to prevent duplication of proprietary designs
- Also available in 3V operation–the P3C18V8Z

APPLICATIONS

- Battery powered instruments
- Laptop and pocket computers
- Industrial control
- Medical Instruments
- Portable communications equipment

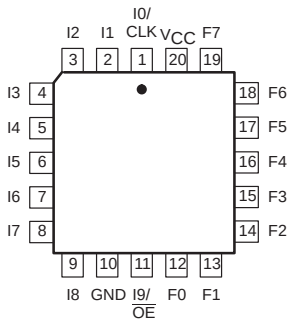
PIN CONFIGURATIONS

D, DB, DH, N, Packages



D = Plasitc Small Outline Large Package (300mil-wide)
DB = Plastic Shrink Small Outline Package (5.3mm wide)
DH = Plastic Thin Shrink Small Outline Package (4.4mm wide)
N = Plastic Dual In-Line Package (DIP) (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

SP00544

PIN DESCRIPTIONS

I	Dedicated Input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)
F	Output/Input Macrocell
CLK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

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ORDERING INFORMATION

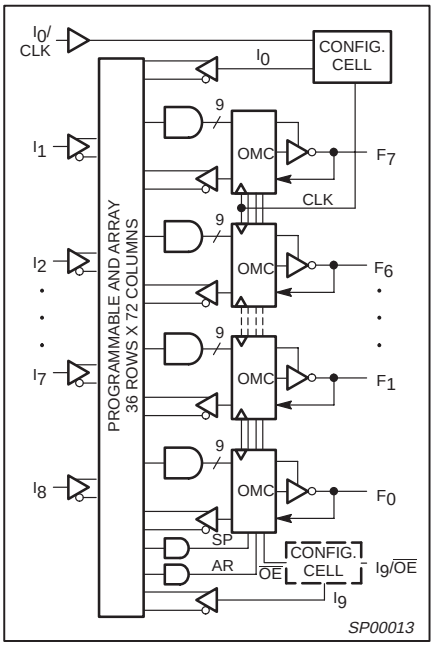
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin (300mil-wide) Plastic Dual In-Line Package, 25ns t_{PD}	Commercial Temperature Range ± 5% Power Supplies	PLC18V8Z25N	SOT146-1
20-Pin (350mil square) Plastic Leaded Chip Carrier Package		PLC18V8Z25A	SOT380-1
20-Pin (300mil-wide) Plastic Small Outline Large Package		PLC18V8Z25D	SOT163-1
20-Pin (5.3mm-wide) Plastic Shrink Small Outline Package		PLC18V8Z25DB	SOT339-1
20-Pin (4.4mm-wide) Plastic Thin Shrink Small Outline Package		PLC18V8Z25DH	SOT360-1
20–Pin (300mil–wide) Plastic Dual In–Line Package. 35ns t_{PD}		PLC18V8Z35N	SOT146–1
20–Pin (350mil square) Plastic Leaded Chip Carrier Package		PLC18V8Z35A	SOT380–1
20–Pin (300mil square) Plastic Small Outline Large Package Package		PLC18V8Z35D	SOT163–1
20–Pin (5.3mm–wide) Plastic Shrink Small Outline Package		PLC18V8Z35DB	SOT339–1
20–Pin (4.4mm–wide) Plastic Thin shrink Small Outline Package		PLC18V8Z35DH	SOT260–1
20-Pin (300mil-wide) Plastic Dual In-Line Package 25ns t_{PD}	Industrial Temperature Range ± 10% Power Supplies	PLC18V8ZIAN	SOT146-1
20-Pin (350mil square) Plastic Leaded Chip Carrier Package		PLC18V8ZIAA	SOT380-1
20-Pin (300mil-wide) Plastic Small Outline Large Package		PLC18V8ZIAD	SOT163-1
20-Pin (5.3mm-wide) Plastic Shrink Small Outline Package		PLC18V8ZIADB	SOT339-1
20-Pin (4.4mm-wide) Plastic Thin Shrink Small Outline Package		PLC18V8ZIADH	SOT360-1
20–Pin (300mil–wide) Plastic Dual In–Line Package, 40ns t_{PD}		PLC18V8ZIN	SOT146–1
20–Pin (350mil square) Plastic Leaded chip Carrier Package		PLC18V8ZIA	SOT380–1
20–Pin (300mil square) Plastic Small Outline Large Package		PLC18V8ZZID	SOT163–1
20–Pin (5.3mm–wide) Plastic Shrink Small Outline Package		PLC18V8ZIDB	SOT339–1
20–Pin (4.4mm–wide) Plastic Thin Shrink Small Outline Package		PLC18V8ZIDH	SOT360–1

PAL DEVICE TO PLC18V8Z OUTPUT PIN CONFIGURATION CROSS REFERENCE

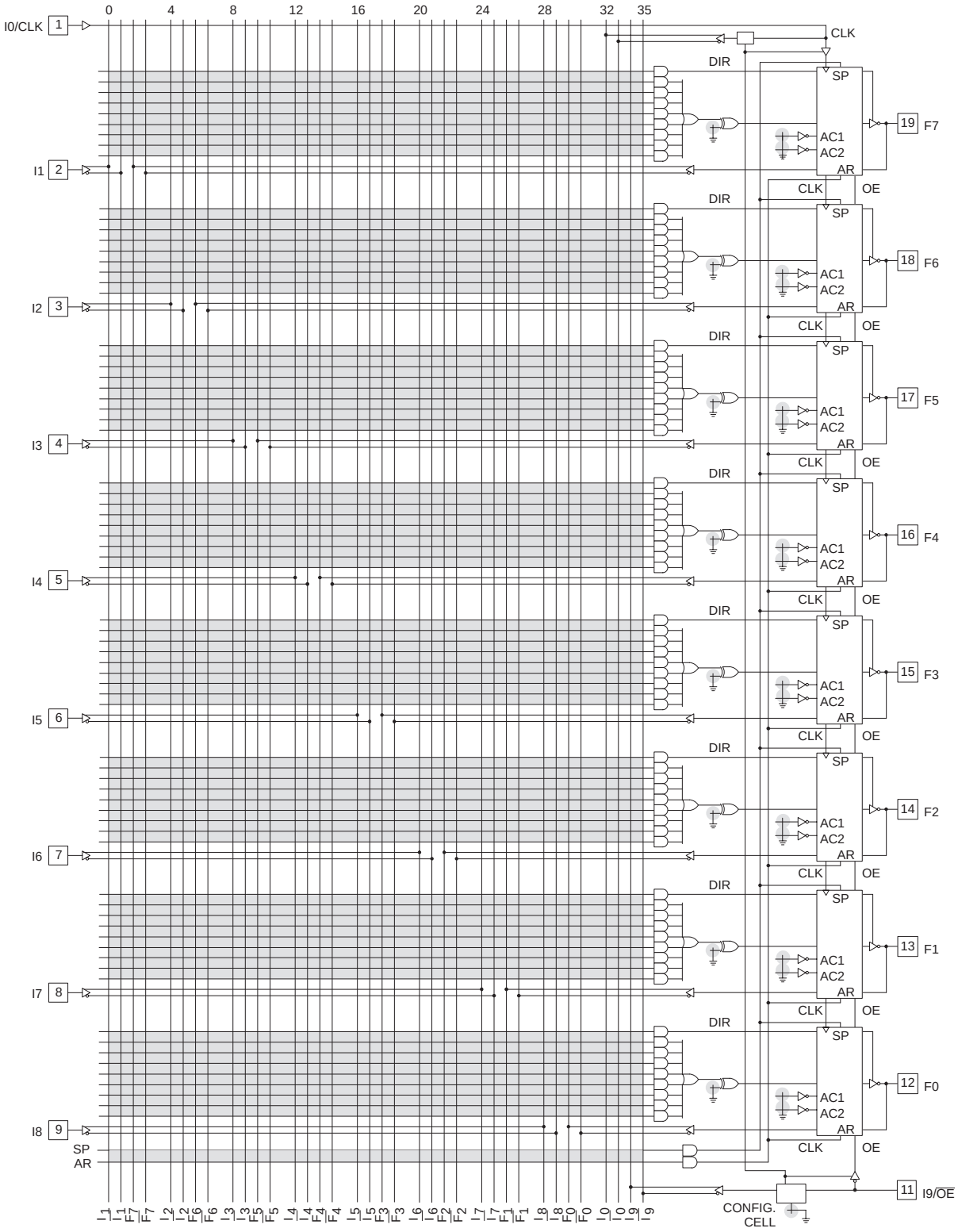
PIN NO.	PLC 18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	$I_9/\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

The Philips Semiconductors' state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Philips Semiconductors to functionally test the devices prior to shipment to the customer. Additionally, this allows Philips Semiconductors to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



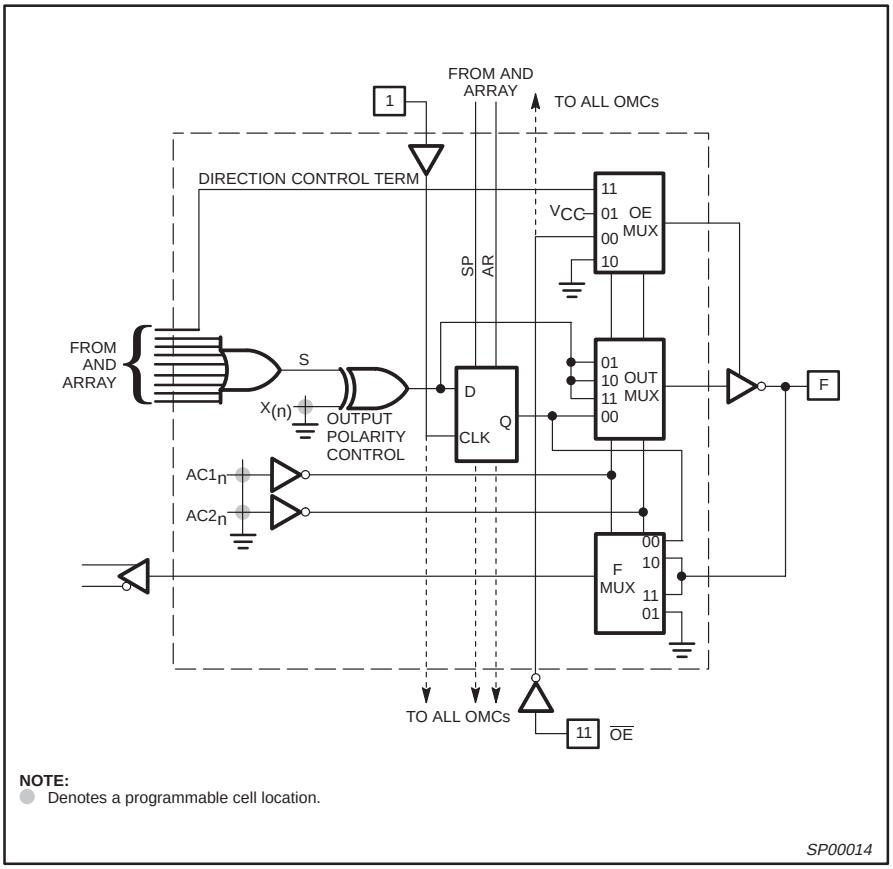
NOTES:
In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
Denotes a programmable cell location.

SP00012

OUTPUT MACRO CELL (OMC)



THE OUTPUT MACRO CELL (OMC)

The PLC18V8Z series devices have 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the configuration cell table, 4 different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

DESIGN SECURITY

The PLC18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

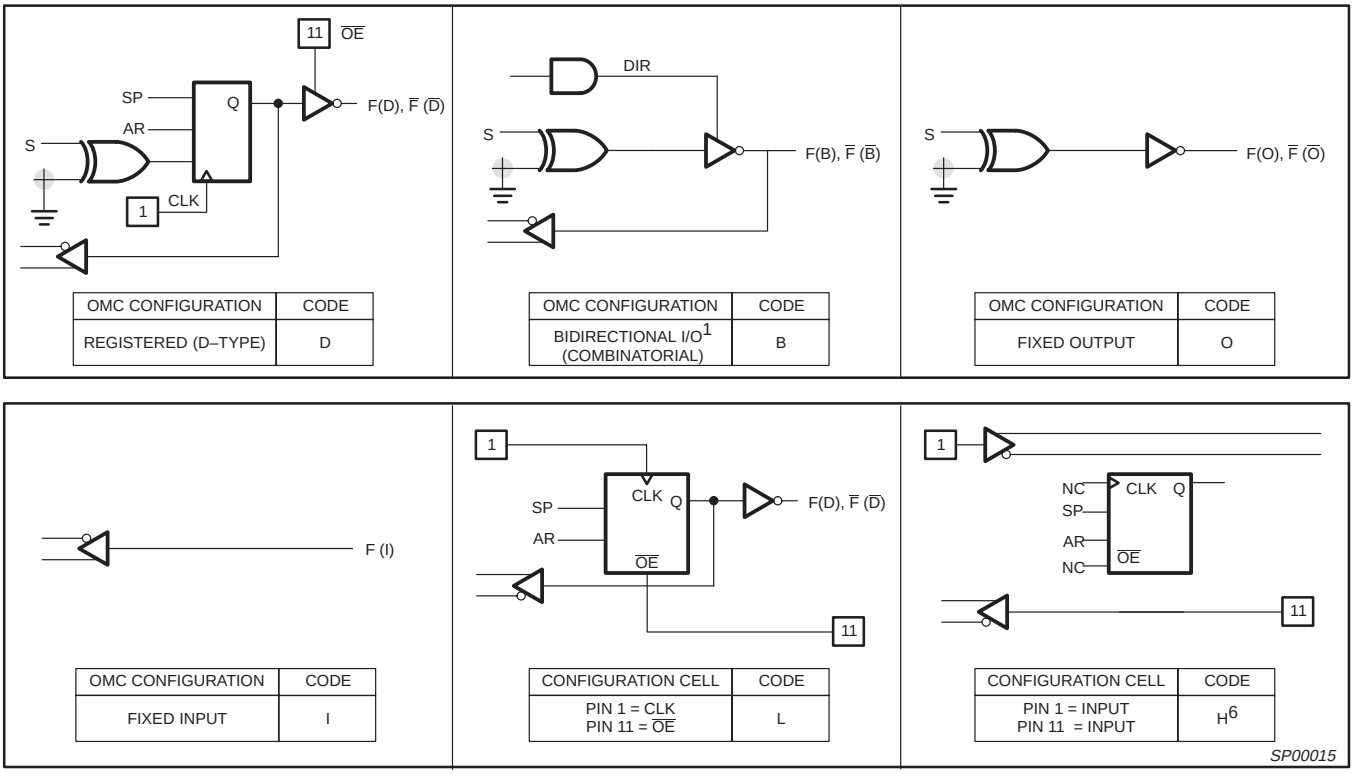
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_1$	$AC2_N$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registerd OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

ARCHITECTURE CONTROL—AC1 and AC2



OMC CONFIGURATION	CODE
REGISTERED (D–TYPE)	D

OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B

OMC CONFIGURATION	CODE
FIXED OUTPUT	O

OMC CONFIGURATION	CODE
FIXED INPUT	I

CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L

CONFIGURATION CELL	CODE
PIN 1 = INPUT PIN 11 = INPUT	H[6]

NOTES:
A factory shipped unprogrammed device is configured such that:
1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic “0” (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D).

ABSOLUTE MAXIMUM RATINGS[1]

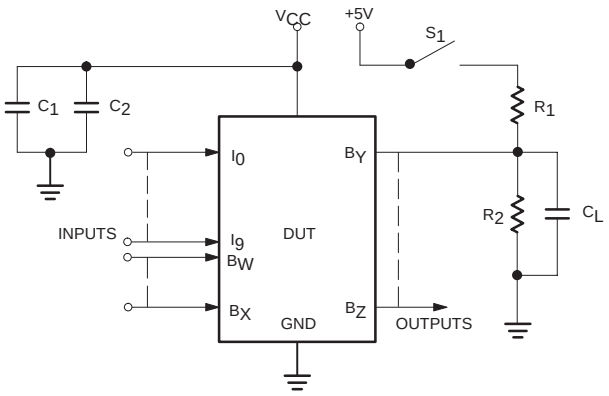
SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{CC}	Operating supply voltage	4.5 to 5.5 (Industrial) 4.75 to 5.25 (Commercial)	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} + 0.5	V_{DC}
$\Delta t/\Delta V$	Input/clock transition rise or fall[2]	250	ns/V maximum
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	–40 to +85 (Industrial) 0 to +75 (Commercial)	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All digital circuits can oscillate or trigger prematurely when input rise and fall times are very long. When the input signal to a device is at or near the switching threshold, noise on the line will be amplified and can cause oscillation which, if the frequency is low enough, can cause subsequent stages to switch and give erroneous results. For this reason, Schmitt-triggers are recommended if rise/fall times are likely to exceed 250ns at V_{CC} = 4.5V.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

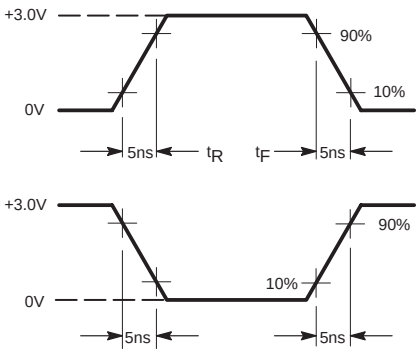
AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

SP00006

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

SP00017

DC ELECTRICAL CHARACTERISTICS

Commercial = 0°≤C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 20µA V_{CC} = MIN, I_{OL} = 24mA			0.100 0.500	V V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –3.2mA V_{CC} = MIN, I_{OH} = –20µA	2.4 V_{CC} – 0.1V			V V
Input current						
I_{IL}	Low[7]	V_{IN} = GND			–10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 –10	µA µA
I_{OS}	Short-circuit[3]	V_{OUT} = GND			–130	mA
I_{CC}	V_{CC} supply current (Standby)	V_{CC} = MAX, V_{IN} = 0 or V_{CC}[8]		20	100	µA
I_{CC}/f	V_{CC} supply current (Active)[4]	V_{CC} = MAX (CMOS inputs)[5, 6]			1.5	mA/MHz
Capacitance						
C_I	Input	V_{CC} = 5V, V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

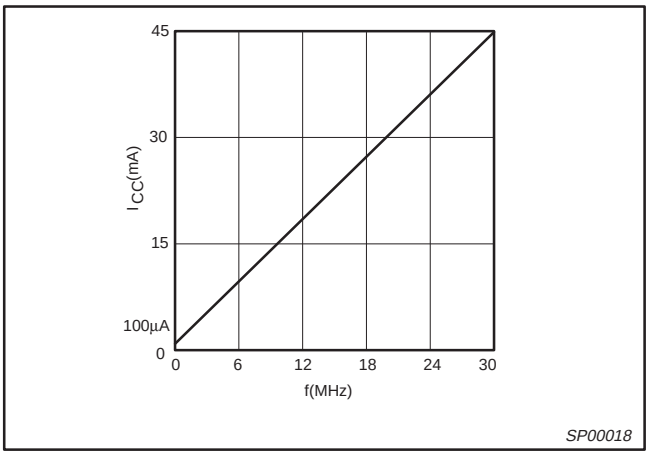


Figure 1. I_{CC} vs Frequency[5, 6] (Worst Case)

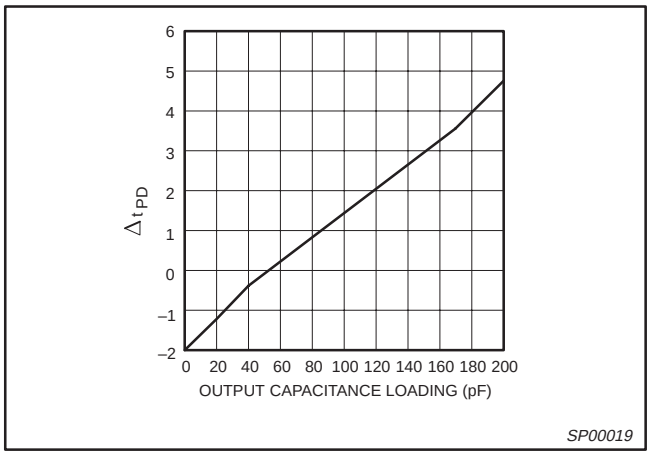


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all outputs switching.
5. ΔI_{CC}/TTL input = 2mA.
6. ΔI_{CC} vs frequency (registered configuration) = 2mA/MHz.
7. I_{IL} for Pin 1 (I_0/CLK) is ± 10µA with V_{IN} = 0.4V.
8. V_{IN} includes CLK and $\overline{OE}$ if applicable.

AC ELECTRICAL CHARACTERISTICS[4]

Commercial = 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V; R_2 = 390Ω

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1]		PLC18V8Z25 (Commercial)		PLC18V8ZIA (Industrial)		UNIT
				R_1 (Ω)	C_L (pF)	MIN	MAX	MIN	MAX	
Pulse width										
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +	200	50	33		33		ns
t_{CKH}	Clock width High	CLK +	CLK –	200	50	15		15		ns
t_{CKL}	Clock width Low	CLK –	CLK +	200	50	15		15		ns
t_{ARW}	Async reset pulse width	I ±, F±	I ∓, F ∓			25		25		ns
Hold time										
t_{IH}	Input or feedback data hold time	CLK +	Input ±	200	50	0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	200	50	18		18		ns
Propagation delay										
t_{PD}	Delay from input to active output	I ±, F±	F±	200	50		25		25	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	200	50		15		15	ns
t_{OE1}[3]	Product term enable to outputs off	I ±, F±	F±	Active-High R = 1.5k Active-Low R = 550	50		25		25	ns
t_{OD1}[2]	Product term disable to outputs off	I ±, F±	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		25	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	OE –	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		20		20	ns
t_{OE2}[3]	Pin 11 output enable to active output	OE +	F±	Active-High R = 1.5k Active-Low R = 550	50		20		20	ns
t_{ARD}	Async reset delay	I ±, F±	F +				30		30	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +			20		20		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +			20		20		ns
t_{PPR}	Power-up reset	V_{CC} +	F +				25		25	ns
Frequency of operation										
f_{MAX}	Maximum frequency	I/($t_{IS} + t_{CKO}$)		200	50		30		30	MHz

NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} – 0.5V) with S_1 open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S_1 closed.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.
4. Leave all the cells on unused product terms intact (unprogrammed) for all patterns.

AC ELECTRICAL CHARACTERISTICS[4]

Commercial = 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V; R_2 = 390Ω

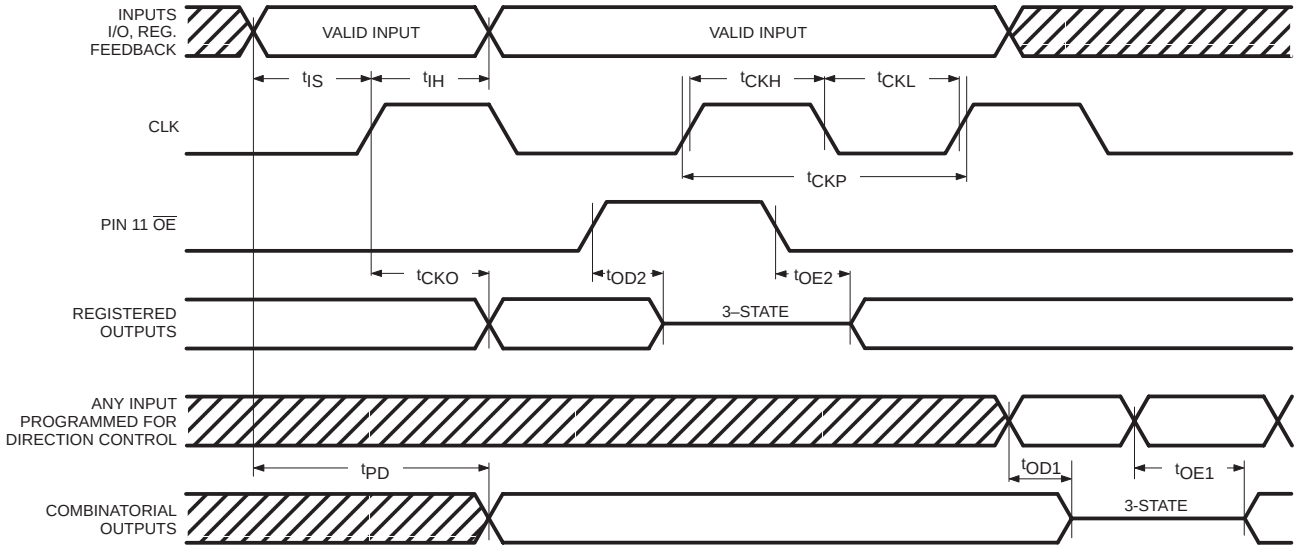
SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1]		PLC18V8Z35 (Commercial)		PLC18V8ZI (Industrial)		UNIT
				R_1 (Ω)	C_L (pF)	MIN	MAX	MIN	MAX	
Pulse width										
t_{CKP}	Clock period (Minimum t_{IS} + t_{CKO})	CLK +	CLK +	200	50	47		57		ns
t_{CKH}	Clock width High	CLK +	CLK –	200	50	20		25		ns
t_{CKL}	Clock width Low	CLK –	CLK +	200	50	20		25		ns
t_{ARW}	Async reset pulse width	I ±, F±	I ∓, F ∓			35		40		ns
Hold time										
t_{IH}	Input or feedback data hold time	CLK +	Input ±	200	50	0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	200	50	25		30		ns
Propagation delay										
t_{PD}	Delay from input to active output	I ±, F±	F±	200	50		35		40	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	200	50		22		27	ns
t_{OE1}[3]	Product term enable to outputs off	I ±, F±	F±	Active-High R = 1.5k Active-Low R = 550	50		35		40	ns
t_{OD1}[2]	Product term disable to outputs off	I ±, F±	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		35		40	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	OE –	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		40	ns
t_{OE2}[3]	Pin 11 output enable to active output	OE +	F±	Active-High R = 1.5k Active-Low R = 550	50		25		30	ns
t_{ARD}	Async reset delay	I ±, F±	F +				35		40	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +			25		30		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +			25		30		ns
t_{PPR}	Power-up reset	V_{CC} +	F +				35		40	ns
Frequency of operation										
f_{MAX}	Maximum frequency	I/(t_{IS} + t_{CKO})		200	50		21		18	MHz

NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} – 0.5V) with S_1 open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S_1 closed.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.
4. Leave all the cells on unused product terms intact (unprogrammed) for all patterns.

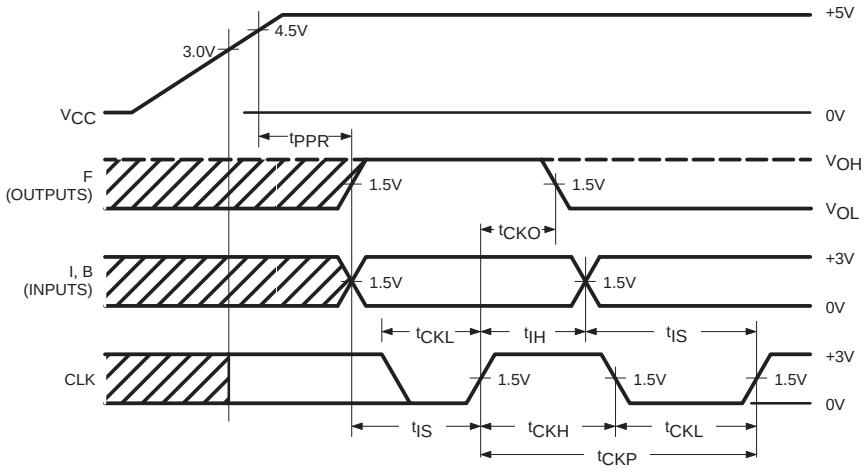
POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC18V8Z. All internal registers will reset to Active-Low (logical “0”) after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an Active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the Active-High output condition during a system power-up condition.

TIMING DIAGRAMS



Switching Waveforms

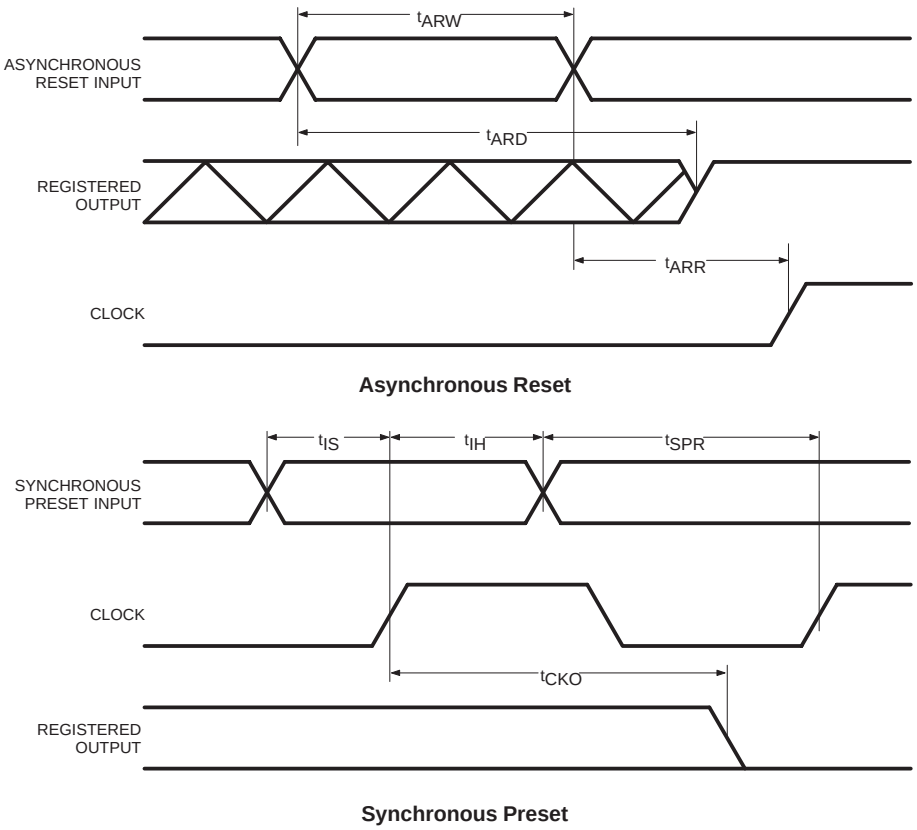


NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Power-Up Reset

SP00020

TIMING DIAGRAMS (Continued)



Asynchronous Reset

Synchronous Preset

SP00021

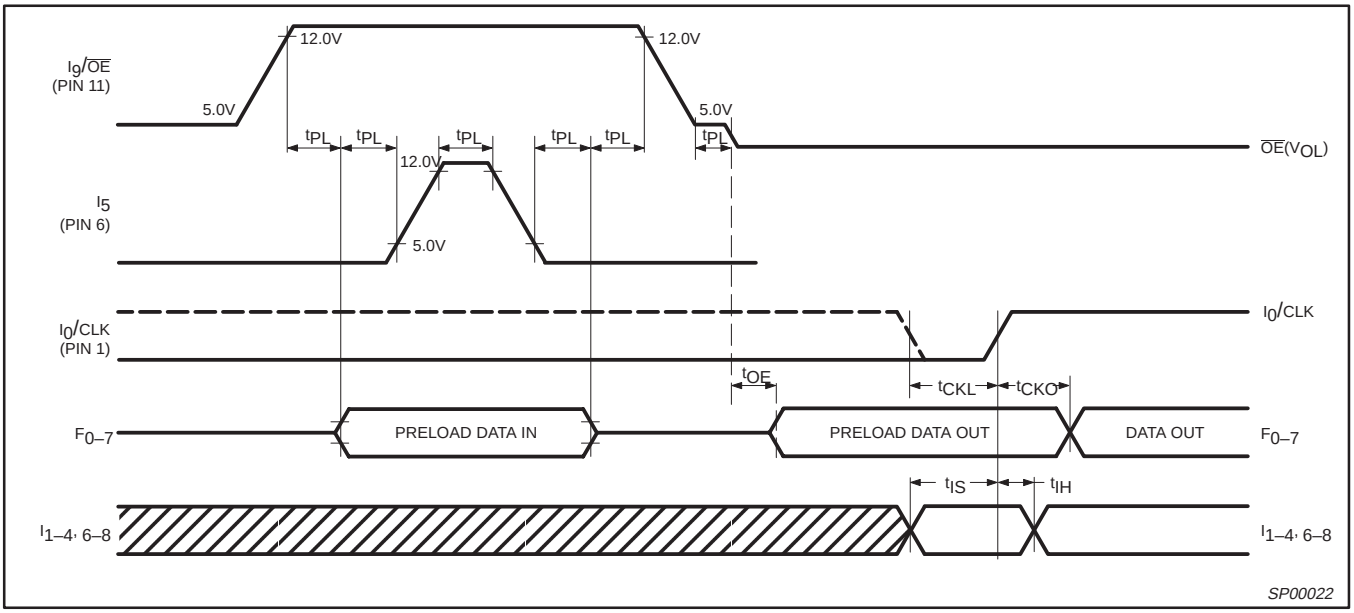
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 (I9/$\overline{OE}$ and I5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F0 – F7, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F0 – F7 during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F0 – F7.

Refer to the voltage waveform for timing and voltage references.
t_{PL} = 10µsec.

REGISTER PRELOAD (DIAGNOSTIC MODE)



LOGIC PROGRAMMING

The PLC18V8Z series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP design software package. ABEL™ and CUPL™ design software packages also support the PLC18V8Z architecture.

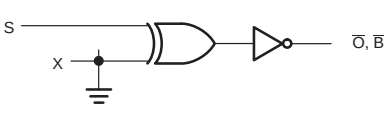
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC18V8Z logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP only.

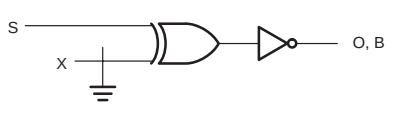
With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY – (O, B)



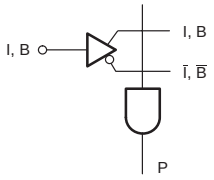
ACTIVE LEVEL	CODE
INVERTING[1]	L



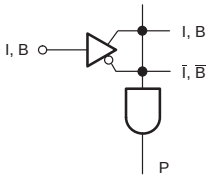
ACTIVE LEVEL	CODE
NON-INVERTING	H

SP00023

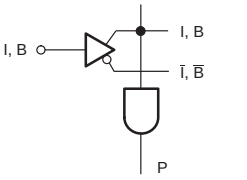
"AND" ARRAY – (I, B)



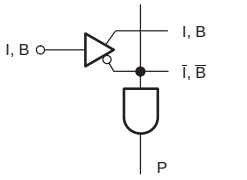
STATE	CODE
DON'T CARE	–



STATE	CODE
INACTIVE[1]	O



STATE	CODE
I, B	H



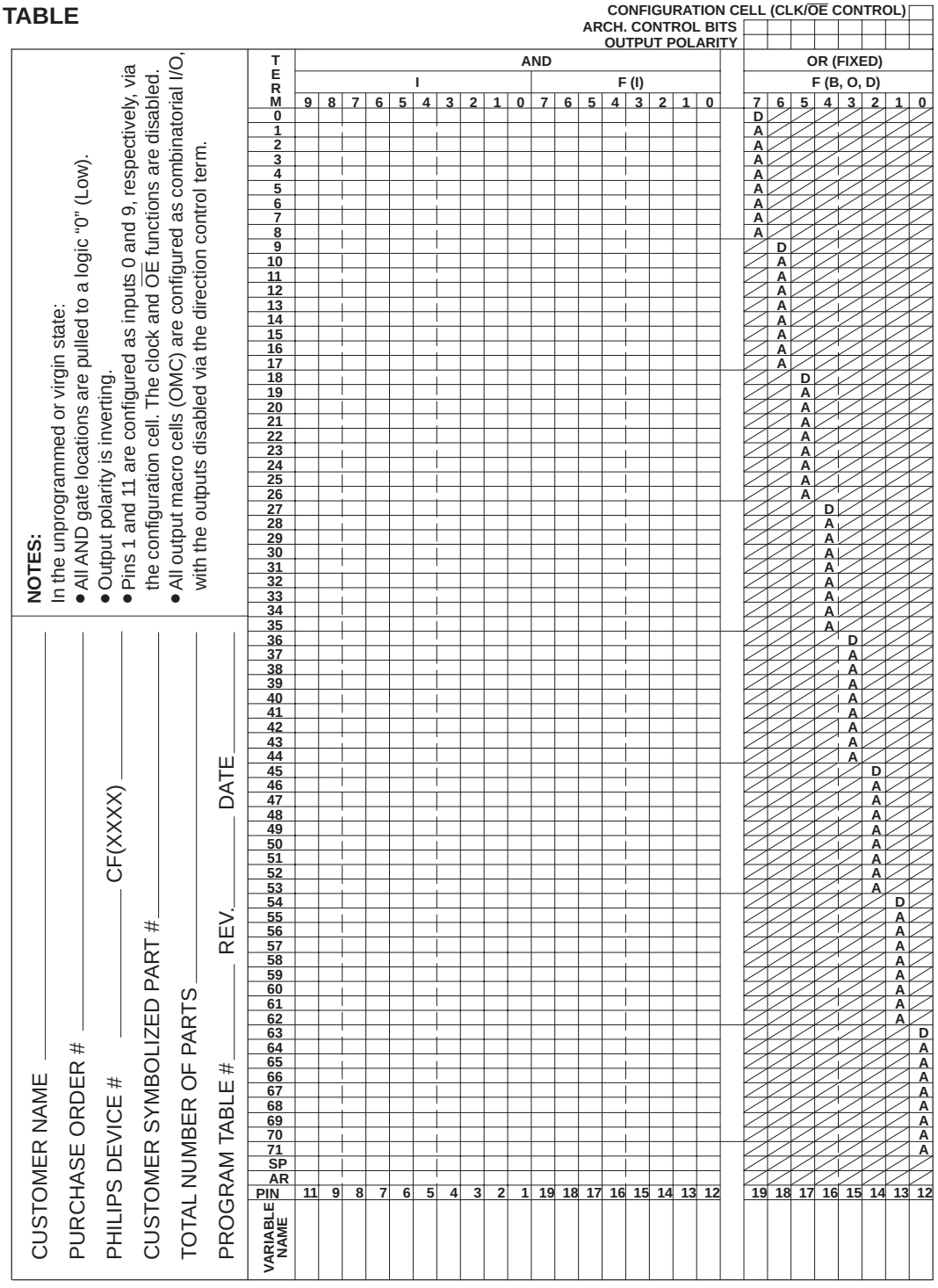
STATE	CODE
$\overline{I}$, $\overline{B}$	L

SP00024

NOTE:
1. A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

PROGRAM TABLE



AND ARRAY	
INACTIVE	O
I, F (I, B)	H
I, F (I, B)	L
**DON'T CARE	–

CONTROL	
OMC ARCH.	
REGISTERED (D-TYPE)	D
FIXED INPUT	I
FIXED OUTPUT	O
BIDIRECTIONAL I/O	B

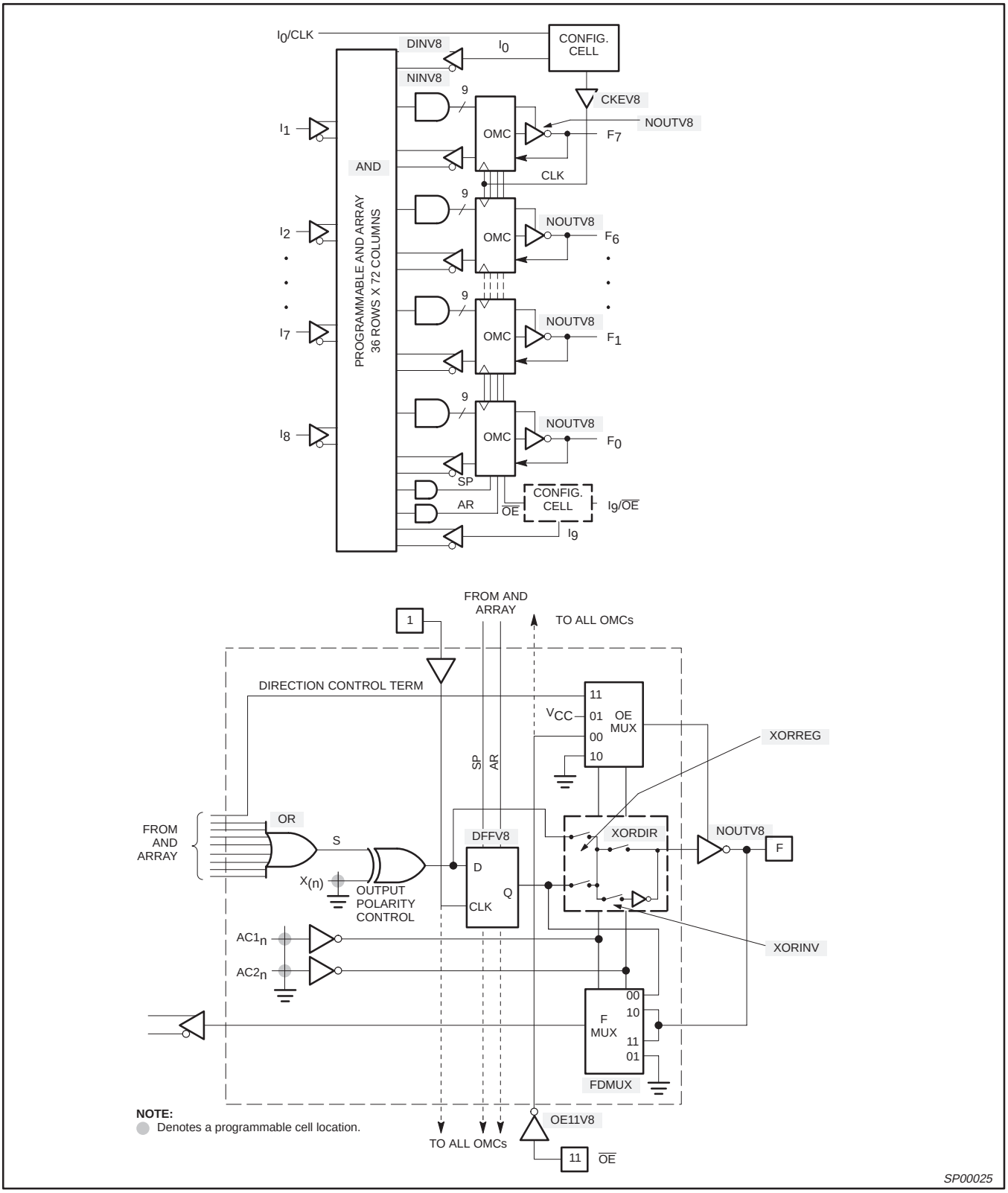
OUTPUT POLARITY	
NON-INVERTING	H
INVERTING	L
CONFIG. CELL*	
PIN 1 = CLK; PIN 11 = OE	L
PIN 1, PIN 11 = INPUT	H

OR ARRAY (FIXED)	
DATA CANNOT BE ENTERED INTO THE OR ARRAY FIELD DUE TO THE FIXED NATURE OF THE DEVICE ARCHITECTURE.	
DIRECTION CONTROL	D
ACTIVE OUTPUT	A
NOT USED	

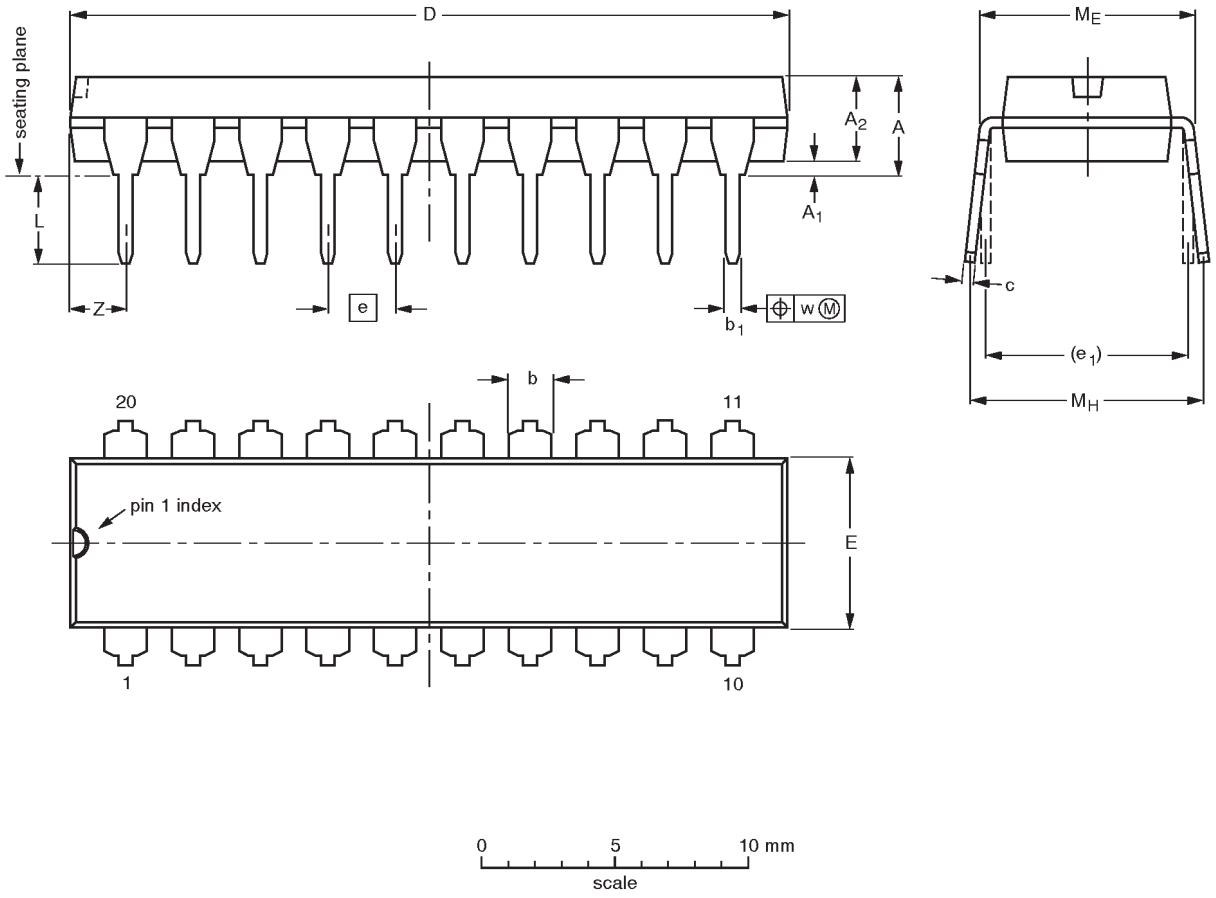
* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.
** FOR SP, AR: "–" IS NOT ALLOWED.

SP00029

SNAP RESOURCE SUMMARY DESIGNATIONS



DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

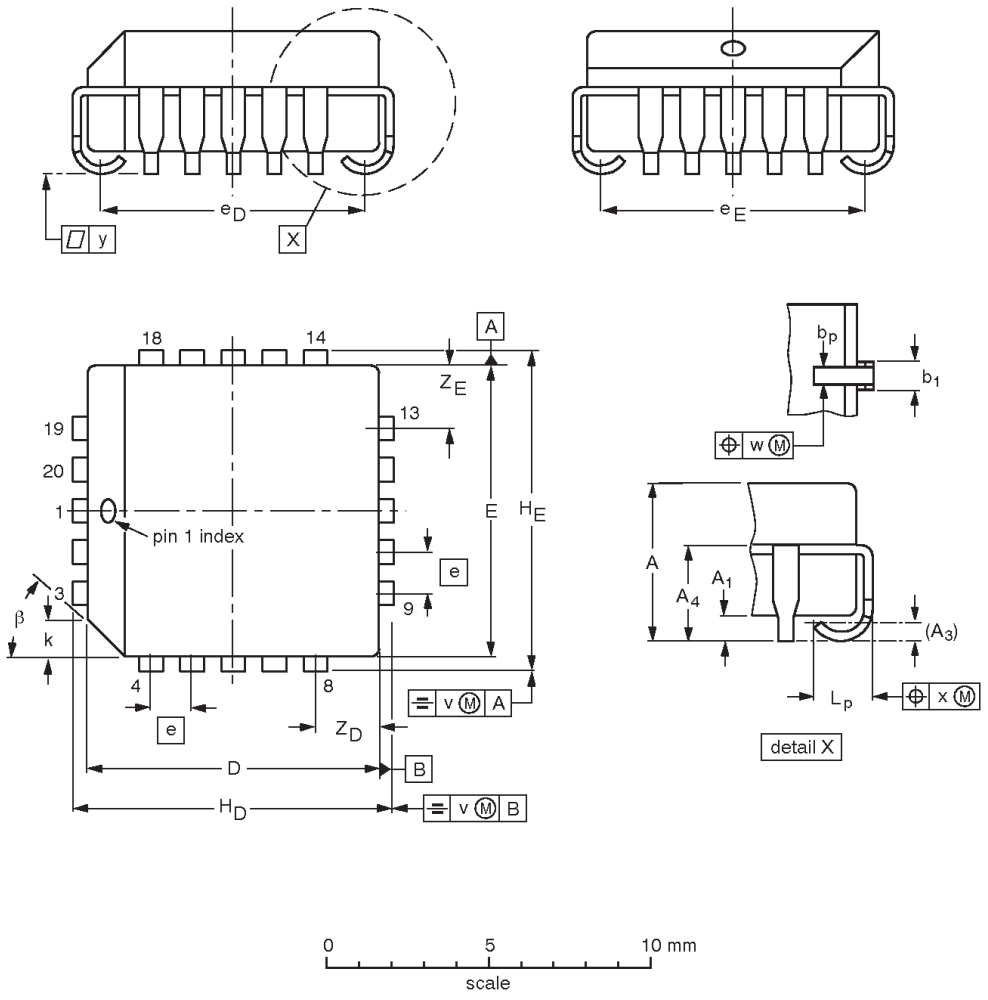
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

PLCC20: plastic leaded chip carrier; 20 leads SOT380-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

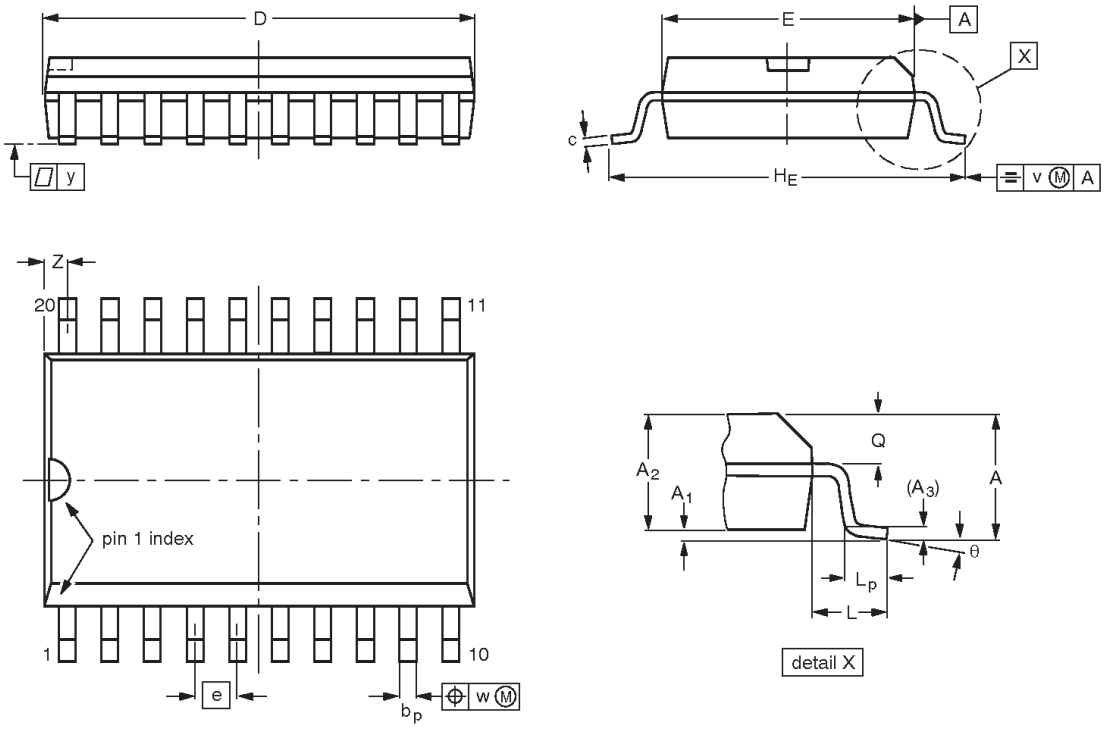
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.356 0.350	0.356 0.350	0.05	0.330 0.290	0.330 0.290	0.395 0.385	0.395 0.385	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

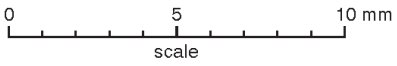
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT380-1		MO-047AA				~~92-11-17~~ 95-02-25

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

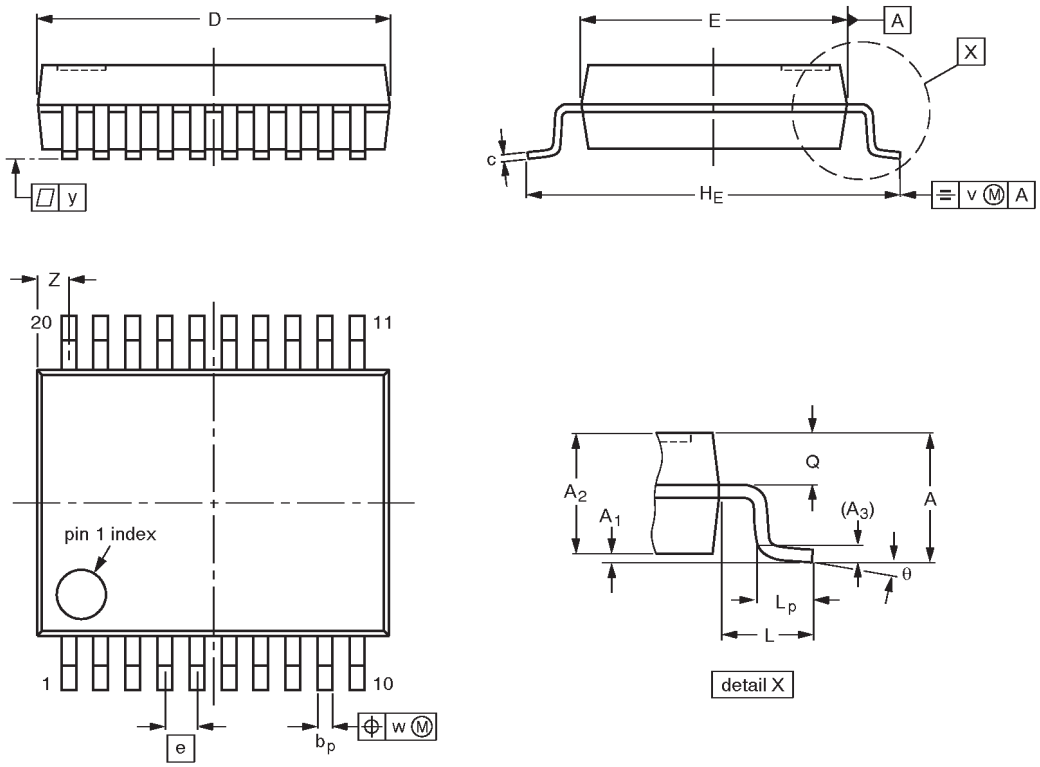
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

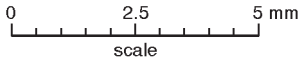
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**





DIMENSIONS (mm are the original dimensions)

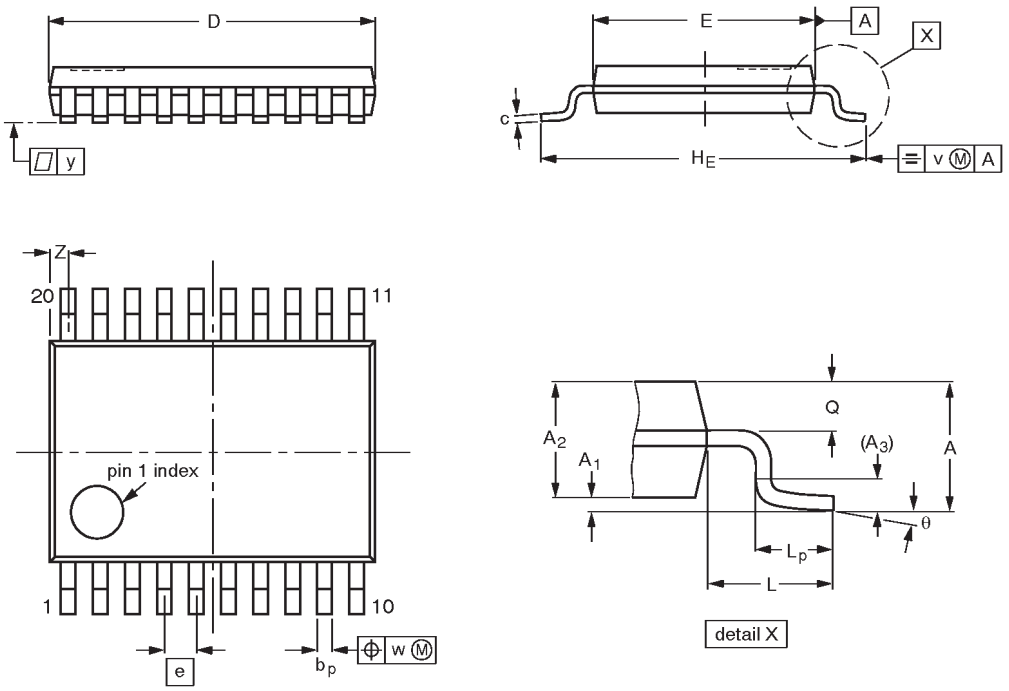
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

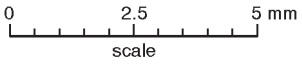
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm SOT360-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Zero standby power CMOS versatile PAL devices

PLC18V8Z

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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