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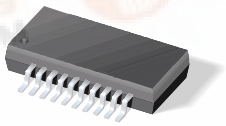


SLES046A – AUGUST 2002 – REVISED SEPTEMBER 2002

3.3-V DUAL PLL MULTICLOCK GENERATOR

FEATURES

- 27-MHz Master Clock Input
- Generated Audio System Clock:
  - SCKO0: 768 f_S (f_S = 44.1 kHz)
  - SCKO1: 384 f_S, 768 f_S (f_S = 44.1 kHz)
  - SCKO2: 256 f_S (f_S = 32, 44.1, 48, 64, 88.2, 96 kHz)
  - SCKO3: 384 f_S (f_S = 32, 44.1, 48, 64, 88.2, 96 kHz)
- Zero PPM Error Output Clocks
- Low Clock Jitter: 50 ps (Typical)
- Multiple Sampling Frequencies:
  - f_S = 32, 44.1, 48, 64, 88.2, 96 kHz
- 3.3-V Single Power Supply
- PLL1705: Parallel Control
  PLL1706: Serial Control
- Package: 20-Pin SSOP (150 mil), Lead-Free Product

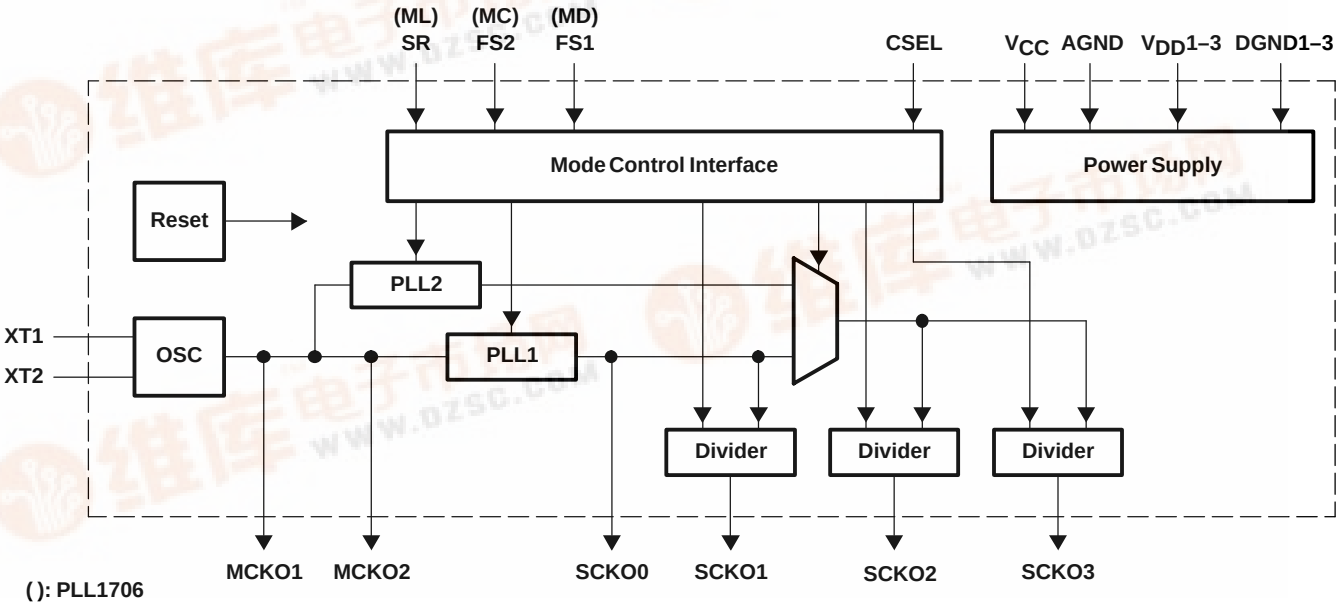
APPLICATIONS

- DVD Players
- DVD Add-On Cards for Multimedia PCs
- Digital HDTV Systems
- Set-Top Boxes

DESCRIPTION

The PLL1705† and PLL1706† are low cost, phase-locked loop (PLL) multiclock generators. The PLL1705 and PLL1706 can generate four system clocks from a 27-MHz reference input frequency. The clock outputs of the PLL1705 can be controlled by sampling frequency-control pins and those of the PLL1706 can be controlled through serial-mode control pins. The device gives customers both cost and space savings by eliminating external components and enables customers to achieve the very low-jitter performance needed for high performance audio DACs and/or ADCs. The PLL1705 and PLL1706 are ideal for MPEG-2 applications which use a 27-MHz master clock such as DVD players, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes.

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The PLL1705 and PLL1706 use the same die and they are electrically identical except for mode control.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PLL1705DBQ	SSOP 20	20DBQ	–25°C to 85°C	PLL1705	PLL1705DBQ	Tube
					PLL1705DBQR	Tape and reel
PLL1706DBQ	SSOP 20	20DBQ	–25°C to 85°C	PLL1706	PLL1706DBQ	Tube
					PLL1706DBQR	Tape and reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	PLL1705 AND PLL1706
Supply voltage: V_{CC}, $V_{DD}1–3$	4 V
Supply voltage differences: V_{CC}, $V_{DD}1–3$	±0.1 V
Ground voltage differences: AGND, DGND1–3	±0.1 V
Digital input voltage: FS1 (MD), FS2 (MC), SR (ML), CSEL	– 0.3 V to (V_{DD} + 0.3) V
Analog input voltage, XT1, XT2	– 0.3 V to (V_{CC} + 0.3) V
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias	–40°C to 125°C
Storage temperature	–55°C to 150°C
Junction temperature	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, $V_{DD}1$–$V_{DD}3$ (= V_{DD}) = V_{CC} = 3.3 V, f_M = 27 MHz, crystal oscillation, f_S = 48 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
	Logic input		CMOS compatible			
V_{IH} (1)	Input logic level		0.7V_{DD}		3.6	Vdc
V_{IL} (1)					0.3 V_{DD}	
I_{IH} (1)	Input logic current	V_{IN} = V_{DD}		65	100	µA
I_{IL} (1)		V_{IN} = 0 V			±10	
	Logic output		CMOS			
V_{OH} (2)	Output logic level	I_{OH} = –4 mA	V_{DD} – 0.4 V			Vdc
V_{OL} (2)		I_{OL} = 4 mA			0.4	Vdc
	Sampling frequency	Standard f_S	32	44.1	48	kHz
		Double f_S	64	88.2	96	
MASTER CLOCK (MCKO1, 2) CHARACTERISTICS (f_M = 27 MHz, C_1 = C_2 = 15 pF, C_L = 20 pF on measurement pin)						
	Master clock frequency		26.73	27	27.27	MHz
V_{IH}	Input level(3)		0.7 V_{CC}			V
V_{IL}					0.3 V_{CC}	
I_{IH}	Input current(3)	V_{IN} = V_{CC}			±10	µA
I_{IL}		V_{IN} = 0 V			±10	
	Output voltage (4)			3.5		Vp-p
	Output rise time	20% to 80% of V_{DD}		2.0		ns
	Output fall time	80% to 20% of V_{DD}		2.0		ns
	Duty cycle	For crystal oscillation	45%	48%	55%	
		For external clock		50%		
	Clock jitter (5)			50		ps
	Power-up time (6)			0.5	1.5	ms
PLL AC CHARACTERISTICS (SCKO0–3) (f_M = 27 MHz, C_L = 20 pF on measurement pin)						
SCKO0	Output system clock frequency	Fixed		33.8688		MHz
SCKO1		Selectable for 44.1 kHz	16.9344		33.8688	
SCKO2		256 f_S	8.192	12.288	24.576	
SCKO3		384 f_S	12.288	18.432	36.864	
	Output rise time	20% to 80% of V_{DD}		2.0		ns
	Output fall time	80% to 20% of V_{DD}		2.0		ns
	Output duty cycle		45	50	55	%
	Output clock jitter (5)			50	100	ps
	Frequency Settling Time(7)	PLL1705, to stated output frequency		50	150	ns
		PLL1706, to stated output frequency		80	200	ns
	Power-up time (8)	To stated output frequency		3	6	ms

(1) Pins 5, 6, 7, 12: FS1/MD, FS2/MC, SR/ML, CSEL (Schmitt-trigger input with internal pulldown, 3.3-V tolerant)
(2) Pins 2, 3, 14, 15, 18, 19: SCKO2, SCKO3, MCKO1, MCKO2, SCKO1, SCKO0
(3) Pin 10: XT1
(4) Pin 11: XT2
(5) Jitter performance is specified as standard deviation of jitter for 27-MHz crystal oscillation and default SCKO frequency setting. Jitter performance varies with master clock mode, SCKO frequency setting and load capacitance on each clock output.
(6) The delay time from power on to oscillation
(7) The settling time when the sampling frequency is changed
(8) The delay time from power on to lockup
(9) f_M = 27-MHz crystal oscillation, no load on MCKO1, MCKO2, SCKO0, SCKO1, SCKO2, SCKO3. Power supply current varies with sampling frequency selection and load condition.
(10) While all bits of CE[6:1] are 0, the PLL1706 goes into power-down mode.

ELECTRICAL CHARACTERISTICS(continued)

all specifications at T_A = 25°C, $V_{DD}1$–$V_{DD}3$ (= V_{DD}) = V_{CC} = 3.3 V, f_M = 27 MHz, crystal oscillation, f_S = 48 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY REQUIREMENTS						
V_{CC}, V_{DD}	Supply voltage range		2.7	3.3	3.6	Vdc
I_{DD} + I_{CC}	Supply current (9)	V_{DD} = V_{CC} = 3.3 V, f_S = 48 kHz		19	25	mA
		Power down(10)		320	500	µA
Power dissipation		V_{DD} = V_{CC} = 3.3 V, f_S = 48 kHz		63	90	mW
TEMPERATURE RANGE						
	Operating temperature		–25		85	°C
θ_{JA}	Thermal resistance	PLL1705/6DBQ: 20-pin SSOP (150 mil)		150		°C/W

(1) Pins 5, 6, 7, 12: FS1/MD, FS2/MC, SR/ML, CSEL (Schmitt-trigger input with internal pulldown, 3.3-V tolerant)
(2) Pins 2, 3, 14, 15, 18, 19: SCKO2, SCKO3, MCKO1, MCKO2, SCKO1, SCKO0
(3) Pin 10: XT1
(4) Pin 11: XT2
(5) Jitter performance is specified as standard deviation of jitter for 27-MHz crystal oscillation and default SCKO frequency setting. Jitter performance varies with master clock mode, SCKO frequency setting and load capacitance on each clock output.
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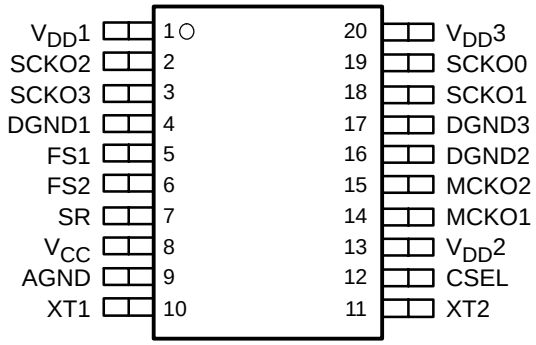
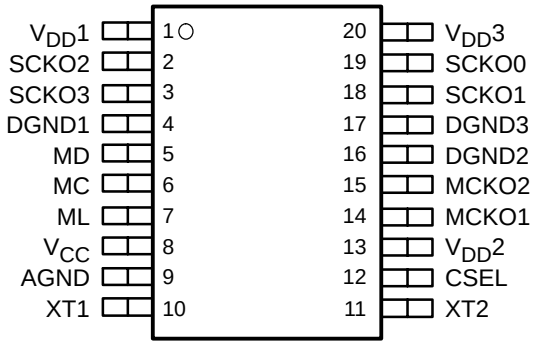
(10) While all bits of CE[6:1] are 0, the PLL1706 goes into power-down mode.

PIN ASSIGNMENTS

PLL1705
(TOP VIEW)



PLL1706
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	9	–	Analog ground
CSEL	12	IN	SCKO1 frequency selection control(1)
DGND1	4	–	Digital ground 1
DGND2	16	–	Digital ground 2
DGND3	17	–	Digital ground 3
FS1(MD)	5	IN	Sampling frequency group control in PLL1705, data input for serial control in PLL1706(1)
FS2(MC)	6	IN	Sampling frequency group control in PLL1705, bit clock input for serial control in PLL1706(1)
MCKO1	14	OUT	27-MHz master clock output 1
MCKO2	15	OUT	27-MHz master clock output 2
SCKO0	19	OUT	System clock output 0 (33.8688 MHz fixed)
SCKO1	18	OUT	System clock output 1 (selectable for 44.1 kHz)
SCKO2	2	OUT	System clock output 2 (256 f_S)
SCKO3	3	OUT	System clock output 3 (384 f_S)
SR(ML)	7	IN	Sampling rate control in PLL1705, load strobe input for serial control in PLL1706(1)
V_{CC}	8	–	Analog power supply, 3.3 V
$V_{DD}1$	1	–	Digital power supply 1, 3.3 V
$V_{DD}2$	13	–	Digital power supply 2, 3.3 V
$V_{DD}3$	20	–	Digital power supply 3, 3.3 V
XT1	10	IN	27-MHz crystal oscillator, or external clock input
XT2	11	OUT	27-MHz crystal oscillator, must be OPEN for external clock input mode

(1) Schmitt-trigger input with internal pulldown.

TYPICAL PERFORMANCE CURVES

JITTER
vs
SAMPLING FREQUENCY

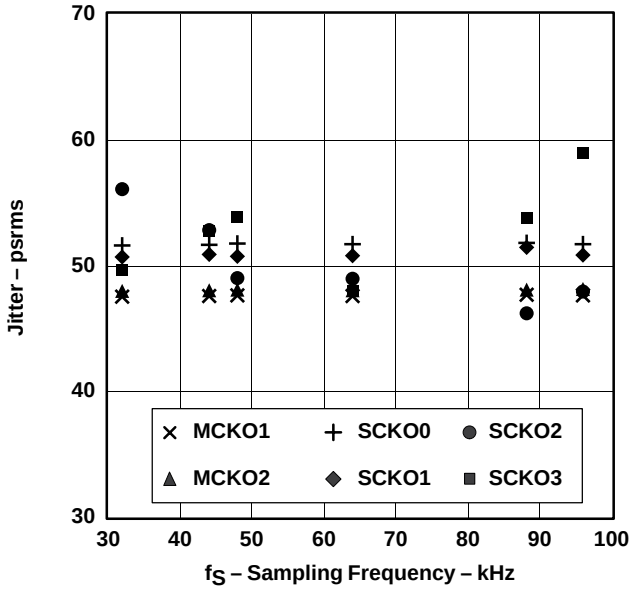


Figure 1

JITTER
vs
LOAD CAPACITANCE

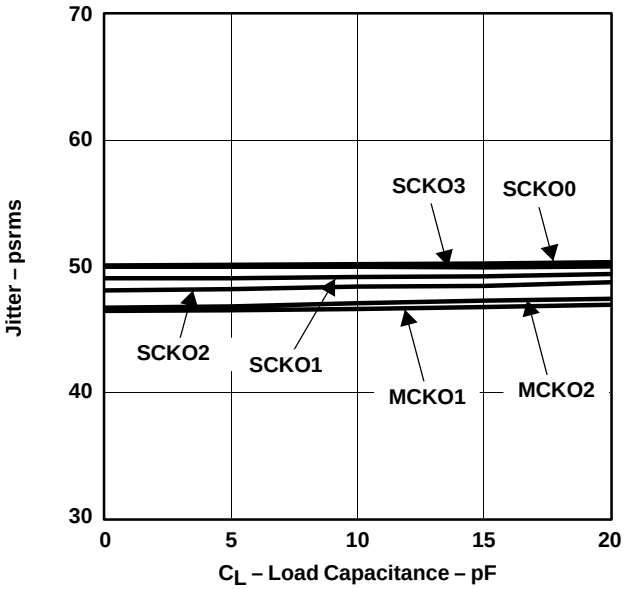


Figure 2

JITTER
vs
SUPPLY VOLTAGE

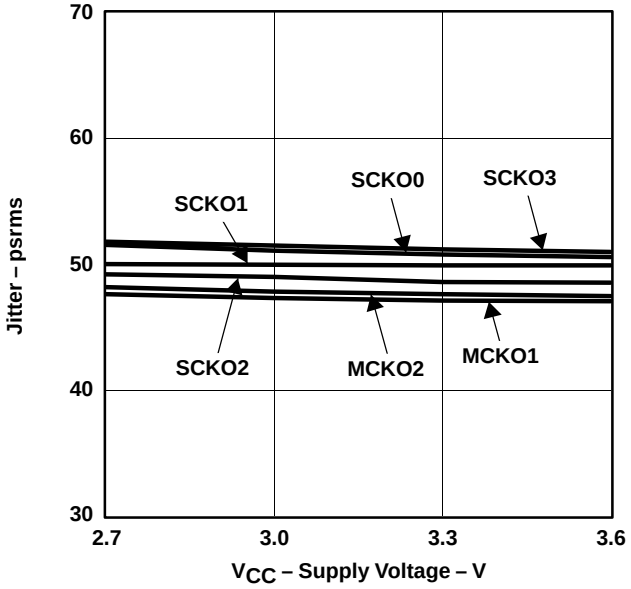


Figure 3

JITTER
vs
FREE-AIR TEMPERATURE

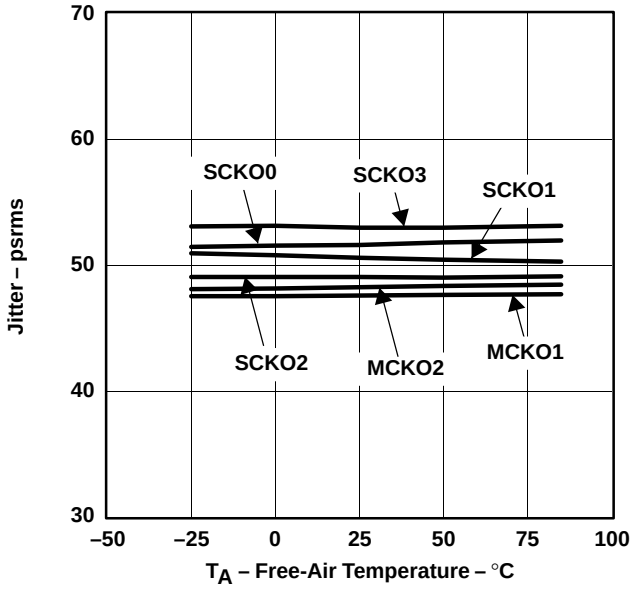


Figure 4

NOTE: All specifications at T_A = 25°C, $V_{DD}1$–3 (= V_{DD}) = V_{CC} = +3.3 V, f_M = 27 MHz, crystal oscillation, C_1, C_2 = 15 pF, default frequency (33.8688 MHz for SCKO0, 33.8688 MHz for SCKO1, 256 f_S and 384 f_S of 48 kHz for SCKO2 and SCKO3), C_L = 20 pF on measurement pin, unless otherwise noted.

DUTY CYCLE vs SUPPLY VOLTAGE

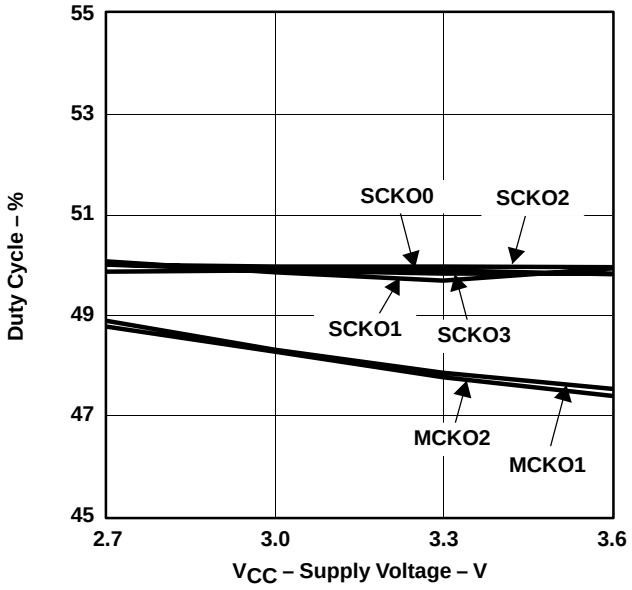


Figure 5

DUTY CYCLE vs FREE-AIR TEMPERATURE

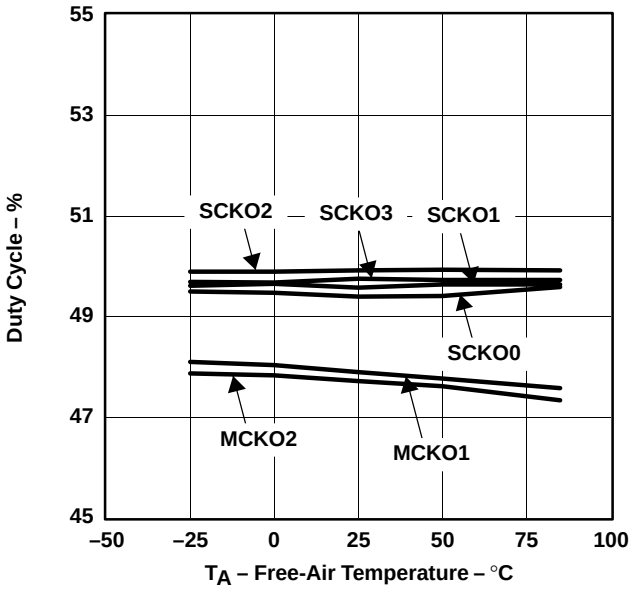


Figure 6

NOTE: All specifications at T_A = 25°C, $V_{DD}1$–3 (= V_{DD}) = V_{CC} = +3.3 V, f_M = 27 MHz, crystal oscillation, C_1, C_2 = 15 pF, default frequency (33.8688 MHz for SCKO0, 33.8688 MHz for SCKO1, 256 f_S and 384 f_S of 48 kHz for SCKO2 and SCKO3), C_L = 20 pF on measurement pin, unless otherwise noted.

THEORY OF OPERATION

MASTER CLOCK AND SYSTEM CLOCK OUTPUT

The PLL1705/6 consists of a dual PLL clock and master clock generator which generates four system clocks and two buffered 27-MHz clocks from a 27-MHz master clock. Figure 7 shows the block diagram of the PLL1705/6. The PLL is designed to accept a 27-MHz master clock.

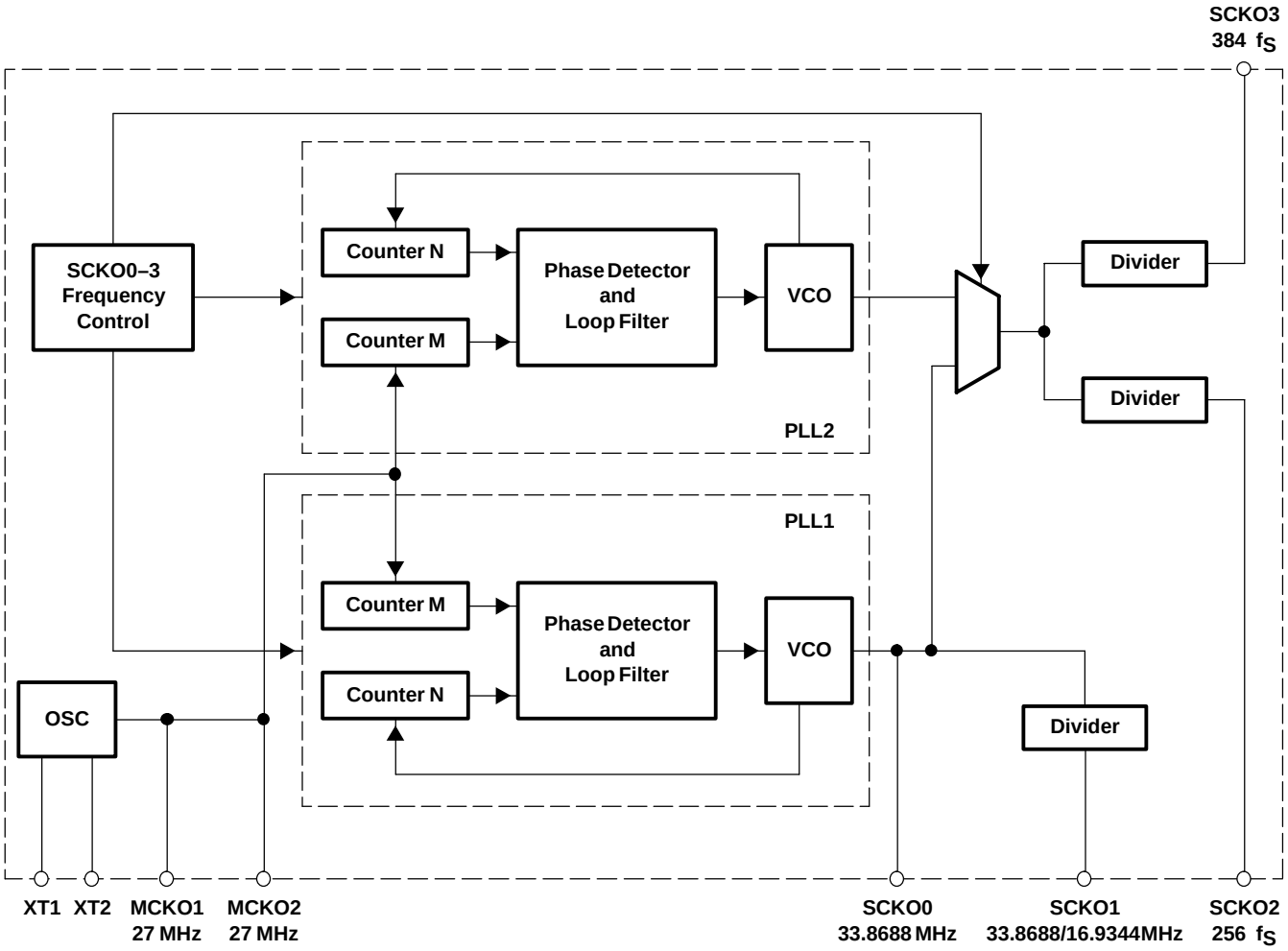


Figure 7. Block Diagram

The master clock can be either a crystal oscillator placed between XT1 (pin 10) and XT2 (pin 11), or an external input to XT1. If an external master clock is used, XT2 must be open. Figure 8 illustrates possible system clock connection options, and Figure 9 illustrates the 27-MHz master clock timing requirement.

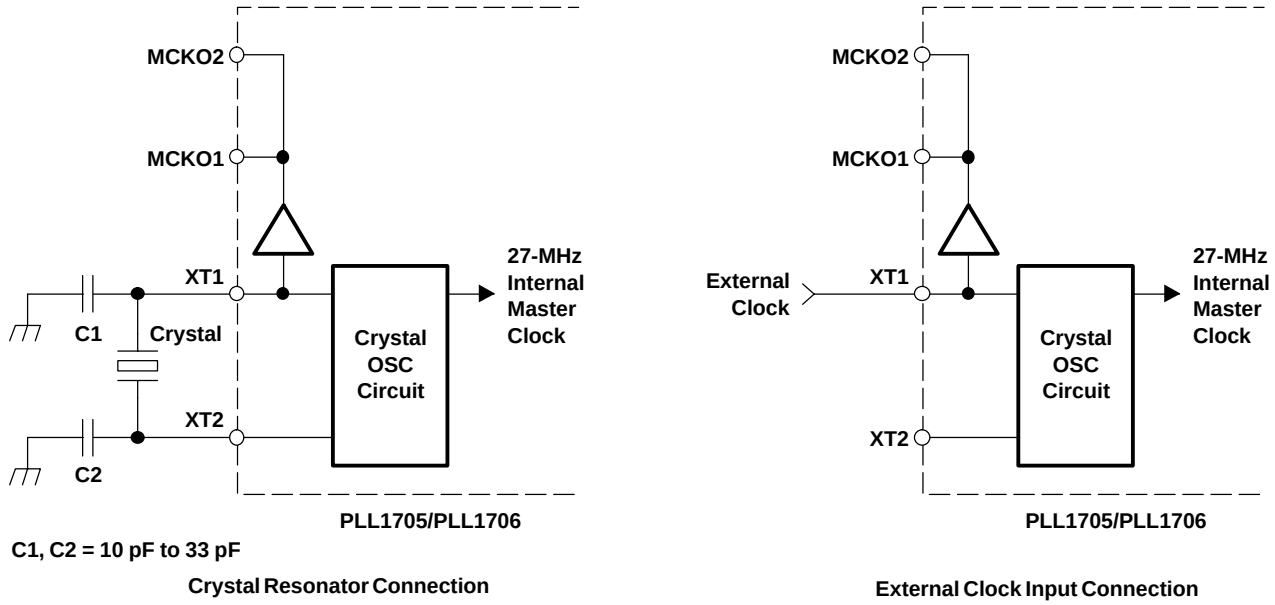
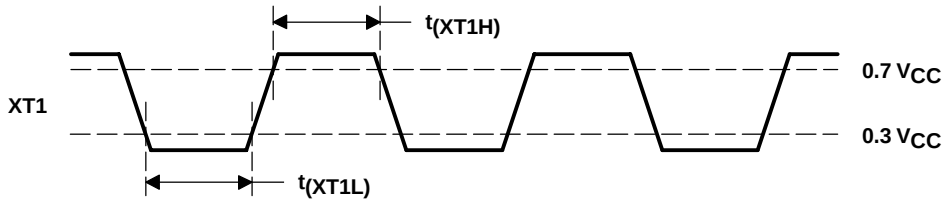


Figure 8. Master Clock Generator Connection Diagram



DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Master clock pulse duration HIGH	t_{XT1H}	10		ns
Master clock pulse duration LOW	t_{XT1L}	10		ns

Figure 9. External Master Clock Timing Requirement

The PLL1705/6 provides a very low-jitter, high-accuracy clock. SCKO0 outputs a fixed 33.8688-MHz clock, SCKO1 outputs 384 f_S or 768 f_S (f_S = 44.1 kHz) which is selected by CSEL (pin 12) for a CD-DA DSP. The output frequency of the remaining clocks is determined by the sampling frequency (f_S) under hardware or software control. SCKO2 and SCKO3 output 256-f_S and 384-f_S system clocks, respectively. Table 2 shows each sampling frequency, which can be programmed. The system clock output frequencies for programmed sampling frequencies are shown in Table 3.

Table 1. Generated System Clock SCKO1 Frequency

CSEL	SCKO1 FREQUENCY
LOW	33.8688 MHz
HIGH	16.9344 MHz

Table 2. Sampling Frequencies

SAMPLING RATE	SAMPLING FREQUENCY (kHz)		
Standard sampling frequencies	32	44.1	48
Double sampling frequencies	64	88.2	96

Table 3. Sampling Frequencies and System Clock Output Frequencies

SAMPLING FREQUENCY (kHz)	SAMPLING RATE	SCKO2 (MHZ)	SCKO3 (MHZ)
32	Standard	8.192	12.288
44.1	Standard	11.2896	16.9344
48	Standard	12.288	18.432
64	Double	16.384	24.576
88.2	Double	22.5792	33.8688
96	Double	24.576	36.864

Response time from power on (or applying the clock to XT1) to SCKO settling time is typically 3 ms. Delay time from sampling frequency change to SCKO settling is 200 ns maximum. This clock transient timing is not synchronized with the SCKOx signals. Figure 10 illustrates SCKO transient timing in the PLL1706. External buffers are recommended on all output clocks in order to avoid degrading the jitter performance of the PLL1705/6.

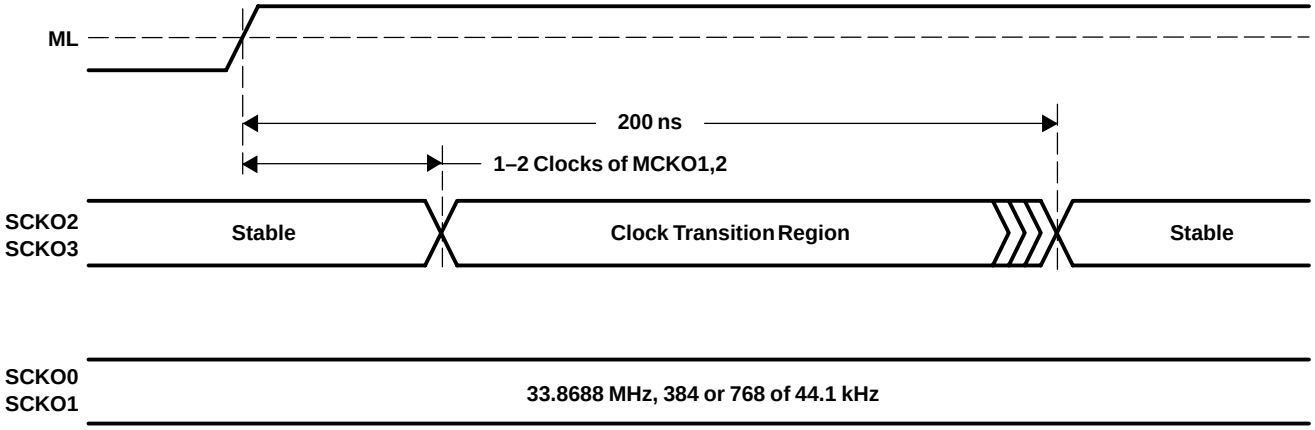


Figure 10. System Clock Transient Timing

POWER-ON RESET

The PLL1705/6 has an internal power-on reset circuit. The mode register of PLL1706 is initialized with default settings by power-on reset. Throughout the reset period, all clock outputs are enabled with the default settings after power up time. Initialization by internal power-on reset is done automatically during 1024 master clocks at V_{DD} > 2.0 V (TYP). Power-on reset timing is shown in Figure 11.

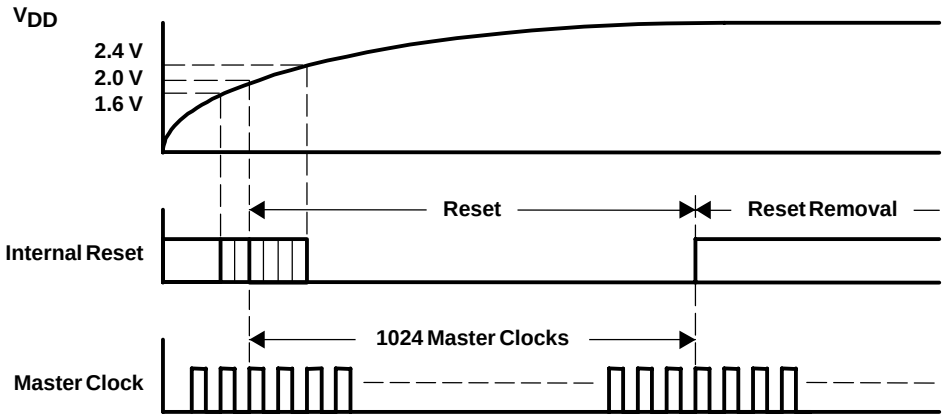


Figure 11. Power-On Reset Timing

FUNCTION CONTROL

The built-in functions of the PLL1705 can be controlled in the parallel mode (hardware mode), which uses SR (pin 7), FS1 (pin 5) and FS2 (pin 6). The PLL1706 can be controlled in the serial mode (software mode), which uses a three-wire interface by ML (pin 7), MC (pin 6), and MD (pin 5). The selectable functions are shown in Table 4.

Table 4. Selectable Functions

SELECTABLE FUNCTION	PARALLEL MODE	SERIAL MODE
Sampling frequency select (32 kHz, 44.1 kHz, 48 kHz)	Yes	Yes
Sampling rate select (standard/double)	Yes	Yes
Each clock output enable/disable	No	Yes
Power down	No	Yes

PLL1705 (Parallel Mode)

In the parallel mode, the following functions can be selected:

Sampling Frequency Group Select

The sampling frequency group can be selected by FS1 (pin 5) and FS2 (pin 6).

FS2 (PIN 6)	FS1 (PIN 5)	SAMPLING FREQUENCY
LOW	LOW	48 kHz
LOW	HIGH	44.1 kHz
HIGH	LOW	32 kHz
HIGH	HIGH	Reserved

Sampling Rate Select

The sampling rate can be selected by SR (pin 7)

SR (PIN 7)	SAMPLING RATE
LOW	Standard
HIGH	Double

PLL1706 (Serial Mode)

The built-in functions of the PLL1706 are shown in Table 5. These functions are controlled using the ML, MC, and MD serial control signals.

Table 5. Selectable Functions

SELECTABLE FUNCTION	DEFAULT
Sampling frequency select (32 kHz, 44.1 kHz, 48 kHz)	48-kHz group
Sampling rate select (standard/double)	Standard
Each clock output enable/disable	Enabled
Power down	Disabled

Program-Register Bit Mapping

The built-in functions of the PLL1706 are controlled through a 16-bit program register. This register is loaded using MD, MC and ML. After the 16 data bits are clocked in using the rising edge of MC, ML is used to latch the data into the register. Table 6 shows the bit mapping of the register. The serial mode control format and control data input timing are shown in Figure 12 and Figure 13, respectively.

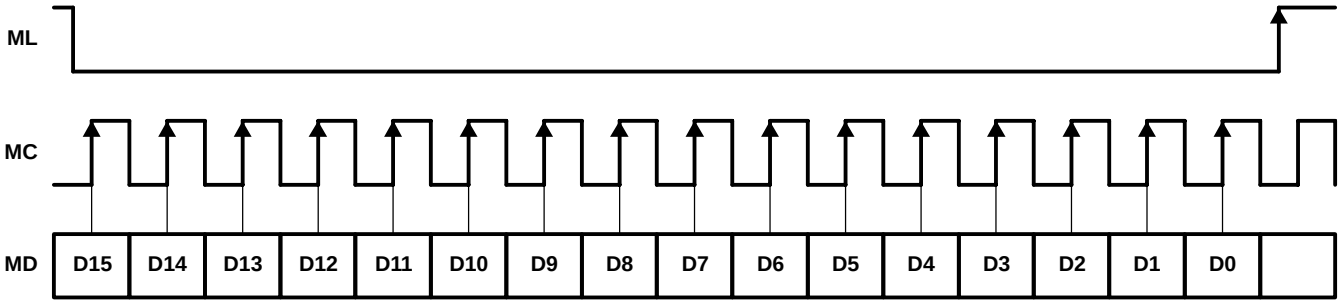
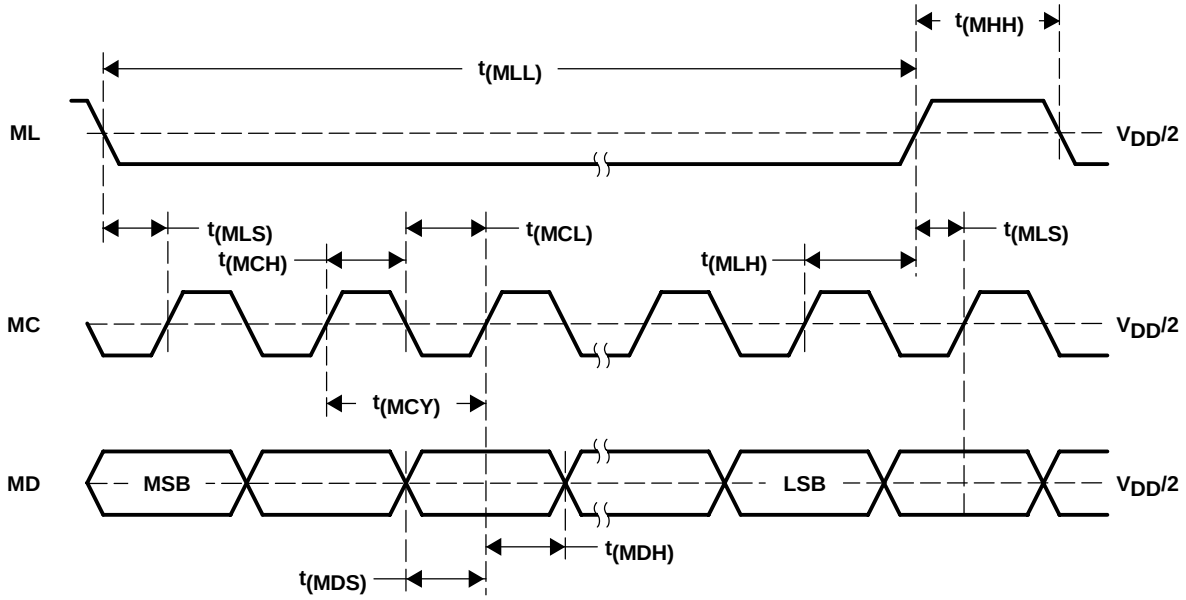


Figure 12. Serial Mode Control Format



DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNIT
MC pulse cycle time	t_{MCY}	100			ns
MC pulse duration LOW	t_{MCL}	40			ns
MC pulse duration HIGH	t_{MCH}	40			ns
MD hold time	t_{MDH}	40			ns
MD setup time	t_{MDS}	40			ns
ML low-level time	t_{MLL}	16			MC clocks(1)
ML high-level time	t_{MHH}	200			ns
ML hold time(2)	t_{MLH}	40			ns
ML setup time(3)	t_{MLS}	40			ns

(1) MC clocks: MC clock period
(2) MC rising edge for LSB to ML rising edge
(3) ML rising edge to the next MC rising edge. If the MC clock is stopped after the LSB, any ML rise time is accepted.

Figure 13. Control Data Input Timing

Mode Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	CE6	CE5	CE4	CE3	CE2	CE1	RSV	SR	FS2	FS1

Table 6. Register Mapping

REGISTER	BIT NAME	DESCRIPTION
Mode control	CE6	MCKO2 output enable/disable
	CE5	MCKO1 output enable/disable
	CE4	SCKO1 output enable/disable
	CE3	SCKO3 output enable/disable
	CE2	SCKO2 output enable/disable
	CE1	SCKO0 output enable/disable
	RSV	Reserved, must be 0
	SR	Sampling rate select
	FS[2:1]	Sampling frequency select

FS[2:1]: Sampling Frequency Group Select

FS2	FS1	SAMPLING FREQUENCY	DEFAULT
0	0	48 kHz	O
0	1	44.1 kHz	
1	0	32 kHz	
1	1	Reserved	

SR: Sampling Rate Select

SR	SAMPLING RATE	DEFAULT
0	Standard	O
1	Double	

CE [6:1]: Clock Output Control

CE1–CE6	CLOCK OUTPUT CONTROL	DEFAULT
0	Clock output disable	
1	Clock output enable	O

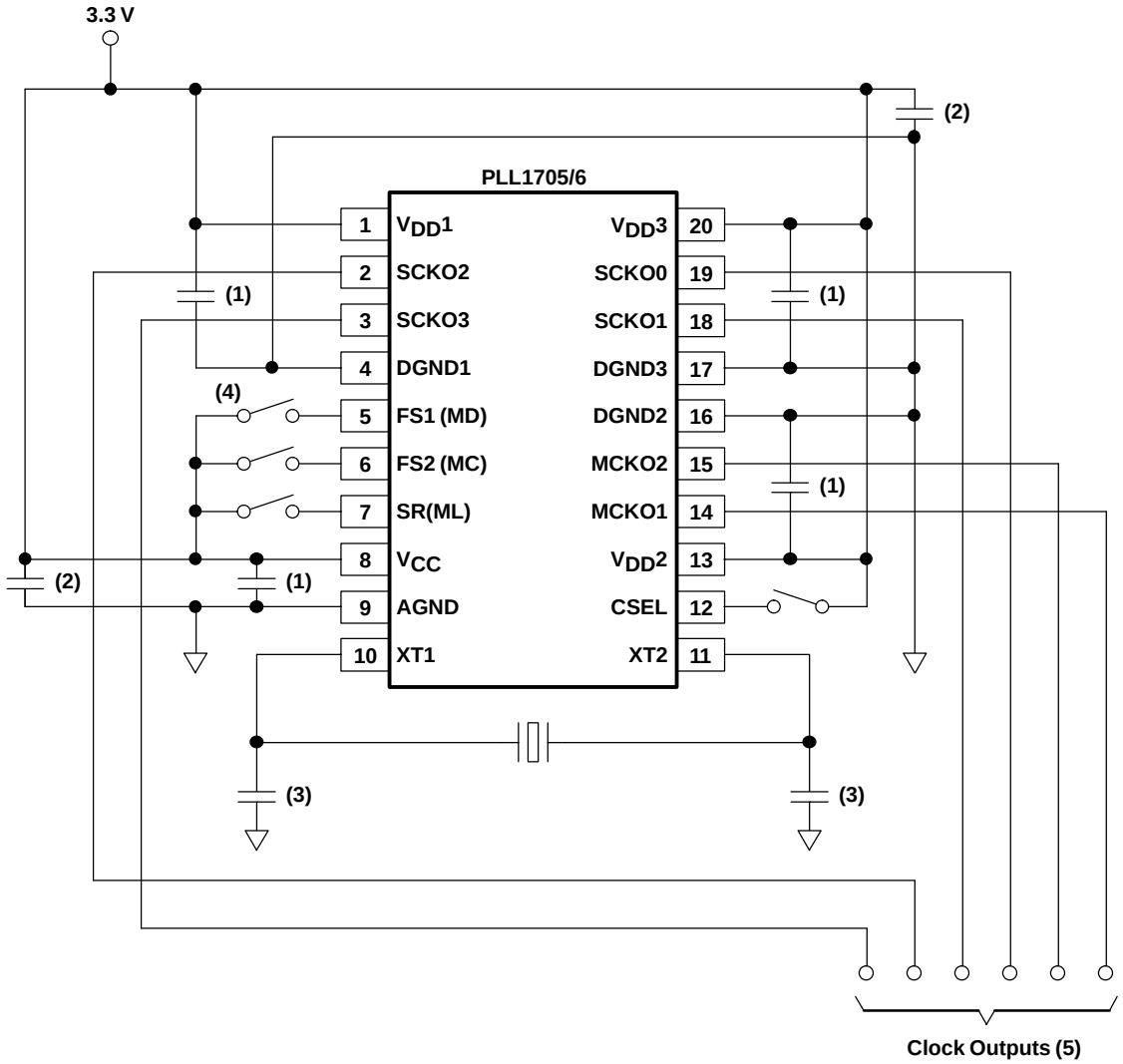
While all the bits of CE [6:1] are 0, the PLL1706 goes into the power-down mode, all dynamic operation including PLLs and the oscillator halt, but serial mode control is enabled for resumption.

CONNECTION DIAGRAM

Figure 14 shows the typical connection circuit for the PLL1705. There are four grounds for digital and analog power supplies. However, the use of one common ground connection is recommended to avoid latch-up or other power-supply-related troubles. Power supplies should be bypassed as close as possible to the device.

MPEG-2 APPLICATIONS

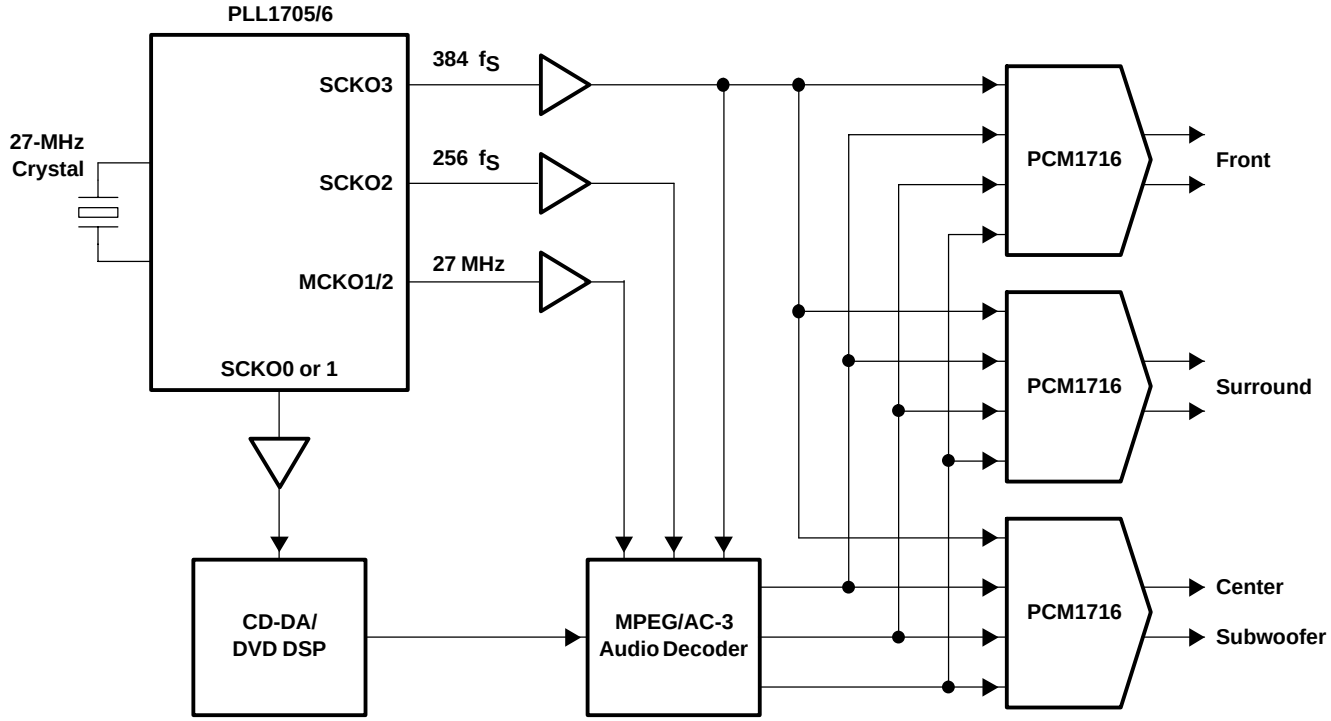
Typical applications for the PLL1705/6 are MPEG-2 based systems such as DVD players, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes. The PLL1705/6 provides audio system clocks for a CD-DA DSP, DVD DSP, Karaoke DSP, and DAC(s) from a 27-MHz video clock.



(1) 0.1-μF ceramic capacitor typical, depending on quality of power supply and pattern layout
(2) 10-μF aluminum electrolytic capacitor typical, depending on quality of power supply and pattern layout
(3) 27-MHz quartz crystal and 10–33 pF × 2 ceramic capacitors, which generate the appropriate amplitude of oscillation on XT1/XT2
(4) This connection is for PLL1705 (parallel mode); when PLL1706 (serial mode) is to be used, control pins must be connected to serial interfaced controller.
(5) For good jitter performance, minimize the load capacitance on the clock output.

Figure 14. Typical Connection Diagram

BLOCK DIAGRAM OF MPEG-2 BASED SYSTEM APPLICATION



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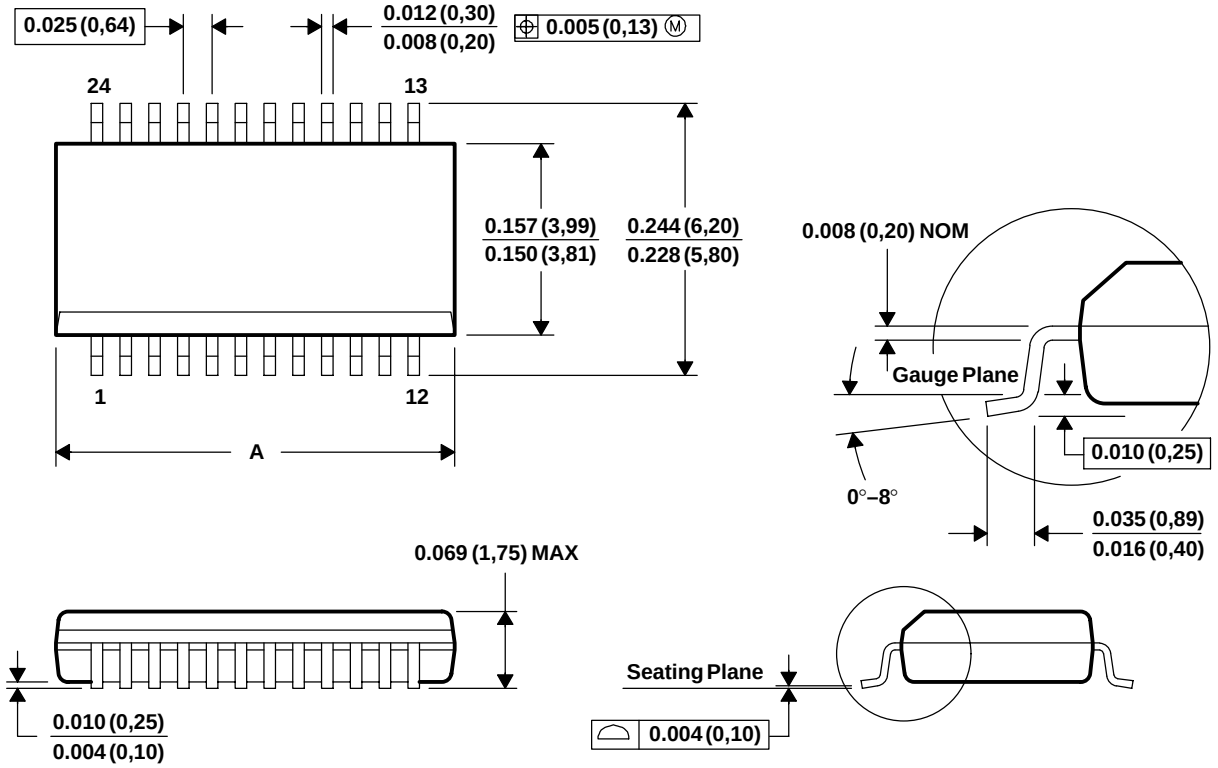
MECHANICAL DATA

DBQ (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**



DIM \ PINS **	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
M0–137 VARIATION (D)	AB	AD	AE	AF

4073301/F 02/02

NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–137.

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