



PM070WX2

Version : 0.1

TECHNICAL SPECIFICATION

MODEL NO. : PM070WX2

☐ Customer's Confirmation

Customer

By

☐ PVI's Confirmation

Confirmed By

Prepared By

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TECHNICAL SPECIFICATION

CONTENTS

NO.	ITEM	PAGE
-	Cover	1
-	Contents	2
1	Application	3
2	Features	3
3	Mechanical Specifications	3
4	Mechanical Drawing of TFT-LCD module	4
5	Input / Output Terminals	6
6	Touch Panel Characteristics	12
7	Absolute Maximum Ratings	13
8	Electrical Characteristics	13
9	Pixel Arrangement	14
10	Display Color and Gray Scale Reference	15
11	Block Diagram	16
12	Interface Timing	17
13	Power On Sequence	22
14	Optical Characteristics	22
15	Handling Cautions	26
16	Reliability Test	27
17	Packing Diagram	28
	Revision History	-

1.Application

This data sheet applies to a color TFT LCD module, PM070WX2.

The application of panel are OA product, portable DVD, car TV(must use Analog to Digital driving board), which requires high quality flat panel display.

Prime View advises your systems use PVI's timing controller IC (PVI-2002A) which will generate proper timing signals to control it.

2. Features

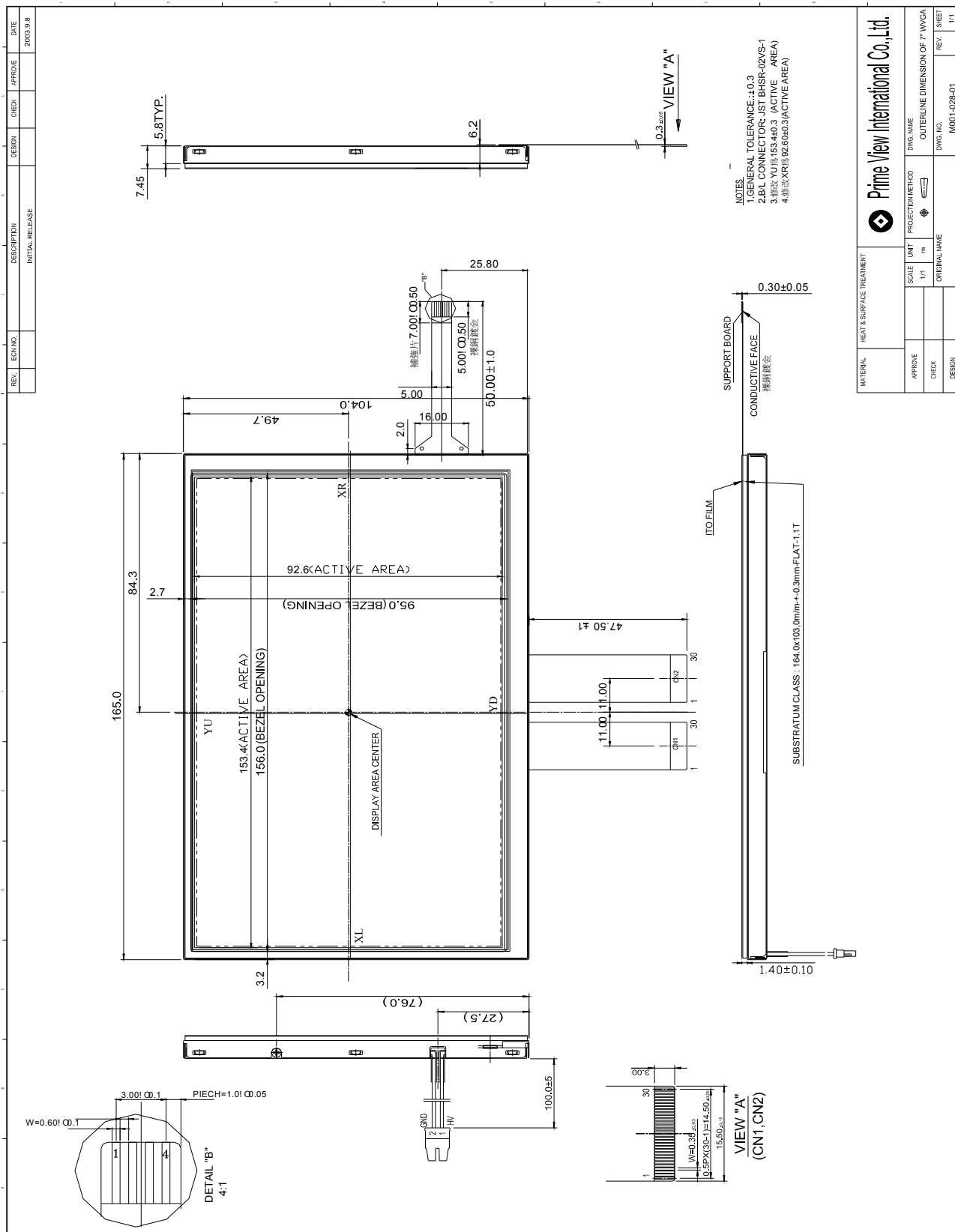
- . Wide VGA (800*480 pixels) resolution
- . Module with resistive type touch panel .
- . Amorphous silicon TFT LCD panel with back-light unit
- . Pixel in stripe configuration
- . Thin and light weight
- . Display Colors : 262,144 colors
- . Optimum Viewing Direction : 6 o'clock
- . TTL transmission interface
- . Wide viewing angle

3.Mechanical Specifications

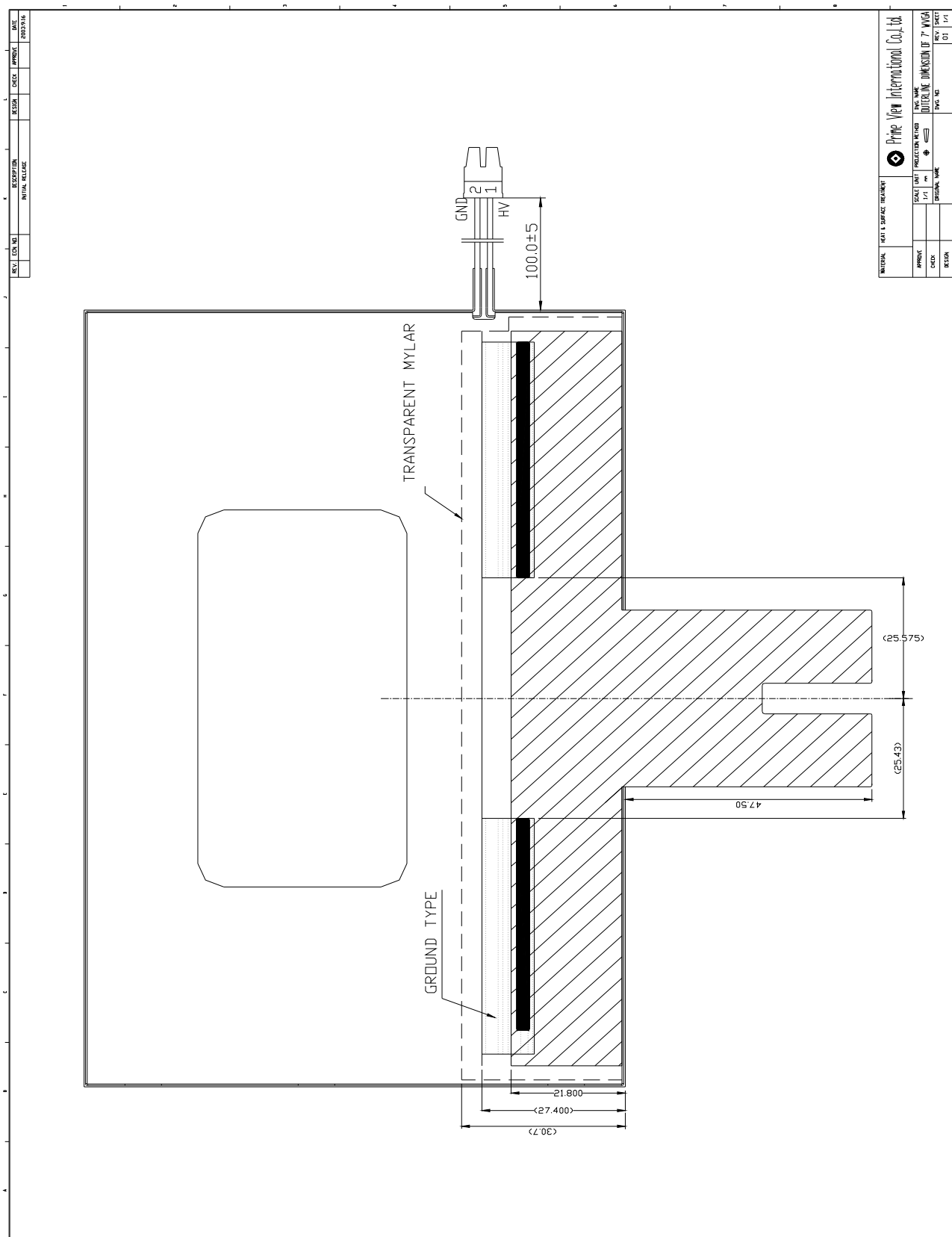
Parameter	Specifications	Unit
Screen Size	7.0(diagonal)	inch
Display Format	800×(R, G, B)×480	dot
Display Colors	262,144	
Active Area	152.4(H)×91.44(V)	mm
Pixel Pitch	0.190(H)×0.190(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	165.0(w)×104.0 (H)×7.45 (typ.) (D)	mm
Weight	175±10	g
Back-light	CCFL, 1 tube	
Surface treatment	Anti-glare and Wide View Film	
Display mode	Normally white	
Surface treatment of Touch Panel	3H	

4.Mechanical Drawing of TFT-LCD Module

Outline Drawing : Front View (unit mm)



Outline Drawing : Rear View (unit mm)



5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

CN 1

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-1
2	VSS1	I	Ground	
3	VDD1	I	Power Supply	
4	CLK	I	Horizontal Shift Clock	
5	VSS1	I	Ground	
6	R/L	I	Right / Left selection	Note 5-1
7	R0	I	Red Data (LSB)	
8	R1	I	Red Data	
9	R2	I	Red Data	
10	R3	I	Red Data	
11	R4	I	Red Data	
12	R5	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0	I	Green Data (LSB)	
15	G1	I	Green Data	
16	G2	I	Green Data	
17	G3	I	Green Data	
18	G4	I	Green Data	
19	G5	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0	I	Blue Data (LSB)	
22	B1	I	Blue Data	
23	B2	I	Blue Data	
24	B3	I	Blue Data	
25	B4	I	Blue Data	
26	B5	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note 5-2
28	REV	I	Data invert control	Note 5-3
29	POL	I	Polarity selection	Note 5-4
30	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-1

CN 2

Pin No.	Symbol	I/O	Function	Remark
1	VSS2	I	Ground	
2	V1	I	Gamma Voltage 1	Note 5-10
3	V2	I	Gamma Voltage 2	Note 5-10
4	V3	I	Gamma Voltage 3	Note 5-10
5	V4	I	Gamma Voltage 4	Note 5-10
6	V5	I	Gamma Voltage 5	Note 5-10
7	V6	I	Gamma Voltage 6	Note 5-10
8	V7	I	Gamma Voltage 7	Note 5-10
9	VSS2	I	Ground	
10	V8	I	Gamma Voltage 8	Note 5-10
11	V9	I	Gamma Voltage 9	Note 5-10
12	V10	I	Gamma Voltage 10	Note 5-10
13	V11	I	Gamma Voltage 11	Note 5-10
14	V12	I	Gamma Voltage 12	Note 5-10
15	V13	I	Gamma Voltage 13	Note 5-10
16	V14	I	Gamma Voltage 14	Note 5-10
17	VSS2	I	Ground	
18	VDD2	I	Voltage for analog circuit	Note 5-10
19	VCOM	I	Common Voltage	
20	XON	I	NC	
21	OE	I	Output Enable	Note 5-5
22	U/D	I	Up / Down Selection	Note 5-6
23	CKV	I	Vertical Shift Clock	Note 5-7
24	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-6
25	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-6
26	VGG	I	Gate On Voltage	Note 5-8
27	GND	I	Ground	
28	VCC	I	Voltage for logic circuit	
29	GND	I	Ground	
30	VEE	I	Gate Off Voltage	Note 5-9

Note 5-1: Select left or right shift

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to right
0	Hi-Z	Input	Right to left

Note 5-2: Latch the polarity of outputs and switch the new data to outputs
At the rising edge (LD), latch the "POL" signal to control the polarity of the outputs.

Note 5-3: Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)
When "REV=1", these data will be inverted.
EX: "00"→"3F", "07"→"38", "15"→"2A"

Note 5-4: Polarity selector for dot-inversion control. Available at the rising edge of LD.
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;
When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-5: When OE is connected to high “1”, the driver outputs are disabled (Gate output = V_{EE}). Under this condition, the operation of registers will not be affected.

Note 5-6: Select up or down shift

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

Note 5-7: Gate driver shift clock

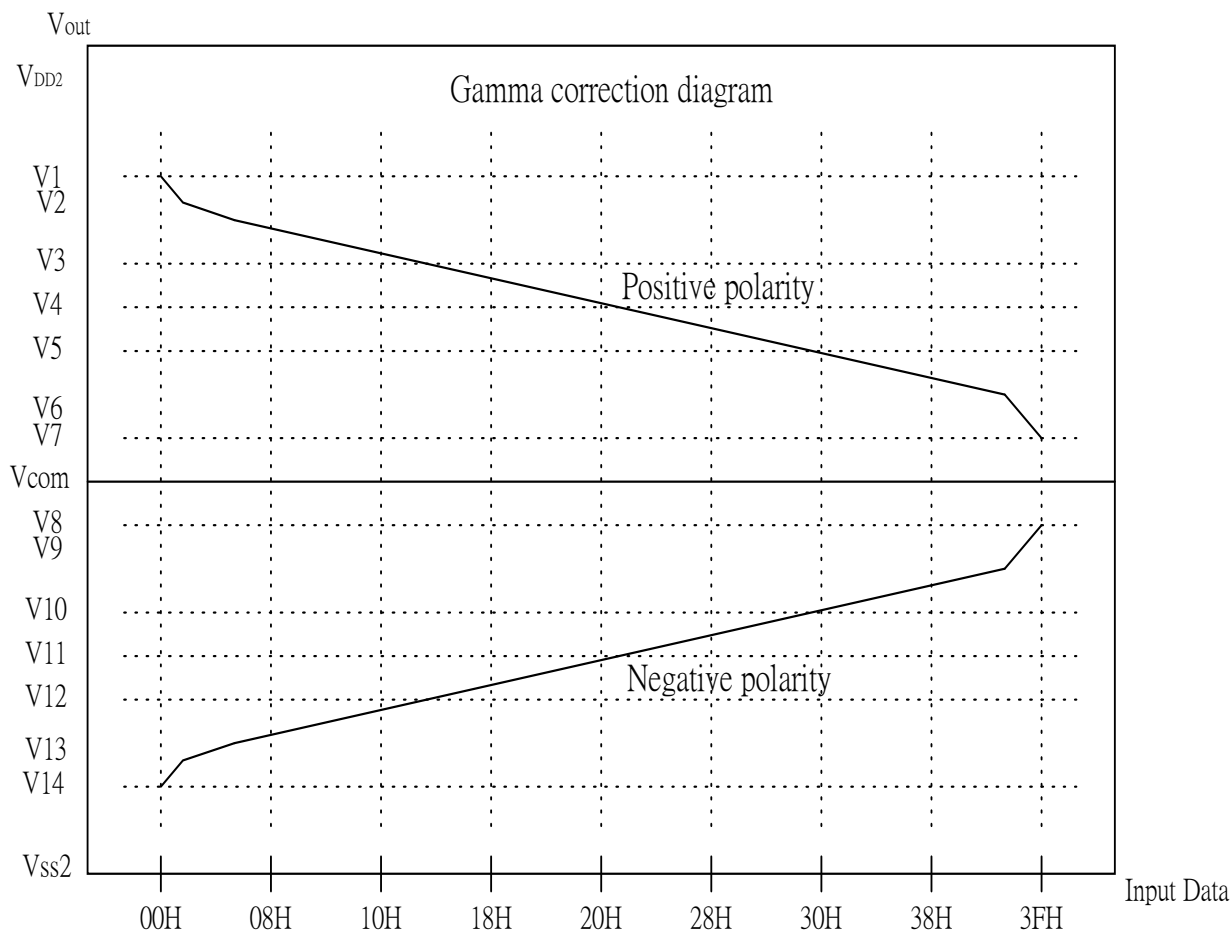
Note 5-8: Gate on voltage, $V_{GG}=27V$.

Note 5-9: Gate off voltage, $V_{EE}=-10V$.

Note 5-10:

1) Relationship between input data and output voltage

The figure below shows the relationship between the input data and the output voltage to panel with the polarity. The range of V1~V7 is for positive polarity, and V8~V14 for negative polarity. Please refer to the following pages to get the related resistor values and voltage calculation method.



Remark: $V_{DD2}-0.1 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V6 \geq V7$; $V8 \geq V9 \geq V10 \geq V11 \geq V12 \geq V13 \geq V14 \geq V_{SS2}+0.1V$.

2) Output voltage and input data

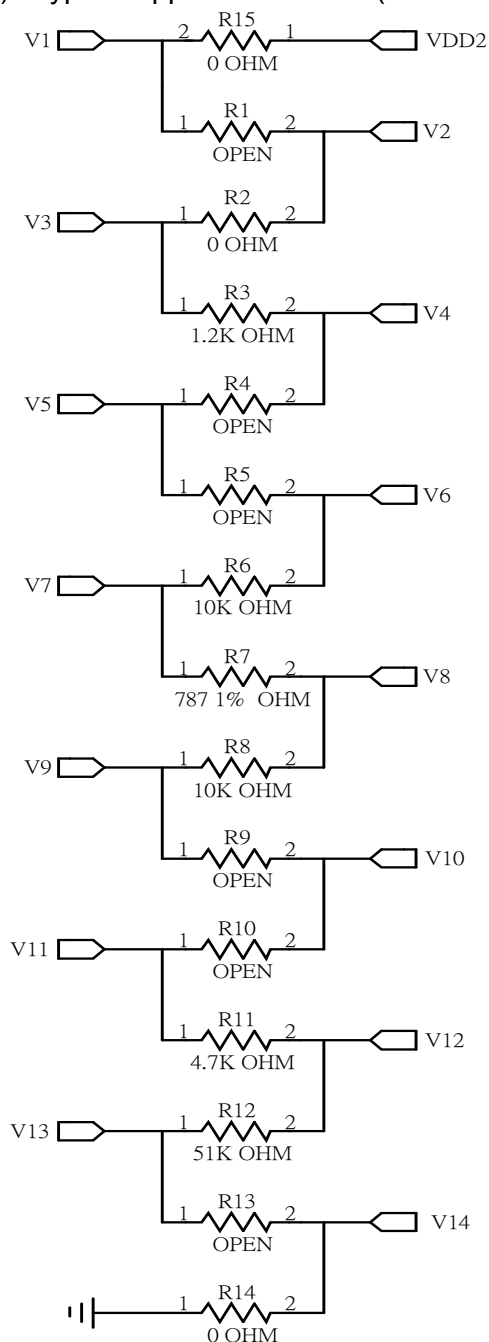
Output Voltage to Panel VS Input Data

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	$V2=V3+(V1-V3) \times 58 / 64.4$	$V13=V14+(V12-V14) \times 6.4 / 64.4$
02H	$V3+(V1-V3) \times 52 / 64.4$	$V14+(V12-V14) \times 12.4 / 64.4$
03H	$V3+(V1-V3) \times 46.4 / 64.4$	$V14+(V12-V14) \times 18 / 64.4$
04H	$V3+(V1-V3) \times 41.2 / 64.4$	$V14+(V12-V14) \times 23.2 / 64.4$
05H	$V3+(V1-V3) \times 36.4 / 64.4$	$V14+(V12-V14) \times 28 / 64.4$
06H	$V3+(V1-V3) \times 32 / 64.4$	$V14+(V12-V14) \times 32.4 / 64.4$
07H	$V3+(V1-V3) \times 27.6 / 64.4$	$V14+(V12-V14) \times 36.8 / 64.4$
08H	$V3+(V1-V3) \times 23.6 / 64.4$	$V14+(V12-V14) \times 40.8 / 64.4$
09H	$V3+(V1-V3) \times 19.6 / 64.4$	$V14+(V12-V14) \times 44.8 / 64.4$
0AH	$V3+(V1-V3) \times 16.4 / 64.4$	$V14+(V12-V14) \times 48 / 64.4$
0BH	$V3+(V1-V3) \times 13.2 / 64.4$	$V14+(V12-V14) \times 51.2 / 64.4$
0CH	$V3+(V1-V3) \times 10.4 / 64.4$	$V14+(V12-V14) \times 54 / 64.4$
0DH	$V3+(V1-V3) \times 7.6 / 64.4$	$V14+(V12-V14) \times 56.8 / 64.4$
0EH	$V3+(V1-V3) \times 4.8 / 64.4$	$V14+(V12-V14) \times 59.6 / 64.4$
0FH	$V3+(V1-V3) \times 2.4 / 64.4$	$V14+(V12-V14) \times 62 / 64.4$
10H	V3	V12
11H	$V4+(V3-V4) \times 19.6 / 22$	$V12+(V11-V12) \times 2.4 / 22$
12H	$V4+(V3-V4) \times 17.6 / 22$	$V12+(V11-V12) \times 4.4 / 22$
13H	$V4+(V3-V4) \times 15.6 / 22$	$V12+(V11-V12) \times 6.4 / 22$
14H	$V4+(V3-V4) \times 13.6 / 22$	$V12+(V11-V12) \times 8.4 / 22$
15H	$V4+(V3-V4) \times 12 / 22$	$V12+(V11-V12) \times 10 / 22$
16H	$V4+(V3-V4) \times 10.4 / 22$	$V12+(V11-V12) \times 11.6 / 22$
17H	$V4+(V3-V4) \times 8.8 / 22$	$V12+(V11-V12) \times 13.2 / 22$
18H	$V4+(V3-V4) \times 7.6 / 22$	$V12+(V11-V12) \times 14.4 / 22$
19H	$V4+(V3-V4) \times 6.4 / 22$	$V12+(V11-V12) \times 15.6 / 22$
1AH	$V4+(V3-V4) \times 5.2 / 22$	$V12+(V11-V12) \times 16.8 / 22$
1BH	$V4+(V3-V4) \times 4 / 22$	$V12+(V11-V12) \times 18 / 22$
1CH	$V4+(V3-V4) \times 3.2 / 22$	$V12+(V11-V12) \times 18.8 / 22$
1DH	$V4+(V3-V4) \times 2.4 / 22$	$V12+(V11-V12) \times 19.6 / 22$
1EH	$V4+(V3-V4) \times 1.6 / 22$	$V12+(V11-V12) \times 20.4 / 22$
1FH	$V4+(V3-V4) \times 0.8 / 22$	$V12+(V11-V12) \times 21.2 / 22$

Output Voltage to Panel VS Input Data(continued)

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	$V5+(V4-V5) \times 12 / 12.8$	$V11+(V10-V11) \times 0.8 / 12.8$
22H	$V5+(V4-V5) \times 11.2 / 12.8$	$V11+(V10-V11) \times 1.6 / 12.8$
23H	$V5+(V4-V5) \times 10.4 / 12.8$	$V11+(V10-V11) \times 2.4 / 12.8$
24H	$V5+(V4-V5) \times 9.6 / 12.8$	$V11+(V10-V11) \times 3.2 / 12.8$
25H	$V5+(V4-V5) \times 8.8 / 12.8$	$V11+(V10-V11) \times 4 / 12.8$
26H	$V5+(V4-V5) \times 8 / 12.8$	$V11+(V10-V11) \times 4.8 / 12.8$
27H	$V5+(V4-V5) \times 7.2 / 12.8$	$V11+(V10-V11) \times 5.6 / 12.8$
28H	$V5+(V4-V5) \times 6.4 / 12.8$	$V11+(V10-V11) \times 6.4 / 12.8$
29H	$V5+(V4-V5) \times 5.6 / 12.8$	$V11+(V10-V11) \times 7.2 / 12.8$
2AH	$V5+(V4-V5) \times 4.8 / 12.8$	$V11+(V10-V11) \times 8 / 12.8$
2BH	$V5+(V4-V5) \times 4 / 12.8$	$V11+(V10-V11) \times 8.8 / 12.8$
2CH	$V5+(V4-V5) \times 3.2 / 12.8$	$V11+(V10-V11) \times 9.6 / 12.8$
2DH	$V5+(V4-V5) \times 2.4 / 12.8$	$V11+(V10-V11) \times 10.4 / 12.8$
2EH	$V5+(V4-V5) \times 1.6 / 12.8$	$V11+(V10-V11) \times 11.2 / 12.8$
2FH	$V5+(V4-V5) \times 0.8 / 12.8$	$V11+(V10-V11) \times 12 / 12.8$
30H	V5	V10
31H	$V7+(V5-V7) \times 26.8 / 27.6$	$V10+(V8-V10) \times 0.8 / 27.6$
32H	$V7+(V5-V7) \times 26 / 27.6$	$V10+(V8-V10) \times 1.6 / 27.6$
33H	$V7+(V5-V7) \times 25.2 / 27.6$	$V10+(V8-V10) \times 2.4 / 27.6$
34H	$V7+(V5-V7) \times 24.4 / 27.6$	$V10+(V8-V10) \times 3.2 / 27.6$
35H	$V7+(V5-V7) \times 23.6 / 27.6$	$V10+(V8-V10) \times 4 / 27.6$
36H	$V7+(V5-V7) \times 22.4 / 27.6$	$V10+(V8-V10) \times 5.2 / 27.6$
37H	$V7+(V5-V7) \times 21.2 / 27.6$	$V10+(V8-V10) \times 6.4 / 27.6$
38H	$V7+(V5-V7) \times 20 / 27.6$	$V10+(V8-V10) \times 7.6 / 27.6$
39H	$V7+(V5-V7) \times 18.4 / 27.6$	$V10+(V8-V10) \times 9.2 / 27.6$
3AH	$V7+(V5-V7) \times 16.8 / 27.6$	$V10+(V8-V10) \times 10.8 / 27.6$
3BH	$V7+(V5-V7) \times 14.8 / 27.6$	$V10+(V8-V10) \times 12.8 / 27.6$
3CH	$V7+(V5-V7) \times 12.8 / 27.6$	$V10+(V8-V10) \times 14.8 / 27.6$
3DH	$V7+(V5-V7) \times 10.4 / 27.6$	$V10+(V8-V10) \times 17.2 / 27.6$
3EH	$V7+(V5-V7) \times 6.4 / 27.6$	$V10+(V8-V10) \times 21.2 / 27.6$
3FH	V7	V8

3) Typical Application Circuit (When $V_{DD2} = +9.5V$)



5-2) Backlight driving

Connector type: JST BHR-02VS-1, PIN No 2 pin, pitch=3.5mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	Wire color : Pink
2	VL2	Input terminal (Low voltage side)	Wire Color : White

Note : Low voltage side of backlight inverter connects with ground of inverter circuits.

6.Touch Panel Characteristics

6.1) Pin assignment:

Pin	Symbol	Function	Remark
1	YU	Upper electrode Y(Upper side)	
2	XR	Lower electrode X(Right side)	
3	YD	Upper electrode Y(Down side)	
4	XL	Lower electrode X(Left side)	

6.2) Electrical Performance:

Parameters	Symbol	MIN.	Typ.	MAX.	Unit	Remark
Terminal Resistance	X	580	840	1200		
	Y	120	180	260		
Input Voltage	V _T		5.0	7.0	V	
Linearity(X ,Y direction)				±1.5	%	
Insulation Impedance		20			M	DC 25V
Response Time				15	ms	
Operation Force				50	g	Note 6-1

Note 6-1 Input through 0.8R stylus or finger.

6.3) Durability Performance

1. Hitting Durability:

At least 1,000,000 times with R8.0mm silicon rubber, 250g , 3times/sec .

2. Sliding Durability:

At least 1,00,000 times with R0.8mm polyacetal stylus , 250g , 60mm/sec.

7. Absolute Maximum Ratings:
 $V_{SS1}=V_{SS2}=GND=0V, T_a=25^{\circ}C$

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{DD1}	-0.3	5.0	V	
	V_{CC}			V	
	V_{DD2}	-0.5	12.0	V	
	V_{GG}	-0.3	40.0	V	
	$V_{GG}-V_{EE}$	-	40	V	
	V_{EE}	-20	0.3	V	
Digital Input	V_{IN}	-0.5	$V_{CC}+0.5$	V	
Backlight Driving Voltage	V_L	-	2000	V	
Backlight Driving Frequency	F_L	0	100	KHz	
Storage Temperature	T_{ST}	-30	+80	$^{\circ}C$	
Operating Temperature	T_{OP}	-20	+80	$^{\circ}C$	

8. Electrical Characteristics
8-1) Recommended Operating Conditions:
 $V_{SS1}=V_{SS2}=GND=0V, T_a=25^{\circ}C$

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	V_{DD1}	3.0	3.3	3.6	V	
	V_{DD2}	9	9.5	10	V	
Supply Voltage for Gate Driver	V_{GG}	-	27	-	V	
	V_{EE}	-	-10	-	V	
	V_{CC}	3.0	3.3	3.6	V	
Digital Input Voltage	V_{IH}	$0.8V_{DD1}$	-	V_{DD1}	V	
	V_{IL}	0	-	$0.2V_{DD1}$	V	

8-2) Recommended Driving Condition for Back Light
 $T_a=25^{\circ}C$

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp Voltage	V_L		580	638	V	$I_L=6mA$
Lamp Current	I_L	4	6	7	mA	Note 8-1
Lamp Frequency	P_L	45	60	80	KHz	Note 8-2
Starting Voltage (25 $^{\circ}C$) (Reference Value)	V_s			820	Vrms	Note 8-3
Starting Voltage (0 $^{\circ}C$) (Reference Value)	V_s			970	Vrms	Note 8-3

Note 8-1: In order to satisfy the quality of B/L, no matter use what kind of inverter, the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-2: The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 8-3: 1. This value is not output voltage of inverter.

2. The voltage of inverter must larger than the starting voltage.

3. The Kick-off times $\geq 1sec$

8-3) Power Consumption

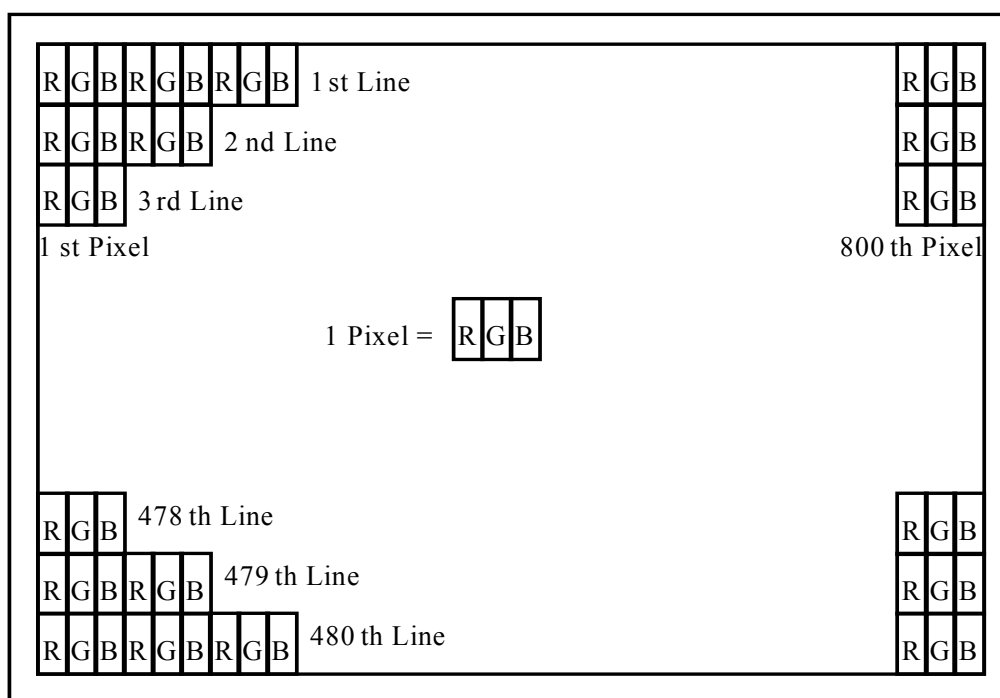
Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	I_{GG}	$V_{GG}=+27V$	0.32	0.41	mA	
Supply Current for Gate Driver (Low level)	I_{EE}	$V_{EE}=-10V$	3.35	4.19	mA	
Supply Current for Source Driver (Digital)	I_{DD1}	$V_{DD1}=+3.3V$	6	10	mA	
Supply Current for Source Driver (Analog)	I_{DD2}	$V_{DD2}=+9.5V$	20	27.5	mA	
Supply Current for Gate Driver (Digital)	I_{CC}	$V_{CC}=+3.3V$	0.01	0.013	mA	
LCD Panel Power Consumption			251.97	347.26	mW	Note 8-4
Back Light Lamp Power Consumption			3.48		W	Note 8-5

Note 8-4: The power consumption for back light is not included.

Note 8-5: Back light lamp power consumption is calculated by $I_L \times V_L$.

9. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

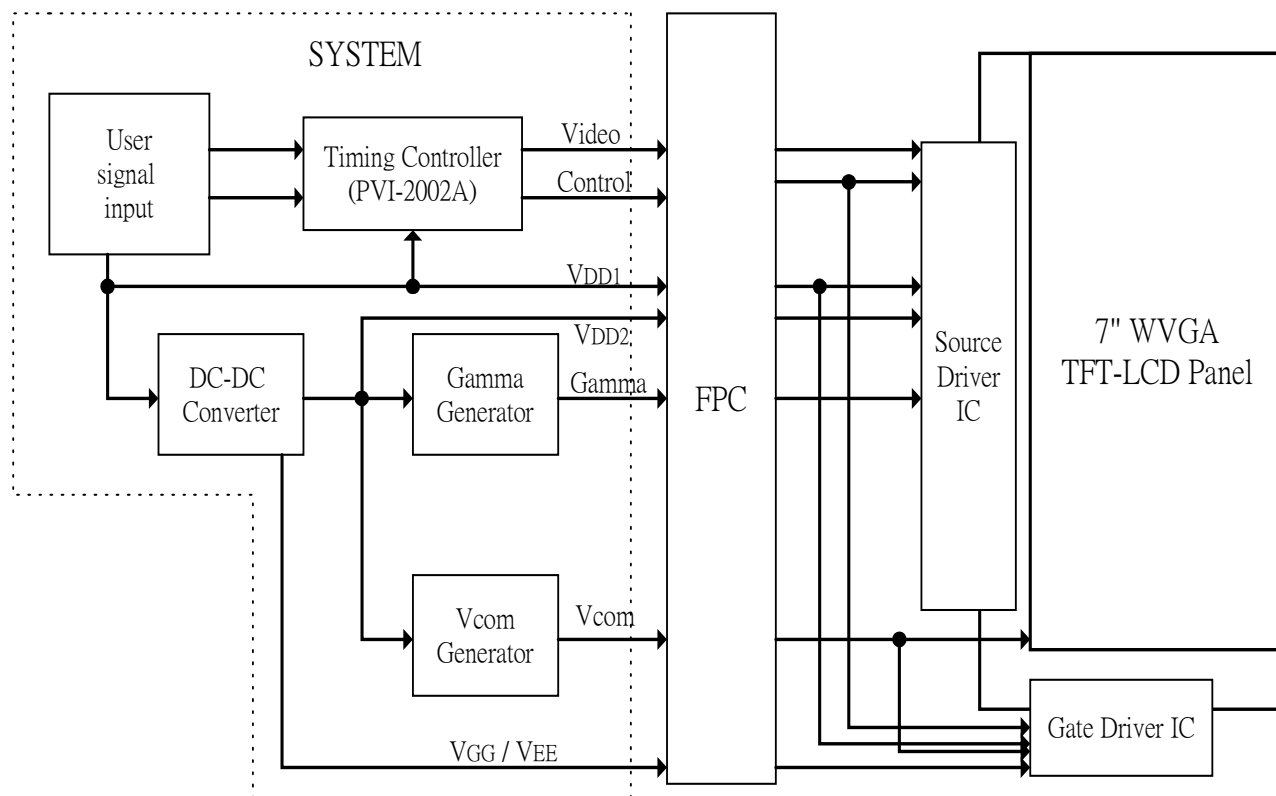


10. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

11. Block Diagram

11-1) TFT-module Block Diagram



12. Interface Timing

12.1) Timing Parameters

AC Electrical Characteristics ($V_{CC}=V_{DD1}=3.3V$, $V_{DD2}=9.5V$, $GND=V_{SS1}=V_{SS2}=0V$, $T_a=25^{\circ}C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	Fclk	-	32	40	MHz
CLK Pulse Width	Tcw	25	-	-	ns
Data Set-up Time	Tsu	4	-	-	ns
Data Hold Time	Thd	2	-	-	ns
Propagation Delay of DIO2/1	Tphl	6	10	15	ns
Time That The Last Data to LD	Tld	1	-	-	Tcw
Pulse width of LD	Twld	2	-	-	Tcw
Time That LD to DIO1/2	Tlds	5	-	-	Tcw
POL Set-up Time	Tpsu	6	-	-	ns
POL Hold Time	Tphd	6	-	-	ns
OE Pulse Width	T _{OE} V	1	-	-	s
CKV Pulse Width	T _{CKV}	500	-	-	ns
STV Set-up Time	T _{SUV}	400	-	-	ns
STV Hold Time	T _{HDV}	400	-	-	ns
Horizontal Display Period	T _{HDP}	-	800	-	Tcw
Horizontal Period Timing Range	T _{HP}	-	1056	-	Tcw
Horizontal Lines Per Field	T _V	484	508	620	T _{HP}
Vertical Display Timing Range	T _{DV}	-	480	-	T _{HP}

12.2) Timing Diagram

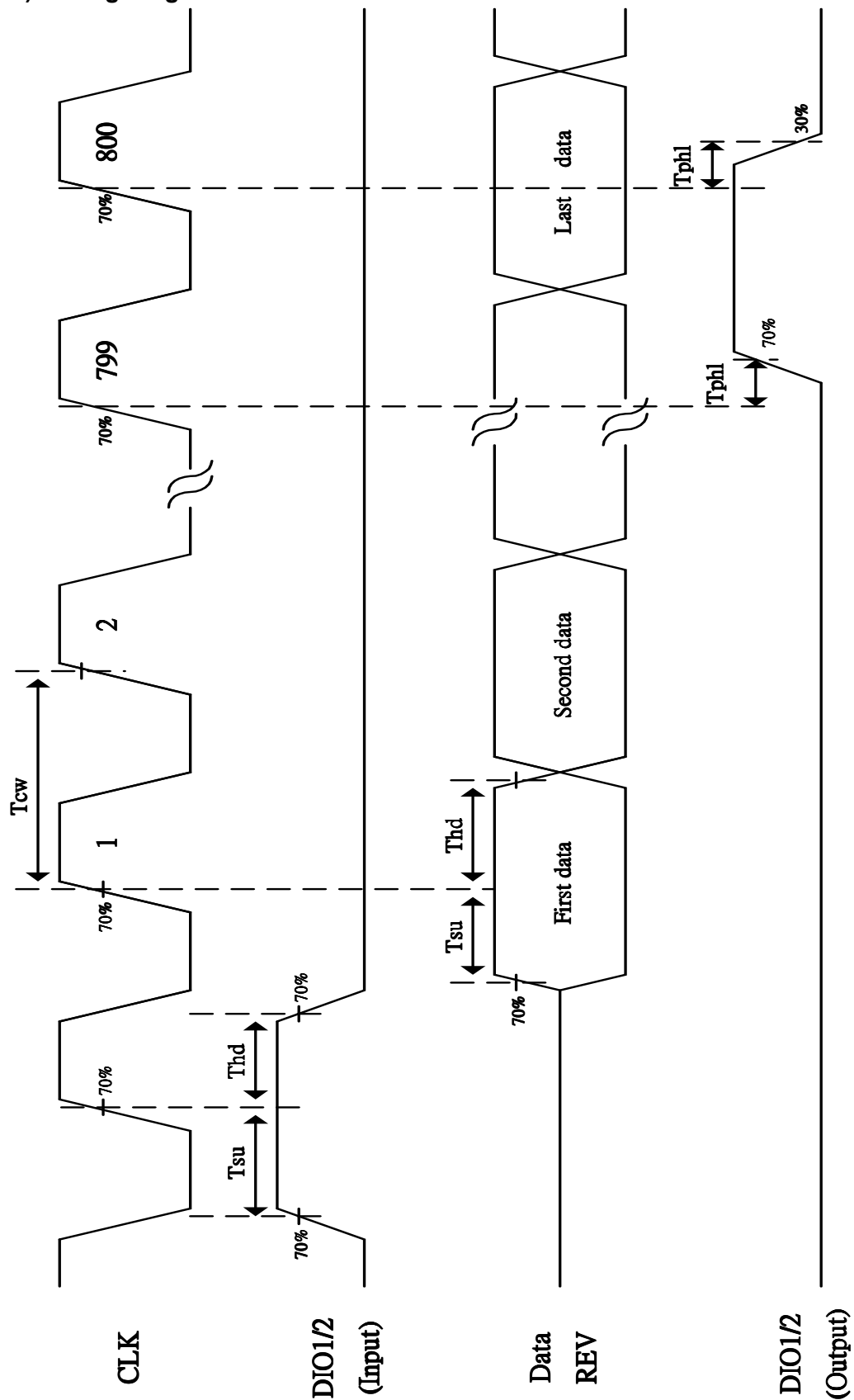


Fig. 11-1 Horizontal timing (1)

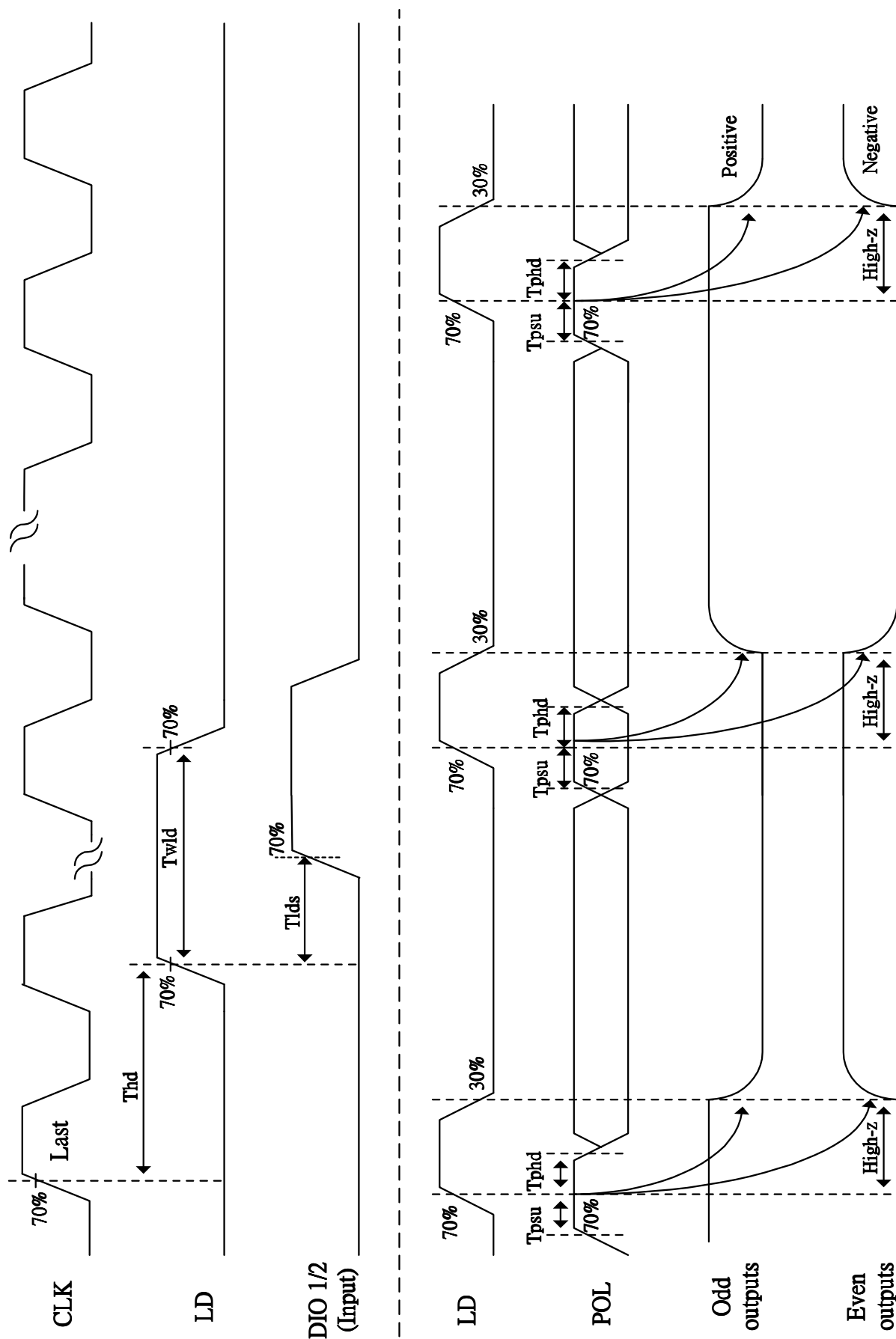


Fig. 11-2 Horizontal timing(2)

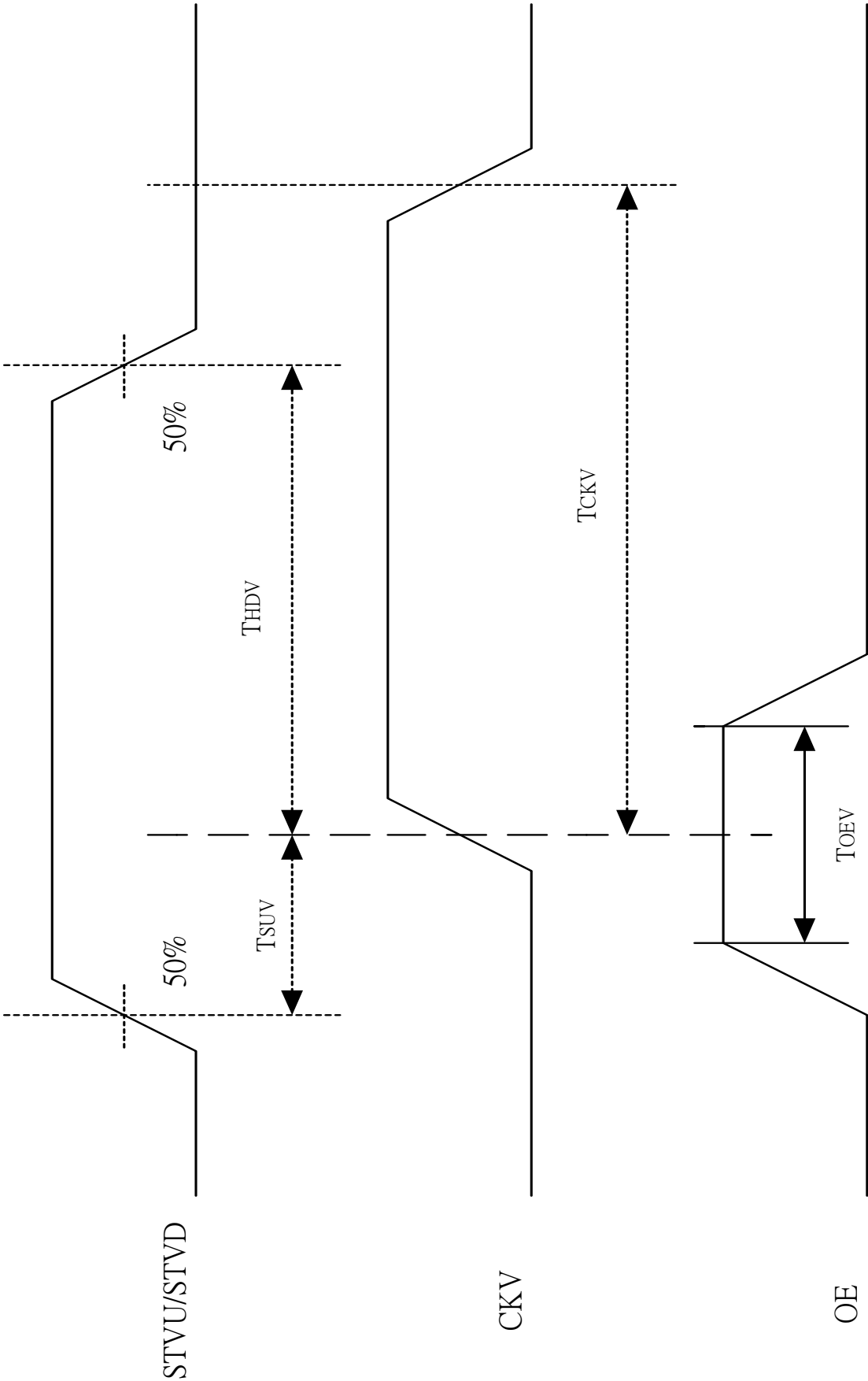


Fig. 11-3 Vertical shift clock timing

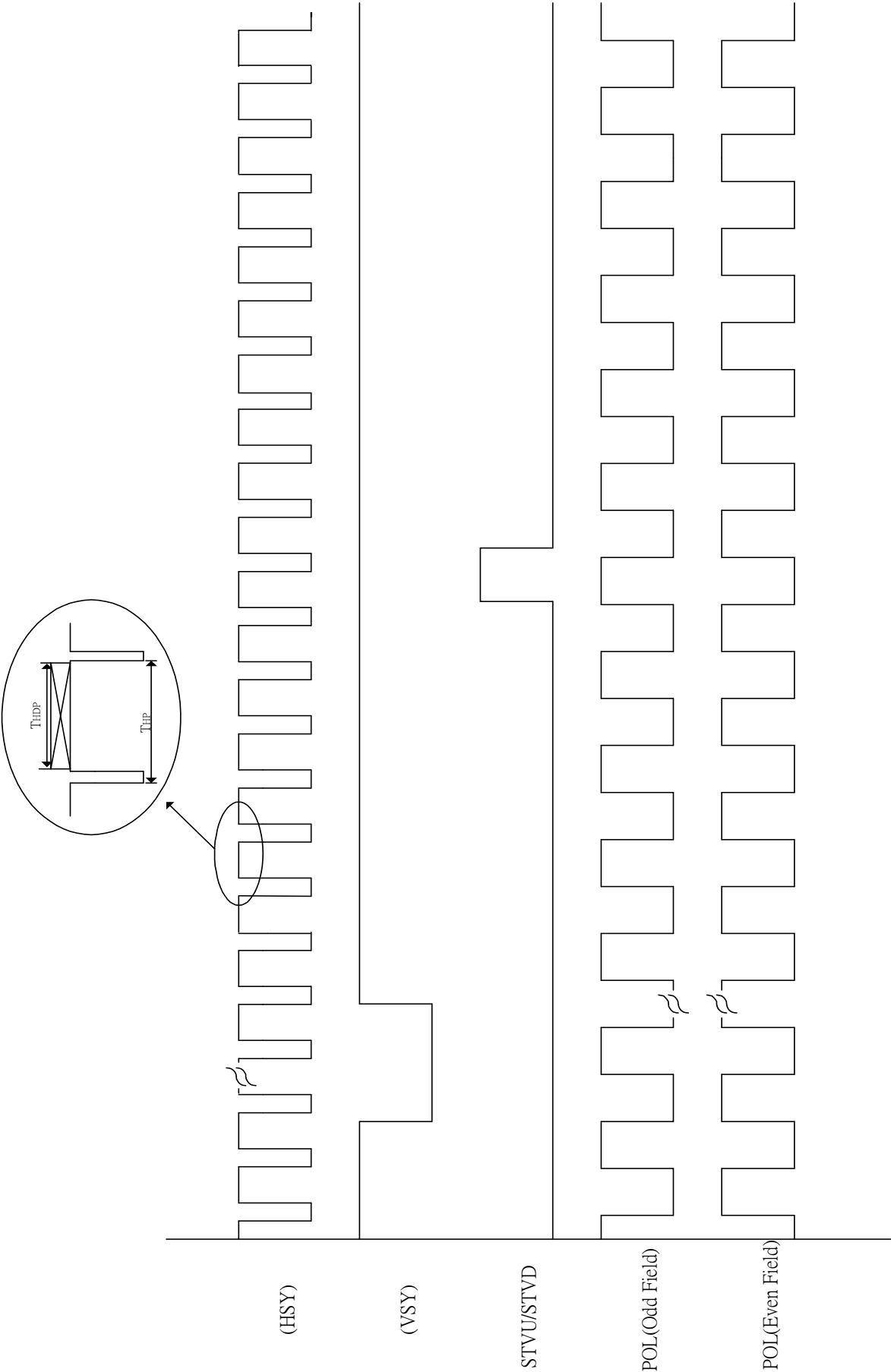
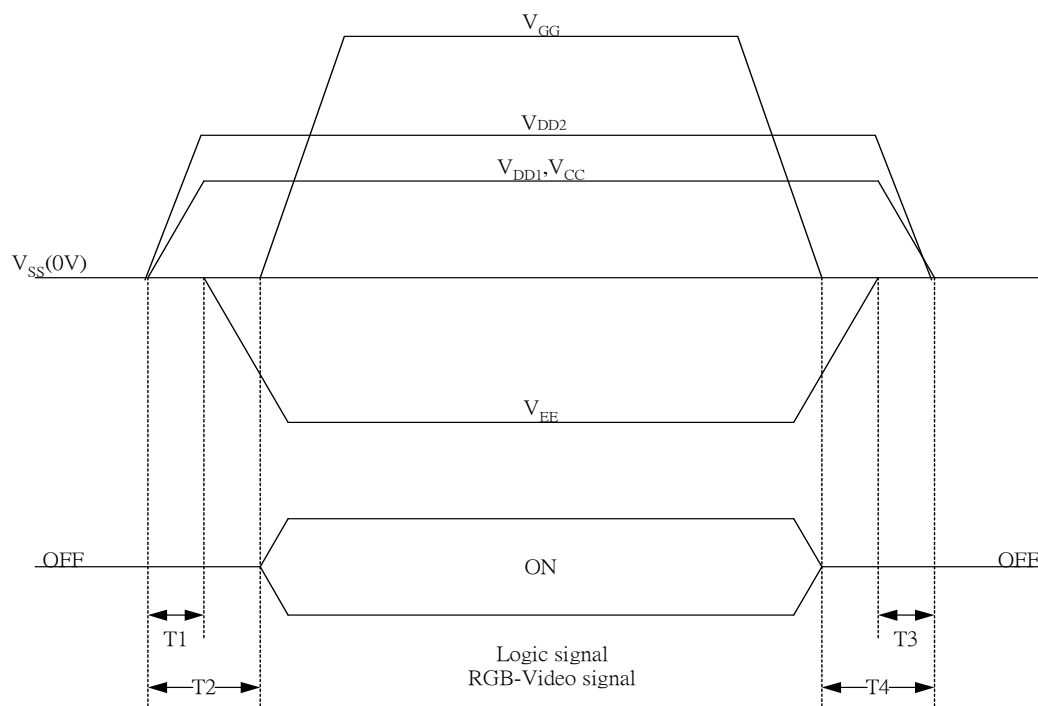


Fig. 11-4 Vertical timing

13. Power On Sequence



$$1. 10\text{ms} \leq T1 < T2$$

$$2. 0\text{ms} < T3 \leq T4 \leq 10\text{ms}$$

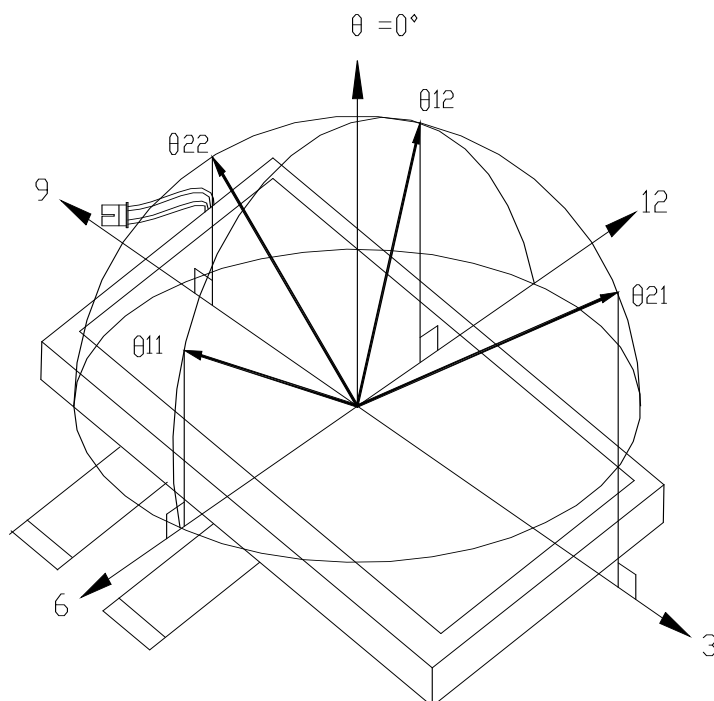
14. Optical Characteristics

14-1) Specification:

$T_a = 25^\circ\text{C}$

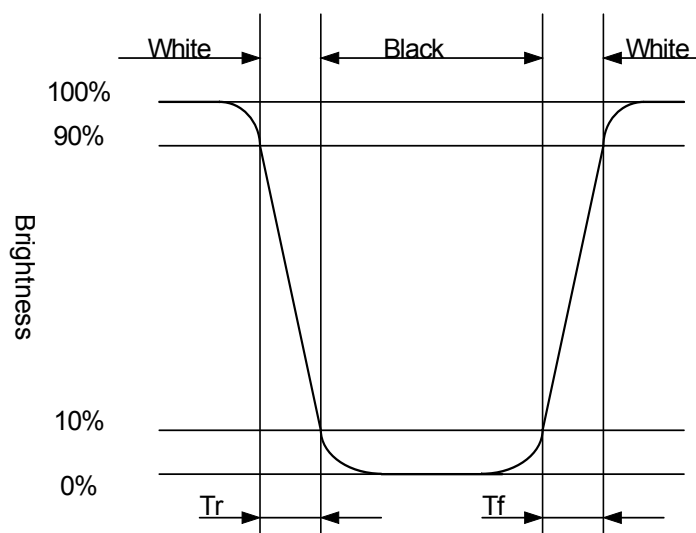
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR > 10	±55	±60		deg	Note 14-1
	Vertical	θ (to 12 o'clock)		35	40	-	deg	
		θ (to 6 o'clock)		50	55	-	deg	
Contrast Ratio		CR		250	400	-	-	Note 14-2
Response time	Rise	Tr	$\theta = 0^\circ$	-	15	30	ms	Note 14-3
	Fall	Tf		-	25	50	ms	
Brightness			$\theta = 0^\circ / \varphi = 0$	300	350		cd/m ²	Note 14-4
Luminance Uniformity		U		70	75	-	%	Note 14-5
Lamp Life Time				25000	-	-	hr	At 6mA
White Chromaticity		x		0.27	0.30	0.33	-	
		y		0.30	0.33	0.36	-	
Cross Talk			$\theta = 0^\circ$	-	-	3.5	%	Note 14-6

Note 14-1: The definitions of viewing angles are as follow



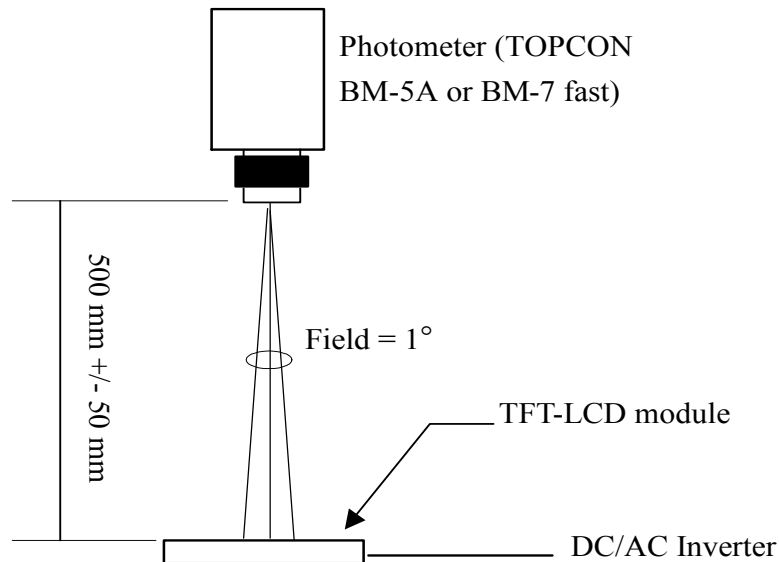
Note 14-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 14-3: Definition of Response Time T_r and T_f :



Note 14-4: All the optical measurement shall be executed 30 minutes after backlight being turn-on.

The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



Optical characteristics measuring configuration

Note 14-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

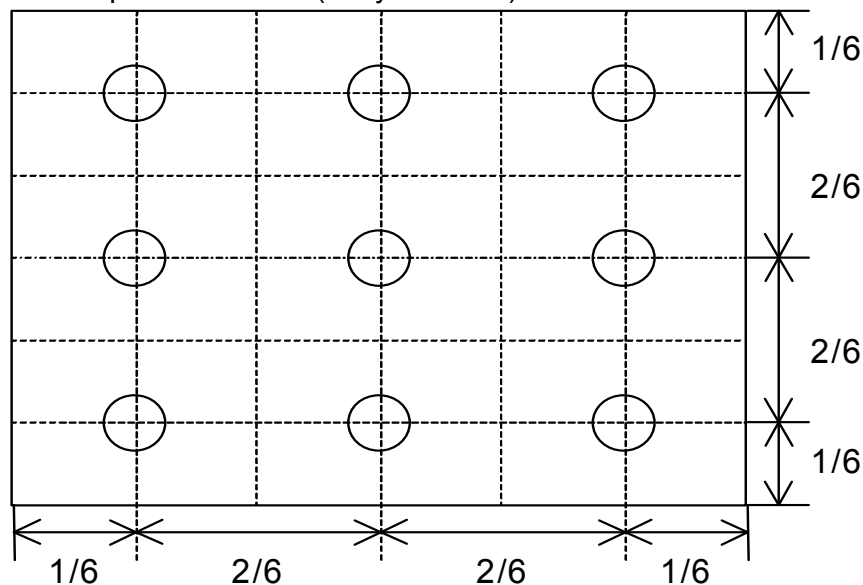
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).



Note 14-6: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A

YB: Brightness of Pattern B

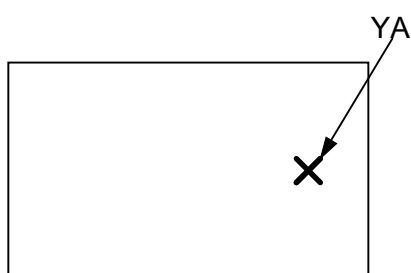
Luminance meter : BM 5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

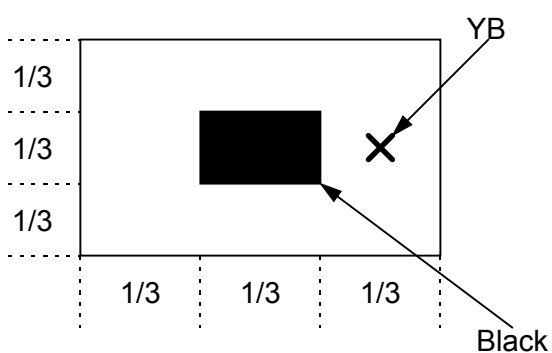
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

Pattern A
(Gray Level 31)



Pattern B
(Gray Level 31, central
black box exclusive)



X: Measuring Point (A and B are at the same point.)

(Gray Level 0)

15. Handling Cautions**15-1) Mounting of module**

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 - 1.The noise from the backlight unit will increase.
 - 2.The output from inverter circuit will be unstable.
 - 3.In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

15-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

15-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

15-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

16. Reliability Test

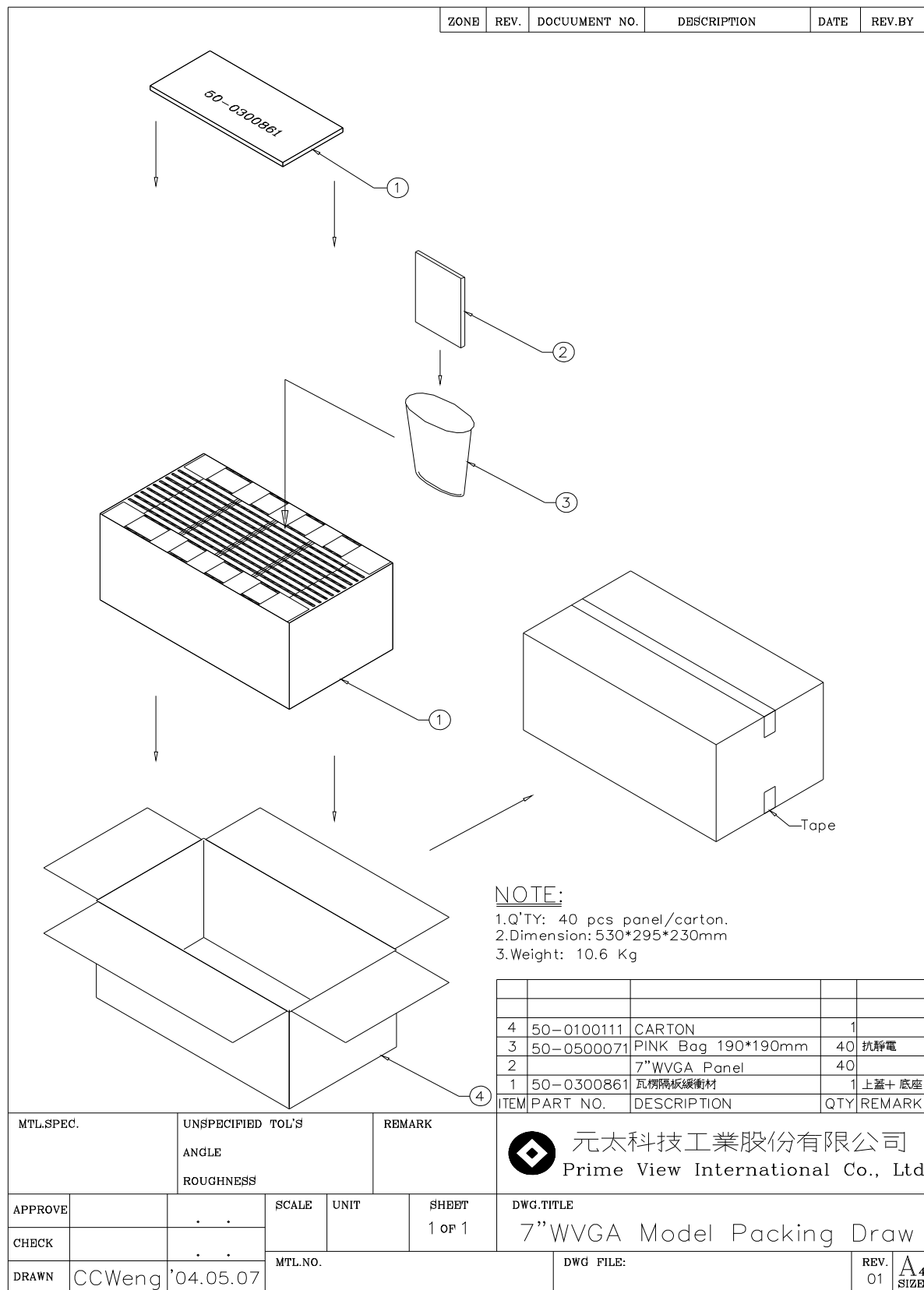
No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +80℃, 240 hrs	
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs	
3	High Temperature Operation Test	Ta = +80℃, 240 hrs	
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-30℃ → +80℃, 200 Cycles 30min 30min	
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz, Amplitude : 1 mm Sweep time: 11 min Test Period: 6 Cycles for each direction of X, Y, Z	
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times	
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal	
10	Hitting Durability Test (Touch panel)	1,000,000 times, with R 8.0 mm silicon rubber, 250g, 3times/sec	
11	Sliding Durability Test (Touch panel)	1,00,000 times, with R 0.8 mm polyacetal stylus, 250g, 60mm/sec	

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Judgement Criteria]

Under the display quality test conditions with normal operation state , there should be no change which may affect practical display function.

17. Packing Diagram


Revision History

Rev.	Issued Date	Revised	Contents
0.1	Apr.12 , 2005		Preliminary