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PMC

PRELIMINARY

Pm29F004

4 Megabit (512K X 8) 5.0 Volt-only CMOS Flash Memory

FEATURES

- **Single Power Supply Operation**
  - 5.0 V ± 10% Read/Program/Erase
- **High Performance Read**
  - 70/90 ns access time
- **Memory Blocks Architecture**
  - One 16 Kbytes top or bottom Boot Block with software lockout
  - Two 8 Kbytes Parameter Blocks
  - One 96 Kbytes Main Block
  - Three 128 Kbytes Main Blocks
- **Automatic Block Erase and Byte Program**
  - Typical 12 µs/byte programming
  - Typical 50 ms block or chip erase
- **Hardware Data Protection**
- **Data# Polling and Toggle Bit Features**
- **Low Power Consumption**
  - Typical 15 mA active read current
  - Typical 40 mA program/erase current
  - Typical 0.1 µA CMOS standby current
- **High Product Endurance**
  - Guarantee 10,000 program/erase cycles
  - Typical 50,000 program/erase cycles
  - Minimum 10 years data retention
- **Industrial Standard Pin-out and Packaging**
  - 32-pin Plastic DIP
  - 32-pin PLCC
- **Manufactured on 0.30 µm process**

GENERAL DESCRIPTION

The Pm29F004 is a 4 Megabit, 5 Volt-only Flash Memory organized as 524,288 bytes of 8 bits each. This device is designed to use a 5.0 Volt power supply to perform in-system programming, 12.0 Volt V_{PP} power supply for program and erase operation is not required. The device can be programmed in standard EPROM programmers as well.

The 4 Megabit memory array is divided into seven blocks of one 16 Kbytes, two 8 Kbytes, one 96 Kbytes, and three 128 Kbytes for BIOS and parameters storage. The seven blocks allow users to flexibly make chip erase or block erase operation. The block erase feature allows a particular block to be erased and reprogrammed without affecting the data in other blocks. After the device performed chip erase or block erase operation, it can be reprogrammed on a byte-by-byte basis.

The device has a standard microprocessor interface as well as JEDEC single-power-supply Flash compatible pin-out and command set. The program operation of Pm29F004 is executed by issuing the program command code into command register. The internal control logic automatically handles the programming voltage ramp-up and timing. The erase operation of Pm29F004 is executed by issuing the chip erase or block erase command code into command register. The internal control logic automatically handles the erase voltage ramp-up and timing. The preprogramming on the array which has not been programmed is not required before the erase operation. The device also features Data# Polling and Toggle Bit function, the end of program or erase operation can be detected by Data# Polling of I/O7 or Toggle Bit of I/O6.

The device has an optional 16 Kbytes top or bottom boot block with a software lockout feature for data security. The boot block can be used to store user secure code. When the lockout feature is enabled, the boot block is permanently protected from being reprogrammed.

The Pm29F004 is manufactured on PMC's advanced 0.30 µm, P-FLASH™, nonvolatile memory process. The device is packaged in a 32-pin DIP and PLCC with access time of 70 and 90 ns.

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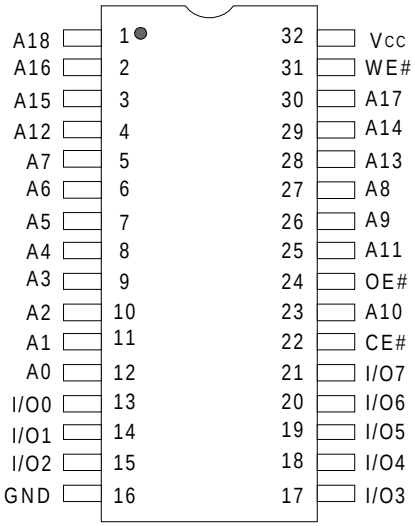
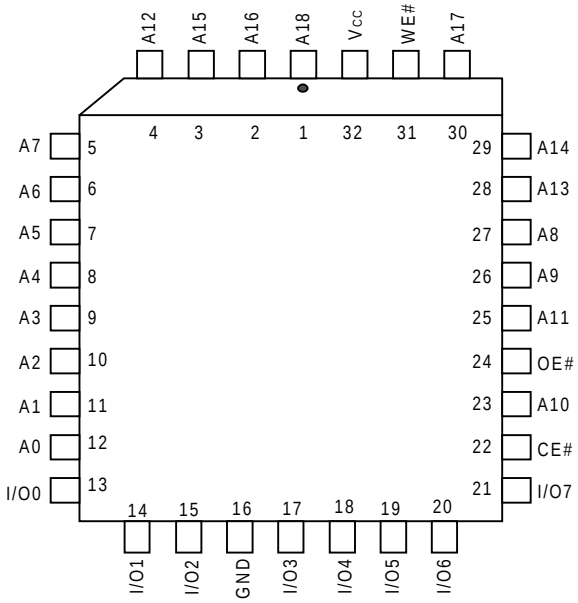
CONNECTION DIAGRAMS

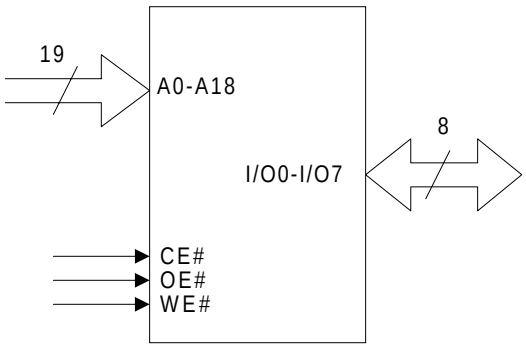


32-Pin PDIP

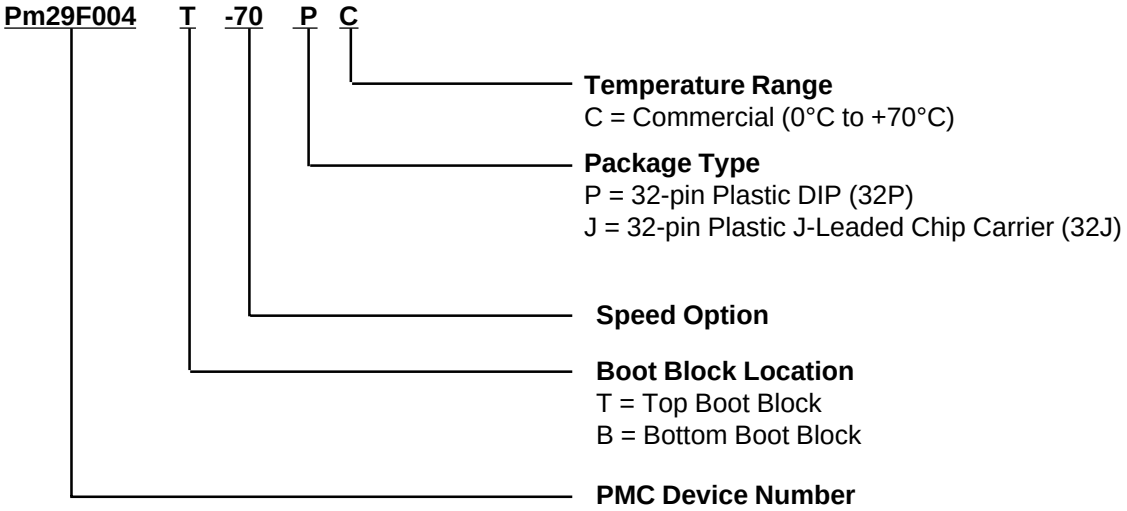


32-Pin PLCC

LOGIC SYMBOL



PRODUCT ORDERING INFORMATION

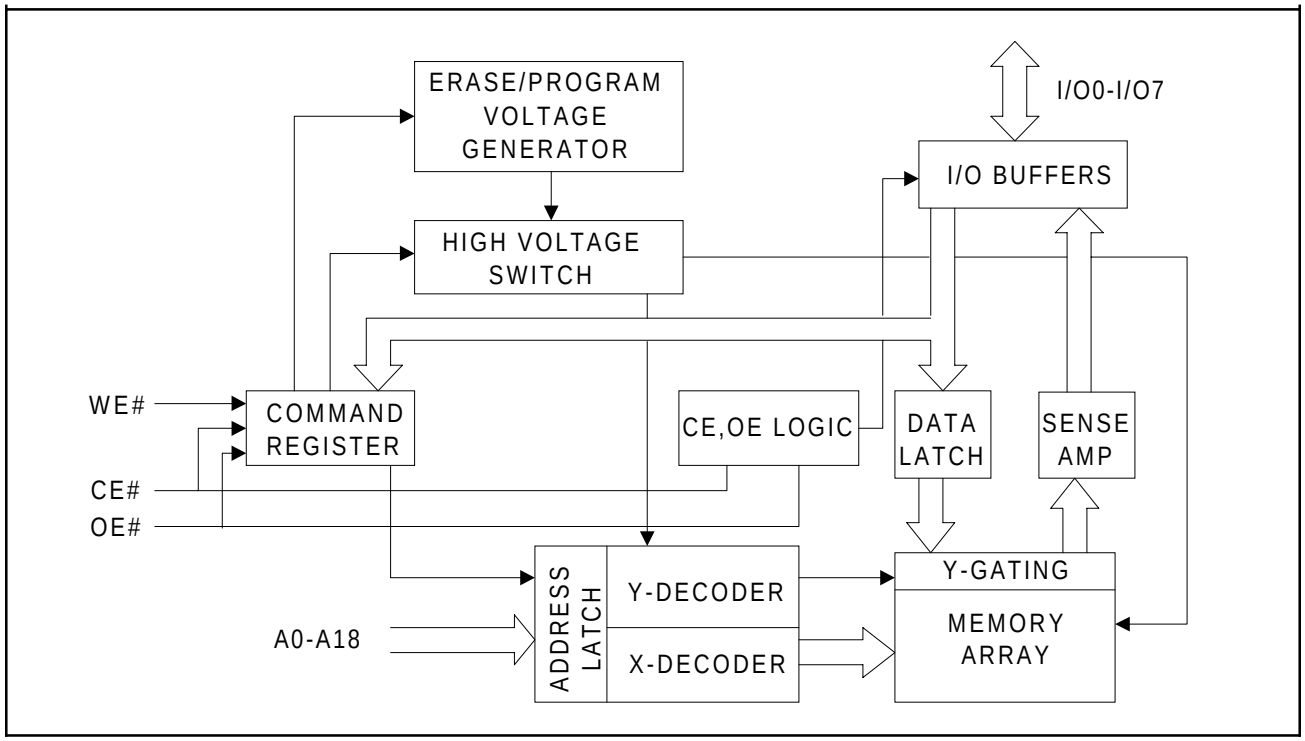


Part Number	t_{ACC} (ns)	Boot Location	Package	Temperature Range
Pm29F004T-70JC	70	Top	32J	Commercial (0°C to +70°C)
Pm29F004T-70PC			32P	
Pm29F004B-70JC		Bottom	32J	
Pm29F004B-70PC			32P	
Pm29F004T-90JC	90	Top	32J	Commercial (0°C to +70°C)
Pm29F004T-90PC			32P	
Pm29F004B-90JC		Bottom	32J	
Pm29F004B-90PC			32P	

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
A0 - A18	INPUT	Address Inputs: For memory addresses and command register. Addresses are internally latched during a write cycle.
CE#	INPUT	Chip Enable: CE# low activates the device's internal circuitries for device operation. CE# high deselects the device and switches into standby mode to reduce the power consumption. Please refer to DC characteristics table.
WE#	INPUT	Write Enable: Activate the device for write operation. WE# is active low.
OE#	INPUT	Output Enable: Control the device's data buffers during a read cycle. OE# is active low.
I/O0 - I/O7	INPUT/ OUTPUT	Data Inputs/Outputs: Inputs array data during program operation, when CE# and WE# are active. Data is internally latched during the write and program cycles. When CE# and OE# are active, the output sends array data, manufacturer code or device code. The data pins float to tri-state when the chip is deselected or the outputs are disabled.
V_{CC}		Device Power Supply
GND		Ground
NC		No Connection

BLOCK DIAGRAM



DEVICE OPERATION

READ OPERATION

The access of Pm29F004 is similar as that of EPROM. To obtain data at the outputs, three control functions must be satisfied:

• CE# is the chip enable and should be pulled low (V_{IL}).

• OE# is the output enable and should be pulled low (V_{IL}).

• WE# is the write enable and should remains high (V_{IH}).

BOOT BLOCK LOCKOUT

The device has a software lockout feature to prevent the data in the boot block from being erased or reprogrammed. The boot block can be located at the top or bottom of the address location. The block size is 16 Kbytes. Once the lockout feature is enable, the boot block can not be erased or reprogrammed. Data in the main memory block can still be updated through the regular programming method. The boot block lockout feature can be turned on by issuing a six-bus-cycle command sequence. Please refer to Table 4 and Chart 4.

BOOT BLOCK LOCKOUT DETECTION

The state of the Boot Block lockout can be detected by software product identification entry. After entry, selects Boot Block address with A0 = “0” and A1 = “1” and then read I/O0. A data of “0” means the lockout feature is disabled and the Boot Block can be erased or programmed. A data of “1” means the lockout feature is enabled and the Boot Block is protected. Product identification exit must be executed before the device returns to read mode.

PRODUCT IDENTIFICATION

The product identification mode can be used to identify the device and the manufacturer by hardware or software operation. The hardware operation mode is activated by applying a 12.0 Volt on A9 pin, typically used by an external programmer to select the right programming algorithm for the device. For detail, please see Bus Operation Modes in Table 3. The software operation mode is activated by three-bus-cycle command. Please see Software Command Definition in Table 4.

DEVICE OPERATION (CONTINUED)

BYTE PROGRAMMING

The programming is a four-bus-cycle operation and the data is programmed into the device (to a logical "0") on a byte-by-byte basis. Please see Software Command Definition in Table 4. A program operation is activated by writing the three-byte command sequence followed by one byte of data into the device. The address are latched on the falling edge of WE# or CE# whichever occurs later, and the data is latched on the rising edge of WE# or CE#, whichever occurs first. The internal control logic automatically handles the internal programming voltages and timing.

A data "0" can not be programmed back to a "1". Only erase operation can convert "0"s to "1"s. The Data# Polling of I/O7 or Toggle Bit of I/O6 can be used to detect when the programming operation is completed.

CHIP ERASE

The entire memory array can be erased through a chip erase operation. Pre-programs the device is not required prior to chip erase operation. Chip erase starts after a six-bus-cycle chip erase command sequence. All commands will be ignored once the chip erase operation has started. The device will return back to read mode after the completion of chip erase. When the boot block lockout feature is enabled, the boot block will not be erased during a chip erase operation. Only the parameter blocks and the main blocks will be erased.

BLOCK ERASE

The memory array is organized into seven blocks: one 16 Kbytes boot block, two 8 Kbytes parameter blocks, one 96 Kbytes and three 128 Kbytes main blocks. A block erase operation allows to erase any individual block. Pre-programs the block is not required prior to block erase operation. If the boot block lockout feature is enable, the block erase command attempts to erase the boot block will be ignored. The block erase command is similar to chip erase command except for the last bus cycle command where the block addresses are used to select the block for erasure and the input data to the I/Os is 30h. Each block erase operation erases one block. Block erase and chip erase are both internally controlled and timed.

I/O7 DATA# POLLING

The Pm29F004 provides Data# Polling feature to indicate the process or the completion of a program or erase cycle. During a program cycle, an attempt to read the device will result in the complement of the last loaded data on I/O7. Once the program cycle is completed, the true data of the last loaded data is valid on all outputs. During a block or chip erase operation, an attempt to read the device will result a "0" on I/O7. After the erase cycle is completed, an attempt to read the device will result a "1" on I/O7.

I/O6 TOGGLE BIT

The Pm29F004 also provides Toggle Bit feature as a method to detect the process or the end of a program or erase cycle. During a program or erase operation, an attempt to read data from the device will result in I/O6 toggling between "1" and "0". When the program or erase operation is complete, I/O6 will stop toggling and valid data will be read. Toggle bit may be accessed at any time during a program or erase cycle.

HARDWARE DATA PROTECTION

Hardware data protection protects the device from unintentional erase or program operation. It is performed in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) Write inhibit: holding any of the signal OE# low, CE# high or WE# high inhibits a write cycle. (c) Noise filter: pulses of less than 20 ns (typical) on the WE# or CE# inputs will not initiate a write cycle.

MEMORY BLOCKS AND ADDRESSES

Table 1. Top Boot Block Address Table (Pm29F004T)

Block	Block Size	Address Range
Main Block 4	128 Kbytes	00000h-1FFFFh
Main Block 3	128 Kbytes	20000h-3FFFFh
Main Block 2	128 Kbytes	40000h-5FFFFh
Main Block 1	96 Kbytes	60000h-77FFFh
Parameter Block 2	8 Kbytes	78000h-79FFFh
Parameter Block 1	8 Kbytes	7A000h-7BFFFh
Boot Block	16 Kbytes	7C000h-7FFFFh

Table 2. Bottom Boot Block Address Table (Pm29F004B)

Block	Block Size	Address Range
Boot Block	16 Kbytes	00000h-03FFFh
Parameter Block 1	8 Kbytes	04000h-05FFFh
Parameter Block 2	8 Kbytes	06000h-07FFFh
Main Block 1	96 Kbytes	08000h-1FFFFh
Main Block 2	128 Kbytes	20000h-3FFFFh
Main Block 3	128 Kbytes	40000h-5FFFFh
Main Block 4	128 Kbytes	60000h-7FFFFh

OPERATING MODES

Table 3. Bus Operation Modes

Mode	CE#	OE#	WE#	ADDRESS	I/O
Read	V_{IL}	V_{IL}	V_{IH}	X (1)	D_{OUT}
Write	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Standby	V_{IH}	X	X	X	High Z
Output Disable	X	V_{IH}	X	X	High Z
Product Identification Hardware	V_{IL}	V_{IL}	V_{IH}	A2 - A18 = X, A9 = V_H (2), A1 = V_{IL}, A0 = V_{IL}	Manufacturer Code (3)
				A2 - A18 = X, A9 = V_H (2), A1 = V_{IL}, A0 = V_{IH}	Device Code (3)

Notes:
1. X can be V_{IL}, V_{IH} or addresses.
2. V_H = 12.0 V ± 0.5 V.
3. Manufacturer Code: 9Dh;
   Device Code: 1Eh (top boot), 2Eh (bottom boot)

COMMAND DEFINITION

Table 4. Software Command Definition

Command Sequence	Bus Cycle	1st Bus Cycle Addr Data	2nd Bus Cycle Addr Data	3rd Bus Cycle Addr Data	4th Bus Cycle Addr Data	5th Bus Cylce Addr Data	6th Bus Cycle Addr Data
Read	1	Addr D_{OUT}					
Chip Erase	6	555h AAh	2AAh 55h	555h 80h	555h AAh	2AAh 55h	555h 10h
Block Erase	6	555h AAh	2AAh 55h	555h 80h	555h AAh	2AAh 55h	BA (1) 30h
Byte Program	4	555h AAh	2AAh 55h	555h A0h	Addr D_{IN}		
Boot Block Lockout (2,3)	6	555h AAh	2AAh 55h	555h 80h	555h AAh	2AAh 55h	555h 40h
Boot Block Lockout Detection (3)	3	555h AAh	2AAh 55h	555h 90h	BA (4) 00h (5)		
					BA (4) 01h (5)		
Product Manufacturer ID	3	555h AAh	2AAh 55h	555h 90h	X00h 9Dh		
Product Device ID (Top Boot)	3	555h AAh	2AAh 55h	555h 90h	X01h 1Eh		
Product Device ID (Bottom Boot)	3	555h AAh	2AAh 55h	555h 90h	X01h 2Eh		
Product ID Exit (6)	3	555h AAh	2AAh 55h	555h F0h			
Product ID Exit (6)	1	XXXh F0h					

Notes:
1. BA = Block address of the block to be erased.

2. When the boot block lockout feature is enabled, the boot block will not be erased when a chip erase command or a block erase command for boot block erasure is issued. Once the boot block is not protected, the boot block will be erased when a chip erase command or a block erase command for boot block erasure is issued.

3. After completion of the boot block lockout enable or detection command, the Product ID Exit command must be issued to return to standard read mode.

4. BA = Block address of the boot block;
   For top boot block location, A0 = “0”, A1 = “1”, and A14-A18 = “1” where A2-A13 = Don’t Care;
   For bottom boot block location, A0 = “0”, A1 = “1”, and A14-A18 = “0” where A2-A13 = Don’t Care.

5. I/O0 = “1” means boot block lockout is enabled, I/O0 = “0” means boot block lockout is disabled.

6. Either one of the Product ID Exit command can be used.

DEVICE OPERATIONS FLOWCHARTS

AUTOMATIC PROGRAMMING

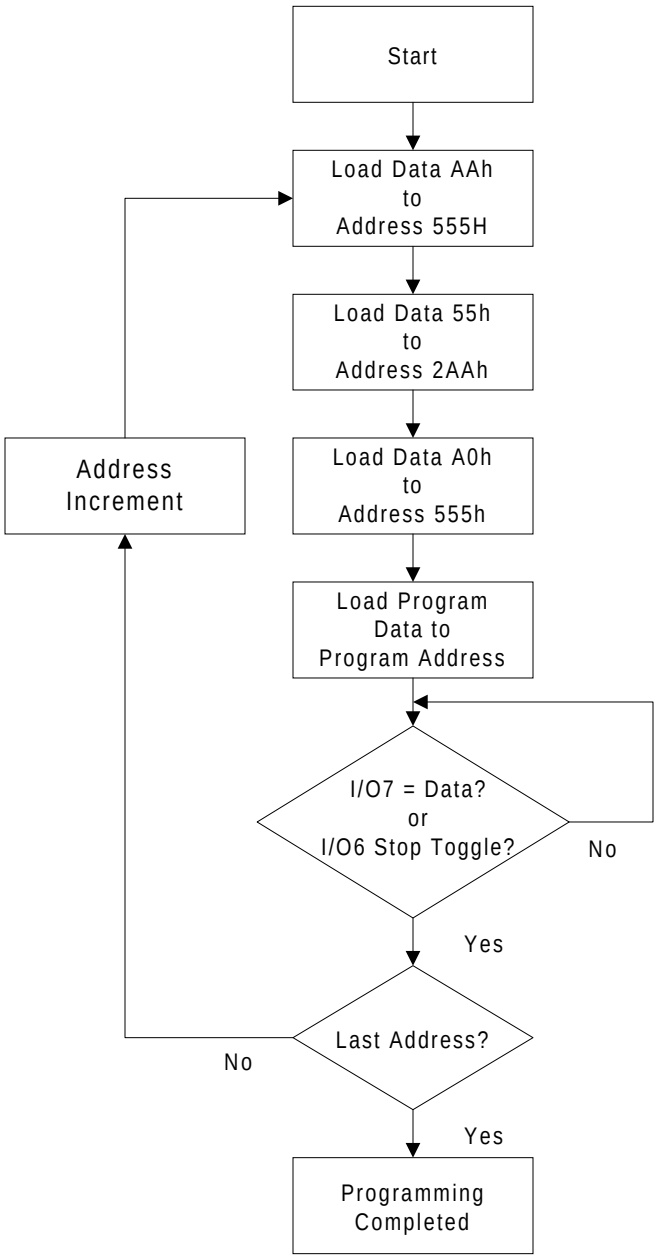
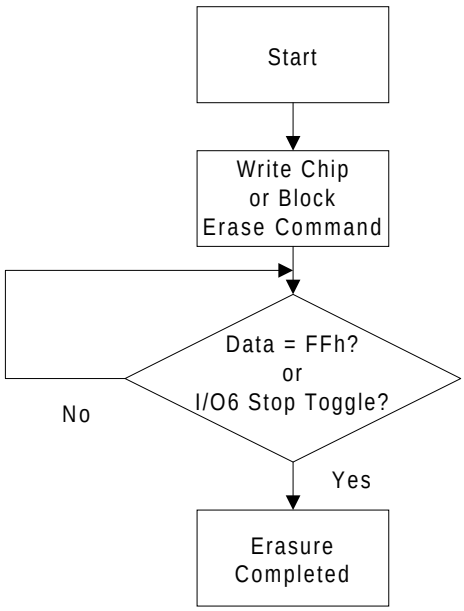


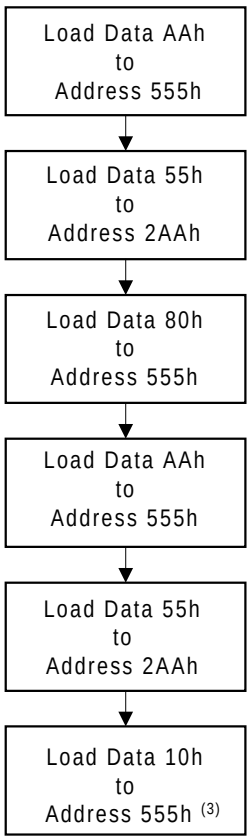
Chart 1. Automatic Programming Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

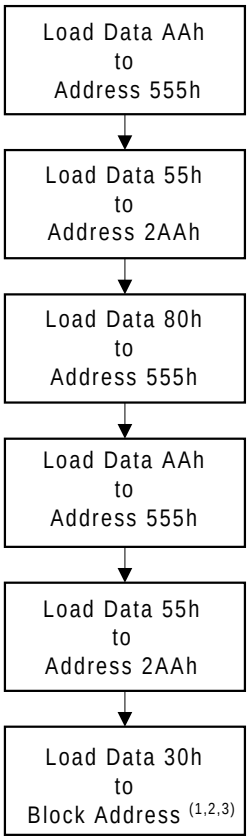
AUTOMATIC ERASE



CHIP ERASE COMMAND



BLOCK ERASE COMMAND

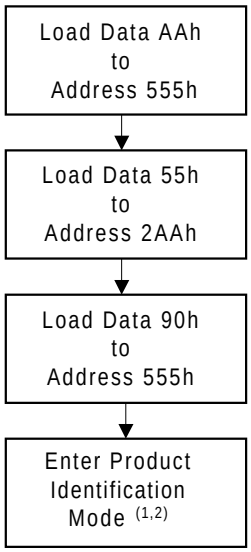


Notes:
1. Please see Software Command Definition in Table 1 and Table 2 for block addresses.
2. Only erase one block per each block erase cycle.
3. When the boot block lockout feature has been enabled, the boot block will not be erased.

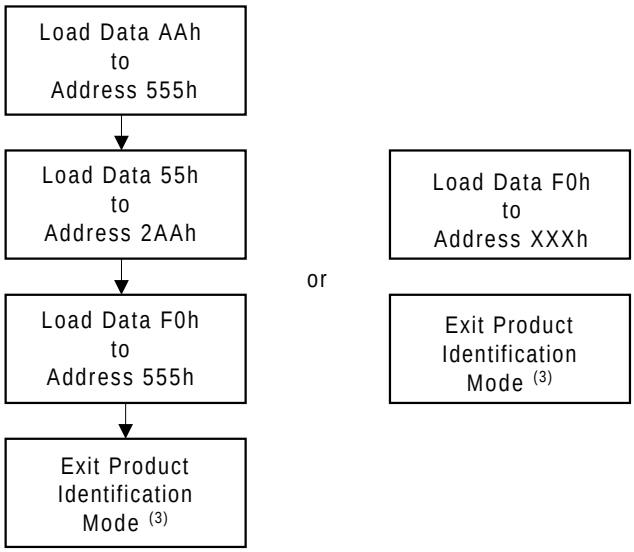
Chart 2. Automatic Erase Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

SOFTWARE PRODUCT IDENTIFICATION ENTRY



SOFTWARE PRODUCT IDENTIFICATION EXIT

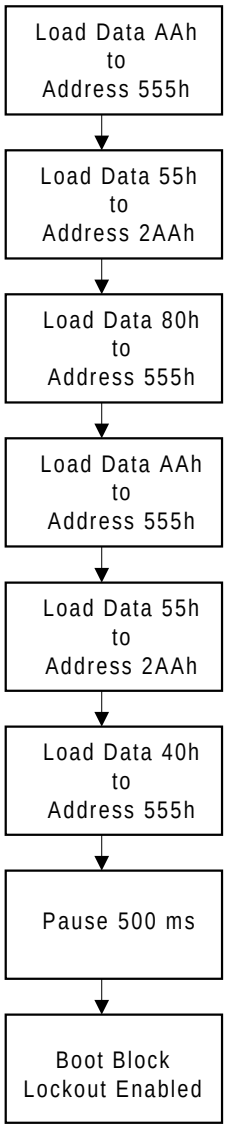


Notes:
1. Manufacturer Code is read when A0-A18 = XX00h, where X = Don't Care;
   Device Code is read when A0-A18 = XX01h.
2. Manufacturer Code = 9Dh;
   Device Code = 1Eh (top boot device);
   Device Code = 2Eh (bottom boot device).
3. The device returns to standard read operation.

Chart 3. Software Product Identification Entry/Exit Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

BOOT BLOCK LOCKOUT ENABLE (1,2)



Notes:
1. Please call manufacturer for the command code to disable the boot block lockout.
2. After excuting the boot block lockout command, the Product ID Exit command must be issued to return to standard read mode.

Chart 4. Boot Block Lockout Enable Flowchart

ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias	-65°C to +125°C
Storage Temperature	-65°C to +125°C
Input Voltage with Respect to Ground on All Pins except A9 pin (2)	-0.5 V to +6.25 V
Input Voltage with Respect to Ground on A9 pin (3)	-0.5 V to +13.0 V
All Output Voltage with Respect to Ground	-0.5 V to V_{CC} + 0.6 V
V_{CC} (2)	-0.5 V to +6.25 V

Notes:
1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
2. Maximum DC voltage on input or I/O pins are +6.25 V. During voltage transitioning period, input or I/O pins may overshoot to V_{CC} + 2.0 V for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.
3. Maximum DC voltage on A9 pin is +13.0 V. During voltage transitioning period, A9 pin may overshoot to +14.0 V for a period of time up to 20 ns. Minimum DC voltage on A9 pin is -0.5 V. During voltage transitioning period, A9 pin may undershoot GND to -2.0 V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

Part Number	**Pm29F004**
Operating Temperature	0°C to 70°C
Vcc Power Supply	4.5 V - 5.5 V

DC CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}, V_{CC} = $V_{CC\ max}$			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}, V_{CC} = $V_{CC\ max}$			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	CE#, OE# = V_{CC} ± 0.5 V		0.1	5	µA
I_{SB2}	V_{CC} Standby Current TTL	CE# = V_{IH} to V_{CC}		0.2	3	mA
I_{CC1}	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		15	30	mA
I_{CC2} (1)	V_{CC} Program/Erase Current			40	60	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, V_{CC} = $V_{CC\ min}$			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = $V_{CC\ min}$	2.4			V

Note: 1. Characterized but not 100% tested.

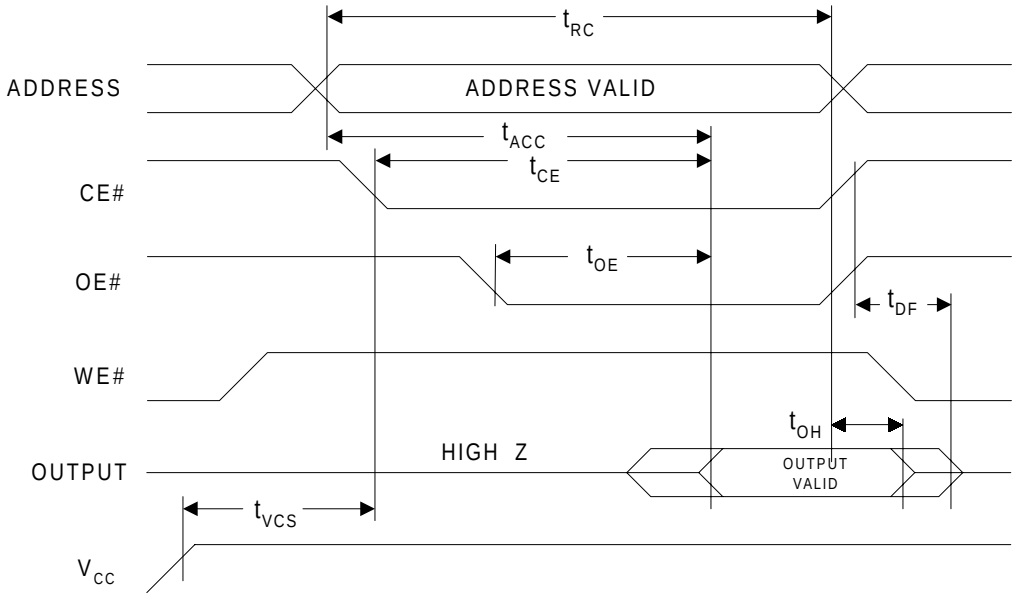
AC CHARACTERISTICS

READ OPERATIONS CHARACTERISTICS

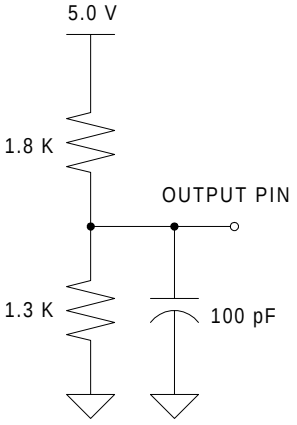
Symbol	Parameter	Pm29F004-70		Pm29F004-90		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	70		90		ns
t_{ACC}	Address to Output Delay		70		90	ns
t_{CE}	CE# to Output Delay		70		90	ns
t_{OE}	OE# to Output Delay		35		40	ns
t_{DF}	CE# or OE# to Output High Z	0	25	0	30	ns
t_{OH}	Output Hold from OE#, CE# or Address, whichever occured first	0		0		ns
t_{VCS}	V_{CC} Set-up Time	50		50		µs

AC CHARACTERISTICS (CONTINUED)

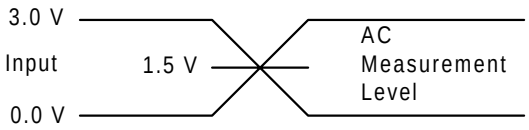
READ OPERATIONS AC WAVEFORMS



OUTPUT TEST LOAD



INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



PIN CAPACITANCE (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

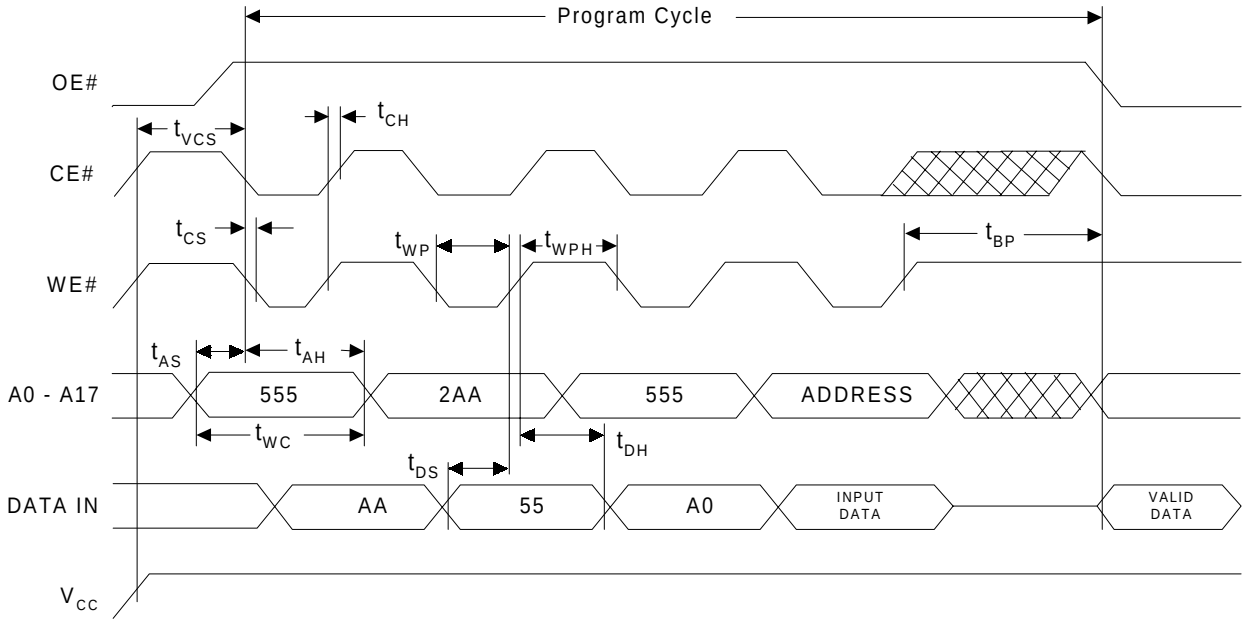
Note: These parameters are characterized and are not 100% tested.

AC CHARACTERISTICS (CONTINUED)

WRITE (PROGRAM/ERASE) OPERATIONS CHARACTERISTICS

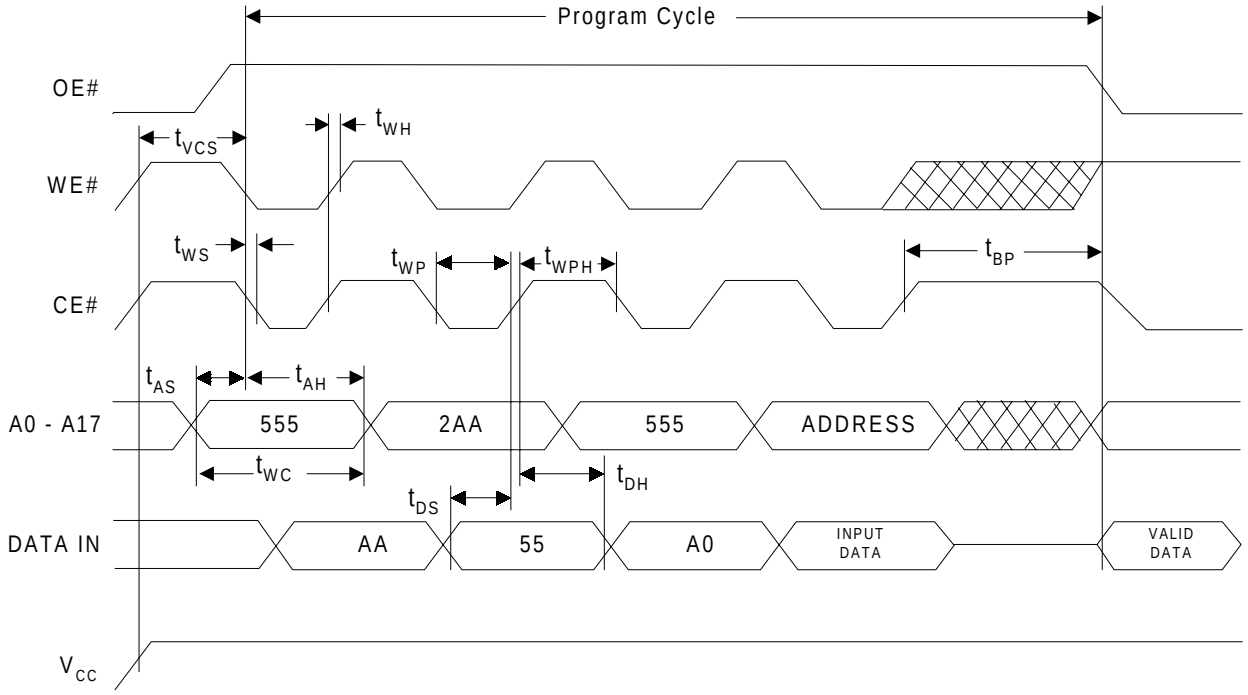
Symbol	Parameter	Pm29F004-70		Pm29F004-90		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	70		90		ns
t_{AS}	Address Set-up Time	0		0		ns
t_{AH}	Address Hold Time	45		50		ns
t_{CS}	CE# Set-up Time	0		0		ns
t_{CH}	CE# Hold Time	0		0		ns
t_{WS}	WE# Set-up Time	0		0		ns
t_{WH}	WE# Hold Time	0		0		ns
t_{DS}	Data Set-up Time	30		45		ns
t_{DH}	Data Hold Time	0		0		ns
t_{WP}	Write Pulse Width	35		45		ns
t_{WPH}	Write Pulse Width High	20		20		ns
t_{BP}	Byte Programming Time		50		50	µs
t_{EC}	Chip or Block Erase Cycle Time		100		100	ms
t_{VCS}	V_{CC} Set-up Time	50		50		µs

PROGRAM OPERATIONS AC WAVEFORMS - WE# CONTROLLED

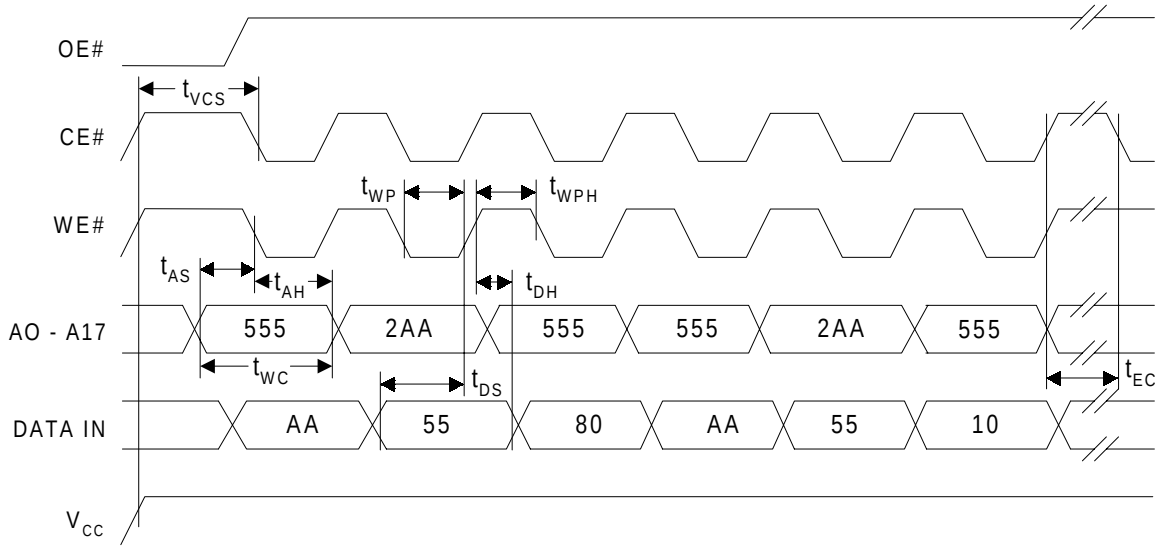


AC CHARACTERISTICS (CONTINUED)

PROGRAM OPERATIONS AC WAVEFORMS - CE# CONTROLLED

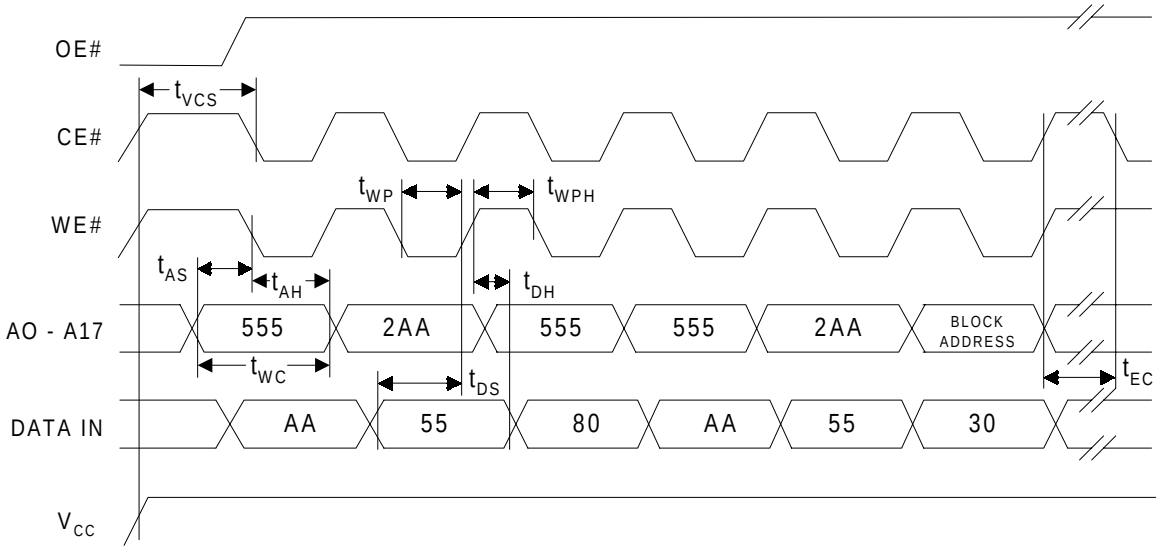


CHIP ERASE OPERATIONS AC WAVEFORMS



AC CHARACTERISTICS (CONTINUED)

BLOCK ERASE OPERATIONS AC WAVEFORMS



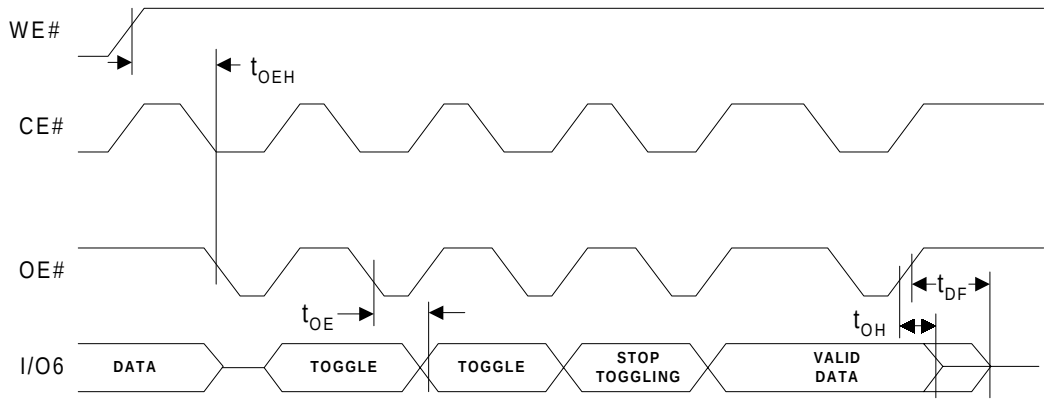
PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Min	Typ	Max	Remarks
Block Erase Time	ms		50	100	From writing erase command to erase completion
Chip Erase Time	ms		50	100	From writing erase command to erase completion
Byte Programming Time	µs		12	50	Excludes the time of four-cycle program command execution
Program/Erase Endurance	Cycles	10,000	50,000		

Note: These parameters are characterized and are not 100% tested.

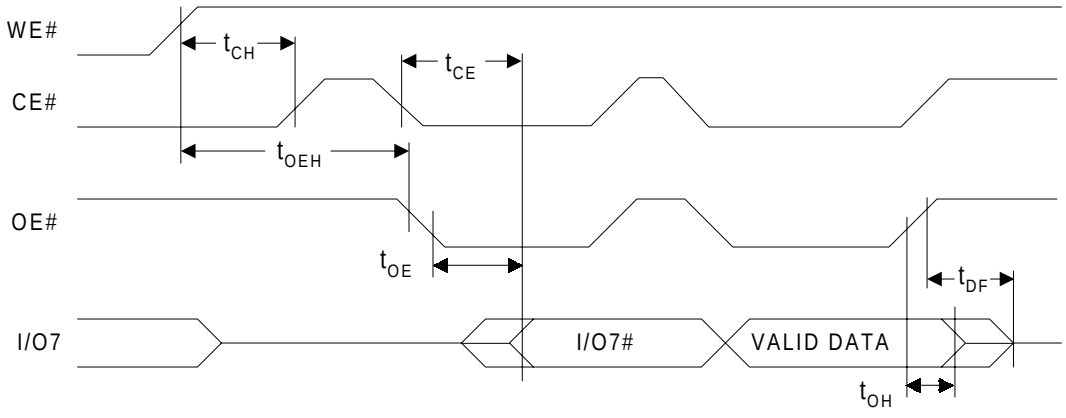
AC CHARACTERISTICS (CONTINUED)

TOGGLE BIT AC WAVEFORMS



Note: Toggling either CE#, OE# or both OE# and CE# will operate Toggle Bit.

DATA# POLLING AC WAVEFORMS

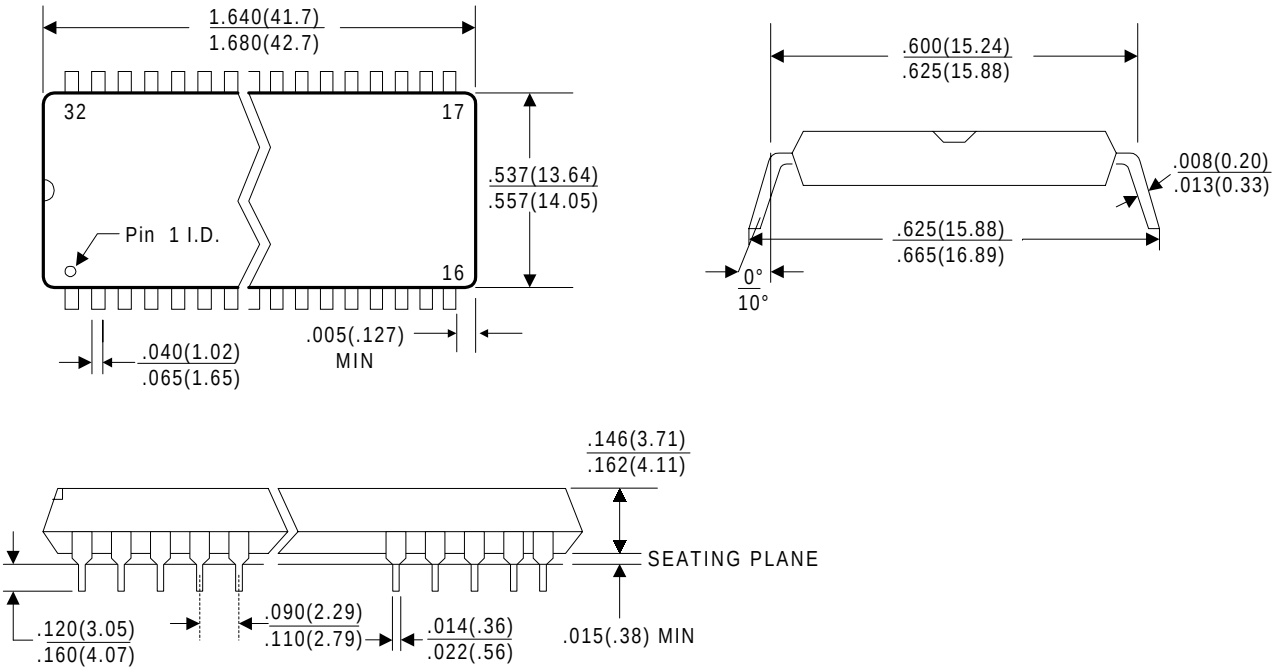


Note: Toggling either CE#, OE# or both OE# and CE# will operate Data# Polling.

PACKAGE TYPE INFORMATION

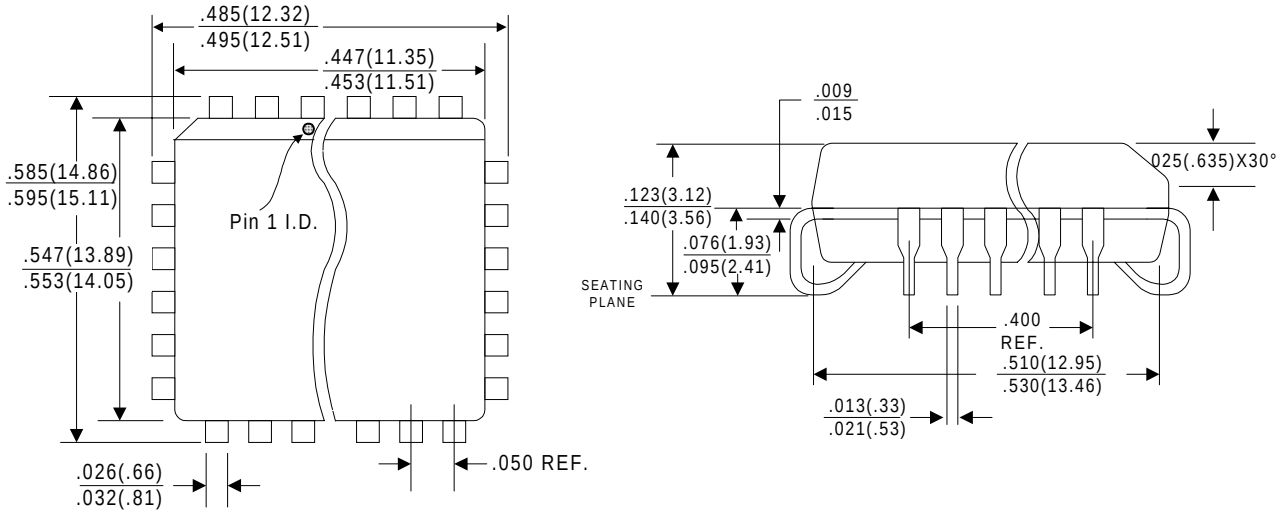
32P

32-Pin Plastic DIP Dimensions in Inches (Millimeters)



32J

32-Pin Plastic Leaded Chip Carrier Dimensions in Inches (Millimeters)



TOP VIEW **SIDE VIEW**