PMC-Sierra

Preliminary

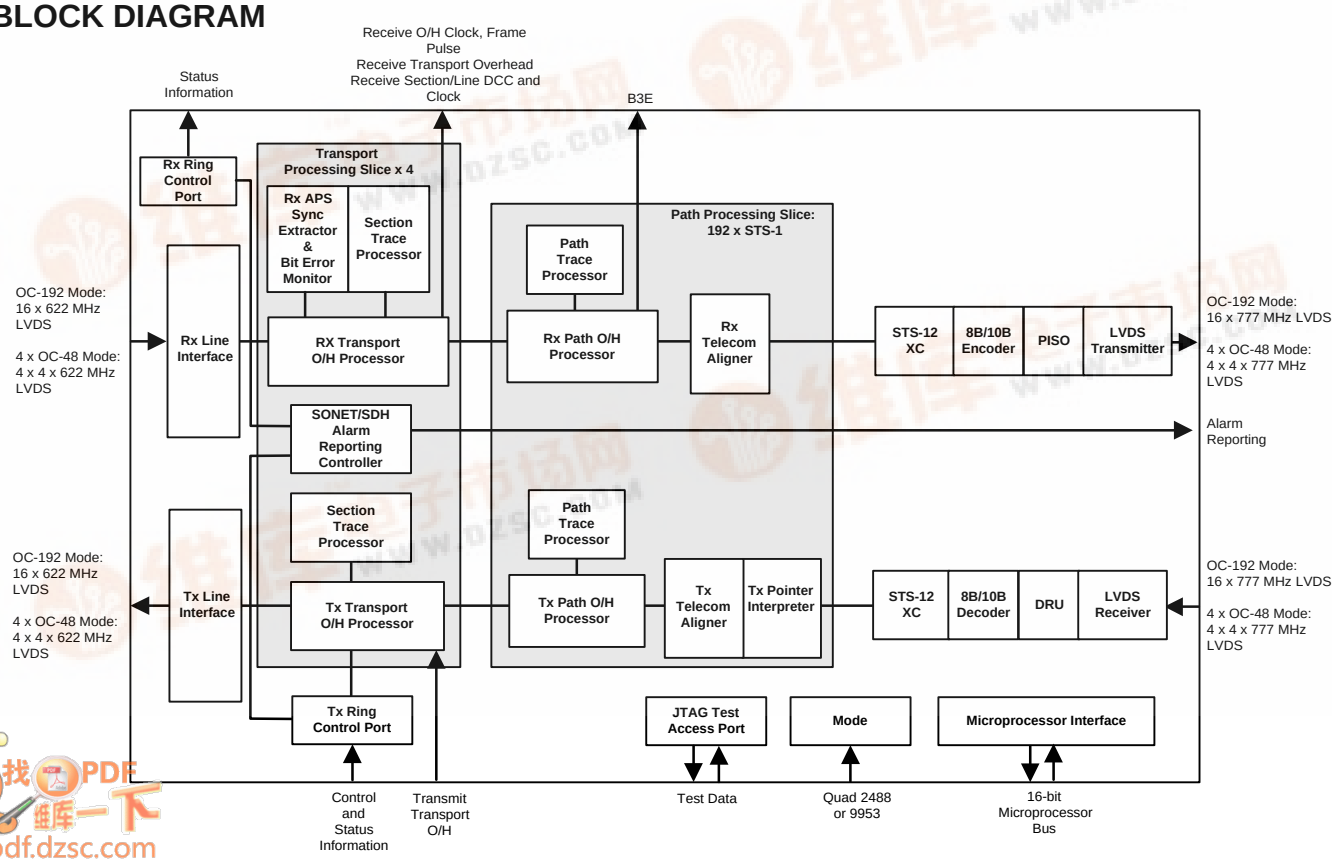
PM5317 SPECTRA-9953

SONET/SDH Payload Extractor/Aligner for 9953 Mbit/s

FEATURES

- Monolithic single channel STS-192/STM-64 or quad channel STS-48/STM-16 SONET/SDH Payload extractor/aligner.
- Designed for use in interface applications operating at serial interface speeds of up to OC-192 rates:
  - single STS-192c (STM-64/AU4-64c);
  - single STS-192 (STM-64/AU4-16c/AU4-4c/AU4/AU3) channelized to STS-1;
  - quad STS-48c (STM-16/AU4-16c);
  - quad STS-48 (STM-16/AU4-4c/AU4/AU3);
  - pointer processing for STS-1, STS-3c, STS-12c, STS-24c, STS-48c, and STS-192c traffic.
- In single STS-192/STM-64 mode, supports a duplex 16-bit 622 MHz LVDS line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.
- In quad STS-48/STM-16 mode, supports four duplex 4-bit 622 MHz LVDS line side interfaces for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.
- Standard OIF SFI-4 (16 x 622 Mbit/s) line side interface.
- Each channel provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section and High Order Path overhead.
- Provides a 16-bit 622 Mbit/s 8B10B encoded (777.7 MHz) ADD and DROP serial TelecomBus interface for grooming a single STS-192/STM-64 stream.
- Provides four 4-bit 622 Mbit/s 8B10B encoded (777.7 MHz) ADD and DROP serial TelecomBus interfaces for grooming four STS-48/STM-16 streams.
- Maps SONET/SDH payloads to system timing, accommodating plesiochronous timing offsets between the line and system timing references, through pointer processing.
- Provides STS-12 cross-connect capability for grooming traffic at the ADD and DROP TelecomBus interface.
- The entire SONET/SDH transport overhead is extracted to and inserted from dedicated pins. Path BIP-8 error counts are extracted to dedicated pins.
- Frames to the SONET/SDH receive stream, inserts framing bytes and STS identification into the transmit stream, and processes or inserts the transport overhead.
- Interprets or generates the STS (AU) pointer bytes (H1, H2, H3), extracts or inserts the synchronous payload envelope(s) and processes or inserts the path overhead.

BLOCK DIAGRAM



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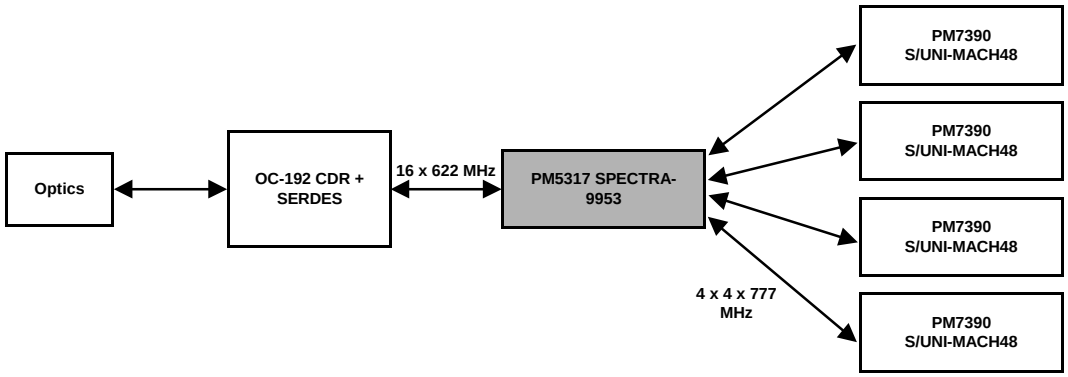
- Supports Automatic Protection Switching (APS):
  - Ring control port communication of path REI and path RDI alarms;
  - Filters the APS channel (K1,K2) bytes into internal registers; inserts the APS channel into the transmit stream.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loop-back from an ADD TelecomBus interface to a DROP TelecomBus interface.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power, 1.8 V CMOS core logic with 3.3 V CMOS/TTL digital inputs and digital outputs (2.5 V tolerant).
- Industrial temperature range (-40 °C to +85 °C).
- 1152 pin FCBGA package.

APPLICATIONS

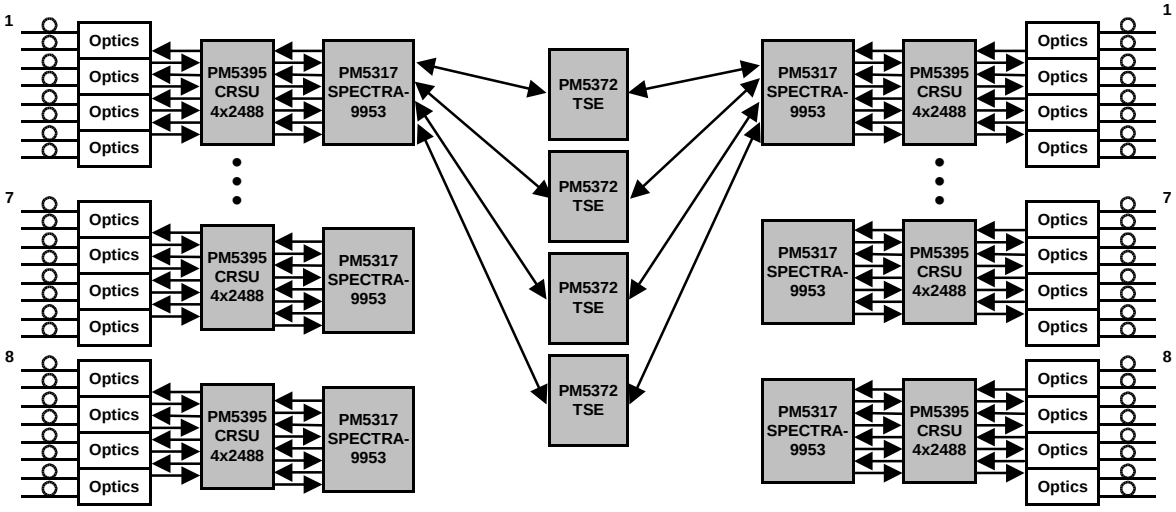
- Channelized STS-192/STM-64 or 4 x STS-48/STM-16 Interfaces for:
  - Optical cross connects;
  - Digital cross connects;
  - Router and switch line cards;
  - ADM aggregate cards for TDM and multiservice applications;
  - Terminal multiplexers;
  - SONET/SDH test equipment.

TYPICAL APPLICATION

OC-192 TO DS3 CARD



160 GIGABIT STS-1 CROSS-CONNECT



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