PM5345

S/UNI-155

SATURN USER NETWORK INTERFACE TELECOM STANDARD PRODUCT

DATA SHEET

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PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
4	June 1998	Data Sheet Reformatted — No Change in Technical Content. Generated R4 data sheet from PMC-920404, R11.

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1 FEATURES

- Monolithic Saturn Network Interface that implements the ATM physical layer for Broadband ISDN according to the ATM Forum User Network Interface Specification and CCITT Recommendation I.432.
- Operates at 155.52 MHz in conjunction with an external clock and data recovery device. Provides on-chip parallel to serial and serial to parallel circuits with pseudo ECL interfaces to process a duplex 155.52 Mbit/s STS-3c/STM-1 data stream.
- Supports a 19.44 Mbyte/s line interface option for devices requiring a byte-serial STS-3c/STM-1 interface.
- Provides 4 cell deep FIFO buffers in both transmit and receive paths with a byte-wide or word-wide system side datapath interface.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power, +5 Volt, CMOS technology.
- 160 pin high performance plastic quad flat pack (PQFP) package.

1.1 The receiver section:

- Frames to the recovered 155.52 Mbit/s stream or to an 19.44 Mbyte/s stream and descrambles the received STS-3c (STM-1) stream.
- Interprets the received payload pointer (H1, H2), extracting the STS-3c synchronous payload envelope (VC4) and path overhead.
- Extracts ATM cells from the received STS-3c synchronous payload envelope using ATM cell delineation and provides optional ATM cell payload descrambling, header check sequence (HCS) error detection and error correction, and idle/unassigned cell filtering.
- Provides a generic 8 bit wide or 16 bit wide datapath interface to read extracted cells from an internal four cell FIFO buffer.

- Extracts all transport overhead bytes and serializes them at 5.184 Mbit/s for optional external processing.

- Extracts all path overhead bytes and serializes them at 576 kbit/s for optional external processing.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (AIS), line far end receive failure (FERF), loss of pointer (LOP), path alarm indication signal (AIS), and path yellow alarm.

- Counts received section BIP-8 (B1) errors, received line BIP-24 (B2) errors, line far end block errors (FEBE), received path BIP-8 (B3) errors and path far end block errors (FEBE) for performance monitoring purposes.

- Counts received HCS errored cells that are discarded, and received HCS errored cells that are corrected and passed on for performance monitoring purposes.

1.2 The transmitter section:

- Provides an internal four cell FIFO into which cells are written using a generic 8 bit wide or 16 bit wide datapath interface

- Provides idle/unassigned cell insertion, HCS generation/insertion, and ATM cell payload scrambling.

- Inserts ATM cells into the transmitted STS-3c (STM-1) synchronous payload envelope using H4 framing.

- Generates the transmit payload pointer (H1, H2) and inserts the path overhead.

- Optionally inserts externally generated path overhead bytes received via a 576 kbit/s serial interface.

- Scrambles the transmitted STS-3c (STM-1) stream and inserts framing bytes (A1, A2) and the identity byte (C1).

- Optionally inserts externally generated transport overhead bytes received via a 5.184 Mbit/s serial interface.

- Interfaces to a downstream physical media device at 155.52 Mbit/s using differential outputs. Alternately, the S/UNI can interface to a parallel to serial converter at 19.44 Mbyte/s

- Optionally inserts path alarm indication signal (AIS), path yellow alarm indication (PYEL), line alarm indication signal (AIS) and line far end receive failure (FERF) indication.

- Inserts path BIP-8 codes (B3), path far end block error (FEBE) indications, line BIP-24 codes (B2), line far end block error (FEBE) indications, section BIP-8 codes (B1) to allow performance monitoring at the far end.

- Allows forced insertion of all zeros data (after scrambling) or corruption of framing byte or section, line, or path BIP-8 codes for diagnostic purposes.

2 APPLICATIONS

- SONET/SDH Based ATM Switching Systems
- SONET/SDH Based ATM Terminals
- B-ISDN User-Network Interfaces
- B-ISDN Network Node Interfaces
- B-ISDN Test Equipment

3 REFERENCES

- ITU-T Recommendation I.432 - "B-ISDN User-Network Interface - Physical Layer Specification", March 1993.
- ANSI T1.624-1993 - "Broadband ISDN User-Network Interfaces - Rates and Formats Specifications".
- ATM Forum - ATM User-Network Interface Specification, V3.0, 1993.

4 APPLICATION INFORMATION

The S/UNI is typically used to implement the core of an ATM User Network Interface by which an ATM terminal is linked to an ATM switching system or ATM switching systems are linked together using SONET/SDH compatible transport. The S/UNI may find application at either end of terminal to switch links or switch to switch links, both in private network (LAN) and public network (WAN) situations.

In this application the S/UNI typically connects on its line side with a twisted pair line receiver or optical receiver, plus a clock and data recovery device and a twisted pair line driver or laser for the transmitter. In this application, the S/UNI is loop timed internally (the recovered 155.52 MHz clock is used in the transmit direction). The drop side interfaces directly with ATM adaptation layer processors. The initial configuration and ongoing control and monitoring of the S/UNI are normally provided via a generic microprocessor interface. The S/UNI supports a "hardware-only" operating mode where an external microprocessor is not required. Typical ATM Adapter card applications are shown in Figure 1 and Figure 2.

Figure 1 - Example 1. Optical ATM Adapter Interface

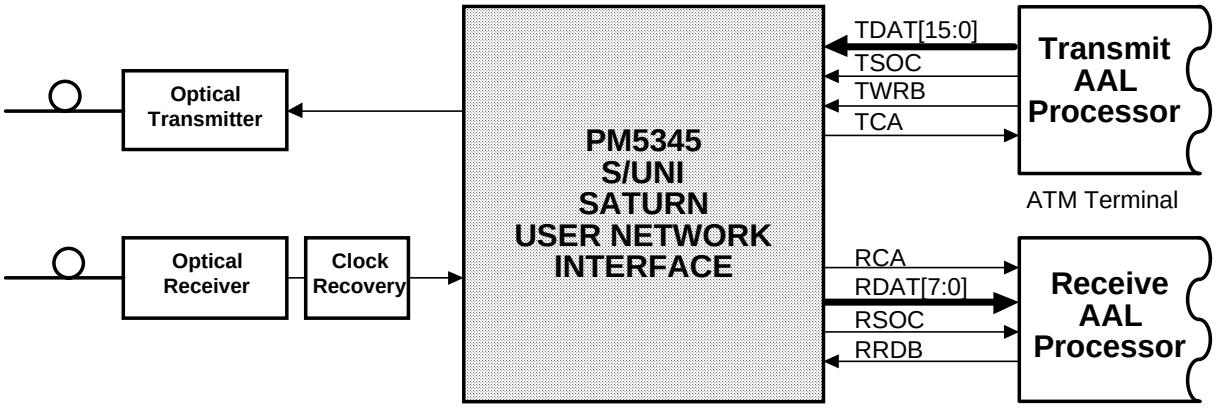


Figure 2 - Example 2. UTP-5 ATM Adapter Interface

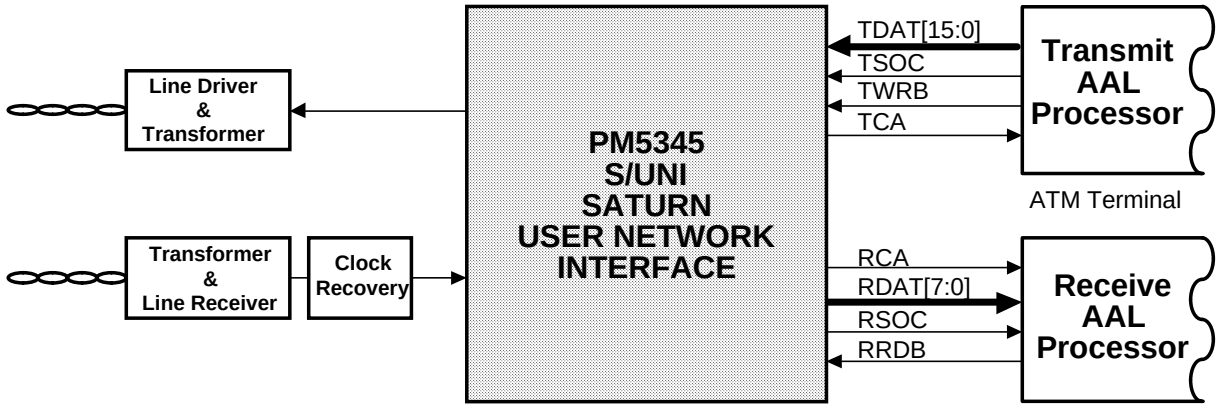
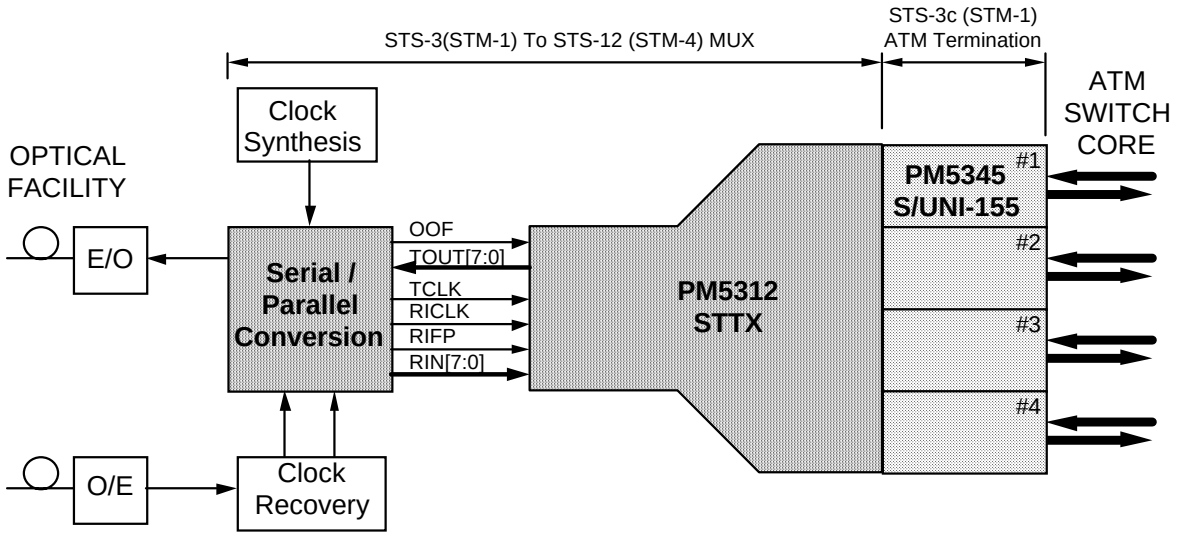


Figure 3 shows a configuration in which the PM5345 S/UNI is used with a PM5312 SONET/SDH Transport Overhead Terminating Transceiver (STTX) and a PM5318 622 Mbit/s Serial/Parallel Converter (SIPO) to implement an ATM backbone interface.

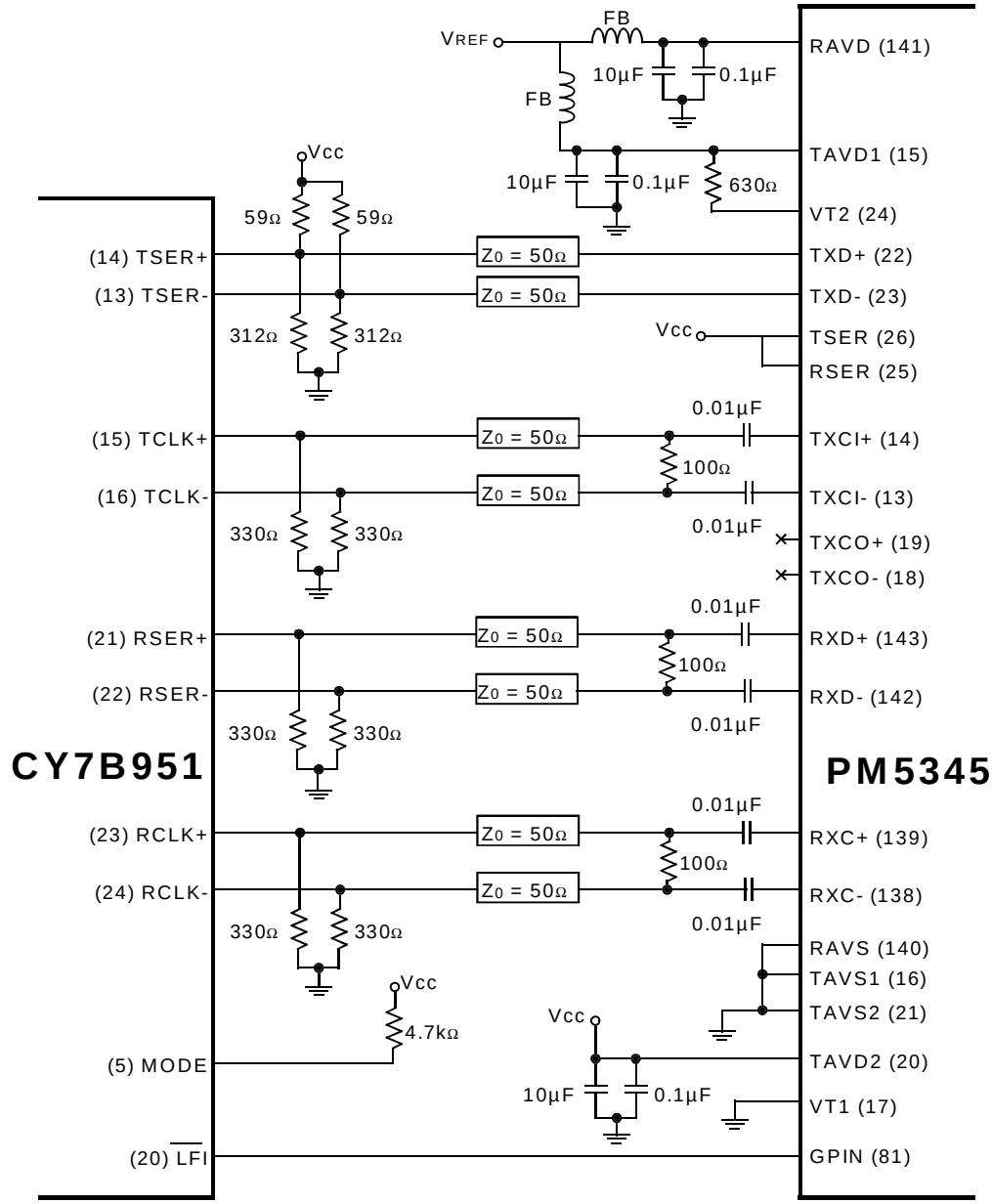
In this application, four STS-3/STM-1 ATM streams are multiplexed into a single STS-12/STM-4 stream for transport over fiber optic cables. The function of the PM5312, PM5318, clock recovery and clock synthesis are also available in the PM5712B 622 Mbit/s SONET/SDH Line Interface Module (SLIM).

Figure 3 - Example 3. OC-12 ATM Switch Port Card Interface



5 INTERFACE EXAMPLES

Figure 4 - Recommended Interface with CY7B951

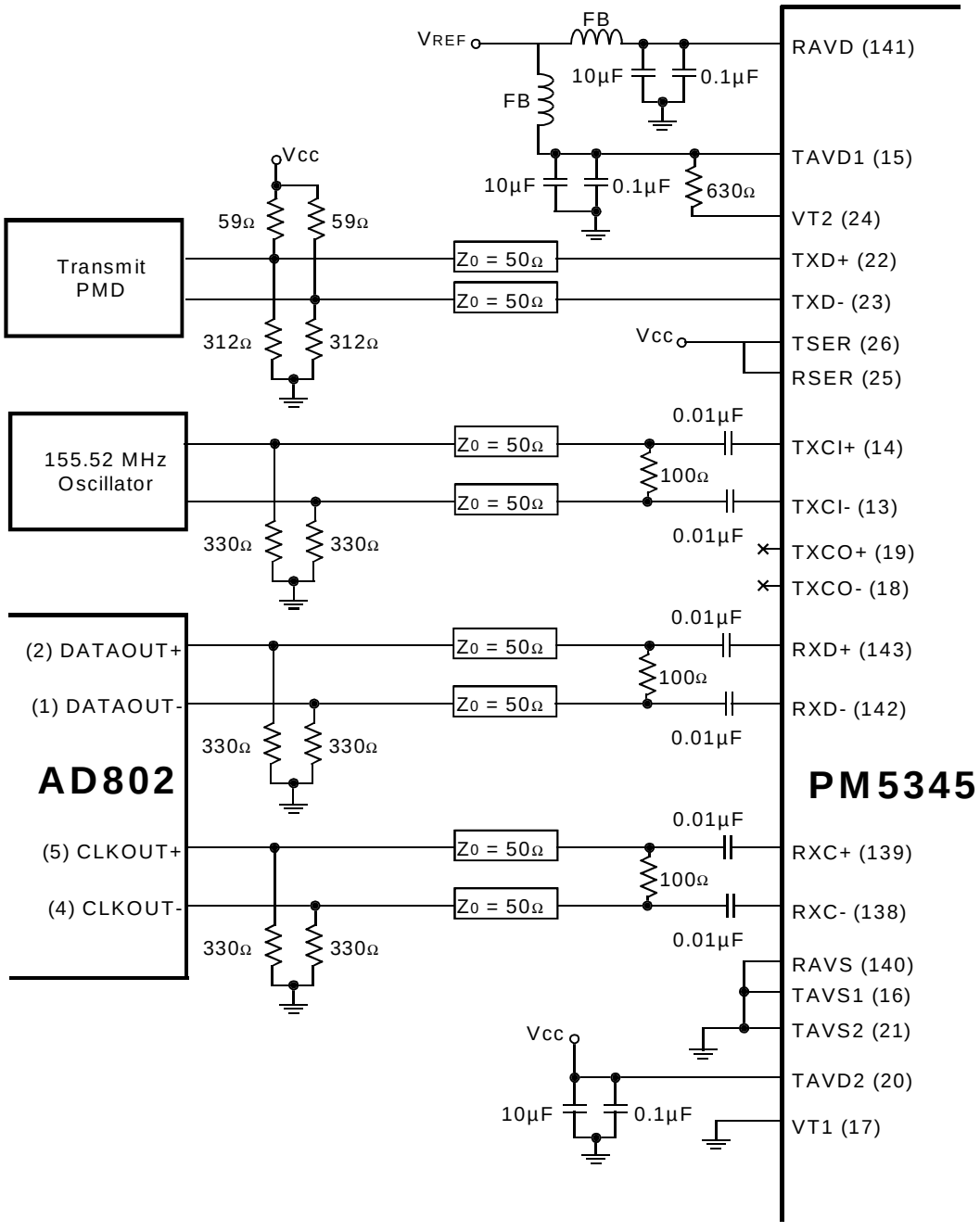


In Figure 4, the interface between the S/UNI and the Cypress CY7B951 is shown.

For optimal performance, the following guidelines should be followed:

- All power pins should be well decoupled, with the capacitors placed as close as possible to the S/UNI power pins.
- Termination resistors and capacitors should be placed as close as possible to the end of the transmission line.
- Source pull-down resistors should be placed as close as possible to the start of the transmission line.
- Traces marked "Zo=50Ω" should be controlled impedance traces. These traces should be kept as short as possible. Other controlled impedances can be used. Contact PMC-Sierra's applications department for information on using the S/UNI in "non-50Ω" controlled impedance environments.
- All inductors are Fair-Rite Products Corp #274-3019-446.

Figure 5 - Recommended Interface with AD802

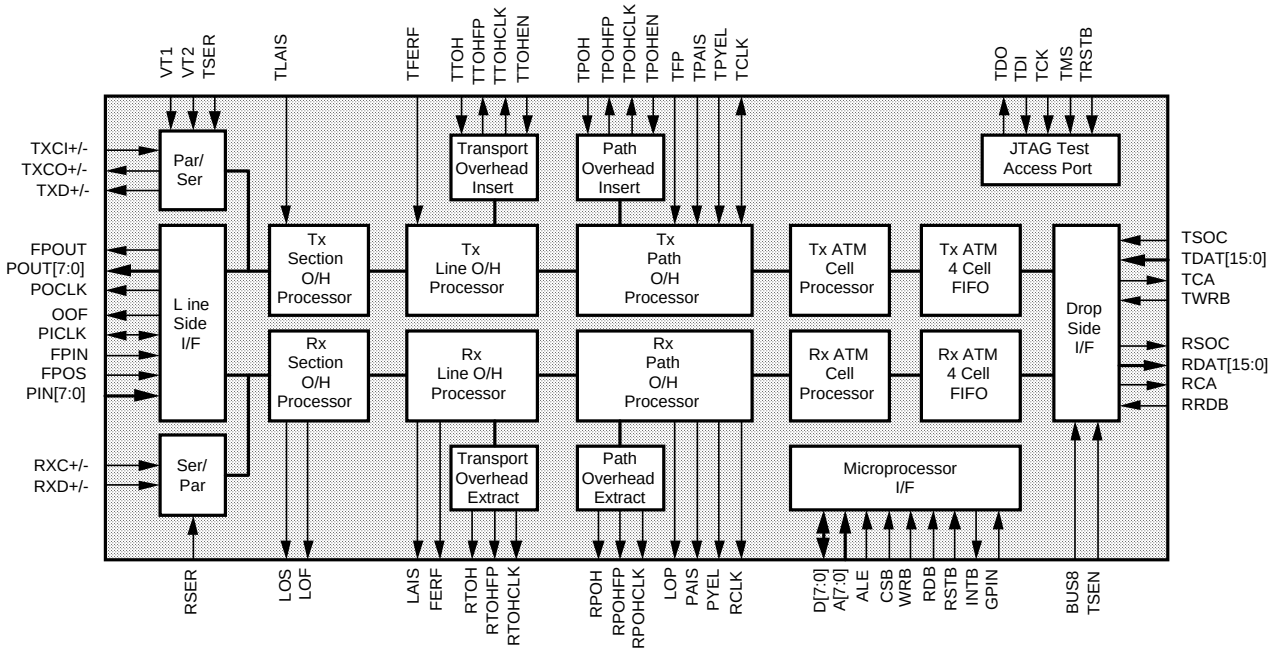


In Figure 5, the interface between the S/UNI and the Analog Devices AD802 is shown. In addition to the AD802, a 155.52 MHz oscillator provides the transmit clock to the S/UNI. Oscillator vendors include CTS Corporation, C-MAC Quartz Crystals Ltd., and Connor Winfield.

For optimal performance, the following guidelines should be followed:

- All power pins should be well decoupled, with the capacitors placed as close as possible to the S/UNI power pins.
- Termination resistors and capacitors should be placed as close as possible to the end of the transmission line.
- Source pull-down resistors should be placed as close as possible to the start of the transmission line.
- Traces marked "Zo=50Ω" should be controlled impedance traces. These traces should be kept as short as possible. Other controlled impedances can be used. Contact PMC-Sierra's applications department for information on using the S/UNI in "non-50Ω" controlled impedance environments.
- All inductors are Fair-Rite Products Corp #274-3019-446.

6 BLOCK DIAGRAM



7 DESCRIPTION

The PM5345 S/UNI SATURN User Network Interface is a monolithic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of a 155 Mbit/s ATM User-Network Interface.

The S/UNI receives SONET/SDH frames, via a bit serial or byte serial interface, and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (Z2, G1) are also accumulated. The S/UNI interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload. In addition to its basic processing of the received SONET/SDH overhead, the S/UNI provides convenient access to all overhead bytes, which are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead.

The S/UNI frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. The ATM cells that are passed are written to a four cell FIFO buffer. The received cells are read from the FIFO using a generic 9 bit wide or 17 bit wide datapath interface. Counts of received ATM cell headers that are errored and uncorrectable and also those that are errored and correctable are accumulated independently for performance monitoring purposes.

The S/UNI transmits SONET/SDH frames, via a bit serial or a byte serial interface, and formats section, line, and path overhead appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (Z2, G1) are also inserted. The S/UNI generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. In addition to its basic formatting of the transmitted SONET/SDH overhead, the S/UNI provides convenient access to all overhead bytes, which are optionally inserted from lower rate serial interfaces, allowing external sourcing of overhead. The S/UNI also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

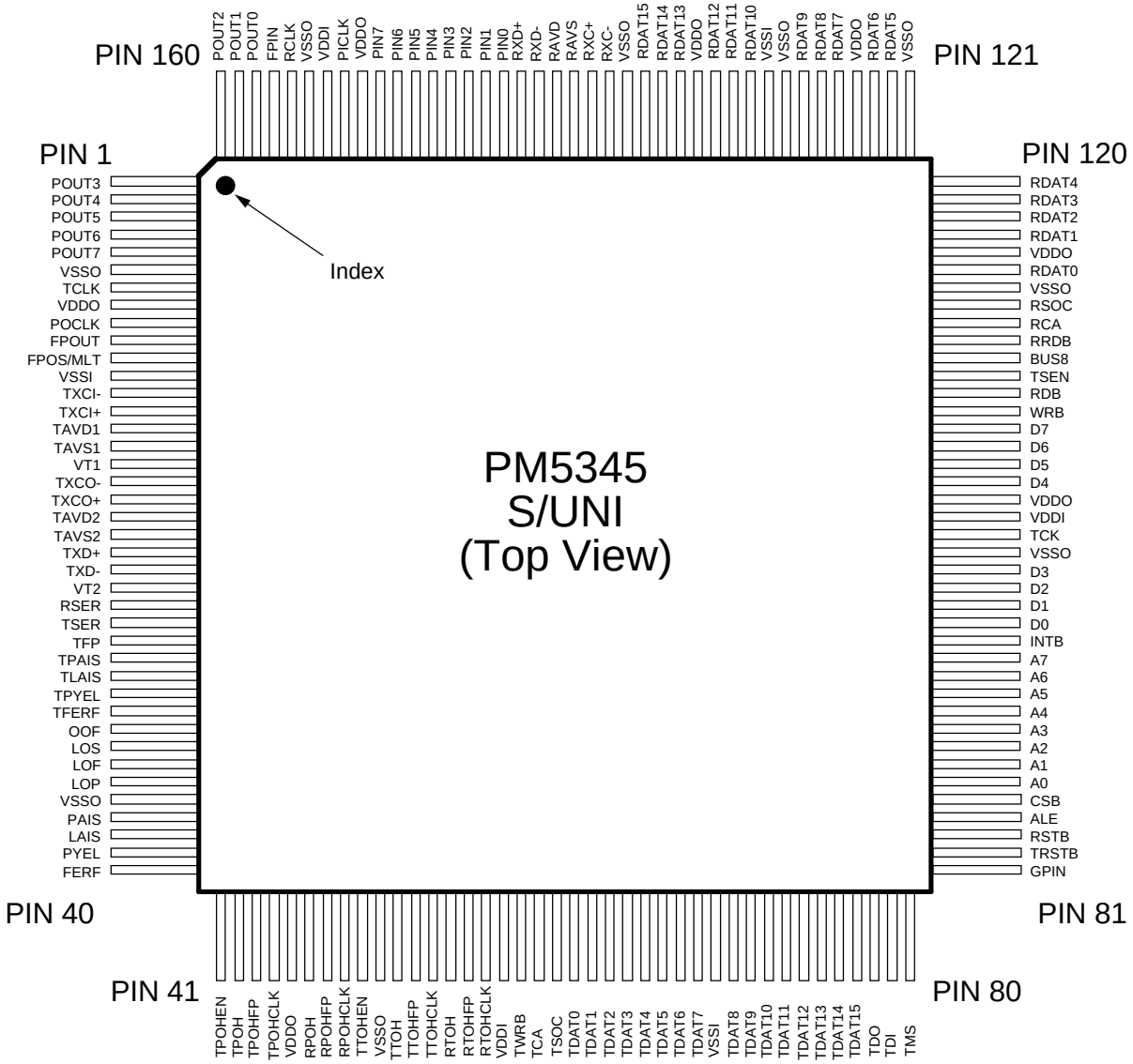
ATM cells are written to an internal four cell FIFO using a generic 9 bit wide or 17 bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. The S/UNI provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

No auxiliary clocks are required directly by the S/UNI as it operates from two 155.52 MHz clocks (bit serial line interface) or two 19.44 MHz clocks (byte serial interface). The S/UNI is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. The S/UNI also provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI is implemented in low power, +5 Volt, CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 160 pin PQFP package.

8 PIN DIAGRAM

The S/UNI is packaged in an 160 pin PQFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.65 mm.



9 PIN DESCRIPTION

Table 1 -

Pin Name	Type	Pin No.	Function
RSER	Input	25	The receive serial input (RSER) selects the receive line interface. RSER is tied high to select the 155.52 Mbit/s interface (on pins RXC+, RXC-, RXD+, and RXD-). RSER is tied low to select the 19.44 Mbyte/s interface (on pins PICLK, PIN[7:0], and FPIN).
RXD+ RXD-	Input	143 142	The receive differential data inputs (RXD+, RXD-) contain the 155.52 Mbit/s receive STS-3c (STM-1) stream when the bit serial interface is selected (RSER is tied high). RXD+/- is sampled on the rising edge of RXC+/- (the falling edge may be used by reversing RXC+/-).
RXC+ RXC-	Input	139 138	The receive differential clock inputs (RXC+, RXC-) contain the receive clock when the bit serial interface is selected (RSER is tied high). RXC+/- is nominally a 155.52 MHz, 50% duty cycle clock. This clock is divided by eight internally to produce RCLK when the bit serial interface is selected and provide timing for the S/UNI receive functions. RXD+/- is sampled on the rising edge of RXC+/-.

Pin Name	Type	Pin No.	Function
PICLK	I/O	153	The parallel input clock (PICLK) provides timing for sampling the received SONET STS-3c (STM-1) stream that is input by the S/UNI when the byte serial interface is selected (RSER is tied low). This clock provides timing for S/UNI receive function operation. PICLK is nominally a 19.44 MHz, 50% duty cycle clock. PIN[7:0] and FPIN are sampled on the rising edge of PICLK. RCLK is a buffered version of PICLK when the byte serial interface is selected. When the 155 Mbit/s serial interface is selected (RSER is tied high), PICLK becomes an output and must not be driven.
RX_VCLK			The test vector clock (RX_VCLK) signal is used during S/UNI production testing to verify internal functionality.
PIN[0] PIN[1] PIN[2] PIN[3] PIN[4] PIN[5] PIN[6] PIN[7]	Input	144 145 146 147 148 149 150 151	The data input (PIN[7:0]) bus carries the STS-3c (STM-1) stream when the byte serial interface is selected (RSER is tied low). PIN[7:0] is sampled on the rising edge of PICLK. PIN[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). PIN[0] is the least significant bit (corresponding to bit 8 of each word, the last bit transmitted).
FPOS/MLT	Input	11	The dual function input (FPOS/MLT) selects both the transmit encoding scheme and the receive frame pulse location depending on the line side interface selected using inputs TSER and RSER.

Pin Name	Type	Pin No.	Function
			When the byte serial receive interface is selected (RSER=0), the FPOS/MLT input selects the frame byte position in the SONET frame indicated by the FPIN input. When FPOS/MLT is tied high, a pulse on FPIN marks the third A2 framing byte position on the PIN[7:0] bus. When FPOS/MLT is tied low, a pulse on FPIN marks the first synchronous payload envelope byte position after the three C1 bytes on PIN[7:0]. When the bit serial transmit interface is selected (TSER=1), the FPOS/MLT input selects MLT-3 encoding of the transmit stream. When FPOS/MLT is tied high, an MLT-3 encoded data stream is transmitted on the TXCO+/- and TXD+/- outputs. When FPOS/MLT is tied low, 155 Mbit/s clock and data are inserted on the TXCO+/- and TXD+/- outputs.
FPIN	Input	157	The active high framing position input (FPIN) signal indicates the SONET frame position on the PIN[7:0] bus. The byte position indicated by FPIN is selected by the FPOS/MLT input as described above. FPIN is sampled on the rising edge of PICLK.
OOF	Output	32	The out of frame (OOF) signal is high while the S/UNI is out of frame. OOF is low while the S/UNI is in-frame. An out of frame occurs when 4 consecutive errored framing patterns (A1 and A2 bytes) have been received. OOF is intended to be used to enable an upstream framing pattern detector to search for the framing pattern when the byte serial interface is selected. This alarm indication is also available via register access. OOF is updated on the falling edge of RCLK.

Pin Name	Type	Pin No.	Function
RCLK	Output	156	The receive clock (RCLK) output provides a timing reference for S/UNI receive outputs. RCLK is a 19.44 MHz, nominally 50% duty cycle clock. RCLK is a buffered version of PICLK when the byte serial interface is selected (RSER is tied low). RCLK is a divide by eight of RXC+/- when the bit serial interface is selected (RSER is tied high).
TSER	Input	26	The transmit serial input (TSER) selects the transmit line interface. TSER is tied high to select the 155.52 Mbit/s interface (on pins TXCI+, TXCI-, TXCO+, TXCO-, TXD+, and TXD-). TSER is tied low to select the 19.44 Mbyte/s interface (on pins TCLK, FPOUT, and POUT[7:0]).
TXD+ TXD-	Output	22 23	The transmit differential data/positive pulse outputs (TXD+, TXD-) contain either NRZ or MLT-3 encoded data when the bit serial interface is selected (TSER is tied high). When NRZ encoding is selected (FPOS/MLT is tied low), the 155.52 Mbit/s transmit STS-3c (STM-1) stream TXD+/- is updated on the falling edge of TXCO+/-. When MLT-3 encoding is selected (FPOS/MLT is tied high), the TXD+/- outputs contain the positive pulses of the MLT-3 encoded stream.
TXCI+ TXCI-	Input	14 13	The transmit differential clock inputs (TXCI+, TXCI-) contain the transmit clock when the bit transmit serial interface is selected. TXCI+/- is nominally a 155.52 MHz, 50% duty cycle clock. This clock provides timing for the S/UNI transmit functions. TXCI+/- may be left unconnected when S/UNI loop timing is enabled (using the S/UNI Master Control Register).

Pin Name	Type	Pin No.	Function
TXCO+ TXCO-	Output	19 18	The transmit differential clock/negative pulse outputs (TXCO+, and TXCO-) contain either the transmit output clock or MLT-3 encoded data when the bit serial interface is selected (TSER is tied high). When NRZ encoding is selected (FPOS/MLT is tied low), TXCO+/- is a buffered version of TXCI+/-. TXD+/- is updated on the falling edge of TXCO+/-. When MLT-3 encoding is selected (FPOS/MLT is tied high), the TXCO+/- outputs contain the negative pulses of the MLT-3 encoded stream.
POCLK	Output	9	The parallel output clock (POCLK) signal provides timing for processing of the data that is output by the S/UNI. POCLK is nominally a 19.44 MHz, 50% duty cycle clock. POCLK is a buffered version of TCLK when the byte serial interface is selected (TSER is tied low). POCLK is a divide by eight of TXCI+/- when the bit serial interface is selected (TSER is tied high).
POUT[0] POUT[1] POUT[2] POUT[3] POUT[4] POUT[5] POUT[6] POUT[7]	Output	158 159 160 1 2 3 4 5	The scrambled data output (POUT[7:0]) bus carries data when the byte serial interface is selected (TSER is tied low). POUT[7:0] is updated on the rising edge of TCLK. POUT[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). POUT[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted).

Pin Name	Type	Pin No.	Function
FPOUT	Output	10	The active high framing position output (FPOUT) signal marks the frame alignment on the POUT[7:0] bus. FPOUT goes high for a single TCLK period while the first synchronous payload envelope byte after the three C1 bytes is present on POUT[7:0]. FPOUT is updated on the rising edge of TCLK.
LOS	Output	33	The loss of signal (LOS) signal is set high when loss of signal is declared. This occurs when a violating period (20 ± 3 µs) of consecutive all zeros bytes is detected on the incoming STS-3c(STM-1) signal (before descrambling). LOS is removed when two valid framing words (A1, A2) are detected and during the intervening time, no violating period of consecutive all zeros patterns is detected. This alarm indication is also available via register access. LOS is updated on the falling edge of RCLK.
LOF	Output	34	The loss of frame (LOF) signal is set high when loss of frame is declared. This occurs when an out-of-frame condition (as indicated by a high level on the OOF output) persists for a period of 3 ms. LOF is removed when an in-frame condition (as indicated by a low level on the OOF output) persists for a period of 3 ms. This alarm indication is also available via register access. LOF is updated on the falling edge of RCLK.

Pin Name	Type	Pin No.	Function
LAIS	Output	38	The line alarm indication signal (LAIS) is set high when line AIS is declared. This occurs when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. This alarm indication is also available via register access. LAIS is updated on the falling edge of RCLK.
FERF	Output	40	The line far end receive failure (FERF) signal is set high when line FERF is declared. This occurs when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. FERF is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. This alarm indication is also available via register access. FERF is updated on the falling edge of RCLK.
LOP	Output	35	The loss of pointer (LOP) signal is set high when loss of pointer is declared. This occurs when a valid pointer (H1, H2) is not found in eight consecutive frames, or if eight consecutive new data flags are detected. LOP is removed when the same valid and normal pointer with a normal new data flag is detected in three consecutive frames. The loss of pointer state is not entered if the incoming stream contains path AIS. This alarm indication is also available via register access. LOP is updated on the falling edge of RCLK.

Pin Name	Type	Pin No.	Function
PAIS	Output	37	The path AIS (PAIS) signal is set high when STS-path AIS is declared. This occurs when an all ones pattern is observed in the pointer bytes (H1, H2) for three consecutive frames. Path AIS is removed when the same valid and normal pointer is detected for three consecutive frames or a legal pointer with an active NDF is received. This alarm indication is also available via register access. PAIS is updated on the falling edge of RCLK.
PYEL	Output	39	The path yellow (PYEL) signal is set high when STS-path yellow alarm is declared. This occurs when bit 5 of the path status byte (G1) is set high for ten consecutive frames. Path yellow is removed when bit 5 of the G1 byte is set low for ten consecutive frames. This alarm indication is also available via register access. PYEL is updated on the falling edge of RCLK.
TLAIS	Input	29	The active high transmit line alarm indication (TLAIS) signal controls the insertion of line AIS. Line AIS is inserted by overwriting the SONET/SDH frame contents with all ones (before scrambling). The section overhead is not overwritten. This function can also be performed via register access. Line AIS insertion is internally synchronized to frame boundaries. The TLAIS input takes precedence over the TTOH and TTOHEN inputs. TLAIS is sampled on the rising edge of POCLK.

Pin Name	Type	Pin No.	Function
TFERF	Input	31	The active high transmit line far end receive failure (TFERF) signal controls the insertion of line FERF. Line FERF is inserted by transmitting the code 110 (binary) in bit positions 6,7, and 8 of the K2 byte. This function can also be performed via register access, or be enabled to occur automatically upon detection of receive line AIS, loss of signal, or loss of frame. The TFERF input takes precedence over the TTOH and TTOHEN inputs. TFERF is sampled on the rising edge of POCLK.
TPAIS	Input	28	The active high transmit path alarm indication (TPAIS) signal controls the insertion of STS-path AIS. A high level on TPAIS forces the insertion of an all ones pattern into the complete synchronous payload envelope, and the payload pointer bytes (H1, H2). Path AIS insertion is internally synchronized to SPE frame boundaries. This function can also be performed via register access. TPAIS is sampled on the rising edge of POCLK.
TPYEL	Input	30	The transmit path yellow alarm (TPYEL) signal controls the insertion of path yellow alarm. A high level on TPYEL forces a logic one to be inserted in the path yellow bit position in the path status byte (G1). This function can also be performed via register access, or be enabled to occur automatically upon detection of receive line AIS, loss of frame, loss of signal, loss of pointer, or STS-path AIS. The TPOH and TPOHEN inputs take precedence over the TPYEL input. TPYEL is sampled on the rising edge of POCLK.

Pin Name	Type	Pin No.	Function
TSEN	Input	109	The tristate enable (TSEN) input selects the configuration of the receive datapath (RDAT[15:0]). When TSEN is tied high, RDAT[15:0] normally operates as a tristate bus controlled by RRDB. When RRDB is high, RDAT[15:0] is tristated. When RRDB is low, RDAT[15:0] is enabled. When TSEN is tied low, RDAT[15:0] normally operates as an output bus, and is always enabled, regardless of the state of RRDB
BUS8	Input	110	The bus width select (BUS8) input selects the transmit and receive datapath widths. When BUS8 is tied high, a 9-bit interface consisting of a start of cell indication, and an 8-bit octet bus is selected. When BUS8 is tied low, a 17-bit interface consisting of a start of cell indication, and a 16-bit word bus is selected.
RRDB	Input	111	The active low receive read strobe (RRDB) is used to read ATM cells from the receive FIFO. When active, RRDB must cycle at a 25 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow. RSOC is updated on the rising edge of RRDB. RDAT[15:0] are updated on the falling edge of RRDB.

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Tristate	115 117 118 119 120 122 123 125 ``•` ```` `ü`` ```• ```` ``ü` ```` •```	```ü`````•`````ü`````•`````ü`````•`````ü`````•`````ü `````````••••at are read from the receive FIFO. When the 17-bit datapath is selected (BUS8 is tied low), RDAT[15:0] contains the 16-bit wide word bus. When the 9-bit datapath is selected (BUS8 is tied high), RDAT[7:0] contains the 8-bit wide word bus (RDAT[15:8] is not used). The RDAT[15:0] bus is tristated while RRDB is high, and TSEN is high. The RDAT[15:0] bus is always driven when TSEN is low, regardless of the level of RRDB. RDAT[15:0] is updated on the falling edge of RRDB.
RSOC	Output	113	The receive start of cell (RSOC) signal marks the start of cell on the RDAT[15:0] bus. When RSOC is high, the first word of the selected data structure is present on the RDAT[15:0] stream. RSOC is updated on the rising edge of RRDB.
RCA	Output	112	The receive cell available (RCA) signal indicates when a cell is available in the receive FIFO. The low to high transition of RCA (indicating that the receive FIFO is not empty) occurs on the falling edge of RCLK. The high to low transition of RCA (indicating that the receive FIFO is empty) occurs on the falling edge of RRDB. The active polarity of this signal is programmable and defaults to active high.

Pin Name	Type	Pin No.	Function
TCLK	I/O	7	The transmit clock (TCLK) provides timing for S/UNI transmit function operation when the byte serial interface is selected (TSER is tied low). TCLK must be a 19.44 MHz, nominally 50% duty cycle clock. POCLK is a buffered version of TCLK when byte serial interface is selected. When the 155 Mbit/s serial interface is selected (TSER is tied high), TCLK becomes an output and should not be driven.
TX_VCLK			The test vector clock (TX_VCLK) signal is used during S/UNI production testing to verify internal functionality.
TFP	Input	27	The active high transmit frame pulse (TFP) signal is used to align the SONET/SDH transport frame generated by the S/UNI device to a system reference when the byte serial interface is selected (TSER is low). TFP should be brought high for a single TCLK period every 2430 TCLK cycles or a multiple thereof. TFP may be tied low if such synchronization is not required. The offset between an active TFP input and the resultant FPOUT pulse is 24 TCLK periods. TFP is sampled on the rising edge of TCLK.
TWRB	Input	58	The transmit write strobe (TWRB) is used to write ATM cells to the four cell transmit FIFO. When active, TWRB cycles at a 25 MHz or lower instantaneous rate. A complete 53 octet cell must be written to the FIFO before being inserted in the STS-3c (STM-1) SPE. Idle/unassigned cells are inserted when a complete cell is not available. TDAT[15:0] and TSOC are sampled on the rising edge of TWRB.

Pin Name	Type	Pin No.	Function
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	Input	61 62 63 64 65 66 67 68 70 71 72 73 74 75 76 77	The transmit cell data (TDAT[15:0]) bus carries the ATM cell octets that are written to the transmit FIFO. When the 17-bit datapath is selected (BUS8 is tied low), TDAT[15:0] contains the 16-bit wide word bus. When the 9-bit datapath is selected (BUS8 is tied high), TDAT[7:0] contains the 8-bit wide octet bus (TDAT[15:8] is not used). TDAT[15:0] is sampled on the rising edge of TWRB.
TSOC	Input	60	The transmit start of cell (TSOC) signal marks the start of cell on the TDAT[15:0] bus. When TSOC is high, the first word of the selected data structure is present on the TDAT[15:0] stream. It is not necessary for TSOC to be present at each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the selected data structure. TSOC is sampled on the rising edge of TWRB.

Pin Name	Type	Pin No.	Function
TCA	Output	59	The transmit cell available (TCA) signal indicates when a cell is available in the transmit FIFO. The low to high transition of TCA (indicating that the transmit FIFO is not full) occurs on the falling edge of POCLK. The high to low transition of TCA (indicating that the transmit FIFO is full) occurs on the falling edge of TWRB. The active polarity of this signal is programmable and defaults to active high.
RTOH	Output	54	The receive transport overhead data (RTOH) signal contains the receive transport overhead bytes (A1, A2, C1, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1, Z2, and E2) extracted from the received SONET/SDH frame. RTOH is updated on the falling edge of RTOHCLK.
RTOHCLK	Output	56	The receive transport overhead clock (RTOHCLK) is nominally a 5.184 MHz clock which provides timing to process the extracted receive transport overhead. RTOHCLK is a gapped 6.48 MHz clock. RTOHCLK is updated on the falling edge of RCLK.
RTOHFP	Output	55	The receive transport overhead frame position (RTOHFP) signal may be used to locate the individual receive transport overhead bits in the transport overhead data stream, RTOH. RTOHFP is logic one while bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH stream. RTOHFP is updated on the falling edge of RTOHCLK.
RPOH	Output	46	The receive path overhead data (RPOH) signal contains the path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the received STS-3c (STM-1) frame. RPOH is updated on the falling edge of RPOHCLK.

Pin Name	Type	Pin No.	Function
RPOHCLK	Output	48	The receive path overhead clock (POHCLK) is nominally a 576 kHz clock which provides timing to process the extracted receive path overhead. RPOHCLK is a gapped 2.16 MHz clock. RPOHCLK is updated on the falling edge of RCLK.
RPOHFP	Output	47	The receive path overhead frame position (RPOHFP) signal may be used to locate the individual receive path overhead bits in the path overhead data stream, RPOH. RPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is present in the RPOH stream. RPOHFP is updated on the falling edge of RPOHCLK.
TTOH	Input	51	The transmit transport overhead data (TTOH) signal contains the transport overhead bytes (A1, A2, C1, E1, F1, D1-D3, K1, K2, D4-D12, Z1, Z2, and E2) and error masks (B1, B2, H1, and H2) which may be inserted, or used to insert section/line BIP or payload pointer bit errors into the transport overhead byte positions transmit STS-3c (STM-1) stream. Insertion is controlled by the TTOHEN input, or by bits in internal registers. TTOH is sampled on the rising edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TTOHEN	Input	49	The transmit transport overhead insert enable (TTOHEN) signal, together with internal register bits, controls the source of the transport overhead data which is transmitted. While TTOHEN is high, values sampled on the TTOH input are inserted into the corresponding transport overhead bit position (for the A1, A2, C1, E1, F1, D1-D3, K1, K2, H3, D4-D12, Z1, Z2, and E2 bytes). While TTOHEN is low, default values are inserted into these transport overhead bit positions. A high level on TTOHEN during the B1, B2 or H1-H2 bit positions enables an error mask. While the error mask is enabled, a high level on input TTOH causes the corresponding B1, B2 or H1-H2 bit position to be inverted. A low level on TTOH allows the corresponding bit position to pass through the S/UNI uncorrupted. TTOHEN is sampled on the rising edge of TTOHCLK.
TTOHCLK	Output	53	The transmit transport overhead clock (TTOHCLK) is nominally a 5.184 MHz clock which provides timing for upstream circuitry that sources the transport overhead stream, TTOH. TTOHCLK is a gapped 6.48 MHz clock. TTOHCLK is updated in the falling edge of POCLK.
TTOHFP	Output	52	The transmit transport overhead frame position (TTOHFP) signal may be used to locate the individual transport overhead bits in the transport overhead data stream, TTOH. TTOHFP is logic one while bit 1 (the most significant bit) of the first framing byte (A1) is expected in the TTOH stream. TTOHFP is updated on the falling edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TPOH	Input	42	The transmit path overhead data (TPOH) signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) and error masks (B3, and H4) which may be inserted, or used to insert path BIP-8 or multiframe bit errors into the path overhead byte positions in the STS-3c (STM-1) stream. Insertion is controlled by the TPOHEN input, or by bits in internal registers. TPOH is sampled on the rising edge of TPOHCLK.
TPOHEN	Input	41	The transmit path overhead insert enable (TPOHEN) signal, together with internal register bits, controls the source of the path overhead data which is inserted in the POUT[7:0] stream. While TPOHEN is high, values sampled on the TPOH input are inserted into the corresponding path overhead bit position (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). While TPOHEN is low, values obtained from internal registers are inserted into these path overhead bit positions. A high level on TPOHEN during the H4 or B3 bit positions enables an error mask. While the error mask is enabled, a high level on input TPOH causes the corresponding B3 or H4 bit position to be inverted. A low level on TPOH allows the corresponding bit position to pass through the S/UNI uncorrupted. TPOHEN is sampled on the rising edge of TPOHCLK.
TPOHCLK	Output	44	The transmit path overhead clock (TPOHCLK) is nominally a 576 kHz clock which provides timing for upstream circuitry that sources the path overhead stream, TPOH. TPOHCLK is a gapped 2.16 MHz clock. TPOHCLK is updated in the falling edge of POCLK.

Pin Name	Type	Pin No.	Function
TPOHFP	Output	43	The transmit path overhead frame position (TPOHFP) signal may be used to locate the individual path overhead bits in the path overhead data stream, TPOH. TPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is expected in the TPOH stream. TPOHFP is updated on the falling edge of TPOHCLK.
GPIN	Input	81	The general purpose input (GPIN) signal may be used to monitor the state of an external alarm or status point (such as a lock detect alarm from an external PMD). An interrupt may be enabled when this signal changes state. GPIN may be asynchronous but should be glitch free. GPIN has an integral pull down resistor.
CSB	Input	85	The active low chip select (CSB) signal is low during S/UNI register accesses. If register accesses are controlled using only the RDB and WRB signals, CSB should be connected to an inverted version of the RSTB input.
RDB	Input	108	The active low read enable (RDB) signal is low during S/UNI register read accesses. The S/UNI drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	107	The active low write strobe (WRB) signal is low during a S/UNI register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.

Pin Name	Type	Pin No.	Function
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	95 96 97 98 103 104 105 106	The bidirectional data bus D[7:0] is used during S/UNI register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]/TRS	Input	86 87 88 89 90 91 92 93	The address bus A[7:0] selects specific registers during S/UNI register accesses. The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS has an integral pull down resistor.
RSTB	Input	83	The active low reset (RSTB) signal provides an asynchronous S/UNI reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	84	The address latch enable (ALE) is active high and latches the address bus A[7:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
INTB	OD Output	94	The active low interrupt (INTB) signal goes low when a S/UNI interrupt source is active, and that source is unmasked. The S/UNI may be enabled to report many alarms or events via interrupts. Examples are loss of signal (LOS), loss of frame (LOF), line AIS, line far end receive failure (FERF), loss of pointer (LOP), path AIS, path yellow, and many others. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
TCK	Input	100	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	80	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	79	The test data input (TDI) signal carries test data into the S/UNI via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate	78	The test data output (TDO) signal carries test data out of the S/UNI via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	82	The active low test reset (TRSTB) signal provides an asynchronous S/UNI test access port reset via the IEEE P1149.1 test access port. If the JTAG port is not used, TRSTB should be tied to RSTB for proper operation. TRSTB has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
VDDI1 VDDI2 VDDI3	Power	57 101 154	The core power (VDDI1 - VDDI3) pins should be connected to a well decoupled +5 V DC in common with VDDO.
VSSI1 VSSI2 VSSI3	Ground	12 69 129	The core ground (VSSI1 - VSSI3) pins should be connected to GND in common with VSSO.
VDDO1 VDDO2 VDDO3 VDDO4 VDDO5 VDDO6 VDDO7	Power	8 45 102 116 124 133 152	The pad ring power (VDDO1 - VDDO7) pins should be connected to a well decoupled +5 V DC in common with VDDI.
VSSO1 VSSO2 VSSO3 VSSO4 VSSO5 VSSO6 VSSO7 VSSO8 VSSO9	Ground	6 36 50 99 114 121 128 137 155	The pad ring ground (VSSO1 - VSSO9) pins should be connected to GND in common with VSSI.
VT1	Input	17	The transmit PECL logic high reference (VT1) pin must be connected to GND.

Pin Name	Type	Pin No.	Function
VT2	Input	24	The transmit PECL logic low reference (VT2) pin is used to control the logic low voltage level of the output PECL pins, TXCO+/- and TXD+/-. VT2 should be connected to TAVD1 through a reference resistor. The PECL outputs can be used in a 50Ω controlled impedance environment. Under these conditions, the reference resistor value is recommended to be 630Ω, ±1%. Additional details are provided in the Interface Examples section.
TAVD1	Ref	15	The reference (TAVD1) pin for the transmit PECL circuitry. TAVD1 should be connected to the Transmit Analog Reference Supply.
TAVS1	Ground	16	The ground (TAVS1) pin for the transmit PECL circuitry. TAVS1 should be connected to GND.
TAVD2	Power	20	The power (TAVD2) pin for the transmit PECL driver pads TAVD2 should be connected to the PECL Driver Supply (normally the +5V D.C. digital supply).
TAVS2	Ground	21	The ground (TAVS2) pin for the transmit PECL driver pads TAVS2 should be connected to GND.
RAVD	Ref	141	The reference (RAVD) pin for the receive PECL circuitry. RAVD should be connected to the Receive Analog Reference Supply.
RAVS	Ground	140	The ground (RAVS) pin for the receive PECL circuitry RAVS should be connected to GND.

Notes on Pin Description:

1. All S/UNI inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except for the TXCI+, TXCI-, RXC+, RXC-, RXD+, and RXD- differential inputs which operate at pseudo ECL (PECL) logic levels.

2. Most S/UNI digital outputs and bidirectionals have 4 mA drive capability, except the POCLK and RCLK outputs which have 8 mA drive capability. All 4

mA and 8 mA outputs are slew rate limited except for the FIFO interface outputs RSOC, RDAT[15:0], RCA and TCA. Differential outputs TXCO+, TXCO-, TXD+, TXD- operate at pseudo ECL (PECL) logic levels.

3. The VSSO and VSSI ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI.

4. The VDDO and VDDI power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI.

10 FUNCTIONAL DESCRIPTION

10.1 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received 155.52 Mbit/s SONET stream to a 19.44 Mbyte/s stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the incoming stream, and performs serial to parallel conversion on octet boundaries.

10.2 Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring.

10.2.1 Framer

The Framer Block determines the in-frame/out-of-frame status of the STS-3c data stream. Output OOF reflects this status, and is updated with timing aligned to RCLK.

While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out-of-frame, upstream circuitry (the SIPO block or an external serial to parallel converter depending on the interface selected using the RSER input) monitors the bit serial STS-3c data stream for an occurrence of the framing pattern. A high level on input FPIN (when the byte serial interface is selected) reinitializes the channel counter to the new frame alignment. The Framer Block verifies that an error free framing pattern is present in the next frame before declaring in-frame.

10.2.2 Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the received byte serial stream. The generating polynomial is $1 + x^6 + x^7$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the identity bytes (C1) are not descrambled. A register bit is provided to disable the descrambling operation.

10.2.3 Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-3c frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16 bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

10.2.4 Loss of Signal

The Loss of Signal Block monitors the scrambled data of the complete STS-3c stream for the absence of 1's. When 20 ± 3 µs of all zeros patterns is detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. LOS is updated with timing aligned to RCLK.

10.2.5 Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. To provide for intermittent out-of-frame conditions, the 3 ms timer is not reset to zero until an in-frame condition persists for 3 ms. The loss of frame is cleared when an in frame condition persists for a period of 3 ms. LOF is updated with timing aligned to RCLK.

10.3 Receive Line Overhead Processor

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring.

10.3.1 FERF Detect

The FERF Detect Block detects the presence of Line Far End Receive Failure in the STS-3c stream. Output FERF is asserted when a 110 binary pattern is

detected in bits 6, 7, and 8 of the K2 byte, for five consecutive frames. FERF is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. FERF is updated with timing aligned to RCLK.

10.3.2 Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (AIS) in the STS-3c stream. Output LAIS is asserted when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte, for five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. LAIS is updated with timing aligned to RCLK.

10.3.3 Error Monitor

The Error Monitor Block calculates the received line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the STS-3c (STM-1) stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-24 code is compared with the BIP-24 code extracted from the STS-3c (STM-1) of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (3 x 8 x 8000) bit errors can be detected per second in an STS-3c (STM-1).

The Error Monitor Block accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, this counter should be polled at least once per second to avoid saturation which in turn may result in missed bit error events.

The Error Monitor Block also accumulates line far end block error indications (contained in the Z2 byte) in a similar manner.

10.4 Transport Overhead Extract Port

The Transport Overhead Extract Port (also known as the Receive Transport Overhead Access Port, RTOP) extracts the 81 bytes of receive transport overhead and serializes them at 5.184 Mbit/s on RTOH for optional external processing.

Output RTOHFP is provided to identify the most significant bit of the A1 framing byte on RTOH. The transport overhead clock, RTOHCLK is nominally a 5.184 MHz clock. RTOH and RTOHFP are updated with timing aligned to RTOHCLK. In turn, RTOHCLK is updated with timing aligned to RCLK.

10.5 Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm and performance monitoring.

10.5.1 Pointer Interpreter

The Pointer Interpreter Block interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead in the incoming STS-3c (or STM-1) stream (the J1 byte).

1. A "normal pointer value" locates the start of the SPE. Note: $0 \leq$ "normal pointer value" ≤ 782, and the new data flag (NDF) field is set to 0110.

2. Any variation from the "normal pointer value" is ignored unless a consistent new value is received three times consecutively, or the new value conforms to one of rules 3, 4, or 5.

3. If the majority of the I-bits of the pointer word are inverted, a positive stuff operation is indicated. The SPE is not present during the three positive stuff opportunity byte positions, and the pointer value is incremented by one.

4. If the majority of the D-bits of the pointer word are inverted, a negative stuff operation is indicated. The SPE is present during the three negative stuff opportunity byte positions, the H3 bytes, and the pointer value is decremented by one.

5. If the NDF field of the pointer is set to 1001 (at least three of the four bits matching), then the coincident pointer value (if normal) replaces the current pointer value at the offset indicated by the new pointer value.

The Pointer Interpreter Block detects loss of pointer (LOP) in the incoming STS-3c or STM-1 stream. The LOP signal is set high when a "normal pointer value" (according to the rules described above) is not found in eight consecutive frames. The LOP signal is set low when a "normal pointer value" is detected in three consecutive frames. Incoming STS Path AIS (H1 and H2 set to all ones) does not cause entry into the LOP state. LOP is updated with timing aligned to RCLK.

The Pointer Interpreter Block detects path AIS in the incoming STS-3c or STM-1 stream. The PAIS signal is set high when an all ones pattern is detected in the pointer bytes (H1 and H2) for three consecutive frames. The PAIS signal is set low when a valid pointer is detected for three consecutive frames. PAIS is updated with timing aligned to RCLK.

The pointer value is used to extract the path overhead from the incoming stream.

10.5.2 SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes and to downstream circuitry to extract the ATM cell payload.

10.5.3 Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBE). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path yellow alarm is detected by extracting bit 5 of the path status byte. The PYEL signal is set high when bit 5 is set high for ten consecutive frames. PYEL is set low when bit 5 is low for ten consecutive frames. PYEL is updated with timing aligned to RCLK.

10.5.4 Path FERF Detect

The Path FERF Detect block monitors the receive path status byte (G1) for the path FERF indication. Path FERF is declared when the 4-bit FEBE field is set to 1001 binary for two consecutive G1 bytes. Path FERF is removed when the 4-bit FEBE field is not set to 1001 hexadecimal for two consecutive G1 bytes.

10.6 Path Overhead Extract

The Path Overhead Extract Block uses timing information from the SPE Timing block to extract, serialize and output the Path Overhead bytes on output RPOH. Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) on RPOH. The path overhead clock, RPOHCLK is nominally a 576 kHz clock. RPOH and RPOHFP are updated with timing aligned to RPOHCLK. In turn, RPOHCLK is updated with timing aligned to RCLK.

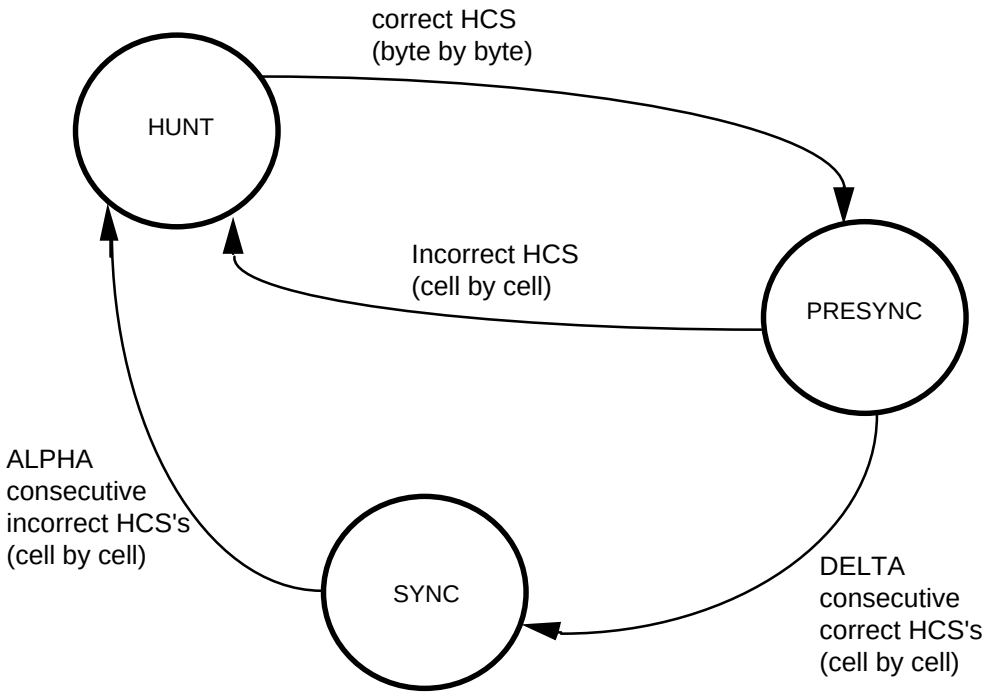
10.7 Receive ATM Cell Processor

The Receive ATM Cell Processor (RACP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. The RACP also provides a four cell deep receive FIFO. This FIFO passes data structures consisting of either 27 16-bit words, or 53 8-bit words and is used to separate the STS-3c line timing from the higher layer ATM system timing.

10.7.1 Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells must be byte aligned before insertion in the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates one at a time to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary and enters the PRESYNC state. This state validates the cell boundary location. If the cell boundary is invalid then an incorrect HCS will be received within the next DELTA cells, at which point a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period then the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 6.

Figure 6 - Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in a maximum average time to delineate of 31 µs.

10.7.2 Descrambler

The self synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the '$x^{43} + 1$' polynomial. The descrambler is disabled for the duration of the header and HCS fields, and may optionally be disabled.

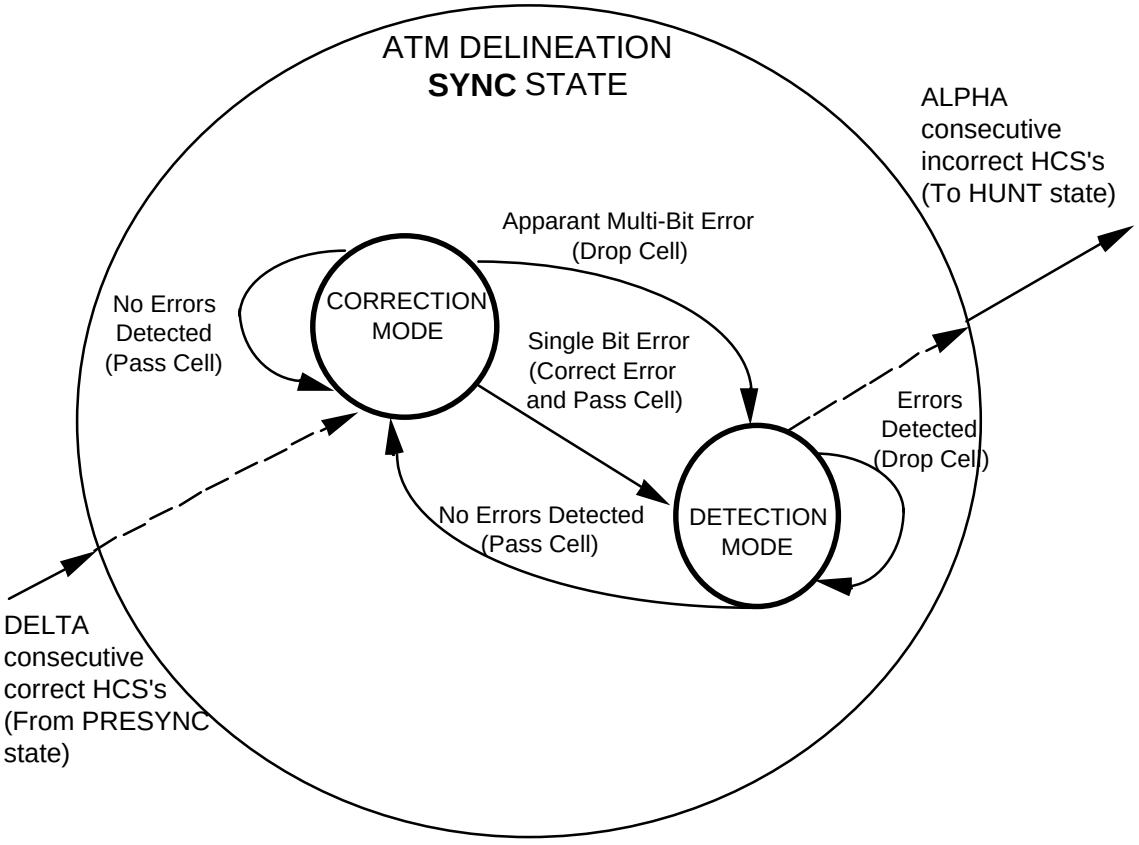
10.7.3 Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RACP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the

corrected header contents match the pattern contained in the 'Match Header Pattern' and 'Match Header Mask' registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the 'Match Header Pattern' and 'Match Header Mask' registers. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The 'Match Header Pattern' and 'Match Header Mask' registers allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RACP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result. While the cell delineation state machine (described above) is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 7:

Figure 7 - HCS Verification State Diagram



In normal operation, the HCS verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single bit error or a multi bit error, the state machine transitions to the 'Detection Mode' state. In this state, the detection of any HCS error causes the corresponding cell to be dropped. Cells containing an error-free HCS are passed, and the state machine transitions back to the 'Correction Mode' state.

10.7.4 Performance Monitor

The Performance Monitor consists of two 8-bit saturating HCS error event counters. One of the counters accumulates correctable HCS errors (that is single HCS bit errors detected while the HCS Verification state machine is in the 'Correction Mode' state described above). The second counter accumulates uncorrectable HCS errors (that is HCS bit errors detected while the HCS Verification state machine is in the 'Detection Mode' state or multiple HCS bit errors detected while the state machine is in the 'Correction Mode' state as described above).

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss HCS error events.

10.7.5 Receive FIFO

The Receive FIFO provides FIFO management and the asynchronous interface between the S/UNI device and the external environment. The receive FIFO can accommodate four cells. The receive FIFO provides for the separation of the STS-3c line or physical layer timing from the ATM layer timing.

The FIFO supports two data structures. The first data structure consists of 27 16-bit words comprising the 5 octet cell header and the 48 octet payload (the HCS byte, along with the header status octet, is passed in this structure). Note that depending on the selected cell filtering options, the header status may be one of the following 1) error-free header, 2) errored and corrected header, or 3) errored and uncorrectable header. The second data structure consists of 53 8-bit words, comprising the 5 octet cell header, and the 48 octet payload.

Management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun or underrun condition, the FIFO is automatically reset. Up to four cells may be lost during the FIFO reset operation. FIFO overruns and underruns are indicated through a maskable interrupt and register bits. The synchronous interface provided to an external device indicates the start of a cell (RSOC) when data is read from the receive FIFO (using RRDB). The asynchronous interface provided to an external device indicates the cell available status (RCA). The cell available status changes from unavailable to available on write cell boundaries with timing derived from the receive line clock (RCLK). The FIFO status changes from available to unavailable on read cell boundaries with timing aligned to the receive read clock (RRDB).

10.8 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the internal 19.44 Mbyte/s STS-3c (STM-1) stream to a 155.52 Mbit/s stream.

10.9 Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion.

10.9.1 Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled by the TLAIS input or through an internal register accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

10.9.2 BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the unscrambled STS-3c (STM-1) stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3c frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling.

BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.9.3 Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) and identity bytes (C1) into the STS-3c (STM-1) frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

10.9.4 Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit serial stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $1 + x^6 + x^7$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled.

The POUT[7:0] outputs are provided by the Scrambler Block and are updated with timing aligned to TCLK. It also provides the FPOUT signal. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

10.10 Transmit Line Overhead Processor

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, and line BIP-24 insertion (B2).

10.10.1 BIP-24 Calculate

The BIP-24 Calculate Block calculates the line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the STS-3c (STM-1) stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-24 code is inserted into the B2 byte positions of the following frame. BIP-24 errors may be continuously inserted under register control for diagnostic purposes.

10.10.2 Line FERF Insert

The Line FERF Insert Block multiplexes the line overhead bytes into the STS-3c (STM-1) output stream and optionally inserts line FERF. Line FERF is inserted by this block when enabled via the TFERF input, or register control. Line FERF

is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the STS-3c stream.

10.10.3 Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP-24 errors (Z2) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit Z2 byte.

10.11 Transport Overhead Insert Port

The Transport Overhead Insert Port (also known as the Transmit Transport Overhead Access Port, TTOP) optionally inserts the 81 bytes of transmit transport overhead from a data stream received serially at 5.184 Mbit/s on TTOH from optional external sources. The TTOHFP output is provided to identify when the most significant bit of the A1 framing byte is expected on TTOH. An enable signal, TTOHEN, is provided to allow per byte control of such optional transport overhead insertion.

The state of the TTOHEN input determines whether the data sampled on TTOH, or the default overhead byte values (shown in figure 5) are inserted in the STS-3c (STM-1) stream. For example, a high level on TTOHEN during the section user channel (F1) bit positions causes the eight values shifted in on TTOH to be inserted in the F1 byte position in the STS-3c stream. A low level on TTOHEN during the section user channel bit positions causes the default value (0x00) to be inserted in the STS-3c stream. Other combinations are also possible.

During the H1, H2, B1 and B2 byte positions in the TTOH stream, a high level on TTOHEN enables an error insertion mask. While the error mask is enabled, a high level on input TTOH causes the corresponding bit in the H1, H2, B1 or B2 byte to be inverted. A low level on TTOH causes the corresponding bit in the B1 or B2 byte to pass through the S/UNI uncorrupted.

Figure 8 - Default Transport Overhead Values

A1 (0xF6)	A1 (0xF6)	A1 (0xF6)	A2 (0x28)	A2 (0x28)	A2 (0x28)	C1 (0x01)	C1 (0x02)	C1 (0x03)
B1 (*)	(0x00)	(0x00)	E1 (0x00)	(0x00)	(0x00)	F1 (0x00)	(0x00)	(0x00)
D1 (0xFF)	(0x00)	(0x00)	D2 (0xFF)	(0x00)	(0x00)	D3 (0xFF)	(0x00)	(0x00)
H1 (*)	H1 (0x93)	H1 (0x93)	H2 (*)	H2 (0xFF)	H2 (0xFF)	H3 (0x00)	H3 (0x00)	H3 (0x00)
B2 (*)	B2 (*)	B2 (*)	K1 (0x00)	(0x00)	(0x00)	K2 (0x00)	(0x00)	(0x00)
D4 (0xFF)	(0x00)	(0x00)	D5 (0xFF)	(0x00)	(0x00)	D6 (0xFF)	(0x00)	(0x00)
D7 (0xFF)	(0x00)	(0x00)	D8 (0xFF)	(0x00)	(0x00)	D9 (0xFF)	(0x00)	(0x00)
D10 (0xFF)	(0x00)	(0x00)	D11 (0xFF)	(0x00)	(0x00)	D12 (0xFF)	(0x00)	(0x00)
Z1 (0x00)	Z1 (0x00)	Z1 (0x00)	Z2 (0x00)	Z2 (0x00)	Z2 (*)	E2 (0x00)	(0x00)	(0x00)

*** : B1, B2 values depend on payload contents**
H1, H2 values depend on startup conditions
Z2 value depends on incoming line bit errors

10.12 Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion, insertion of the synchronous payload envelope, insertion of path level alarm signals and path BIP-8 (B3) insertion.

10.12.1 Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2). The block contains a free running timeslot counter that locates the start of the

synchronous payload envelope based on the generated pointer value and the SONET/SDH frame alignment.

The Pointer Generator Block generates the outgoing pointer as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer bytes. **BIP-8 Calculate**

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the outgoing STS-3c (STM-1) stream. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.12.3 FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. The asynchronous nature of these signals implies that more than eight FEBE events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining FEBEs are transmitted at the next opportunity. Far end block errors may be inserted under register control for diagnostic purposes.

10.12.4 Path FERF Insert

The Path FERF Insert block is used to insert the Path FERF indication into the Path Status (G1) byte. Under register control, the 1001 binary Path FERF indicator can be inserted into the FEBE field of the G1 byte. Path FERF insertion takes precedence over both path overhead insertion by the Path Overhead Insert block and FEBE code insertion by the FEBE Calculate block.

10.12.5 SPE Multiplexer

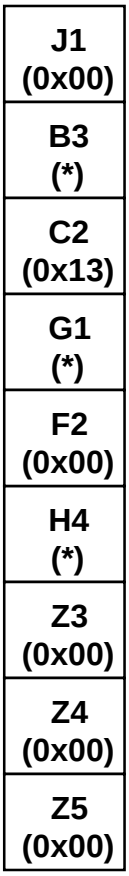
The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the STS-3c (STM-1) stream.

10.13 Path Overhead Insert

The Path Overhead Insert Block provides a bit serial path overhead interface to the TPOP. Any, or all of the path overhead bytes may be sourced from, or modified by the bit serial path overhead stream, TPOH. The individual bits of each path overhead byte are shifted in using the TPOHCLK output. The TPOHFP output is provided to identify when the most significant bit of the Path Trace byte is expected on TPOH. The state of the TPOHEN input, together with an internal register, determines whether the data sampled on TPOH, or the default path overhead byte values (shown in the table below) are inserted in the STS-3c (STM-1) stream. For example, a high level on TPOHEN during the path trace (J1) bit positions causes the eight values shifted in on TPOH to be inserted in the J1 byte position in the STS-3c stream. A low level on TPOHEN during the path trace bit positions causes the default value (0x00) to be inserted in the STS-3c stream. Other combinations are also possible.

During the B3 and H4 byte positions in the TPOH stream, a high level on TPOHEN enables an error insertion mask. While the error mask is enabled, a high level on input TPOH causes the corresponding bit in the B3 or H4 byte to be inverted. A low level on TPOH causes the corresponding bit in the B3 or H4 byte to pass through the TPOP uncorrupted.

Figure 9 - Default Path Overhead Values



*** : B3 value depend on payload contents**
G1 value depends on incoming path bit errors
H4 value depends on cell boundary offset

10.14 Transmit ATM Cell Processor

The Transmit ATM Cell Processor (TACP) inserts H4 framing, provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. The TACP contains a four cell transmit FIFO. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the FIFO.

10.14.1 Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

10.14.2 Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self synchronous scrambler described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be completely disabled.

10.14.3 HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1 is used. The coset polynomial, $x^6+x^4+x^2+1$ is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

10.14.4 Transmit FIFO

The Transmit FIFO provides FIFO management and the asynchronous interface between the S/UNI device and the external environment. The transmit FIFO can accommodate four cells. It provides for the separation of the STS-3c line or physical layer timing from the ATM layer timing.

The FIFO supports two data structures. The first data structure consists of 27 16-bit words comprising the 5 octet cell header and the 48 octet payload (the HCS byte, along with the header error insertion control, is passed in this structure). Note that the header error insertion control allows the programmable insertion of one or more bit errors in the HCS octet. The second data structure consists of 53 8-bit words, comprising the 5 octet cell header, and the 48 octet payload.

Management functions include filling the transmit FIFO, indicating when cells are available to be written to the transmit FIFO, maintaining the transmit FIFO read and write pointers, and detecting a FIFO overrun condition.

Upon detection of an overrun condition, the FIFO is automatically reset. The four cells contained in the overrun FIFO are flushed. Typically, one of the four cells is

being read out of the transmit FIFO when the flushing event occurs. The flushing event corrupts this cell, and the corrupted cell continues to be read out and is inserted in the transmit stream. Any or all of the bytes may be corrupted in this transmitted cell. Note that the HCS calculation occurs after the cell is corrupted, and the result is that a corrupted cell with a valid HCS may be inserted in the transmit stream.

FIFO overruns are indicated through a maskable interrupt and register bits. The synchronous interface provided to an external device expects the start of a cell (TSOC) when the first word of the selected data structure is written to the FIFO (using TWRB). The asynchronous interface provided to an external device indicates the cell available status (TCA). The FIFO status changes from cell unavailable to cell available on read cell boundaries with timing derived from the transmit line clock (POCLK). The FIFO status changes from cell available to cell unavailable on write cell boundaries with timing aligned to the transmit write clock (TWRB).

10.15 Line Side Interface

A 19.44 Mbyte/s TTL-compatible receive and transmit line side interface is provided. The bit serial or byte serial line interface selection is done using the TSER and RSER inputs.

10.15.1 Receive Interface

The low speed receive interface is a generic byte wide interface for interconnection with an upstream serial to parallel converter, or with an upstream byte interleaved demultiplexer.

When operating with the serial to parallel converter, the device is expected to provide data that is demultiplexed according to SONET/SDH byte boundaries along with a 19.44 MHz clock. In addition, the upstream serial to parallel converter is expected to provide a framing pattern detector that performs part of the framing function. The serial to parallel converter need not perform descrambling as this is provided by the S/UNI. When enabled to search for frame alignment by the S/UNI OOF output being high, the upstream device should realign to any occurrence of the SONET/SDH framing pattern, and provide an appropriate pulse on the S/UNI FPIN input. The upstream device should ignore framing patterns and retain its byte alignment when the S/UNI OOF output is low.

When operating with the byte interleaved demultiplexer, the receive interface processes an STS-3c/STM-1 streams which has been demultiplexed from a higher rate stream such as an STS-12/STM-4. In this case, the frame alignment is known, and the demultiplexer indicates the frame alignment by providing an appropriate pulse on the FPIN input.

10.15.2 Transmit Interface

The low speed transmit interface is a generic byte wide interface for interconnection with a downstream parallel to serial converter, or a downstream byte interleaved multiplexer.

When operating with the parallel to serial converter, the transmit interface provides scrambled data and a 19.44 MHz clock.

When operating with the byte interleaved multiplexer, the transmit interface provides an STS-3c/STM-1 stream which is multiplexed to a higher rate stream such as an STS-12/STM-4. In this case, the transmit interface provides unscrambled data and a 19.44 MHz clock.

10.16 Drop Side Interface

10.16.1 Receive Interface

The drop side receive interface can be accessed through a generic 16-bit or 8-bit wide interface.

External circuitry is notified, using the RCA signal, when a cell is available in the receive FIFO. External circuitry may then read the cell from the buffer as a word wide stream (along with a bit marking the first word of the cell) at instantaneous rates of up to 25 MHz.

Two cell data structure options are supported as described in the Receive ATM Cell Processor block description above.

10.16.2 Transmit Interface

The drop side transmit interface can be accessed through a generic 16-bit or 8-bit wide interface.

External circuitry is notified, using the TCA signal, when a cell may be written to the transmit FIFO. The cell is written to the FIFO as a word wide stream (along

with a bit marking the first word of the cell) at instantaneous rates of up to 25 MHz.

Two cell data structure options are supported as described in the Transmit ATM Cell Processor block description above.

10.17 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI. The register set is accessed as follows:

10.18 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI identification code is 053450CD hexadecimal.

10.19 Register Memory Map

Table 2 -

Address	Register
0x00	S/UNI Master Reset and Identity
0x01	S/UNI Master Configuration
0x02	S/UNI Master Interrupt Status
0x04	S/UNI Master Clock Monitor
0x05	S/UNI Master Control
0x06-0x07	Reserved
0x08-0x0B	Reserved
0x0C-0x0F	Reserved
0x10	RSOP Control/Interrupt Enable
0x11	RSOP Status/Interrupt Status
0x12	RSOP Section BIP-8 LSB
0x13	RSOP Section BIP-8 MSB

Address	Register
0x14	TSOP Control
0x15	TSOP Diagnostic
0x16-0x17	TSOP Reserved
0x18	RLOP Control/Status
0x19	RLOP Interrupt Enable/Status
0x1A	RLOP Line BIP-24 LSB
0x1B	RLOP Line BIP-24
0x1C	RLOP Line BIP-24 MSB
0x1D	RLOP Line FEBE LSB
0x1E	RLOP Line FEBE
0x1F	RLOP Line FEBE MSB
0x20	TLOP Control
0x21	TLOP Diagnostic
0x22-0x23	TLOP Reserved
0x24-0x27	Reserved
0x28-0x2B	Reserved
0x2C-0x2F	Reserved
0x30	RPOP Status/Control
0x31	RPOP Interrupt Status
0x32	RPOP Reserved
0x33	RPOP Interrupt Enable
0x34	RPOP Reserved
0x35	RPOP Reserved
0x36	RPOP Reserved
0x37	RPOP Path Signal Label
0x38	RPOP Path BIP-8 LSB / Load Meters
0x39	RPOP Path BIP-8 MSB
0x3A	RPOP Path FEBE LSB

Address	Register
0x3BH	RPOP Path FEBE MSB
0x3C-0x3F	RPOP Reserved
0x40	TPOP Control/Diagnostic
0x41	TPOP Pointer Control
0x42	TPOP Source Control
0x43	TPOP Reserved
0x44	TPOP Reserved
0x45	TPOP Arbitrary Pointer LSB
0x46	TPOP Arbitrary Pointer MSB
0x47	TPOP Reserved
0x48	TPOP Path Signal Label
0x49	TPOP Path Status
0x4A	TPOP Reserved
0x4B-0x4F	TPOP Reserved
0x50	RACP Control/Status
0x51	RACP Interrupt Enable/Status
0x52	RACP Match Header Pattern
0x53	RACP Match Header Mask
0x54	RACP Correctable HCS Error Count
0x55	RACP Uncorrectable HCS Error Count
0x56-0x5F	RACP Reserved
0x60	TACP Control/Status
0x61	TACP Idle/Unassigned Cell Header Pattern
0x62	TACP Idle/Unassigned Cell Payload Octet Pattern
0x63-0x67	TACP Reserved
0x68-0x7F	Reserved
0x80	S/UNI Master Test

Address	Register
0x81-0xFF	Reserved for Test

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[7]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 0x00: S/UNI Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	ID[6]	0
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision of the S/UNI to be read by software permitting graceful migration to support for newer, feature enhanced versions of the S/UNI. It also provides software reset capability.

ID[6:0]:

The ID bits can be read to provide a binary S/UNI revision number.

RESET:

The RESET bit allows the S/UNI to be reset under software control. If the RESET bit is a logic one, the entire S/UNI is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI out of reset. Holding the S/UNI in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise the effect of a software reset is equivalent to that of a hardware reset.

Register 0x01: S/UNI Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	GPINE	0
Bit 6	R/W	AUTOFEBE	1
Bit 5	R/W	AUTOFERF	1
Bit 4	R/W	AUTOYEL	1
Bit 3	R/W	TCAINV	0
Bit 2	R/W	RCAINV	0
Bit 1	R/W	MODE[1]	0
Bit 0	R/W	MODE[0]	1

MODE[1:0]:

The MODE[1:0] bits select the operational rate. The default configuration selects STS-3c rate operation. Other combinations are reserved for selecting STS-1 or STS-12 rate operation in future versions.

RCAINV:

The RCAINV bits select the active polarity of the RCA signal. The default configuration selects RCA to be active high, indicating that a received cell is available when high. When RCAINV is set to logic one, the RCA signal becomes active low.

TCAINV:

The TCAINV bits select the active polarity of the TCA signal. The default configuration selects TCA to be active high, indicating that a cell is available in the transmit FIFO when high. When TCAINV is set to logic one, the TCA signal becomes active low.

AUTOYEL

The AUTOYEL bit determines whether STS path yellow alarm is sent immediately upon detection of an incoming alarm. When AUTOYEL is set to logic one, STS path yellow alarm is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), line AIS, loss of pointer (LOP), or STS path AIS.

AUTOFERF

The AUTOFERF bit determines whether line far end receive failure (FERF) is sent immediately upon detection of an incoming alarm. When AUTOFERF is set to logic one, line FERF is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), or line AIS.

AUTOFEBE

The AUTOFEBE bit determines whether line and path far end block errors are sent upon detection of an incoming line and path BIP error events. When AUTOFEBE is set to logic one, one line or path FEBE is inserted for each line or path BIP error event. When AUTOFEBE is set to logic zero, incoming line or path BIP error events do not generate FEBE events.

GPINE

The GPINE bit is an interrupt enable for the GPIN input. When GPINE is set to logic one, an interrupt is generated when the GPIN input changes state.

Register 0x02: S/UNI Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R	GPINV	X
Bit 6	R	PFERFI	X
Bit 5	R	GPINI	X
Bit 4	R	TACPI	X
Bit 3	R	RACPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is high when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RACPI:

The RACPI bit is high when an interrupt request is active from the RACP block. The RACP interrupt sources are enabled in the RACP Interrupt Enable/Status Register.

TACPI:

The TACPI bit is high when an interrupt request is active from the TACP block. The TACP interrupt sources are enabled in the TACP Interrupt Control/Status Register.

GPINI:

The GPINI bit is high when a transition is detected on the GPIN input. The interrupt is acknowledged by reading this register. This bit is reset immediately after a read to this register. The GPIN interrupt is enabled in the S/UNI Master Configuration Register.

PFERFI:

The PFERFI interrupt bit is set high when entering and exiting path FERF. Path FERF is declared when the binary pattern, 1001 is detected in the Path Status (G1) byte's FEBE field for two consecutive G1 bytes. Path FERF is removed when two consecutive non 1001 binary patterns are detected in the G1 byte. This bit is reset immediately after a read to this register. The PFERFI interrupt is enabled in the S/UNI Master Control Register.

GPINV:

The GPINV bit reflects the current value of the S/UNI GPIN input.

Register 0x04: S/UNI Master Clock Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	RCLKA	X
Bit 0	R	POCLKA	X

This register provides activity monitoring on S/UNI clock inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures. Depending on the selected interface (bit serial or byte serial), this register monitors activity on the PICLK and TCLK inputs, or the RXC+/- and TXCI+/- inputs.

POCLKA:

The POCLK active (POCLKA) bit monitors for low to high transitions on the POCLK output. POCLKA is set high on a rising edge of POCLK, and is set low when this register is read.

RCLKA:

The RCLK active (RCLKA) bit monitors for low to high transitions on the RCLK output. RCLKA is set high on a rising edge of RCLK, and is set low when this register is read.

Register 0x05: S/UNI Master Control

Bit	Type	Function	Default
Bit 7	R/W	PFERFE	0
Bit 6	R	PFERFV	X
Bit 5	R/W	TPFERF	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LLE	0
Bit 1	R/W	DLE	0
Bit 0	R/W	LOOPT	0

This register controls the timing and high speed loopback features of the S/UNI.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the S/UNI. Loop time operation should only be activated while the bit serial interface is selected. When LOOPT is a logic zero, the transmitter timing is derived from inputs TXCI+ and TXCI- when the bit serial interface is selected (TSER is tied high), or from the TCLK input when the byte serial interface is selected (TSER is tied low).

When LOOPT is a logic one, and the bit serial interface is selected (TSER and RSER are both tied high), the transmitter timing is derived from the receiver, inputs RXCI+ and RXCI-. Loop timed operation is not supported when the byte serial interface is selected (TSER and RSER are both tied low). For byte serial operation, loop time operation should be performed in the bit serial PMD.

DLE:

The DLE bit enables the S/UNI diagnostic loopback. Diagnostic loopback may only be activated while the bit serial interface is selected. When DLE is a logic one, the transmit STS-3c stream is connected to the receive stream. The diagnostic loopback may be performed only when the bit serial interfaces are selected.

LLE:

The LLE bit enables the S/UNI line loopback. Line loopback may only be activated while the bit serial interface is selected (TSER and RSER are both tied high). When LLE is a logic one, RXD+, RXD-, RXC+, and RXC- are connected internally to TXD+, TXD-, TXCO+, and TXCO- respectively.

TPFERF:

The TPFERF bit forces the S/UNI to transmit PATH FERF. When TPFERF is set to logic one, Path FERF is transmitted by setting the Path Status (G1) byte's FEBE field to 1001 binary. When TPFERF is set to logic zero, the G1 byte's FEBE field is inserted by the TPOP block.

PFERFV:

The PFERFV bit reflects the current Path FERF state. When logic one, the S/UNI is currently detecting Path FERF in the receive stream. When logic zero, Path FERF is not detected in the receive stream.

PFERFE:

The PFERFE bit enables the S/UNI Path FERF interrupt. When logic one, the S/UNI INTB output is asserted when there is a change in the Path FERF state. When logic zero, the S/UNI INTB output is not affected by the change in Path FERF states.

Register 0x10: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out of frame alarm. When OOFE is set to logic one, an interrupt is generated when the out of frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit, register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the descrambling of the STS-3c (STM-1) stream. When DDS is a logic zero, descrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x11: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out of frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:

The OOFI bit is the out of frame interrupt status bit. OOFI is set high when a change in the out of frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x12: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x13: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (B1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the RPOP Path BIP-8 LSB / Load Meters register (0x38). Writing to register address 0x38 loads all the error counter registers in the RSOP, RLOP, RPOP and RACP blocks.

Register 0x14: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 7	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET frame being set to 1 prior to scrambling except for the section overhead. The LAIS bit is logically ORed with the external TLAIS input.

The DC1 bit controls the overwriting of the identity byte(s) in the STS-3c stream. When DC1 is set low, the identity bytes of the constituent STS-1s in the STS-3c stream are programmed as specified in the references: STS-1 #1 C1 = 01 hexadecimal, STS-1 #2 C1 = 02 hexadecimal, STS-1 #N C1 = N hexadecimal. When DC1 is set high the PIN[7:0] identity byte positions in each of the constituent STS-1s are not overwritten.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-3c (STM-1) stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x15: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 7		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the STS-3c (STM-1) stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x18: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R	LAISV	0
Bit 0	R	FERFV	0

FERFV:

The FERFV bit is read to determine the far end receive failure state of the RLOP. When FERFV is high, the RLOP has declared line FERF.

LAISV:

The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x19: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	FERFE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	FERFI	X

FERFI:

The FERFI bit is the far end receive failure interrupt status bit. FERFI is set high when a change in the line FERF state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP-24 interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (Z2) is detected. This bit is cleared when this register is read.

FERFE:

The FERFE bit is an interrupt enable for the far end receive failure alarm. When FERFE is set to logic one, an interrupt is generated when the FERF alarm changes state.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-24 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-24 error (B2) is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBE (Z2) is detected.

Register 0x1A: RLOP Line BIP-24 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x1B: RLOP Line BIP-24

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x1C: RLOP Line BIP-24 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-24 errors (B2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-24 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP-24 Registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the RPOP Path BIP-8 LSB / Load Meters register (0x38). Writing to register address 0x38 loads all the error counter registers in the RSOP, RLOP, RPOP and RACP blocks.

Register 0x1D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x1E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x1F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (Z2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-24 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the RPOP Path BIP-8 LSB / Load Meters register (0x38). Writing to register address 0x38 loads all the error counter registers in the RSOP, RLOP, RPOP and RACP blocks.

Register 0x20: TLOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	FERF	0

FERF:

The FERF bit controls the insertion of line far end receive failure (FERF). When FERF is set to logic one, the TLOP inserts line FERF into the transmit SONET stream. Line FERF is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte of the STS-3c (STM-1) stream. The FERF bit is logically ORed with the external TFERF input.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x21: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP24	0

DBIP24:

The DBIP24 bit controls the insertion of bit errors continuously in the line BIP-24 bytes (B2). When DBIP24 is set to logic one, the B2 bytes are inverted.

Register 0x30: RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	LOP	X
Bit 4		Unused	X
Bit 3	R	PAIS	X
Bit 2	R	PYEL	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	0

This register allows the status of path level alarms to be monitored.

PYEL, PAIS,LOP:

The PYEL, PAIS, and LOP bits reflect the current state of the corresponding path level alarms.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x31: RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PYELI	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI, BIPEI:

The BIPEI and FEBEI bits are set to logic one when the corresponding event, a path BIP-8 error or path FEBE is detected.

PYELI, PAISI, LOPI:

The PYELI, PAISI, and LOPI bits are set to logic one when a transition occurs in the corresponding alarm state.

PSLI:

The PSLI bit is set to logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register.

These bits (and the interrupt) are cleared when this register is read.

Register 0x33: RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PYELE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

When a 1 is written to the FEBEE interrupt enable bit position, the reception of one or more FEBEs will activate the interrupt output.

BIPEE:

When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt output.

PYELE, PAISE:

When a 1 is written to the PYELE interrupt enable bit position, a change in the path yellow state will activate the interrupt output. When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt output.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt output.

PSLE:

When a 1 is written to the PSLE interrupt enable bit position, a change in the path signal label will activate the interrupt output.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x37: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

This register allows the received path signal label byte to be read.

PSL[7:0]:

The PSL7 - PSL0 bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for two consecutive frames.

Register 0x38: RPOP Path BIP-8 LSB / Load Meters

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x39: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

These registers allow path BIP-8 errors to be accumulated.

PBE[15:0]:

Bits PBE[15:0] represent the number of path BIP-8 errors (B3) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 Registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

Writing to the RPOP Path BIP-8 LSB / Load Meters register (0x38) also loads all the error counter registers in the RSOP, RLOP, RPOP and RACP blocks.

Register 0x3A: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE7	X
Bit 6	R	PFE6	X
Bit 5	R	PFE5	X
Bit 4	R	PFE4	X
Bit 3	R	PFE3	X
Bit 2	R	PFE2	X
Bit 1	R	PFE1	X
Bit 0	R	PFE0	X

Register 0x3B: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE15	X
Bit 6	R	PFE14	X
Bit 5	R	PFE13	X
Bit 4	R	PFE12	X
Bit 3	R	PFE11	X
Bit 2	R	PFE10	X
Bit 1	R	PFE9	X
Bit 0	R	PFE8	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

Bits PFE[15:0] represent the number of path FEBE errors (G1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within approximately 1µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

Register 0x40: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

This register allows insertion of path level alarms and diagnostic signals.

PAIS:

The PAIS bit controls the insertion of STS path alarm indication signal. This register bit value is logically ORed with the input TPAIS. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.

DB3:

The DB3 bit controls the inversion of the B3 byte value. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame. This bit overrides the state of the B3 error insertion mask controlled by the TPOHEN primary input. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x41: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NSE:

The NSE bit controls the insertion of negative pointer movements. A zero to one transition on this bit enables the insertion of a single negative pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the Arbitrary Pointer Registers. Normally the Arbitrary Pointer Registers are

written to set up the arbitrary new pointer value, the S-bit values, and the NDF pattern. A logic one is then written to this bit position to load the new pointer value. The new data flag bit positions are set to the programmed NDF pattern for the first frame; subsequent frames have the new data flag bit positions set to the normal pattern (0110) unless the NDF bit described above is set to a logic one. This bit is automatically cleared after the new payload pointer has been loaded.

Note: When loading an out of range pointer (that is a pointer with a value greater than 782), the TPOP continues to operate with timing based on the last valid pointer value. The out of range pointer value will of course be inserted in the STS-3c (STM-1) stream. Although a valid SPE will continue to be generated, it is unlikely to be extracted by downstream circuitry which should be in a loss of pointer state.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x42: TPOP Source Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SRCZ5	0
Bit 5	R/W	SRCZ4	0
Bit 4	R/W	SRCZ3	0
Bit 3	R/W	SRCC2	0
Bit 2	R/W	SRCG1	0
Bit 1	R/W	SRCF2	0
Bit 0	R/W	SRCJ1	0

This register facilitates selection between internal generation or external sourcing of path overhead bytes.

SRCJ1, SRCF2, SRCG1, SRCC2, SRCZ3, SRCZ4, SRCZ5:

The SRCnn bits are logically ORed with input TPOHEN to select the source for the path overhead bytes in the transmit STS-3c (STM-1) stream. For example, when a logic one is written to SRCJ1, the J1 byte is inserted from the data sampled on primary input TPOH during the J1 byte position. When a logic zero is written to SRCJ1, the J1 byte source is determined by input TPOHEN.

If the source bit is set to logic zero and the TPOHEN input is not used to select the primary input TPOH, the default values are inserted as specified in Fig. 6, Default Path Overhead Values.

Register 0x45: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7], APTR[6], APTR[5], APTR[4], APTR[3], APTR[2], APTR[1], APTR[0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

Register 0x46: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	0
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9], APTR[8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

S[1], S[0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer.

NDF[3], NDF[2], NDF[1], NDF[0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the Pointer Control Register) or when new data flag generation is enabled using the NDF bit in the TPOP Pointer Control Register.

Register 0x48: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	1
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	1
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label.

C2[7], C2[6], C2[5], C2[4], C2[3], C2[2], C2[1], C2[0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream when primary input TPOHEN is low during the path signal label bit positions in the path overhead input stream, TPOH.

Register 0x49: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PYEL	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

FEBE[3], FEBE[2], FEBE[1], FEBE[0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte when the SRCG1 bit of the TPOP Source Control Register is logic zero and primary input TPOHEN is low during the path status FEBE bit positions in the path overhead input stream, TPOH. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated on primary input FEBE during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

PYEL:

The PYEL bit controls the insertion of STS path yellow alarm. This register bit value is logically ORed with the input TPYEL. When a logic one is written to this bit position, the PYEL bit position in the path status byte is set high. When a logic zero is written to this bit position, the PYEL bit position in the path status byte is set low. This bit has no effect if the SRCG1 bit of the TPOP Source Control Register is logic one or primary input TPOHEN is high during the path status yellow alarm bit position in the path overhead input stream, POH, in which case the value is inserted from TPOH.

G1[2], G1[1], G1[0]:

The G1[2:0] bits are inserted in the unused bit positions in the path status byte when the SRCG1 bit of the Source Control Register is logic zero and primary input TPOHEN is low during the unused bit positions in the path overhead input stream, TPOH.

Register 0x50: RACP Control/Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6		Unused	X
Bit 5	R/W	PASS	0
Bit 4	R/W	DISCOR	0
Bit 3	R/W	HCSPASS	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DDSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell receive FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload. When DDSCR is a logic one, cell payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic zero, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic one, cells are passed to the receive FIFO regardless of errors detected in the HCS. Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

DISCOR:

The DISCOR bit disables the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

PASS:

The PASS bit controls the function of the cell filter. When PASS is written with a logic zero, all cells matching the cell filter are dropped. When PASS is a logic one, the match header pattern registers are ignored and filtering of cells with VPI and VCI fields set to 0 is not performed. The default state of this bit together with the default states of the bits in the Match Mask and Match Pattern Registers enable the dropping of cells containing all zero VCI and VPI fields.

OOCDV:

The OOCDV bit indicates the cell delineation state. When OOCDV is set high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states, and is hunting for the cell boundaries in the synchronous payload envelope. When OOCDV is set low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x51: RACP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	OOCDE	0
Bit 6	R/W	HCSE	0
Bit 5	R/W	FIFOE	0
Bit 4	R	OOCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	FUDRI	X

FUDRI:

The FUDRI bit is set high when a FIFO underrun occurs. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register.

UHCSI:

The UHCSI bit is set high when an uncorrectable HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI:

The CHCSI bit is set high when a correctable HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set high when a change of cell delineation state has occurred. The OOCDI bit is set high when the RACP block transitions from the PRESYNC state to the SYNC state and from the SYNC state to the HUNT state. This bit is reset immediately after a read to this register.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun or a FIFO underrun error condition. When FIFOE is set to logic one, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a correctable or an uncorrectable HCS error. When HCSE is set to logic one, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change of cell delineation state. When OOCDE is set to logic one, the interrupt is enabled.

Register 0x52: RACP Match Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third and fourth bits of the first octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of cells matching this pattern.

Register 0x53: RACP Match Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	0
Bit 6	R/W	MGFC[2]	0
Bit 5	R/W	MGFC[1]	0
Bit 4	R/W	MGFC[0]	0
Bit 3	R/W	MPTI2]	0
Bit 2	R/W	MPTI[1]	0
Bit 1	R/W	MPTI[0]	0
Bit 0	R/W	MCLP	0

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third and fourth bits of the first octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MPTI3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

Register 0x54: RACP Correctable HCS Error Count

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

CHCS[7:0]:

The CHCS[7:0] bits indicate the number of correctable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the correctable HCS error count register address, or to the uncorrectable HCS error count register address.

Register 0x55: RACP Uncorrectable HCS Error Count

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

UHCS[7:0]:

The UHCS[7:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the correctable HCS error count register address, or to the uncorrectable HCS error count register address.

Register 0x60: TACP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	FIFOE	0
Bit 6	R	TSOCI	X
Bit 5	R	FOVRI	X
Bit 4	R/W	DHCS	0
Bit 3	R/W	HCS	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted.

HCS:

The HCS bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCS is a logic zero, the HCS is generated and inserted internally. When HCS is a logic one, the HCS octet read from the FIFO is inserted transparently into the transmit cell stream.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope.

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. Normally a single TSOCI is indicated during startup as the S/UNI write address counter is synchronized to the system cell alignment. If The TSOCI indication is edge triggered. Thus multiple TSOCI indications are not generated if the TSOC input is held high. This bit is reset immediately after a read to this register.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun error condition, or when the TSOC input is sampled high during any position other than the first word of the selected data structure. When FIFOE is set to logic one, the interrupt is enabled.

Register 0x61: TACP Idle/Unassigned Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

PTI[3:0]:

The PTI[3:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

Register 0x62: TACP Idle/Unassigned Cell Payload Octet Pattern

Bit	Type	Function	Default
Bit 7	R/W	ICP[7]	0
Bit 6	R/W	ICP[6]	1
Bit 5	R/W	ICP[5]	1
Bit 4	R/W	ICP[4]	0
Bit 3	R/W	ICP[3]	1
Bit 2	R/W	ICP[2]	0
Bit 1	R/W	ICP[1]	1
Bit 0	R/W	ICP[0]	0

ICP[7:0]:

The ICP[7:0] bits contain the pattern inserted in the payload octets of the idle or unassigned cell. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. Bit ICP[7] corresponds to the most significant bit of the octet, the first bit transmitted.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. PECL output pins, TXCO+/- and TXD+/- are not affected. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[7]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI also supports a standard IEEE 1149.1 five signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port. Boundary scan is not provided for the PECL pins TXCI+/-, TXCO+/-, TXD+/-, RXC+/- and RXD+/-.

12.1 Test Mode Register Memory Map

Table 3 -

Address	Register
0x00-0x7F	Normal Mode Registers
0x80	Master Test
0x81-0xFF	Reserved For Test

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x80: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI test features. All bits, except PMCTST, are reset to zero by a reset of the S/UNI.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI . While the HIZIO bit is a logic one, all output pins of the S/UNI except the data bus, output TDO and the PECL outputs are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The

DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic one.

12.2 Test Mode 0 Details

In test mode 0, the S/UNI allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register should be set to logic one.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one and the following addresses must be written with 00H: 91H, 95H, 99H, A1H, B1H, C1H, D1H and E1H. The byte interface (TSER=0 and RSER=0) must be selected and clock edges must be provided on inputs TCLK and PICLK when these clocks are not being tested.

Reading the following address locations returns the values for the indicated inputs:

Table 4 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90H							FPIN	PICLK
92H	PIN[7]	PIN[6]	PIN[5]	PIN[4]	PIN[3]	PIN[2]	PIN[1]	PIN[0]
94H						TLAIS		
A0H	TTOHEN			TFERF			TTOH	TCLK
C0H				TPYEL	TPAIS			
C3H							TPOH	TPOHEN
C4H								TFP
D0H					BUS8			

The following inputs can not be read using the IOTST feature: TXCI+/-, FPOS/MLT, RXC+/-, RXD+/-, RSER, D[7:0], A[7:0], ALE, CSB, WRB, RDB,

RSTB, GPIN, TSEN, RRDB, TWRB, TDAT[15:0], TSOC, TRSTB, TMS, TCK, TDI and TSER.

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Table 5 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90H			LOF	OOF	LOS			
92H		INT +						
93H						RTOH	RTOHCLK	RTOHFP
96H	POUT[7]	POUT[6]	POUT[5]	POUT[4]	POUT[3]	POUT[2]	POUT[1]	POUT[0]/
								FPOUT
98H				FERF	LAIS			
B0H				PAIS				
B2H			LOP					
B3H					PYEL	RPOHFP	RPOH	RPOHCLK
C2H							TTOHCLK	TTOHFP
C3H					TPOHCLK	TPOHFP		

+ bit INT corresponds to output INTB. INTB is an open drain output and should be pulled high for proper operation. Writing a logic one to the INT bit allows the S/UNI to drive INTB low. Writing a logic zero to the INT bit tristates the INTB output.

The following outputs can not be controlled using the IOTST feature: TXCO+/-, TXD+/-, POCLK, RCLK, D[7:0], RCA, RDAT[15:0], RSOC, TCA and TDO.

12.3 JTAG Test Port

The S/UNI JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 6 - Instruction Register

	Length - 3 bits		
Instructions	Selected	Instruction	
	Register	Codes, IR[2:0]	
	EXTEST	Boundary Scan	000
	IDCODE	Identification	001
	SAMPLE	Boundary Scan	010
	BYPASS	Bypass	011
	BYPASS	Bypass	100
	STCTEST	Boundary Scan	101
	BYPASS	Bypass	110
	BYPASS	Bypass	111

Table 7 - Identification Register

Length	32 bits
Version number	0H
Part Number	5345H
Manufacturer's identification code	0CDH
Device identification	053450CDH

Table 8 - Boundary Scan Register

	Length - 120 bits		
Pin/Enable	**Boundary**	**Pin/Enable**	**Boundary**
	Scan Register		**Scan Register**
	Bit		**Bit**
a[7:0]	119:112	tsen	66
ale	111	bus8	65
csb	110	rrdb	64

wrb	109	rsoc	63
rdb	108	rdat[15:0]	62:47
rstb	107	rdatenb	46 (For RDAT[15:0])
gpin	106	rca	45
d[7:0]	105:98	tdat[15:0]	44:29
oen	97 (for d[7:0])	tsoc	28
intb	96	twrb	27
hiz	95	tca	26
pin[7:0]	94:87 (pin[1] = DID)	tfp	25
rser	86	tpoh	24
fpin	85	tpohen	23
fpos/mlt	84	tpyel	22
piclk/ser_piclk	83	tpais	21
piclk_oen	82 (For PICLK)	tpohclk	20
rclk	81	tpohfp	19
oof	80	ttoh	18
lof	79	ttohen	17
los	78	ttohfp	16
lais	77	ttohclk	15
ferf	76	tferf	14
rtohfp	75	tser	13
rtohclk	74	tlais	12
rtoh	73	tclk/tclk_ser	11
pais	72	tclk_oen	10 (FOR TCLK)
lop	71	poclk	9
pyel	70	fpout	8
rpohfp	69	pout[7:0]	7:0
rpoh	68		
rpohclk	67		

13 OPERATION

Overhead Byte Usage

Under normal operating conditions, the S/UNI processes a subset of the complete transport overhead present in an STS-3c/STM-1 stream. The byte positions processed by the S/UNI are indicated in figure 7. The complete transport overhead may be inserted and extracted through the Receive and Transmit Transport Overhead Access Ports. Similarly, the path overhead may be inserted and extracted through the Receive and Transmit Path Overhead Access Ports.

Figure 10 - Overhead Byte Usage

A1	**A1**	**A1**	**A2**	**A2**	**A2**	**C1**	**C1**	**C1**
B1								
H1	**H1**	**H1**	**H2**	**H2**	**H2**	**H3**	**H3**	**H3**
B2	**B2**	**B2**				**K2**		
					Z2			

TRANSPORT OVERHEAD SOH

B3
C2
G1
H4

PATH OVERHEAD POH

A1, A2: The frame alignment bytes (A1, A2) locate the SONET frame in the 155.52 Mbit/s stream. The transmitter inserts these bytes in the outgoing stream. The receiver searches for the A1, A2 bit sequence in the incoming stream. A1 and

A2 are not scrambled by the frame synchronous SONET scrambler.

C1: The identification bytes identify the individual STS-1s in the byte interleaved STS-3c stream. The sequence 0x01, 0x02, 0x03 is inserted in the transmit direction. These bytes are ignored in the receive direction. C1 is not scrambled by the frame synchronous SONET scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function. B1 is calculated over all bits of the previous frame after scrambling. B1 is placed in the current frame before scrambling. Receive B1 errors are accumulated in an error event counter.

H1, H2: The pointer value bytes locate the start of the synchronous payload envelope (SPE) in the SONET/SDH frame. In the transmit direction, a fixed pointer value of zero, with a normal new data flag indication, is inserted in the first H1-H2 pair. The concatenation indication is inserted in the remaining two H1-H2 pairs. In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function. B2 is calculated over all bits of the line overhead, and the SPE capacity of the previous frame before scrambling. B2 is placed in the current frame before scrambling. Receive B2 errors are accumulated in an error event counter.

K2: The K2 byte is used to identify line layer maintenance signals. In the transmit direction, line FERF is inserted by setting bits 6, 7, and 8 of the K2 byte to the pattern '110'. Line AIS is inserted by overwriting the line overhead (including bits 6, 7, and 8 of the K2 byte), and the SPE with the all ones pattern before scrambling. In the receive

direction, bits 6, 7, and 8 of the K2 byte are examined to determine the presence of the line AIS, and the line FERF maintenance signals.

Z2: The growth byte provides a line far end block error function for remote performance monitoring. In the transmit direction, the number of B2 errors detected in the previous interval is inserted. This number has 25 legal values, namely 0 to 24 errors. In the receive direction, a legal Z2 byte value is added to the line FEBE event counter.

B3: The path bit interleaved parity byte provides a path error monitoring function. B3 is calculated over all bits of the SPE capacity of the previous frame before scrambling. B3 is placed in the current frame before scrambling. Receive B3 errors are accumulated in an error event counter.

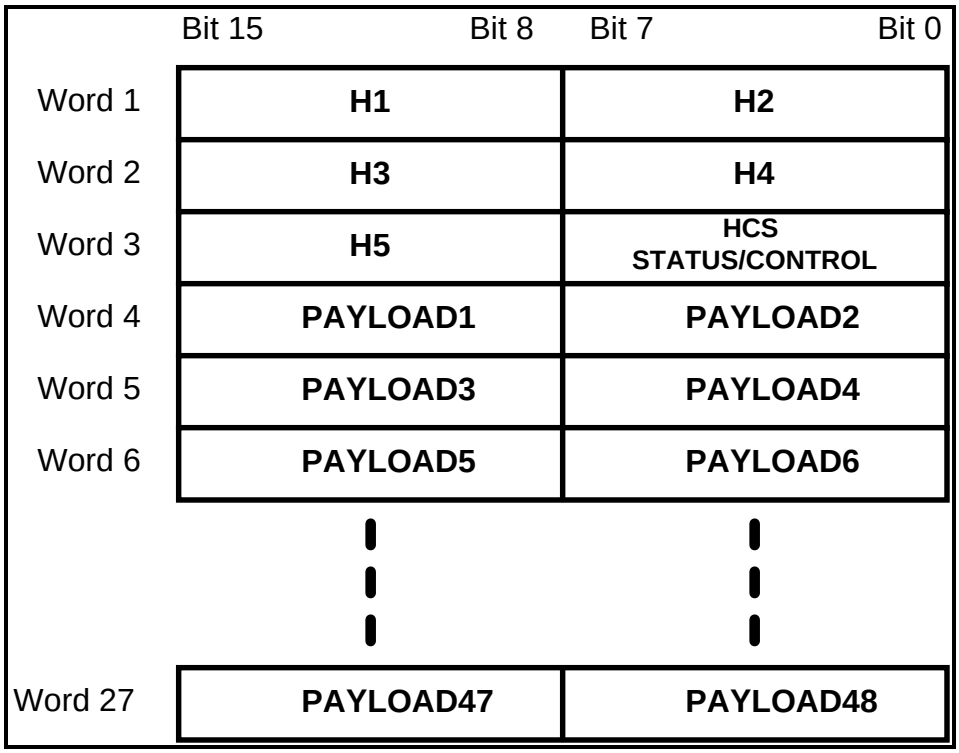
G1: The path status byte provides a path far end block error function, and provides control over the path yellow and the path FERF maintenance signals. In the transmit direction, path yellow alarm and path FERF maintenance signals are inserted, and the number of B3 errors detected in the previous interval is inserted. This number has 9 legal values, namely 0 to 8 errors. A tenth value, namely 1001 binary is used to indicate path FERF. In the receive direction, a legal G1 byte value is added to the path FEBE event counter. In addition, path yellow and path FERF alarms are detected.

H4: The cell offset indicator byte indicates the offset in bytes between itself, and the first cell boundary following the H4 byte. This byte is inserted correctly in the transmit direction, and is ignored in the receive direction.

Cell Data Structures

ATM cells may be passed to/from the S/UNI using one of two defined data structures. A 9 bit structure, consisting of a start of cell indication, and an 8-bit wide word, is defined, along with a 17 bit structure, consisting of a start of cell indication, and a 16-bit wide word. The selection of 8-bit word width versus 16-bit word width is made using primary input BUS8. The available data structures are shown in the figures 8, and 9:

Figure 11 - 16-bit Word Width Data Structure



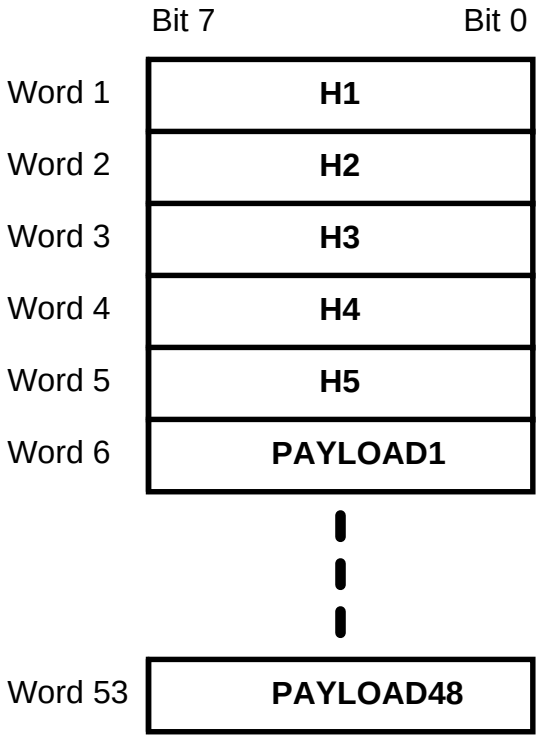
This data structure is selected by tying the BUS8 input low. Twenty-seven 16-bit words are contained in this data structure. Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all zeros pattern in these 8 bits indicates that the associated header is error free. An all ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RACP Control/Status Register is set to logic zero, the all ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TACP Control Register determines whether the HCS is calculated internally, or is inserted directly from the upper 8

bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted).

Figure 12 - 8-bit Word Width Data Structure



This data structure is selected by tying the BUS8 input high. Fifty-three 8-bit words are contained in this data structure. Bit 7 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first cell header octet). Word 5 of this structure contains the HCS octet.

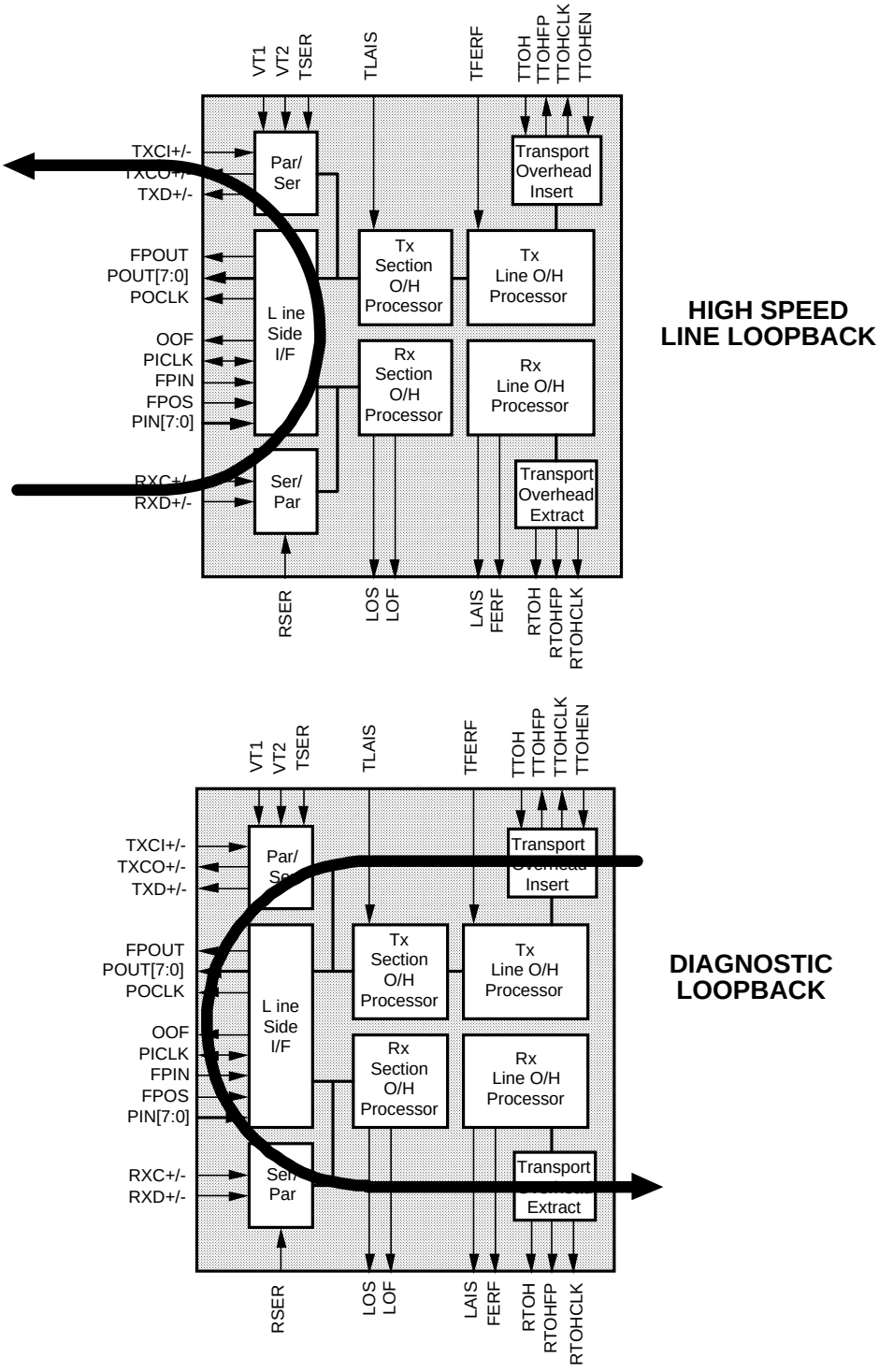
In the receive direction, cells containing uncorrectable header errors are dropped while the HCSPASS bit in the RACP Control/Status Register is set to logic zero. No header status information is passed within this data structure; error free headers, and "corrected" headers are passed while HCSPASS is a logic zero. Error free headers, "corrected" headers, and headers containing uncorrectable errors are passed while HCSPASS is a logic one.

In the transmit direction, the HCS bit in the TACP Control Register determines whether the HCS is calculated internally, or is inserted directly from Word 5.

Loopback Operation

The S/UNI supports two loopback functions: line loopback, and diagnostic loopback. The diagnostic loopback connects the high speed transmit data and clock to the high speed receive data and clock as shown in the partial block diagram in figure 10. The line loopback connects the high speed receive data and clock to the transmit data and clock. Both loopbacks may only be activated when the bit serial interface is selected (RSER and TSER are both tied high). Diagnostic loopback and line loopback are activated by bits contained in the S/UNI Master Control Register.

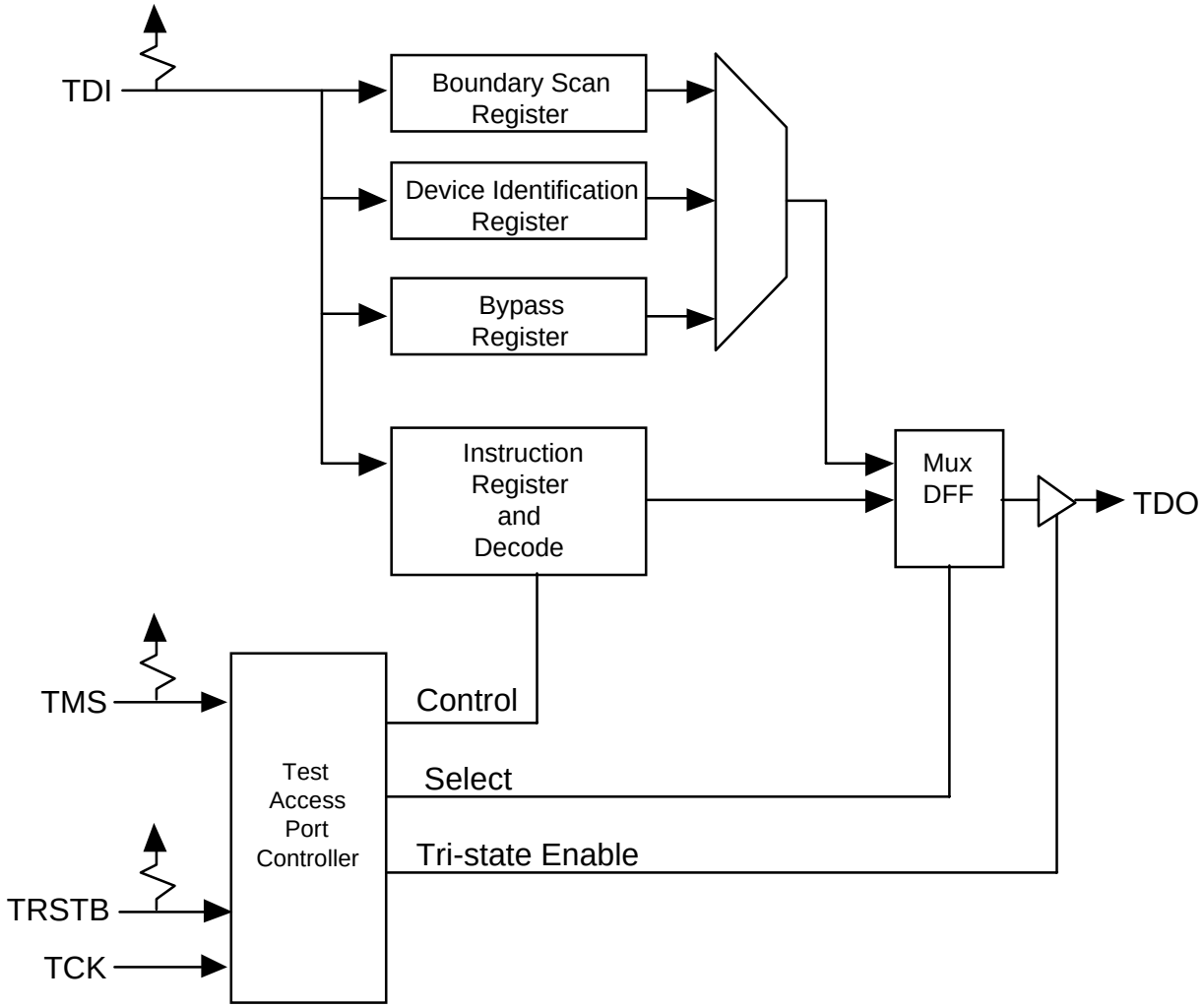
Figure 13 - Loopback Operation



JTAG Support

The S/UNI supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 14 - Boundary Scan Architecture



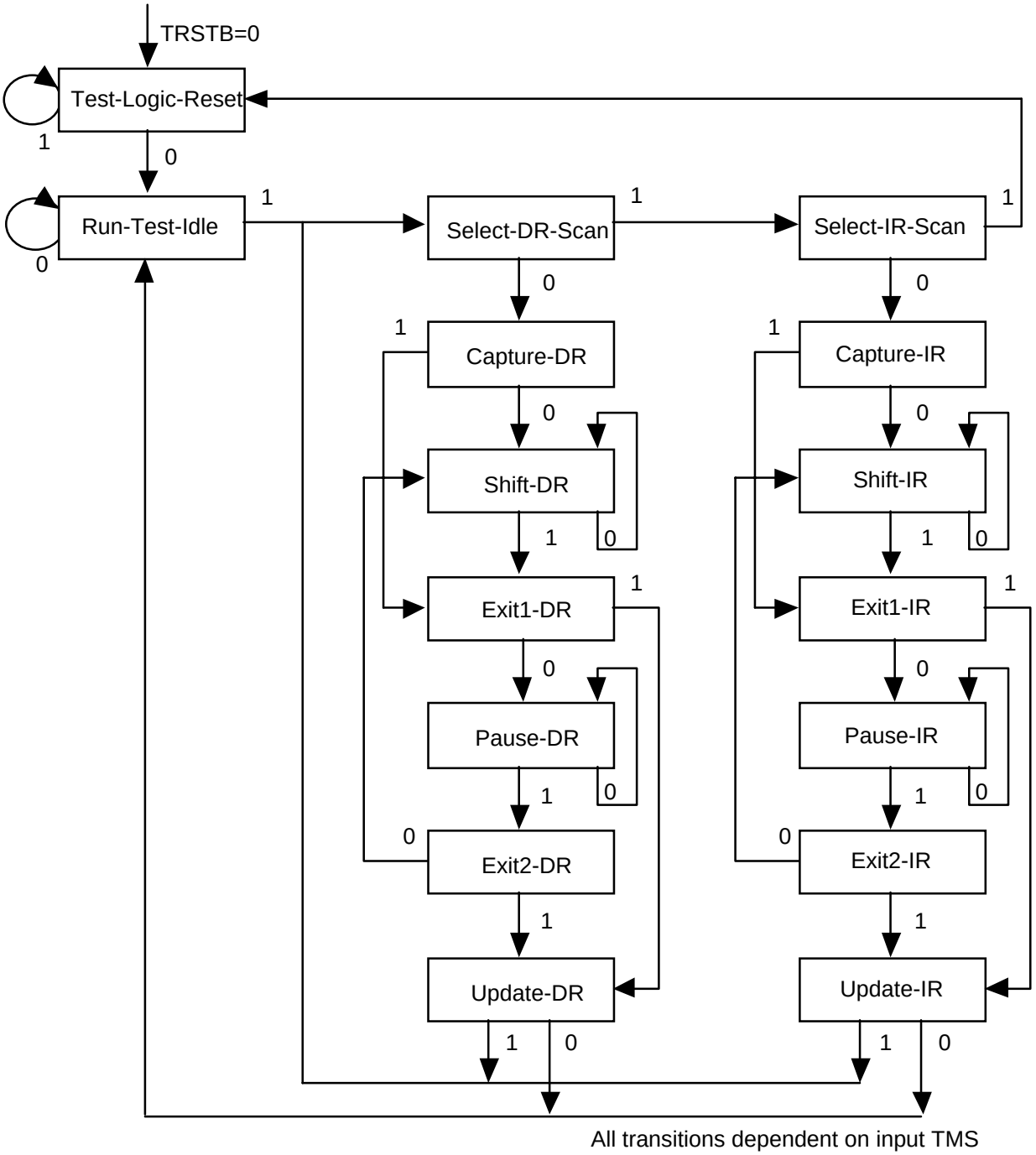
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 15 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

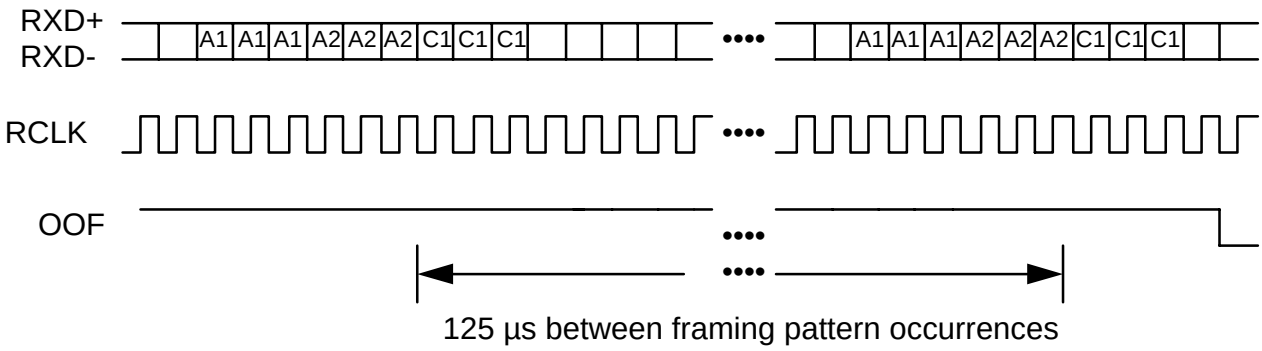
INTEST

The internal test instruction is used to exercise the device's internal core logic. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Update-DR state, patterns shifted in on input, TDI are used to drive primary inputs. During the Capture-DR state, primary outputs are sampled and loaded into the boundary scan register.

14 FUNCTIONAL TIMING

14.1 Line Side Receive Interface

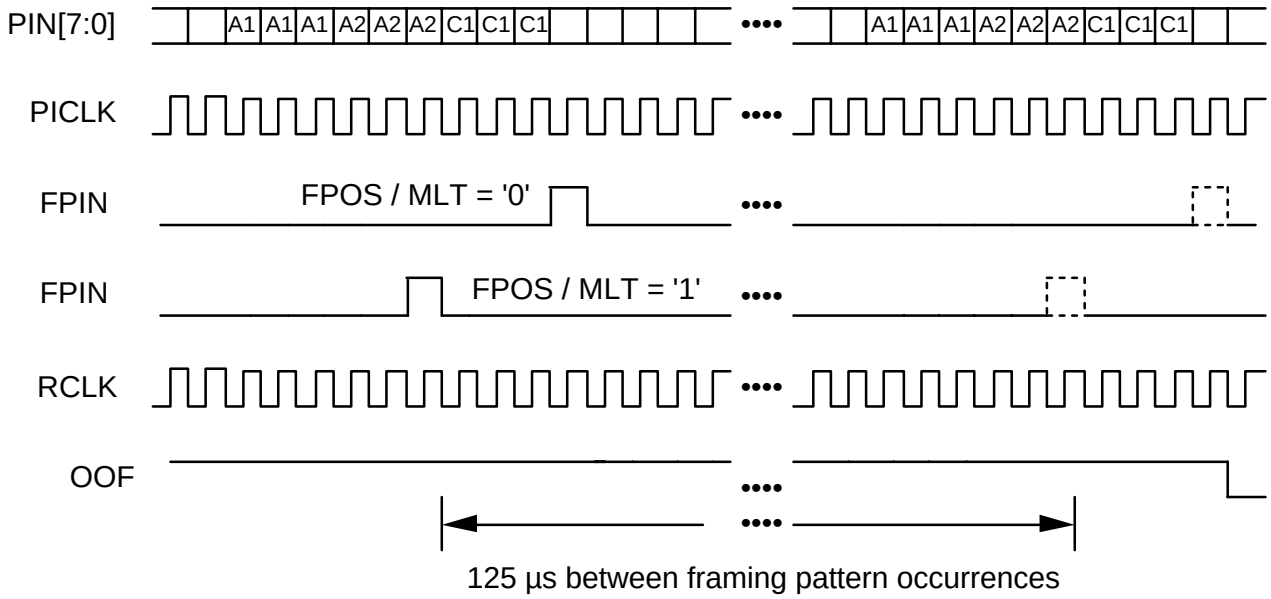
Figure 16 - In Frame Declaration (bit serial interface, RSER=1)



The In Frame Declaration (bit serial interface, RSER = 1) timing diagram (Figure 16) illustrates the declaration of in-frame by the S/UNI when processing a 155.52 Mbit/s stream on RXD+/RXD-. The S/UNI searches the incoming stream for an occurrence of the 48 bit framing pattern (three A1 bytes followed by three A2 bytes). In frame is declared when the framing pattern is observed for the second time, 125 µs after the first occurrence, and in the intervening period (125 µs), no occurrences of the 48 bit framing pattern were detected. This algorithm results in a maximum average reframe time of 250 µs in the absence of mimic framing patterns.

RCLK is generated by dividing the bit serial clock (RXC+, RXC-) by eight. The falling edge of RCLK is used to update OOF.

Figure 17 - In Frame Declaration (byte serial interface, RSER=0)

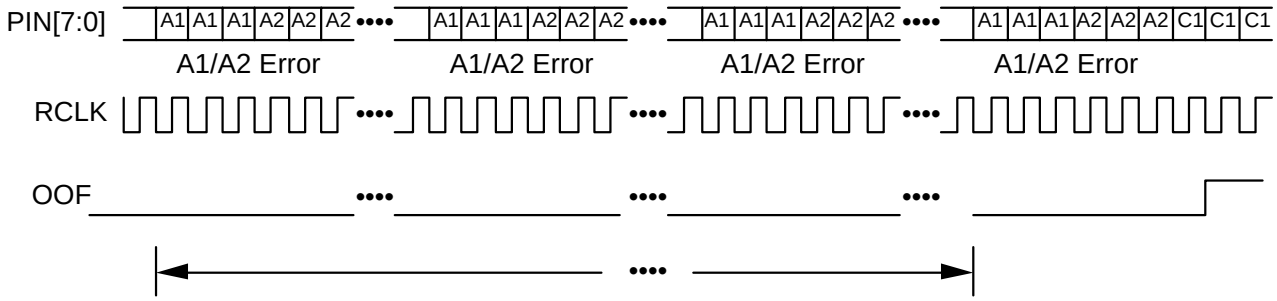


The In Frame Declaration (byte serial interface, RSER=0) Timing (Figure 17) illustrates the declaration of in-frame by the S/UNI when processing a 19.44 Mbyte/s stream on PIN[7:0]. An upstream serial to parallel converter, or byte interleaved demultiplexer indicates the location of the SONET frame using the FPIN input. The byte position marked by FPIN may be controlled using the FPOS/MLT input as illustrated in timing diagram. The frame verification is initialized by a pulse on FPIN while the S/UNI is out of frame. In frame is declared if the framing pattern is observed in the correct byte positions in the following frame, and in the intervening period (125 µs) no additional pulses were present on FPIN. The S/UNI ignores pulses on FPIN while in frame. This algorithm results in a maximum average reframe time of 250 µs in the absence of mimic framing patterns.

When operating with a byte interleaved multiplexer, it is likely that the SONET frame alignment is already known. The S/UNI will not declare in frame unless the SONET framing pattern is present in the demultiplexed stream.

RCLK is a buffered version of the byte serial input clock (PICLK). The falling edge of RCLK is used to update OOF.

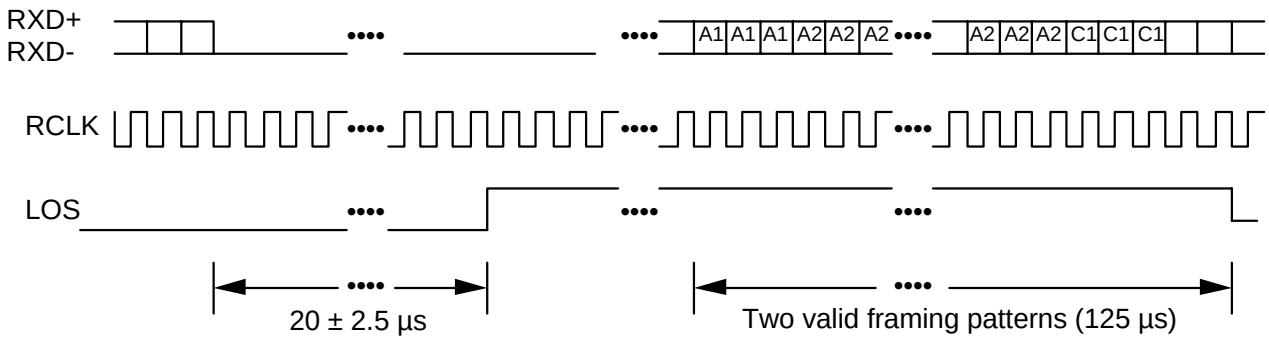
Figure 18 - Out of Frame Declaration



Four consecutive frames containing framing pattern errors

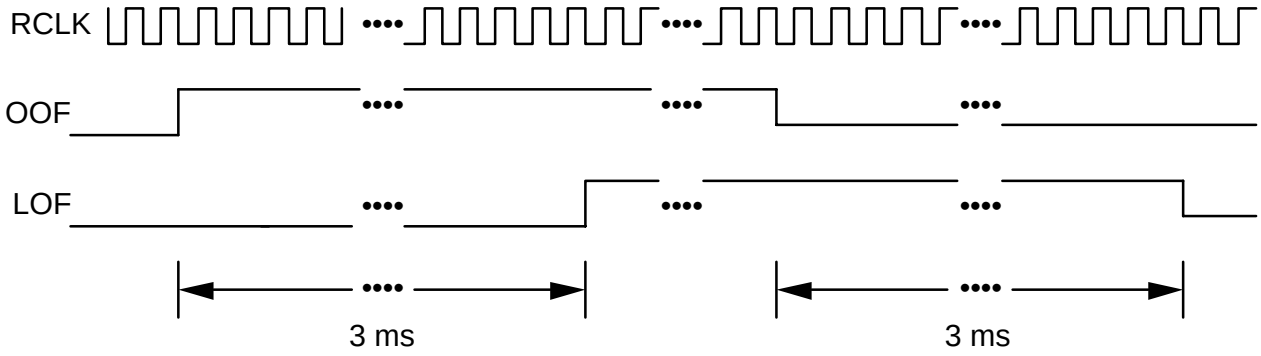
The Out of Frame Declaration Timing Diagram (Figure 18) illustrates the declaration of out of frame. The byte serial interface timing is shown; the bit serial interface timing is similar. In an STS-3c/STM-1 stream, the framing pattern is a 48 bit pattern that repeats once per frame. Out of frame is declared when one or more errors are detected in this pattern for four consecutive frames as illustrated. In the presence of random data, out of frame will normally be declared within 500 µs.

Figure 19 - Loss of Signal Declaration/Removal



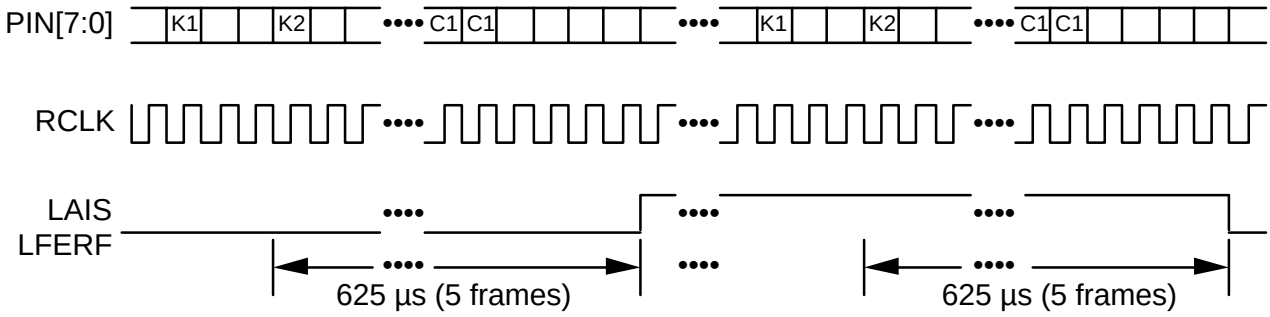
The Loss of Signal Declaration/Removal Timing Diagram (Figure 19) illustrates the operation of the LOS output. LOS is declared when a violating period of all zeros (20 ±2.5 µs) is observed on RXD+/RXD- (note that the same criteria applies to PIN[7:0] when processing a byte serial stream). LOS is removed when two valid framing patterns are observed, and in the intervening period (125 µs), no violating periods of all zeros is observed.

Figure 20 - Loss of Frame Declaration/Removal



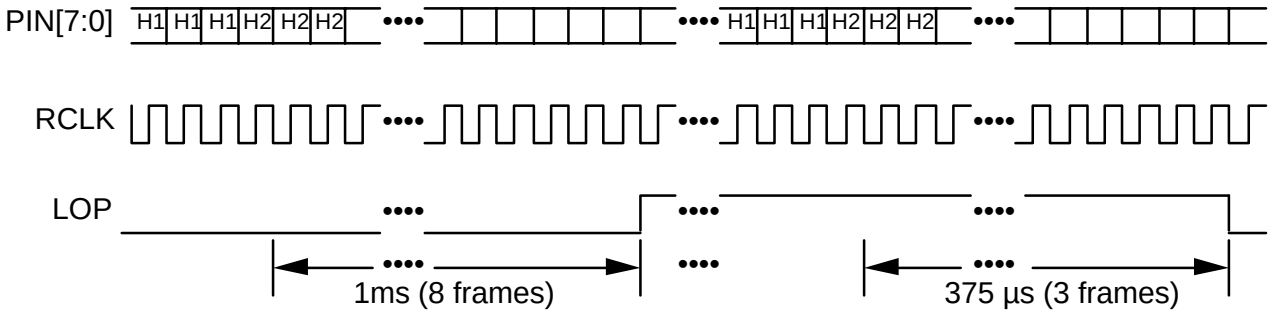
The Loss of Frame Declaration/Removal Timing Diagram (Figure 20) illustrates the operation of the LOF output. LOF is an integrated version of OOF. LOF is declared when an out of frame condition persists for 3 ms. LOF is removed when an in frame condition persists for 3 ms.

Figure 21 - Line AIS and Line FERF Declaration/Removal



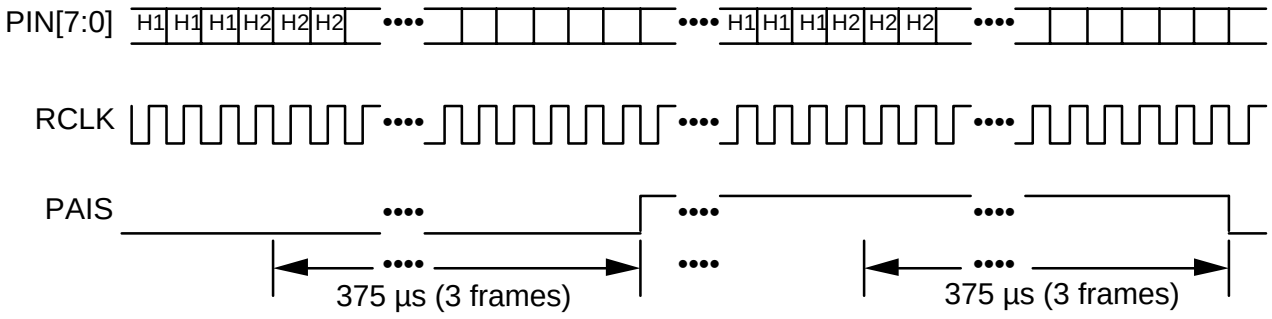
The Line AIS and Line FERF Declaration/Removal Timing Diagram (Figure 21) illustrates the operation of the LAIS and FERF outputs. LAIS (FERF) is declared when the binary pattern '111' ('110') is observed in bits 6,7, and 8 of the K2 byte for five consecutive frames. LAIS (FERF) is removed when any pattern other than the binary pattern '111' ('110') is observed in bits 6,7, and 8 of the K2 byte for five consecutive frames. LAIS and FERF may be declared or removed once per frame.

Figure 22 - Loss of Pointer Declaration/Removal



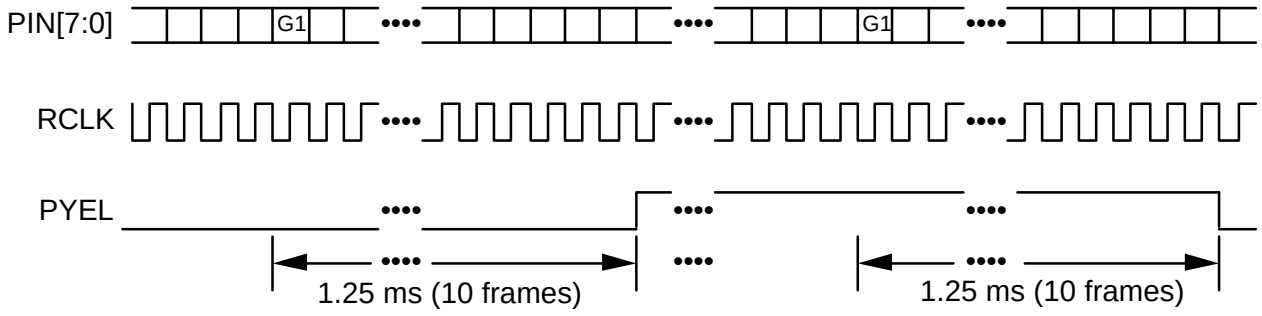
The Loss of Pointer Declaration/Removal Timing Diagram (Figure 22) illustrates the operation of the LOP output. LOP is declared when a valid pointer cannot be determined (according to the pointer interpretation rules contained in the references) for eight consecutive frames. LOP is removed as soon as a valid pointer is determined.

Figure 23 - Path AIS Declaration/Removal



The Path AIS Declaration/Removal Timing Diagram (Figure 23) illustrates the operation of the PAIS output. PAIS is declared when an all ones pattern is detected in the pointer value bytes (H1, H2) for three consecutive frames. PAIS is removed as soon as a valid pointer is determined.

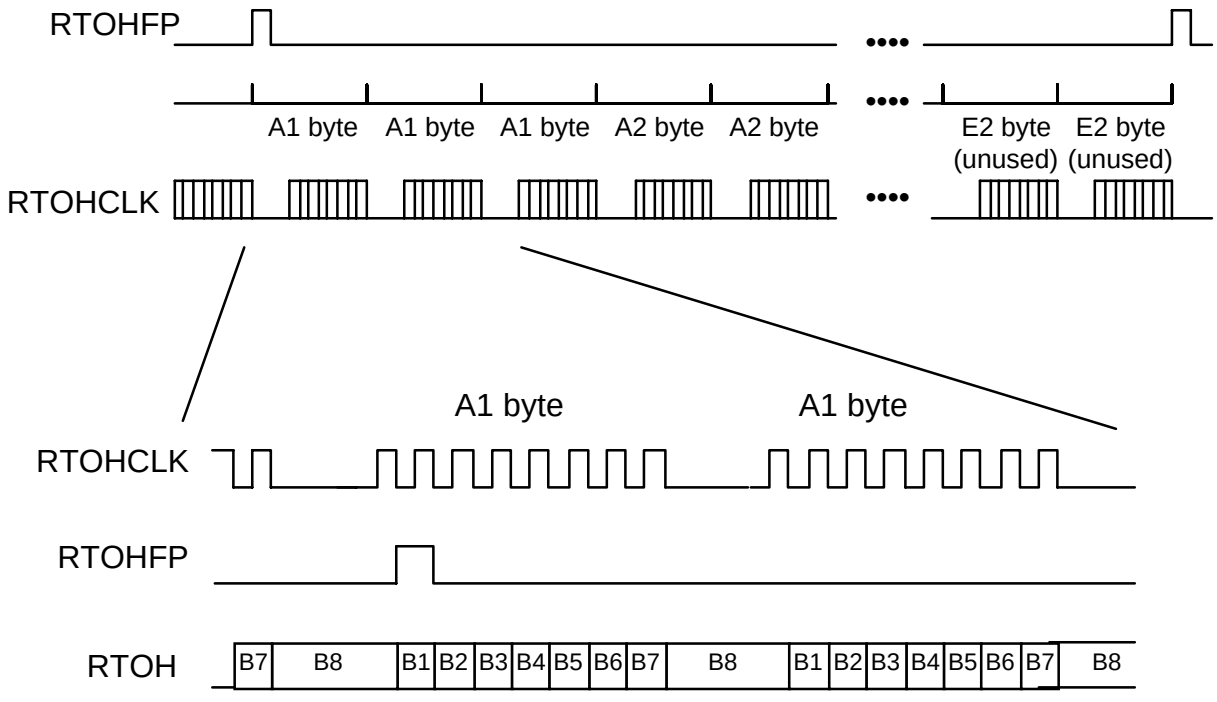
Figure 24 - Path Yellow Alarm Declaration/Removal



The Path Yellow Alarm Declaration/Removal Timing Diagram (Figure 24) illustrates the operation of the PYEL output. PYEL is declared when the yellow bit position in the path status byte (G1) is set to logic one for ten consecutive frames. PYEL is removed when the yellow bit position is set to logic zero for ten consecutive frames.

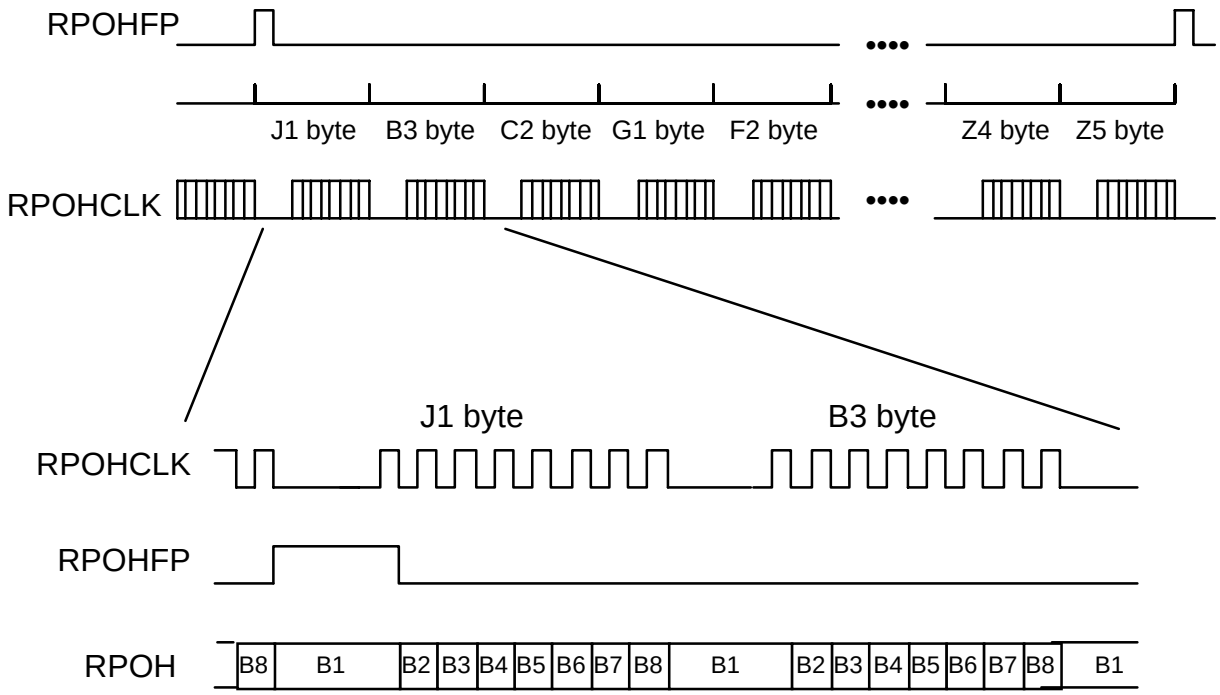
14.2 Overhead Access

Figure 25 - Transport Overhead Extraction



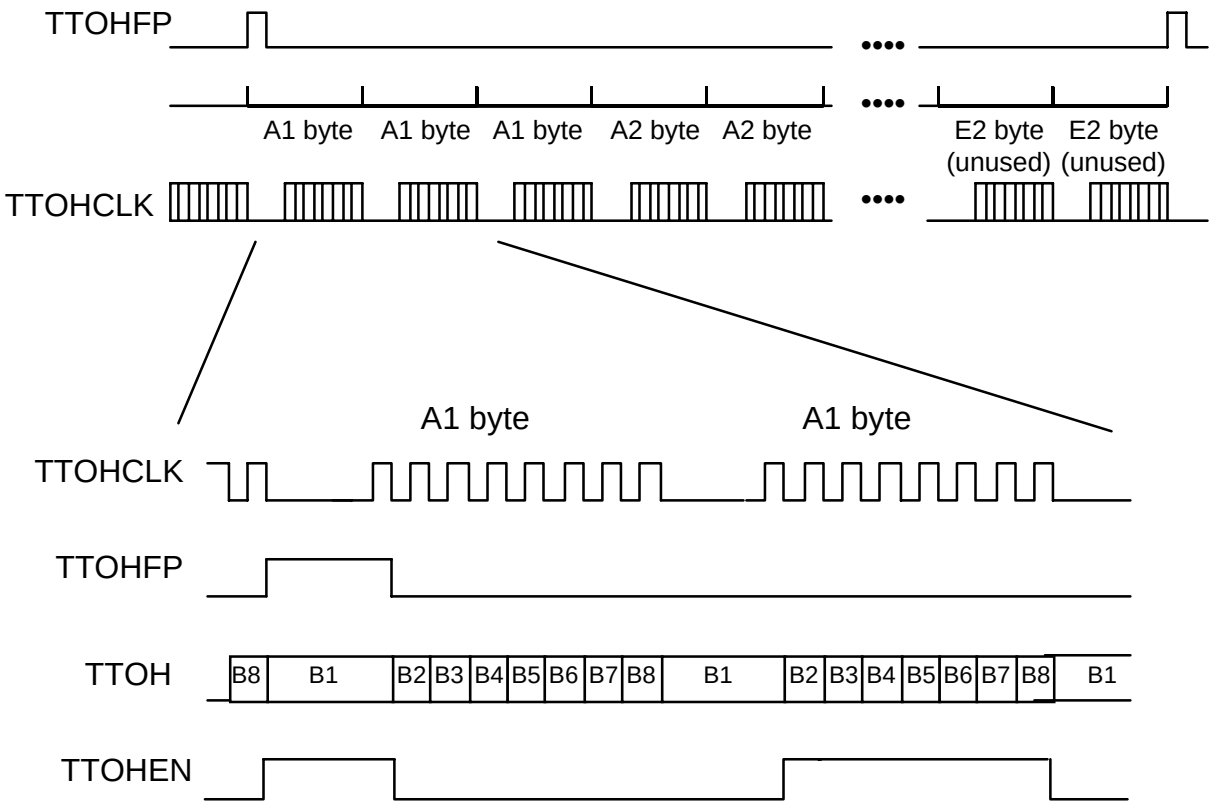
The Transport Overhead Extraction Timing Diagram (Figure 25) illustrates the transport overhead extraction interface. The transport overhead extraction clock, RTOHCLK is nominally a 5.184 MHz clock, and is derived from the receive line clock, RCLK. The entire transport overhead (the complete 9 row by 9 column structure) is extracted, serialized and output on RTOH over a frame time.

Figure 26 - Path Overhead Extraction



The Path Overhead Extraction Timing Diagram (Figure 26) illustrates the path overhead extraction interface. The path overhead extraction clock, RPOHCLK is nominally a 576 kHz clock, and is derived from the receive line clock, RCLK. The entire path overhead (the complete 9 byte structure) is extracted, serialized and output on RPOH over a frame time.

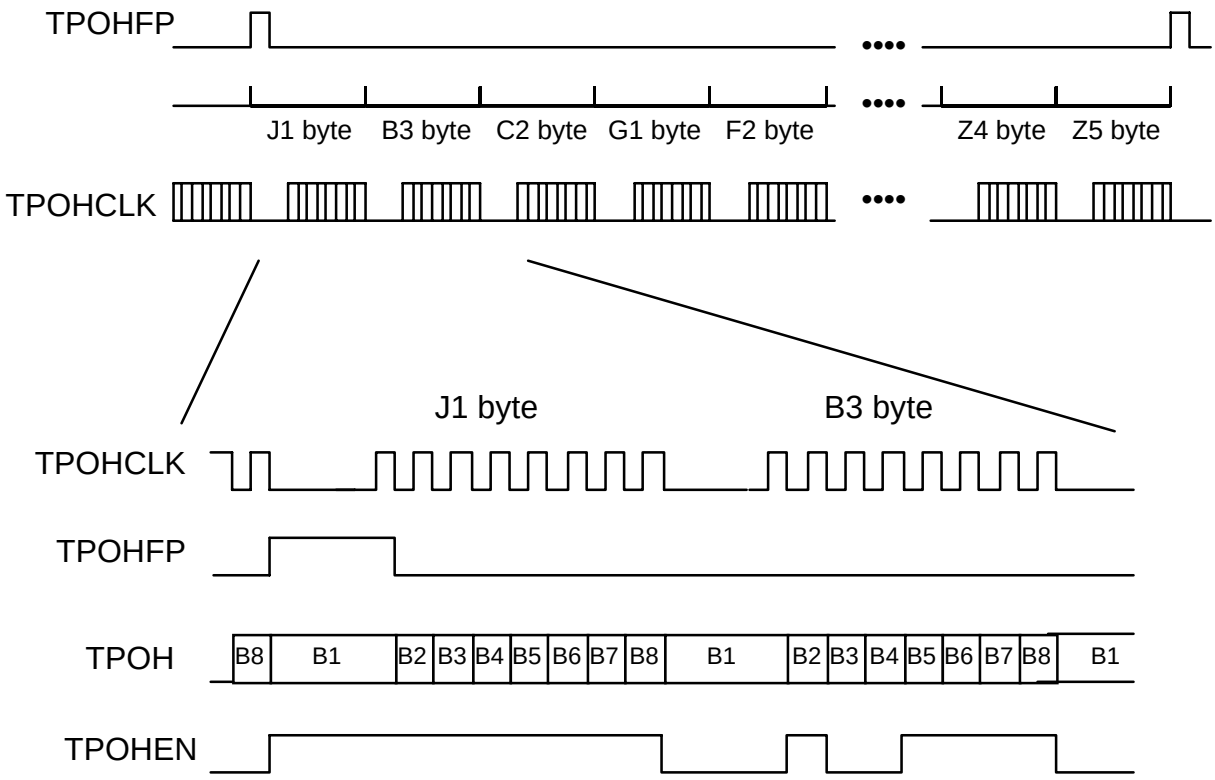
Figure 27 - Transport Overhead Insertion



The Transport Overhead Insertion Timing Diagram (Figure 27) illustrates the transport overhead insertion interface. Output TTOHCLK is nominally a 5.184 MHz clock, and is used to update output TTOHFP, and to sample input TTOH and TTOHEN. The value sampled on TTOHEN during the first overhead bit position of a given overhead byte determines whether the values sampled on TTOH are inserted in the transmit stream. In Figure 27, TTOHEN is held high during the bit 1 position of the first A1 byte in the TTOH stream. The eight bit values sampled on input TTOH during the first A1 byte period are inserted in the first A1 byte position in the STS-3c (STM-1) stream. Similarly, if TTOHEN is held low during the bit 1 position of the second A1 byte, the default value (0x28) is inserted in the second A1 byte position in the STS-3c (STM-1) stream.

An error insertion feature is also provided for the B1, B2, H1, and H2 byte positions. When TTOH is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being inserted in the STS-3c (STM-1) stream (TTOHEN must be sampled high during the first bit position to enable the error insertion mask).

Figure 28 - Path Overhead Insertion

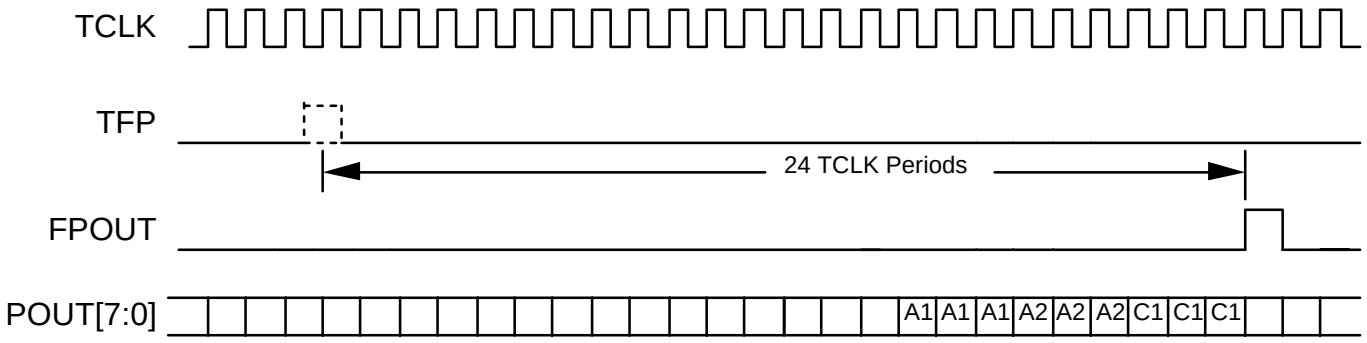


The Path Overhead Insertion Timing Diagram (Figure 28) illustrates the path overhead insertion interface. Output TPOHCLK is nominally a 576 kHz clock, and is used to update output TPOHFP, and to sample inputs TPOH and TPOHEN. In Figure 28, TPOHEN is held high throughout the eight bit positions of the J1 byte. The eight bit values sampled on input TPOH are inserted in the J1 byte position in the STS-3c/STM-1 stream. If TPOHEN was low during any of the 8 bit locations, the internally generated bit values of the corresponding bit positions would be inserted in the J1 byte.

For the B3 and H4 byte positions, an error insertion feature is provided. In Figure 28, TPOHEN is held high during bit positions 2, 5, 6, 7, and 8 of the B3 byte. The values sampled on input TPOH are used as an error mask in the corresponding bit positions (2, 5, 6, 7, and 8) of the B3 byte in the STS-3c/STM-1 stream. If TPOH and TPOHEN are high during a bit location, the corresponding bit of the internally generated B3 byte is inverted before transmission.

14.3 Line Side Transmit Interface

Figure 29 - Frame Alignment

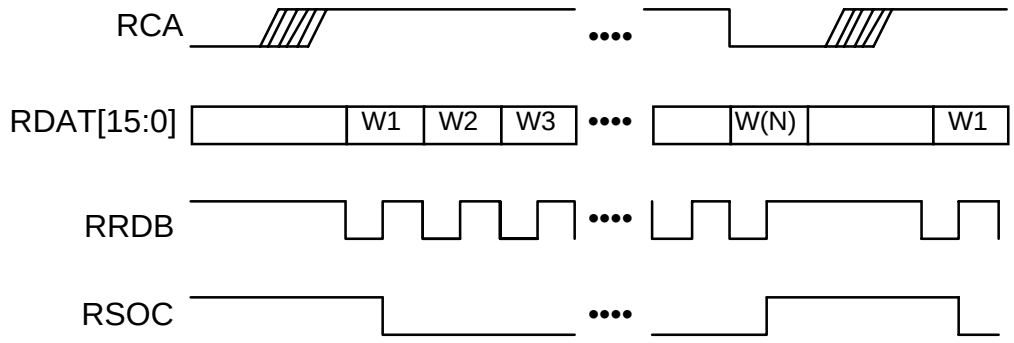


The Frame Alignment Timing Diagram (Figure 29) illustrates the alignment of the STS-3c/STM-1 transmit stream to the outgoing frame position marker (FPOUT).

Input TFP is used to align the transport overhead in the transmit stream. This alignment is useful in applications where the S/UNI is connected to a byte interleaved multiplexer (for example when multiplexing four STS-3/STM-1 streams into a single STS-12/STM-4 stream). The offset between the TFP alignment input, and the FPOUT alignment marker is 24 POCLK periods.

14.4 Drop Side Receive Interface

Figure 30 - Receive FIFO



The Receive FIFO Timing Diagram (Figure 30) illustrates the operation of the drop side receive interface. The RCA output transitions from 0 to 1 (with timing aligned to the receive line clock, RCLK) when a cell is available in the FIFO.

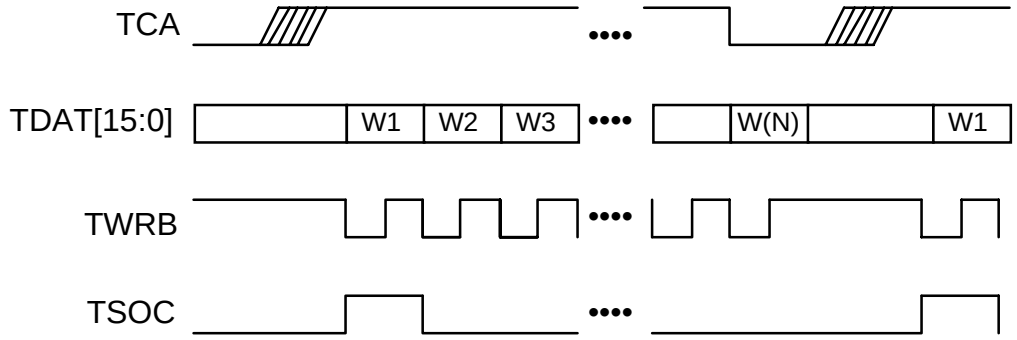
RRDB should be held high until the cell is available. Transitions on RRDB while RCA is low cause the FIFO to underrun.

When the 16 bit word interface is selected (BUS8=0), the period of RRDB should be at most 100 ns to avoid overrunning the FIFO. RSOC is high during the first word of the 27 word data structure.

When the 8 bit word interface is selected (BUS8=1), the period of RRDB should be at most 50 ns to avoid overrunning the FIFO. RSOC is high during the first word of the 53 word data structure.

14.5 Drop Side Transmit Interface

Figure 31 - Transmit FIFO



The Transmit FIFO Timing Diagram (Figure 31) illustrates the operation of the drop side transmit interface. The TCA output transitions from 0 to 1 (with timing aligned to the transmit line clock, POCLK) when the FIFO contains one empty cell. TWRB should be held high until the cell is available. Transitions on TWRB while TCA is low cause the FIFO to overrun.

When the 16 bit word interface is selected (BUS8 is tied low), TSOC is expected to be high during the first word of the 27 word data structure. It is not necessary for TSOC to be present each cell; the transmit cell write address is generated by an internal counter that flywheels in the absence of TSOC. An interrupt may be generated if TSOC is sampled high during any word other than the first word of the data structure, and the transmit cell write address counter is reset to the first word of the data structure.

When the 8 bit word interface is selected (BUS8 is tied high), TSOC is expected to be high during the first word of the 53 word data structure. It is not necessary for TSOC to be present each cell; the transmit cell write address is generated by an internal counter that flywheels in the absence of TSOC. An interrupt may be

generated if TSOC is sampled high during any word other than the first word of the data structure, and the transmit cell write address counter is reset to the first word of the data structure.

15 ABSOLUTE MAXIMUM RATINGS

Table 9 -

Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±500 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C
Power Dissipation	1.5 W

16 D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = 5 V ±5%

(Typical Conditions: T_A = 25°C, V_{DD} = 5 V)

Table 10 -

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply (VDDI[3:1], VDDO[7:1], TAVD2)	4.75	5	5.25	Volts	
V_{TAVD1}	Transmit Analog Reference Supply	4.75		5.25	Volts	$V_{PISWING}$ = 600 mV
V_{RAVD}	Receive Analog Reference Supply	4.75		5.25	Volts	$V_{PISWING}$ = 600 mV
I_{TAVD1}	Transmit Analog Reference Supply Current		2.5		mA	
I_{RAVD}	Receive Analog Reference Supply Current		3.5		mA	
I_{RVT2}	Transmit Drive Level Reference Input Current		3.5		mA	
I_{TAVD2}	PECL Driver Supply Current		44		mA	
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
$V_{PISWING}$	Input Swing (TXCI+/-, RXC+/-, RXD+/- Only)	0.6		1.0	Volts	Input swing assuming signal is AC coupled as illustrated in figures 1 and 2
V_{OL}	Output or Bidirectional Low Voltage (TTL Only)		0.1	0.4	Volts	V_{DD} = min, I_{OL} = 8 mA for outputs RCLK and POCLK. I_{OL} = 4 mA for all other digital outputs, Note 3
V_{POL}	Output Low Voltage (PECL Only)			VTERM - 0.6	Volts	Note 6
V_{OH}	Output or Bidirectional High Voltage (TTL Only)	2.4	4.7		Volts	V_{DD} = min, I_{OH} = 8 mA for outputs RCLK and POCLK. I_{OH} = 4 mA for all other digital outputs, Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			1.0	Volts	

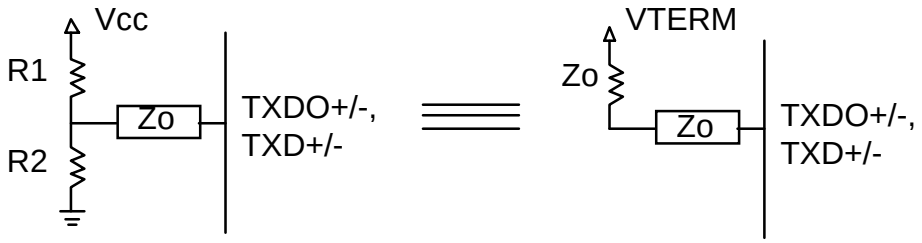
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{ILPD}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 1, 3
I_{IHPD}	Input High Current	-200	-83	-20	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP}	Operating Current Processing Cells (sum of all currents into device)			235 135	mA mA	V_{DD} = 5.25 V, Outputs unloaded TXCI+/- = 155.52 MHz RXC+/- = 155.52 MHz VDD = 5.25V, TTL Outputs unloaded, PECL interface disabled TCLK = 19.44 MHz PICLK = 19.44 MHz

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bidirectional pin with internal pull-down resistor.
5. Typical values are given as a design aid. The product is not tested to these values.

The PECL output low voltage is specified relative to the termination voltage (VTERM) as illustrated below:

Figure 32 -



$$R1 \,//\, R2 = Zo$$

$$VTERM = \frac{R2}{(R1 + R2)} * Vcc$$

This specification is applicable when the S/UNI is operated as illustrated in figures 1 and 2 (a 50Ω controlled impedance environment with R1 = 59 Ω and R2 = 312 Ω).

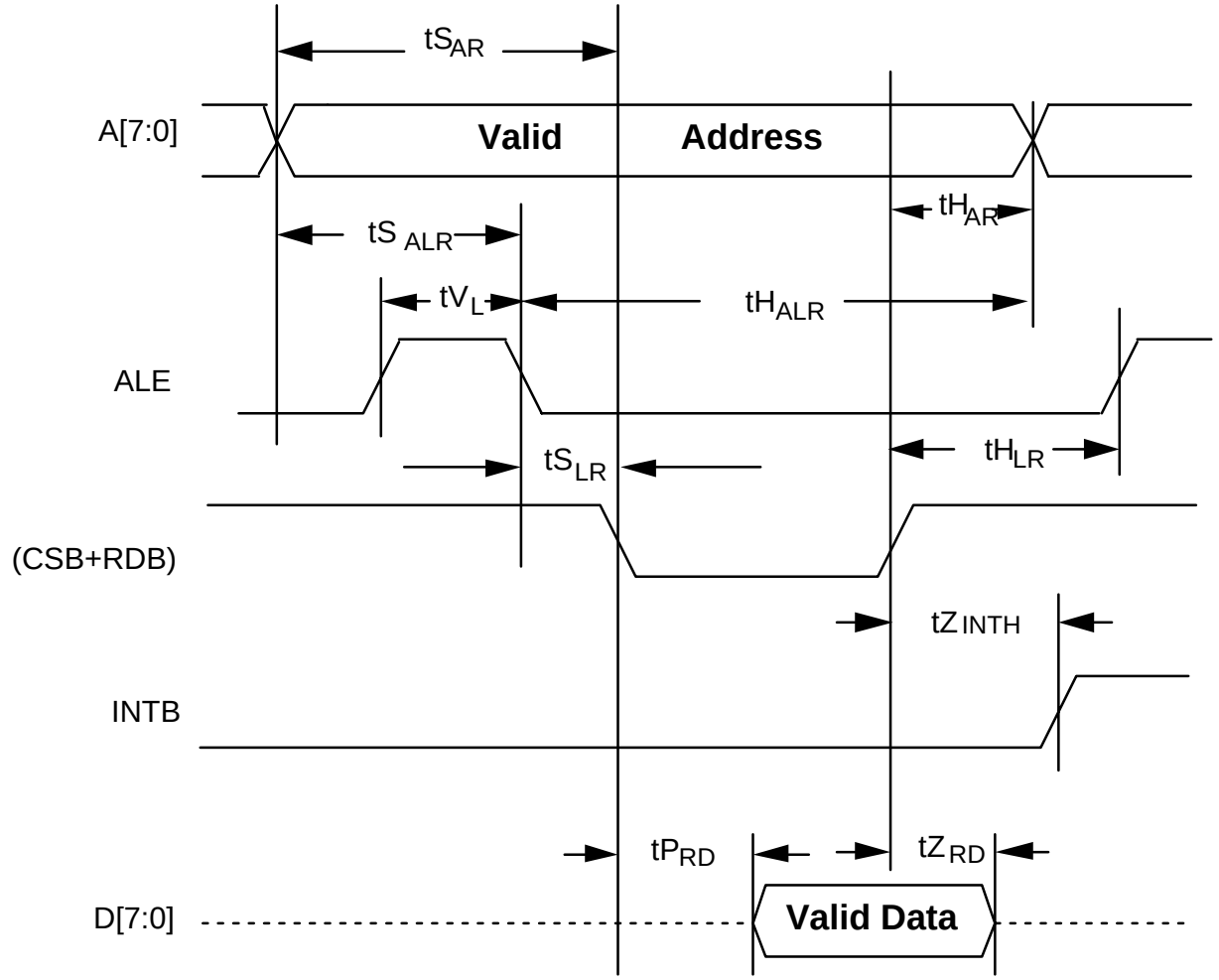
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±5%)

Table 11 - Microprocessor Interface Read Access (Figure 33)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 33 - Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.

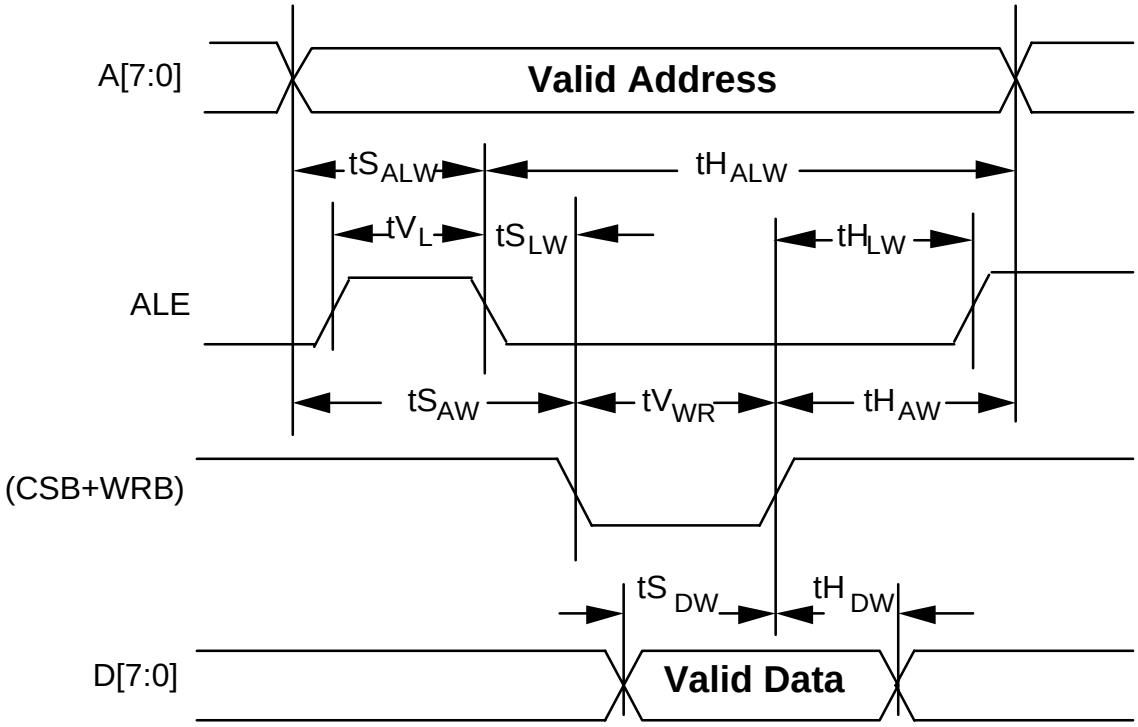
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 12 - Microprocessor Interface Write Access (Figure 34)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 34 - Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18 S/UNI TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±5%)

Table 13 - Line Side Receive Interface (Figure 35)

Symbol	Description	Min	Max	Units
	PICLK Frequency (nominally 19.44 MHz)		20	MHz
	PICLK Duty Cycle	40	60	%
	RXC+/RXC- Frequency (nominally 155.52 MHz)		156	MHz
	RXC+/RXC- Duty Cycle	40	60	%
tP_{RCLK}	PICLK Edge to RCLK Edge	2	20	ns
tP_{OOF}	PICLK Low to OOF Valid	2	30	ns
tS_{PIN}	PIN[7:0] Set-up time to PICLK	10		ns
tH_{PIN}	PIN[7:0] Hold time to PICLK	5		ns
tS_{FPIN}	FPIN Set-up time to PICLK	10		ns
tH_{FPIN}	FPIN Hold time to PICLK	5		ns
tS_{RXD}	RXD+/RXD- Setup time to rising RXC+/RXC-	2		ns
tH_{RXD}	RXD+/RXD- Hold time to rising RXC+/RXC-	1		ns

Figure 35 - Line Side Receive Interface Timing

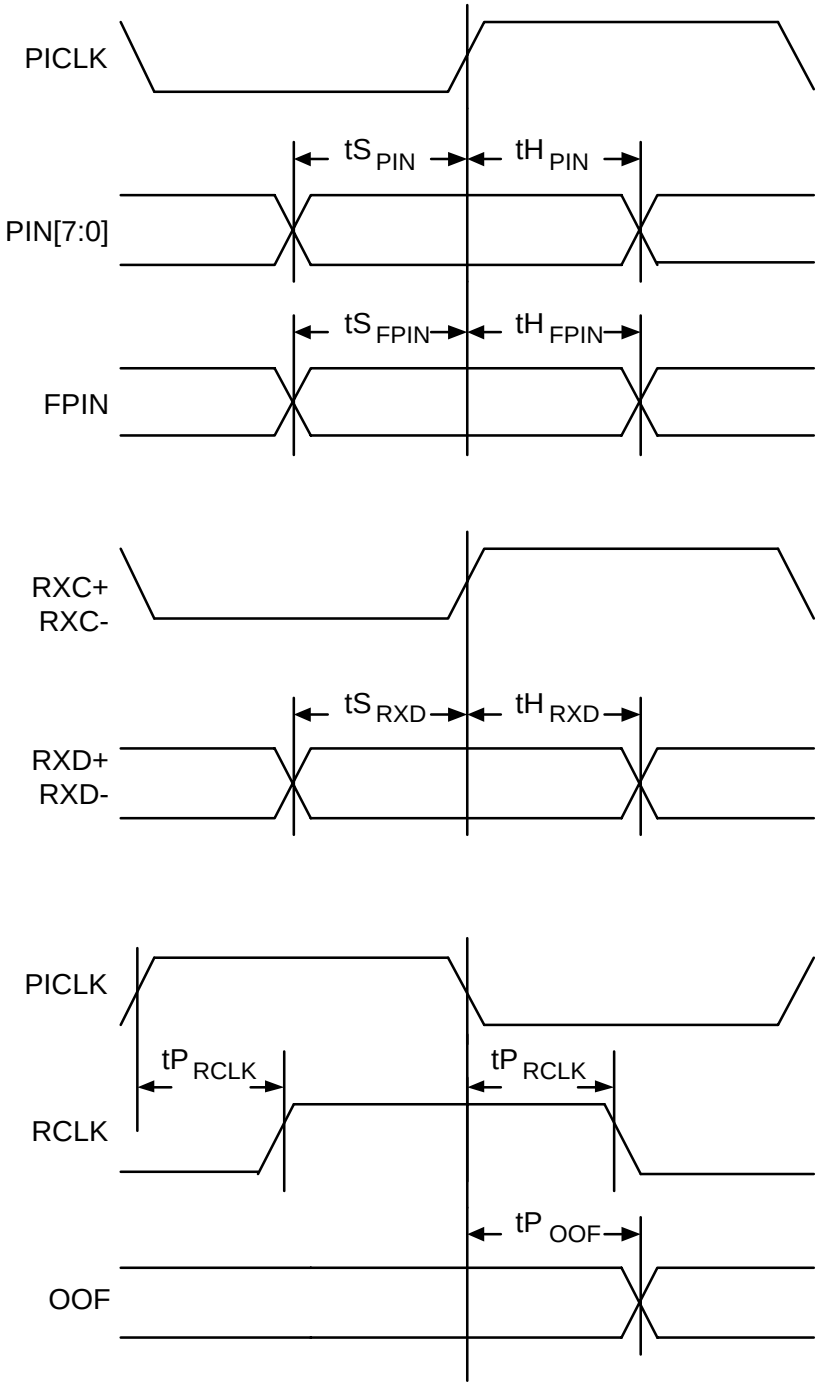


Table 14 - Receive Alarm Output (Figure 36)

Symbol	Description	Min	Max	Units
tP_{OOF}	RCLK Low to OOF Valid	3	20	ns
tP_{LOF}	RCLK Low to LOF Valid	3	20	ns
tP_{LOS}	RCLK Low to LOS Valid	3	20	ns
tP_{LAIS}	RCLK Low to LAIS Valid	3	20	ns
tP_{FERF}	RCLK Low to FERF Valid	3	20	ns
tP_{LOP}	RCLK Low to LOP Valid	3	25	ns
tP_{PAIS}	RCLK Low to PAIS Valid	3	25	ns
tP_{PYEL}	RCLK Low to PYEL Valid	3	25	ns

Figure 36 - Receive Alarm Output Timing

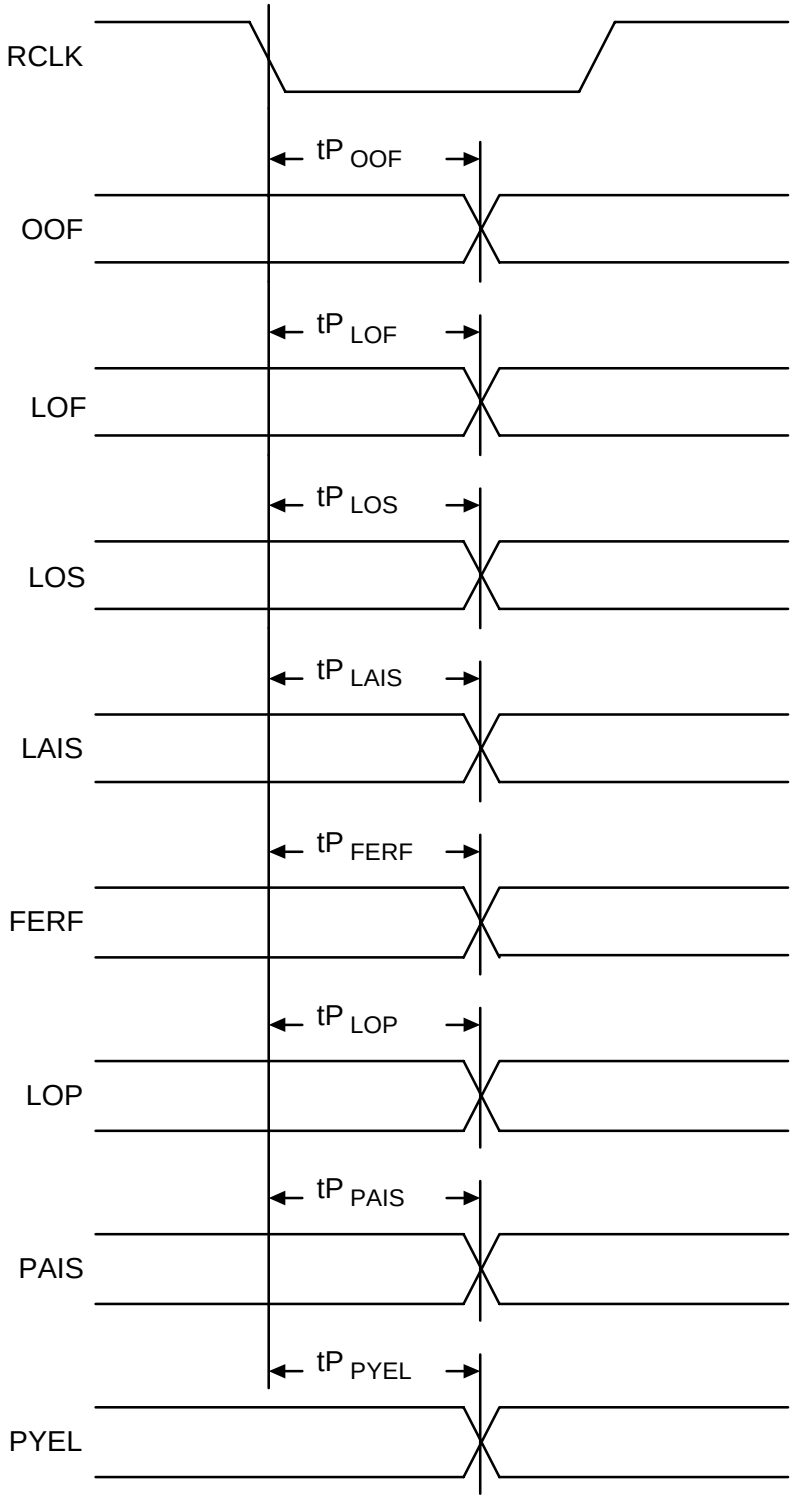


Table 15 - Receive Overhead Access (Figure 37)

Symbol	Description	Min	Max	Units
$t_{PRTOHCLK}$	RCLK High to RTOHCLK Valid	0	40	ns
$t_{PRPOHCLK}$	RCLK Low to RPOHCLK Valid	5	40	ns
t_{PRTOH}	RTOHCLK Low to RTOH Valid	-5	20	ns
$t_{PRTOHFP}$	RTOHCLK Low to RTOHFP Valid	-5	20	ns
t_{PRPOH}	RPOHCLK Low to RPOH Valid	-5	20	ns
$t_{PRPOHFP}$	RPOHCLK Low to RPOHFP Valid	-5	20	ns

Figure 37 - Receive Overhead Access Timing

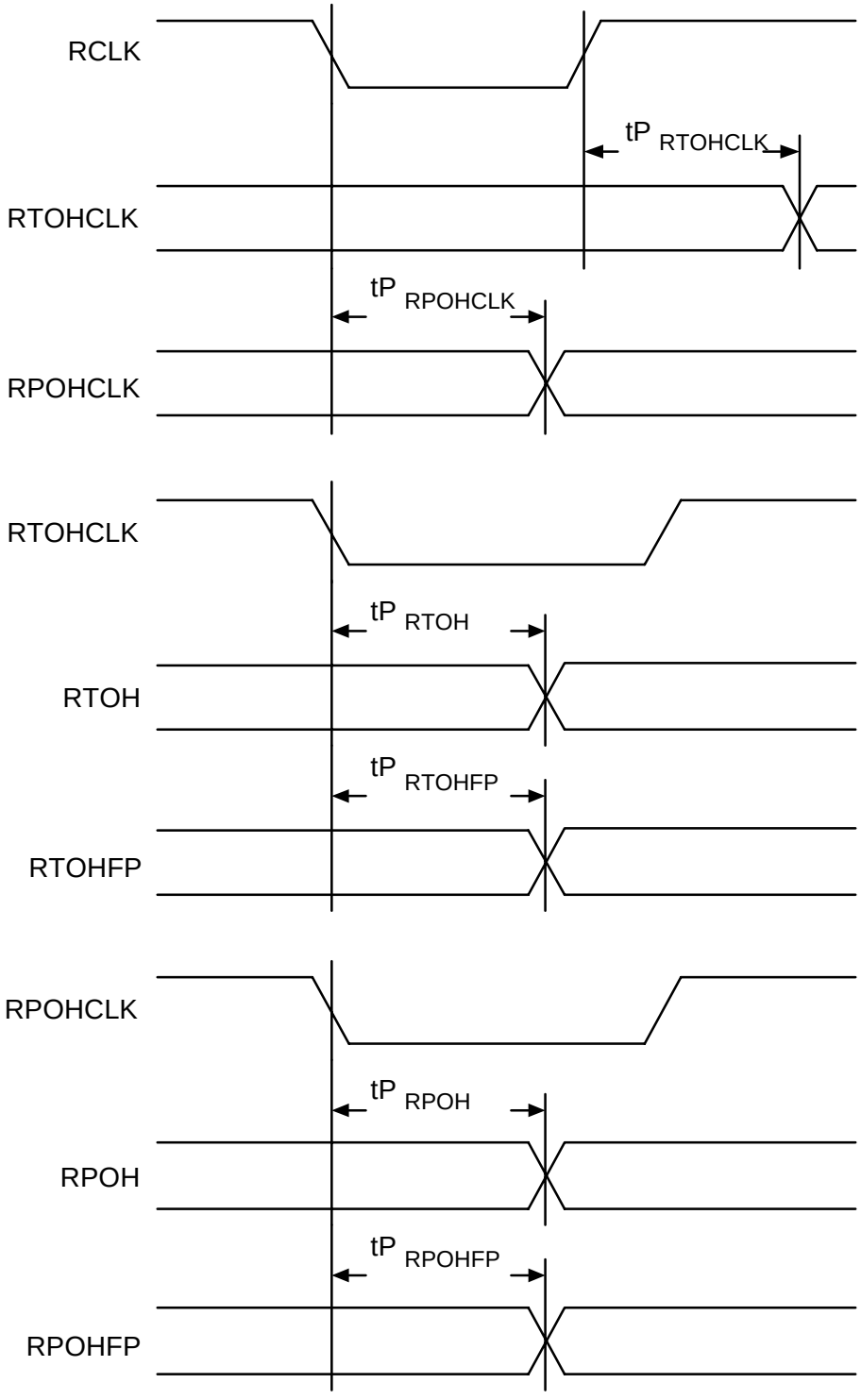


Table 16 - Line Side Transmit Interface (Figure 38)

Symbol	Description	Min	Max	Units
	TCLK Frequency (nominally 19.44 MHz)		20	MHz
	TCLK Duty Cycle	40	60	%
	TXCI+/TXCI- Frequency (nominally 155.52 MHz)		156	MHz
	TXCI+/TXCI- Duty Cycle	40	60	%
tP_{POCLK}	TCLK Edge to POCLK Edge	3	20	ns
tP_{FPOUT}	TCLK High to FPOUT Valid	3	20	ns
tP_{POUT}	TCLK High to POUT Valid	3	20	ns
tS_{TFP}	TFP Set-up time to TCLK	10		ns
tH_{TFP}	TFP Hold time to TCLK	5		ns
tP_{TXD}	TXCO+/TXCO- Low to TXD+/TXD- Valid	-1	1	ns

Figure 38 - Line Side Transmit Interface Timing

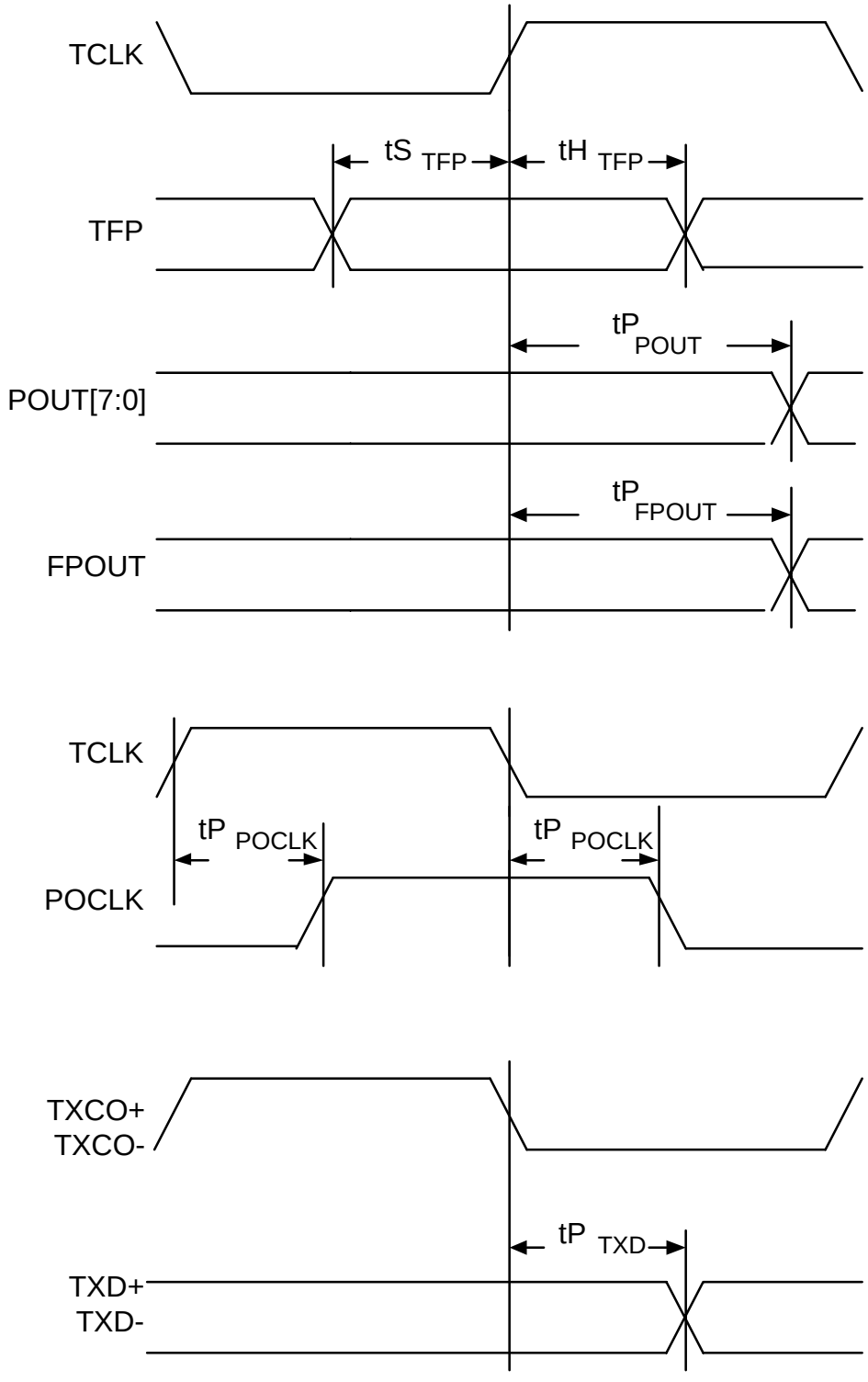


Table 17 - Transmit Alarm Input (Figure 39)

Symbol	Description	Min	Max	Units
tS_{TLAIS}	TLAIS Set-up time to POCLK	10		ns
tH_{TLAIS}	TLAIS Hold time to POCLK	5		ns
tS_{TFERF}	TFERF Set-up time to POCLK	10		ns
tH_{TFERF}	TFERF Hold time to POCLK	5		ns
tS_{TPAIS}	TPAIS Set-up time to POCLK	10		ns
tH_{TPAIS}	TPAIS Hold time to POCLK	5		ns
tS_{TPYEL}	TPYEL Set-up time to POCLK	10		ns
tH_{TPYEL}	TPYEL Hold time to POCLK	5		ns

Figure 39 - Transmit Alarm Input Timing

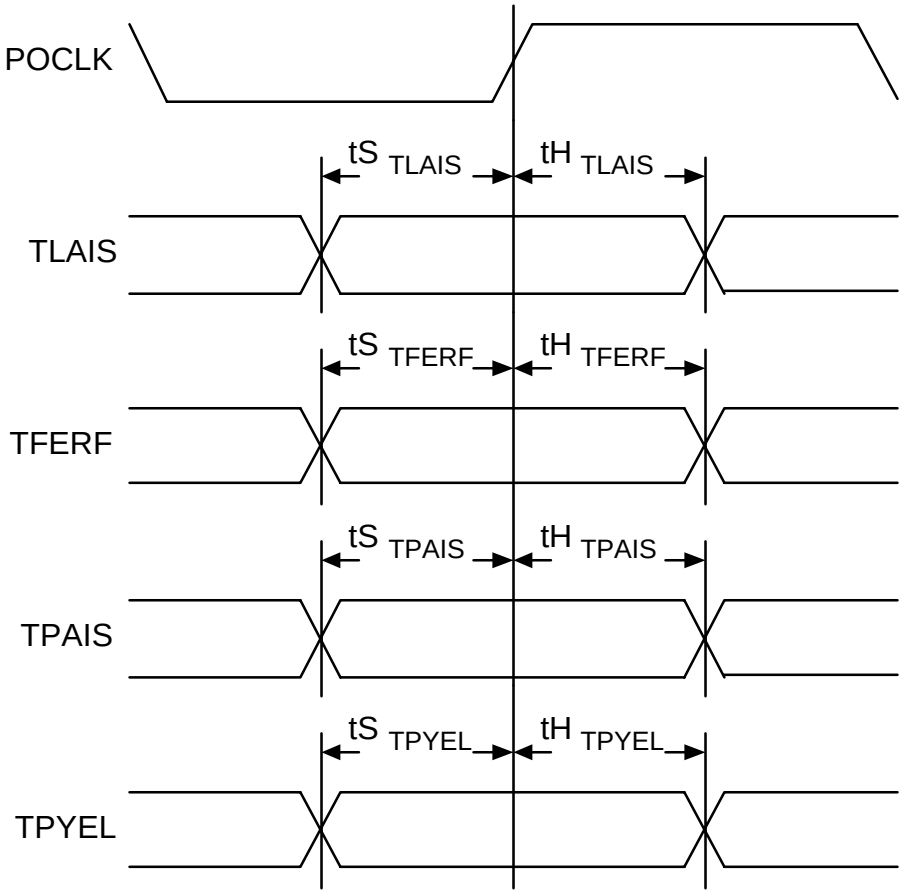
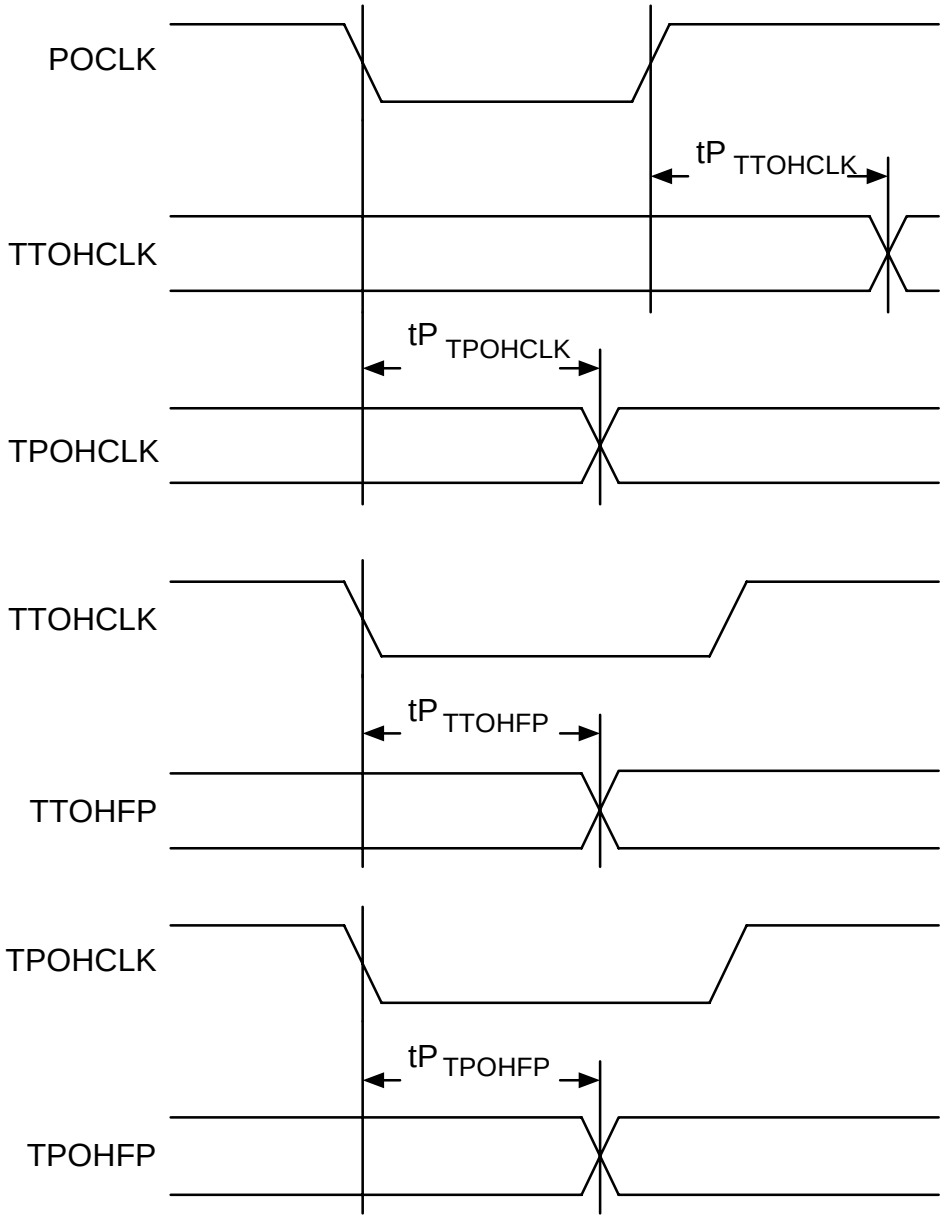


Table 18 - Transmit Overhead Access (Figure 40)

Symbol	Description	Min	Max	Units
$t_{PTTOHCLK}$	POCLK High to TTOHCLK Valid	-5	20	ns
$t_{PTPOHCLK}$	POCLK Low to TPOHCLK Valid	-5	20	ns
$t_{PTTOHFP}$	TTOHCLK Low to TTOHFP Valid	-5	20	ns
$t_{PTPOHFP}$	TPOHCLK Low to TPOHFP Valid	-5	20	ns
t_{STTOH}	TTOH Set-up time to TTOHCLK	25		ns
t_{HTTOH}	TTOH Hold time to TTOHCLK	5		ns

Symbol	Description	Min	Max	Units
tS_{TOHEN}	TTOHEN Set-up time to TTOHCLK	25		ns
tH_{TOHEN}	TTOHEN Hold time to TTOHCLK	5		ns
tS_{TPOH}	TPOH Set-up time to TPOHCLK	25		ns
tH_{TPOH}	TPOH Hold time to TPOHCLK	5		ns
tS_{POHEN}	TPOHEN Set-up time to TPOHCLK	25		ns
tH_{POHEN}	TPOHEN Hold time to TPOHCLK	5		ns

Figure 40 - Transmit Overhead Access Timing



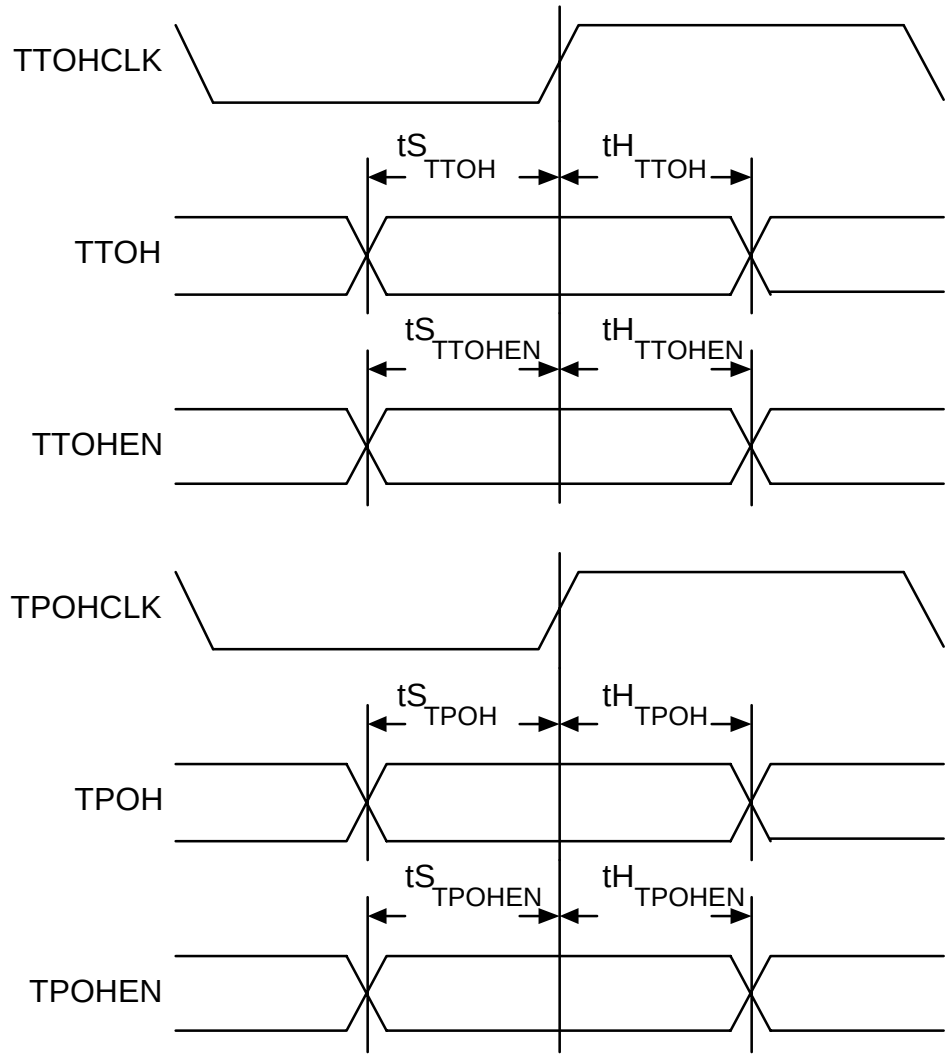


Table 19 - Drop Side Receive Interface (Figure 41)

Symbol	Description	Min	Max	Units
tR_{CYC}	FIFO Read Cycle Time	40		ns
tV_{RRDB}	Valid FIFO Read Pulse Width	15		ns
tV_{RRDBH}	FIFO Read High Pulse Width	17		ns
tP_{RDAT}	RRDB Low to RDAT[15:0] Valid	2	16	ns
tP_{RCA}	RRDB Low to RCA Low Valid	2	17	ns

Symbol	Description	Min	Max	Units
tP_{RSOC}	RRDB High to RSOC Valid	2	19	ns

Figure 41 - Drop Side Receive Interface Timing (TSEN = 0)

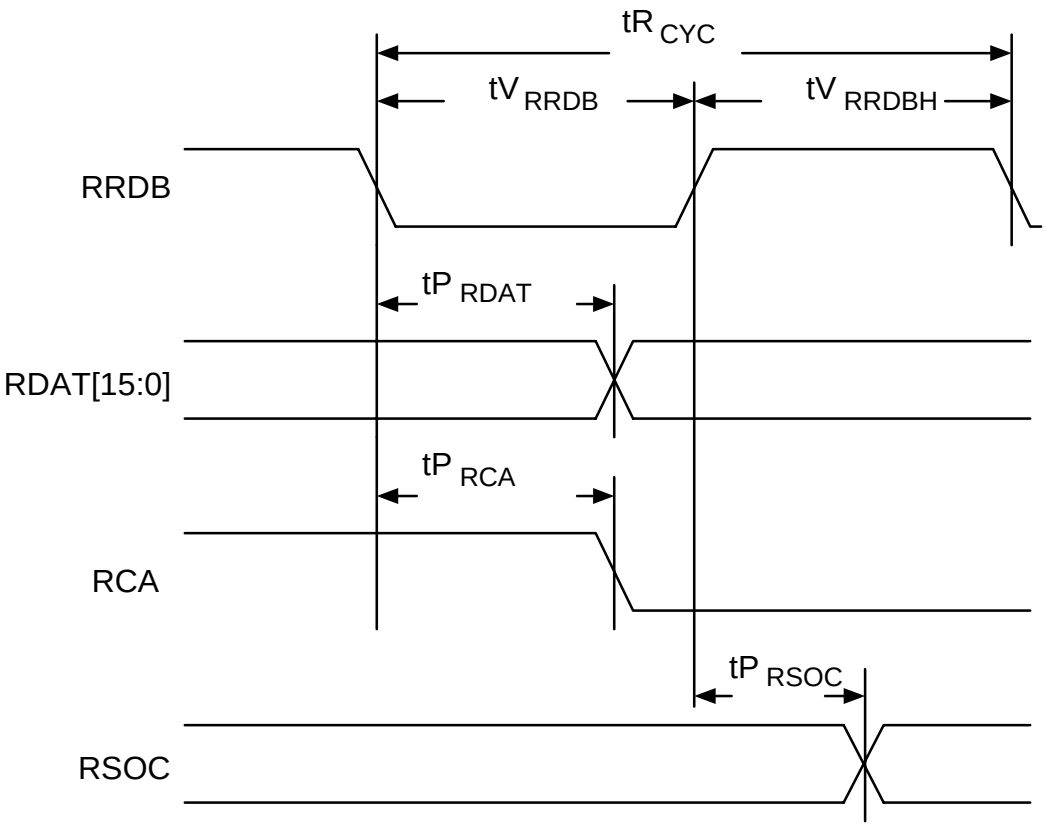


Table 20 - Drop Side Receive Interface (Figure 42)

Symbol	Description	Min	Max	Units
tR_{CYC}	FIFO Read Cycle Time	40		ns
tV_{RRDB}	Valid FIFO Read Pulse Width	15		
tV_{RRDBH}	FIFO Read High Pulse Width	17		
tP_{RDAT}	RRDB Low to RDAT[15:0] Valid	2	16	ns
tZ_{RDAT}	RRDB High to RDAT[15:0] Tristate	2	15	ns

Symbol	Description	Min	Max	Units
tP_{RCA}	RRDB Low to RCA Low Valid	2	17	ns
tP_{RSOC}	RRDB High to RSOC Valid	2	19	ns

Figure 42 - Drop Side Receive Interface Timing (TSEN = 1)

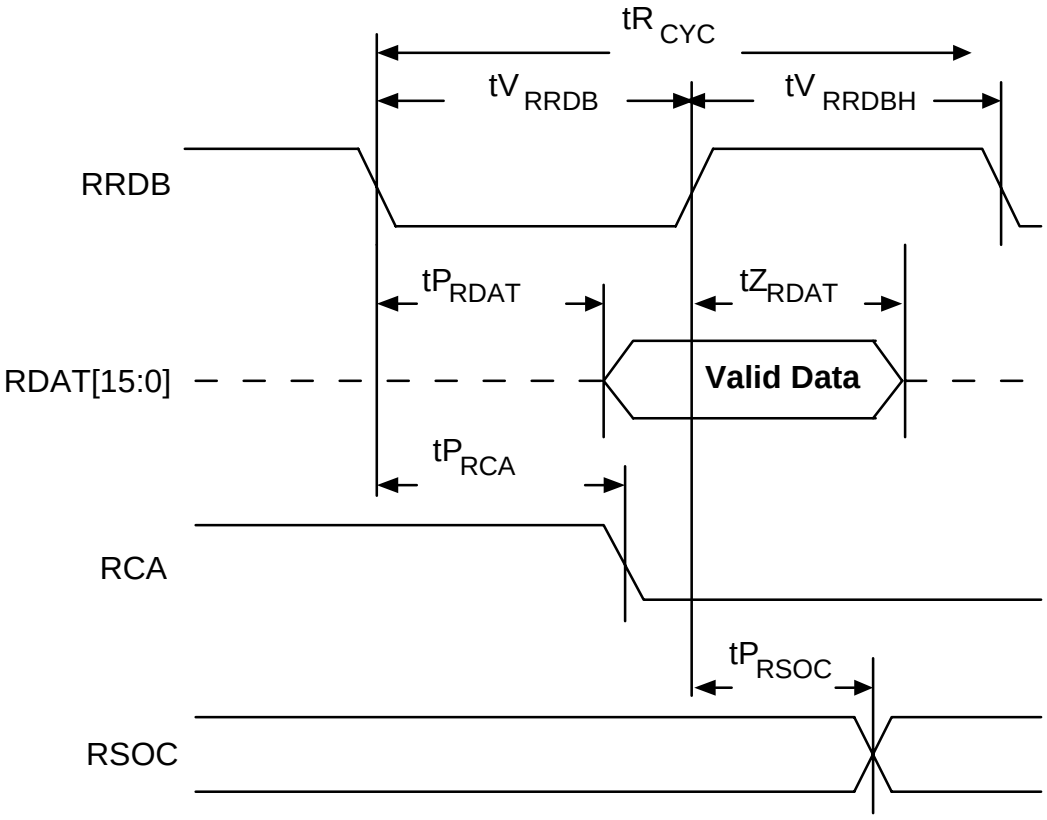


Table 21 - Drop Side Transmit Interface (Figure 43)

Symbol	Description	Min	Max	Units
tW_{CYC}	FIFO Write Cycle Time	40		ns
tV_{TWRB}	Valid FIFO Write Pulse Width	15		ns
tV_{TWRBH}	FIFO Write High Pulse Width	17		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TWRB	5		ns

Symbol	Description	Min	Max	Units
tH_{TDAT}	TDAT[15:0] Hold time to TWRB	5		ns
tS_{TSOC}	TSOC Set-up time to TWRB	5		ns
tH_{TSOC}	TSOC Hold time to TWRB	5		ns
tP_{TCA}	TWRB Low to TCA Valid	2	19	ns

Figure 43 - Drop Side Transmit Interface

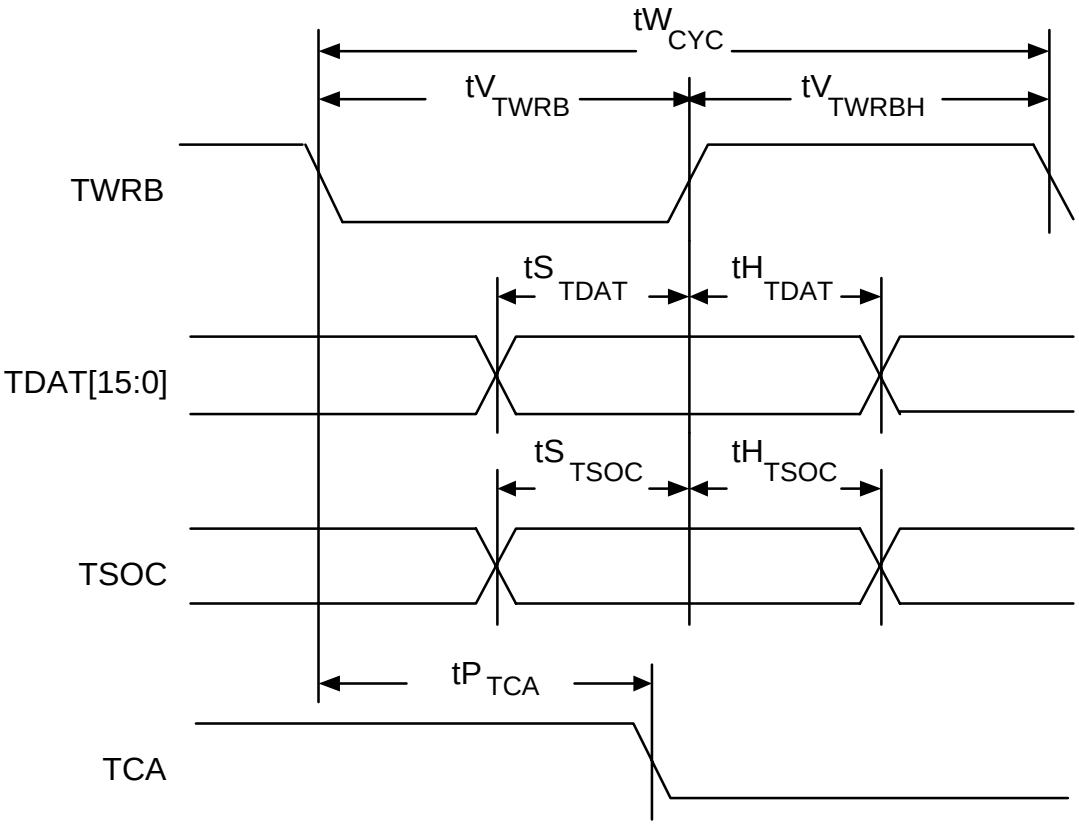
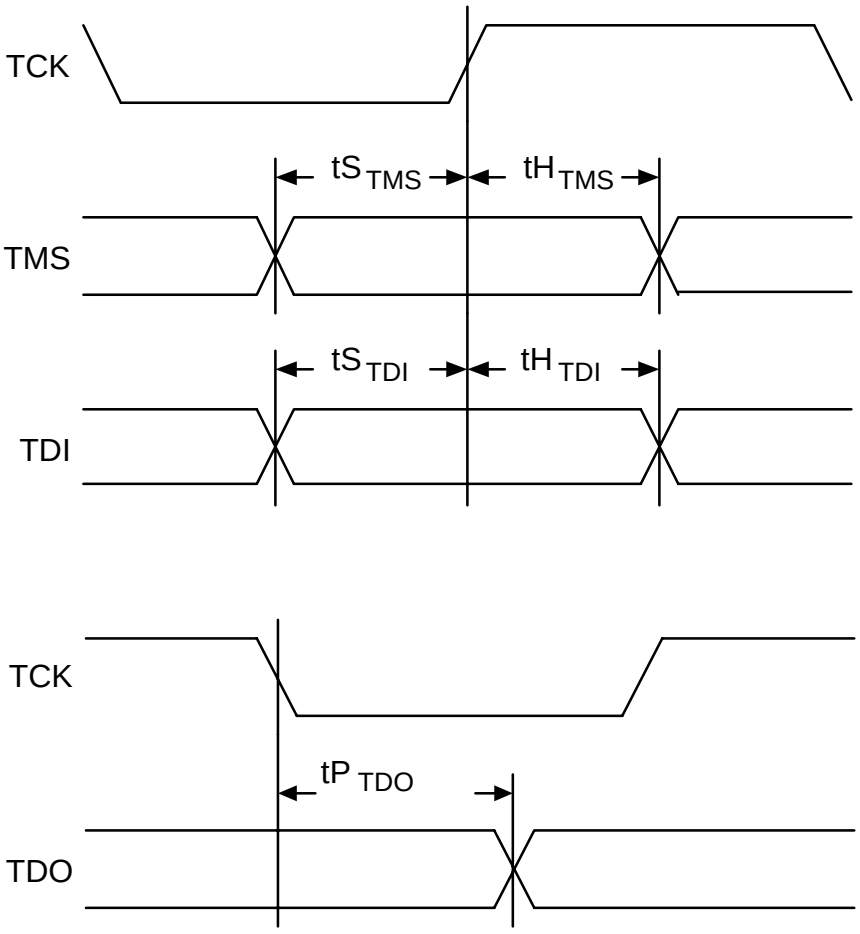


Table 22 - JTAG Port Interface (Figure 44)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%

Symbol	Description	Min	Max	Units
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

Figure 44 - JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between a TTL input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between a TTL input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. When a set-up time is specified between a PECL input and a clock, the set-up time is the time in nanoseconds from the crossing point of the input to the crossing point of the clock.

4. When a hold time is specified between a PECL input and a clock, the hold time is the time in nanoseconds from the crossing point of the input to the crossing point of the clock.

Notes on Output Timing:

1. TTL output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. PECL output propagation delay time is the time in nanoseconds from the crossing point of the reference signal to the crossing point of the output.

3. Maximum and minimum TTL output propagation delays are measured with a 50 pF load on the outputs.

4. Maximum and minimum PECL output propagation delays are measured with the PECL outputs terminated into a 50Ω equivalent load.

19 ORDERING AND THERMAL INFORMATION

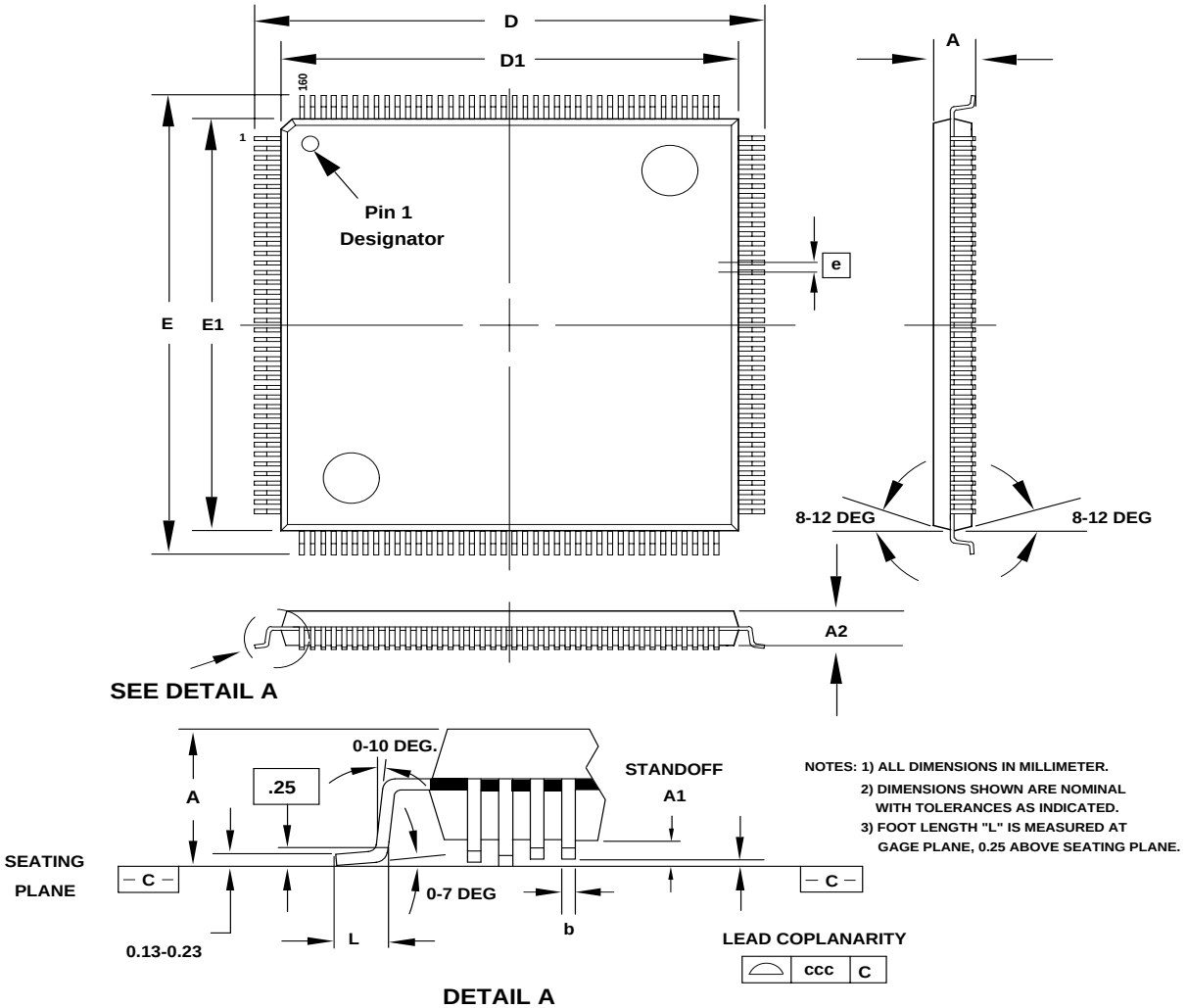
Table 23 -

PART NO.	DESCRIPTION
PM5345-RC	160 Pin Copper Leadframe Plastic Quad Flat Pack (PQFP)

Table 24 -

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5345-RC	0°C to 70°C	47 °C/W	14 °C/W

20 MECHANICAL INFORMATION



DETAIL A

NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOLERANCES AS INDICATED.
3) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, 0.25 ABOVE SEATING PLANE.

PACKAGE TYPE: 160 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.42	0.25	3.17	30.95	27.85	30.95	27.85	0.73		0.22	
Nom.			3.42	31.20	28.00	31.20	28.00	0.88	0.65		
Max.	4.07	0.39	3.68	31.45	28.10	31.45	28.10	1.03		0.38	0.10

NOTES

NOTES

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