PM5381

S/UNI-® 2488

S/UNI-2488

SATURN USER NETWORK INTERFACE FOR 2488 MBIT/S

DATASHEET

PROPRIETARY AND CONFIDENTIAL

PRELIMINARY

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1 FEATURES

1.1 General

- Single chip ATM and POS User-Network Interface operating at 2488.32 Mbit/s.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615(1619)/1662 of the PPP Working Group of the Internet Engineering Task Force (IETF).
- Processes bit-serial 2488.32 Mbit/s STS-48 (STM-16-16c) data streams with on-chip clock and data recovery and clock synthesis.
- Complies with Bellcore GR-253-CORE jitter tolerance, jitter transfer and intrinsic jitter criteria.
- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section and High Order Path overhead.
- Provides UTOPIA Level 3 32-bit wide System Interface (clocked up to 104 MHz) with parity support for ATM applications.
- Provides SATURN POS-PHY Level 3™ 32-bit System Interface (clocked up to 104 MHz) for Packet over SONET (POS), or ATM applications.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from the line side transmit stream to the line side receive stream interface.
- Provides support for automatic protection switching via a 4-bit LVDS 777.76 MHz port.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8V CMOS core logic with 3.3V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and outputs are 3.3V compatible.
- Industrial temperature range (-40C to +85C).
- 416 pin UBGA package.

1.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) and the section trace byte (J0) into the transmit stream; descrambles the received stream and scrambles the transmit stream.
- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 and B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the M1 byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B1 errors.
- Extracted and optionally inserts on dedicated pins the SONET/SDH transport overhead for an STS-48c/STM-16c frame.
- Extracts and serializes on dedicated pins the data communication channels (D1-D3, D4-D12) and inserts the corresponding signals into the transmit stream.
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers. Inserts the APS channel into the transmit stream.
- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream. Inserts the synchronization status message (S1) byte into the transmit stream.
- Extracts a 64 byte (Bellcore compatible) or 16 byte (ITU compatible) section trace (J0) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the accepted message via the microprocessor port. Inserts a 64 byte or 16 byte section trace (J0) message using an internal register bank for the transmit stream.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), and protection switching byte failure alarms on the receive stream.
- Configurable to force Line AIS in the transmit stream.
- Provides automatic transmit line RDI insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).
- Provides automatic DROP bus line AIS insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).
- Support Automatic Protection Switching (APS) via a serial 4x777.76 LVDS mate protection port.

1.3 SONET Path / SDH High Order Path

- Interprets the received payload pointer (H1, H2) and extracts the STS-48c/STM-16c synchronous payload envelope and path overhead.
- Detects loss of pointer (LOP), path alarm indication signal (PAIS) and path (normal and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream.
- Extracts and insert the entire SONET/SDH path overhead to and from dedicated pins. The path overhead bytes may be sourced from internal registers or from bit serial path overhead input stream. Path overhead insertion may also be disabled.
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ) and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream.
- Extracts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the captured, accepted and expected message via the microprocessor port. Inserts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the transmit stream.
- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.
- Counts received path remote error indications (REI's) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block basis independent of the accumulation of BIP-8 errors.
- Provides automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (LAIS, LOP, LOPCON, PAIS, PAISCON, PTIM, PTIU, PLM, PLU, UNEQ, PDI).

1.4 The Receive ATM Processor

- Extracts ATM cells from the received STS-48c/STM16-16c channel payloads using ATM cell delineation.
- Provides ATM cell payload de-scrambling.
- Performs header check sequence (HCS) error detection and correction, and idle/unassigned cell filtering.
- Detects out of cell delineation (OCD) and loss of cell delineation (LCD) alarms.

- Counts number of received cells, idle cells, erred cells and dropped cells.
- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide datapath interfaces (clocked up to 104 MHz) with parity support to read extracted cells from an internal 8 cell FIFO buffer.

1.5 The Receive POS Processor

- Supports packet based link layer protocols using byte synchronous HDLC framing.
- Performs self-synchronous POS data de-scrambling on the received STS-48c/STM16c-16c payloads using the $x^{43}+1$ polynomial.
- Performs flag sequence detection and terminates the received POS frames.
- Performs frame check sequence (FCS) validation for CRC-CCITT and CRC-32 polynomials.
- Performs control escape de-stuffing or byte de-stuffing of the POS stream.
- Detects packet abort sequence.
- Checks for minimum and maximum packet lengths. Optionally deletes short packets and marks those exceeding the maximum length as erred.
- Permits FCS stripping on the POS-PHY output data stream.
- Provides a SATURN POS-PHY Level 3 compliant 32-bit datapath interface (clocked up to 104 MHz) with parity support to read packet data from an internal 256 byte FIFO buffer.

1.6 The Transmit ATM Processor

- Provides idle/unassigned cell insertion.
- Optionally provides HCS generation/insertion, and ATM cell payload scrambling.
- Counts the number of transmitted cells.
- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide datapath interfaces (clocked up to 104 MHz) with parity support for writing cells into an internal channel FIFO.

1.7 The Transmit POS Processor

- Supports any packet based link layer protocol using byte synchronous and bit synchronous framing like PPP, HDLC and Frame Relay.
- Performs self-synchronous POS data scrambling using the $1+X^{43}$ polynomial.

- Encapsulates packets within a POS/HDLC frame.
- Performs flag sequence insertion.
- Performs byte stuffing for transparency processing.
- Optionally performs frame check sequence generation using the CRC-CCITT and CRC-32 polynomials.
- Aborts packets under the direction of the host or when the FIFO underflows.
- Provides a SATURN POS-PHY Level 3 compliant 32-bit wide datapath (clocked up to 104 MHz) with parity support to an internal FIFO buffer.

2 APPLICATIONS

- ATM/ Multi-service Enterprise, Access, Edge and Core switches
- Packet Over Sonet interfaces for Access, Edge and Core routers
- SONET/SDH Add/Drop Multiplexers and Terminal Multiplexers with data processing capabilities
- DWDM Optical networking equipment requiring SONET/SDH capabilities
- Network Interface Cards and Uplinks

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4 DEFINITIONS

The following table defines the abbreviations for the S/UNI-2488.

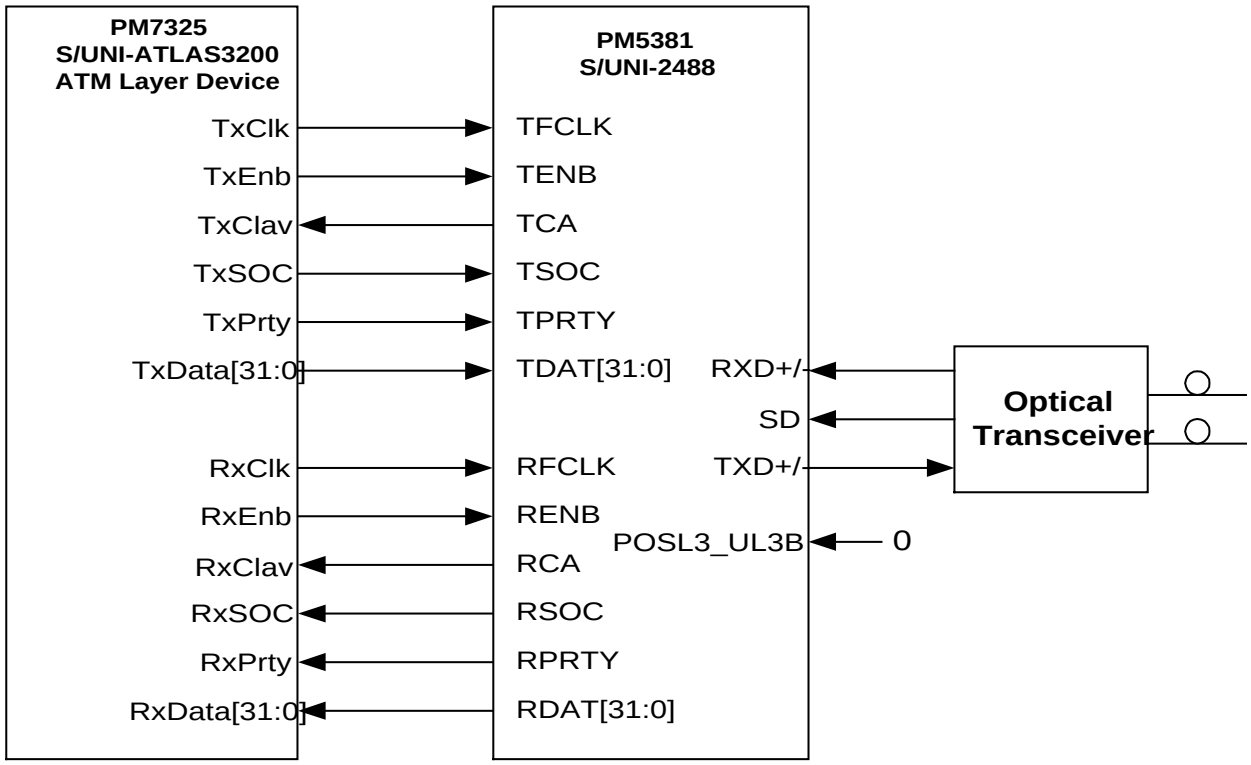
ATM	Asynchronous Transfer Mode
CSU	Clock Synthesis Unit
DRU	Data Recovery Unit
FCS	Frame Check Sequence
FIFO	First-In-First-Out storage element
HCS	Header Check Sequence
LVDS	Low Voltage Differential Signaling
NNI	Network-to-Network Interface
POS	Packet Over SONET
PRGM	PRBS Generator and Monitor
RCFP	Receive Cell and Frame Processor Block
RHPP	Receive High order Path Processor
RRMP	Receive Regenerator Multiplexer Processor
RTTP	Received Tail Trace Processor
RXSDQ	Receive Scalable Data Queue FIFO
RXSIF	Receive Slave Interface (UL3 or POS L3)
SRLI	SONET/SDH Receive Line Interface
STLI	SONET/SDH Transmit Line Imterface
STSI	SONET/SDH Time Slot Interchange
SVCA	SONET/SDH Virtual Container Aligner
TCFP	Transmit Cell and Frame Processor Block
THPP	Transmit High order Path Processor
TRMP	Transmit Regenerator Multiplexer Processor
TTTP	Transmit Tail Trace Processor
TXSIF	Transmit Slave Interface (UL3 or POS L3)

5 APPLICATION EXAMPLES

The PM5381 S/UNI-2488 is applicable to equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interfaces (UNI), ATM Network-Network Interfaces (NNI), as well as Packet over SONET (POS) interfaces. The POS interface can support several packet based protocols, including the Point-to-Point Protocol (PPP). The S/UNI-2488 may find application at either end of switch-to-switch links, router to router links, switch to router links or switch-to-terminal links, in public and privite wide area networks (WAN). The S/UNI-2488 provides a comprehensive feature set as well as full compliance to WAN synchronization requirements. The S/UNI-2488 performs the mapping of either ATM cells or POS frames into the SONET/SDH STS-48 (STM-16-16c) synchronous payload envelope (SPE) and processes applicable SONET/SDH section, line and path overheads.

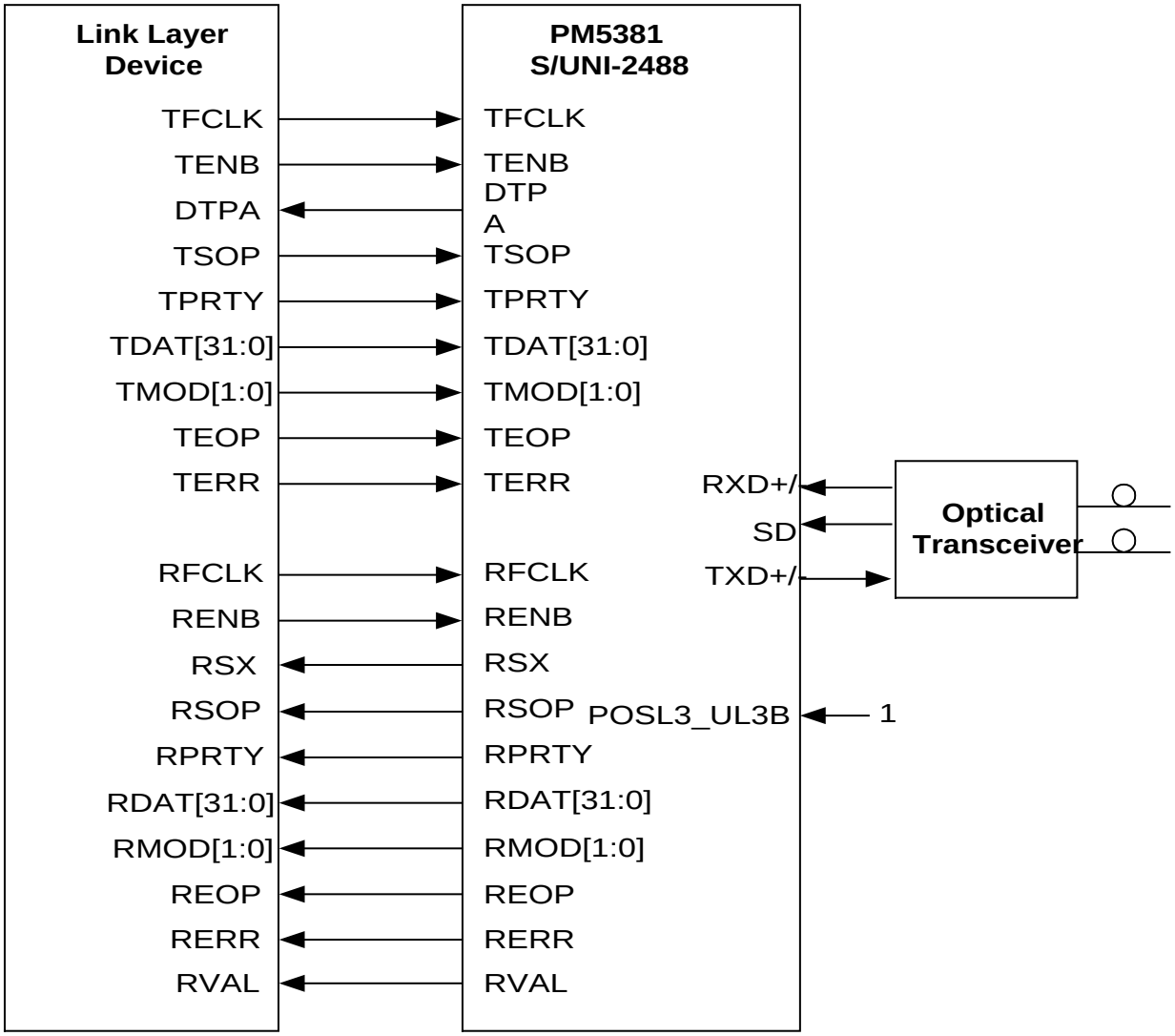
In a typical STS-48 (STM-16-16c) ATM application, the S/UNI-2488 performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. On the system side, the S/UNI-2488 interfaces directly with ATM layer processors and switching or adaptation functions using a UTOPIA Level 3 compliant 32-bit (clocked up to 104 MHz) synchronous FIFO style interface. An application with a UTOPIA Level 3 system side interface is shown in Figure 1. The initial configuration and ongoing control and monitoring of the S/UNI-2488 are normally provided via a generic microprocessor interface.

Figure 1: STS-48 (STM-16-16c) ATM (UTOPIA Level 3) Switch Port Application



In a typical Packet over SONET application (i.e. using the PPP protocol) the S/UNI-2488 performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. On the system side, the S/UNI-2488 interfaces directly with a data link layer processor using a SATURN POS-PHY Level 3 32-bit (clocked up to 104 MHz) synchronous FIFO interface over which packets are transferred. The initial configuration and ongoing control and monitoring of the S/UNI-2488 are normally provided via a generic microprocessor interface.

Figure 2: STS-48 (STM-16-16c) Packet over SONET (POS-PHY Level 3) Router Application



6 BLOCK DIAGRAM

Figure 3:Normal Operation

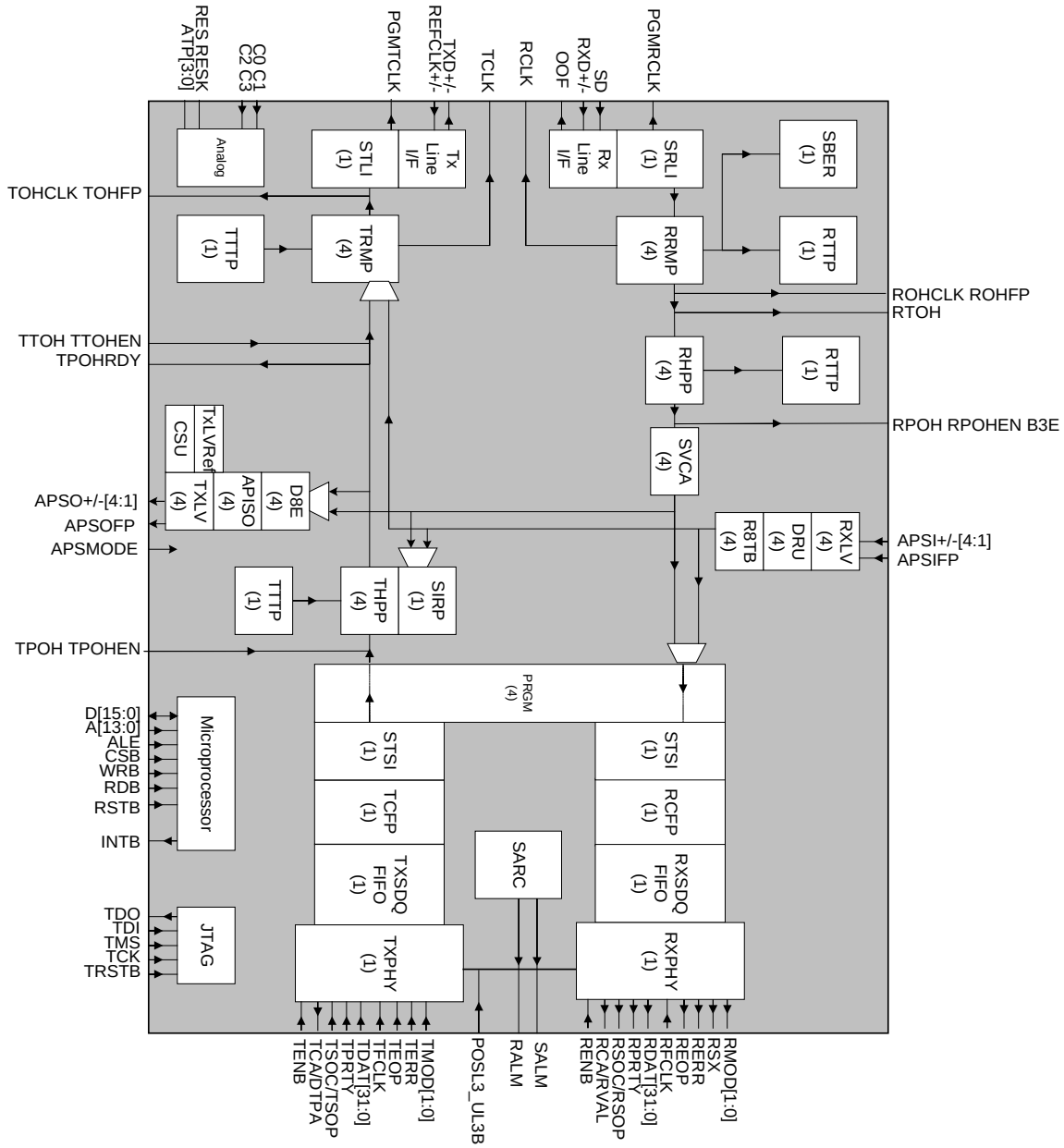


Figure 4:Loopback modes

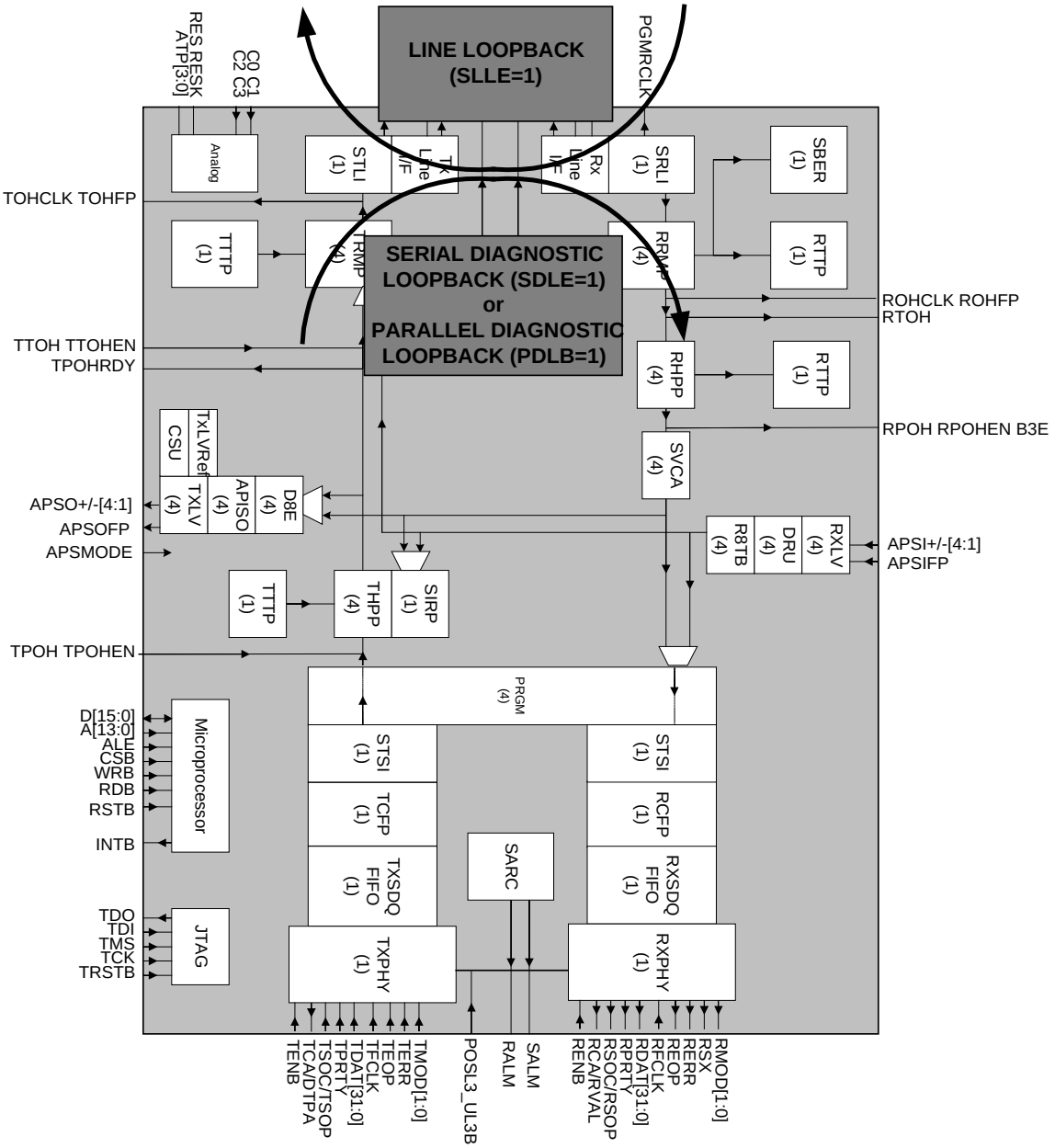


Figure 5: APS Working

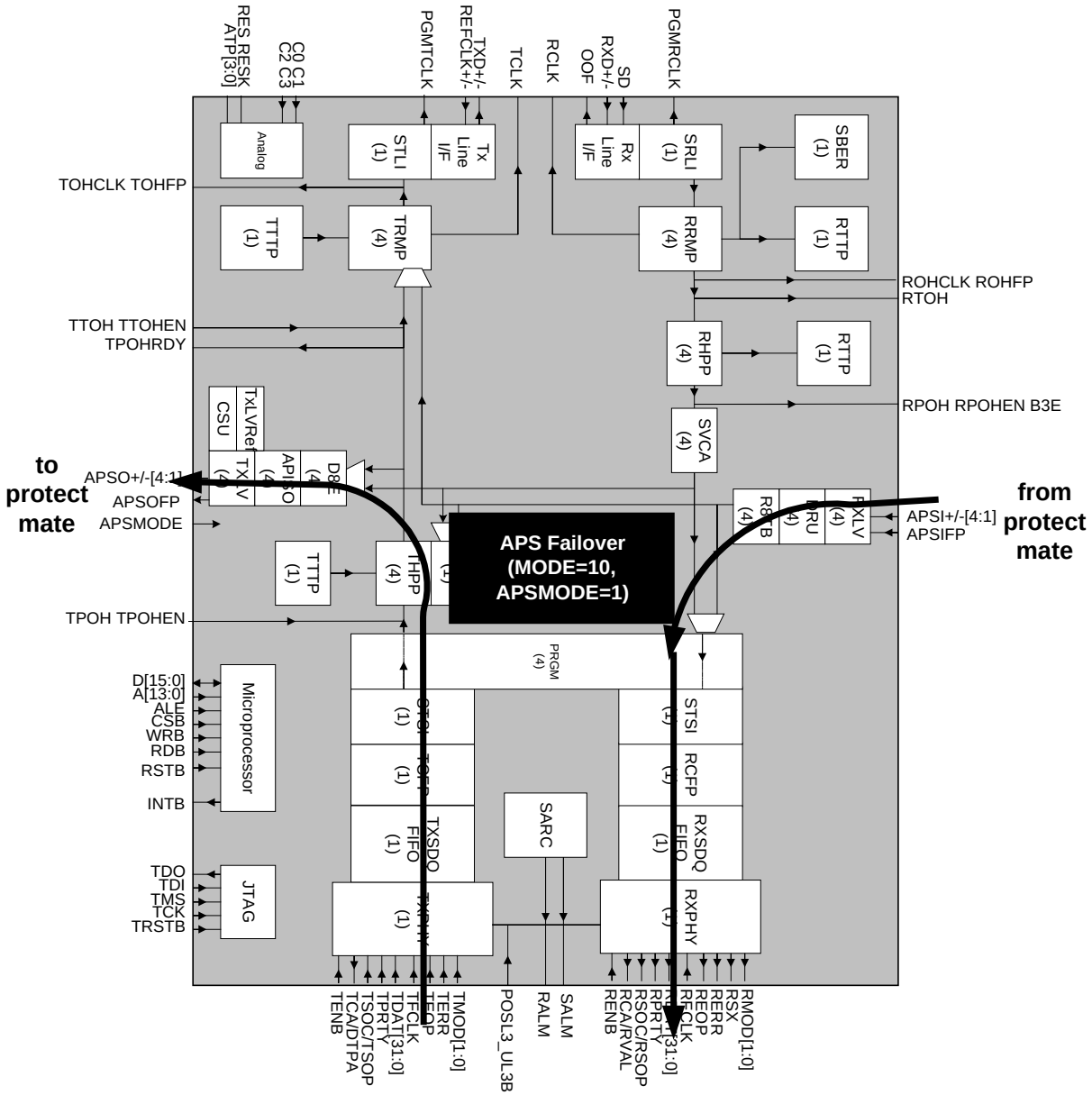
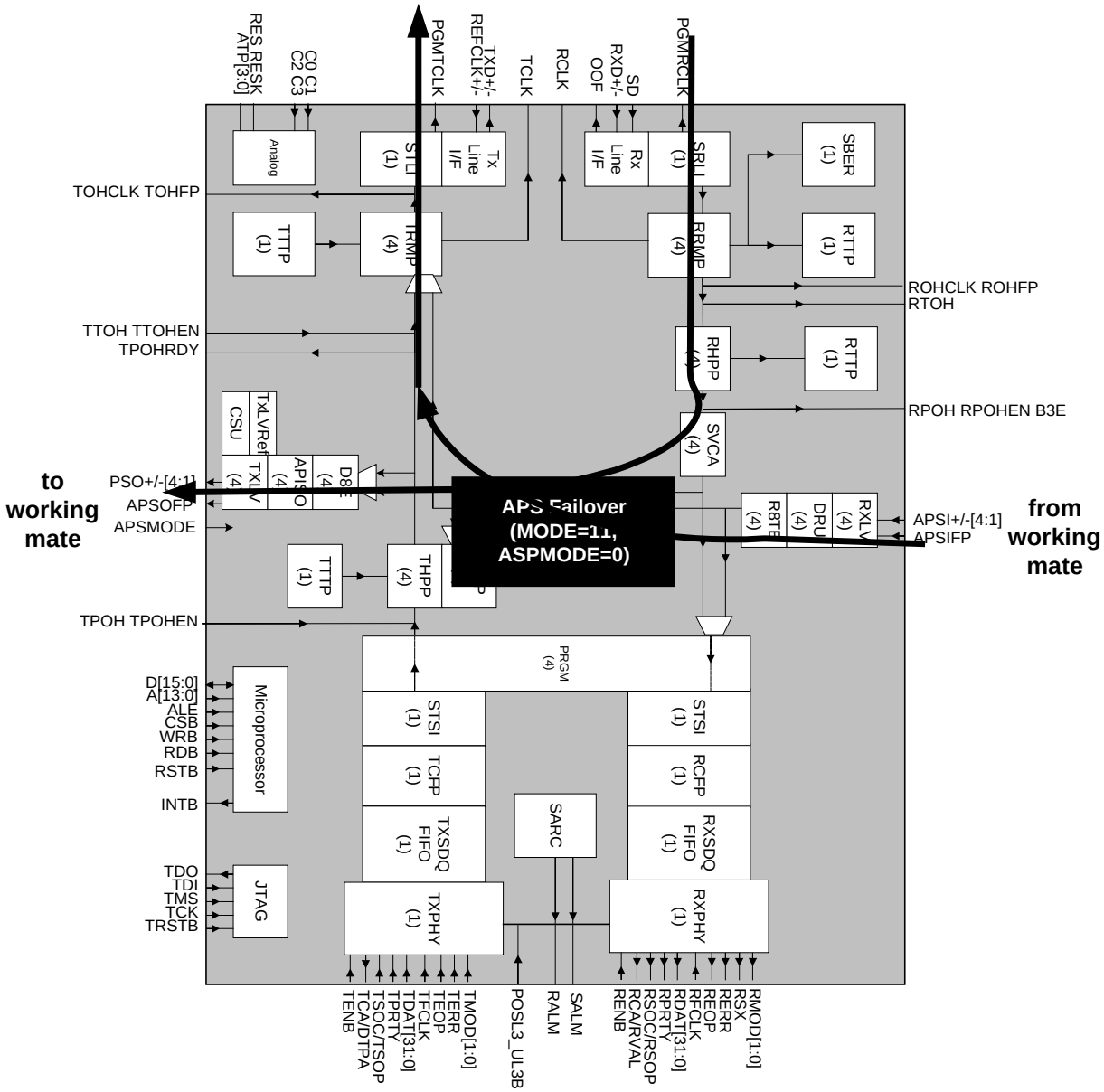


Figure 6: APS Protect



7 DESCRIPTION

The PM5381 S/UNI-2488 SATURN User Network Interface is a monolithic integrated circuit that implements SONET/SDH processing, ATM mapping and Packet over SONET mapping functions at the STS-48 (STM-16-16c) 2488.32 Mbit/s rate.

The S/UNI-2488 receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. The S/UNI-2488 performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path remote error indications (M1, G1) are also accumulated. The S/UNI-2488 interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cells or POS frames.

When used to implement an ATM UNI or NNI, the S/UNI-2488 frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be optionally dropped. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled and are written to a 8-cell FIFO buffer. The received cells are read from the FIFO using a 32-bit wide UTOPIA Level 3 (clocked up to 104 MHz) datapath interface. Counts of received ATM cell headers that are errored and uncorrectable and those that are errored and correctable are accumulated independently for performance monitoring purposes.

When used to implement packet transmission over a SONET/SDH link, the S/UNI-2488 extracts Packet over SONET (POS) frames from the SONET/SDH synchronous payload envelope. Frames are verified for correct construction and size. The control escape characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive FIFO. The received packets are read from the FIFO through a 32-bit POS-PHY Level 3 (clocked up to 104 MHz) system side interface. Valid and FCS errored packet counts are provided for performance monitoring. The S/UNI-2488 Packet over SONET implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay.

The S/UNI-2488 transmits SONET/SDH streams using a bit serial interface. The S/UNI-2488 synthesizes the transmit clock from a 155.52MHz frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity codes (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The S/UNI-2488 generates the payload pointer (H1, H2) and inserts the synchronous payload envelope that carries the ATM or POS frames. The S/UNI-2488 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

When used to implement an ATM UNI or NNI, ATM cells are written to an internal 8 cell FIFO using a 32-bit wide UTOPIA Level 3 (clocked up to 104 MHz) datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI-2488 provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement a Packet over SONET/SDH link, the S/UNI-2488 inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to be transmitted are written into a 256-byte FIFO through a 32-bit SATURN POS-PHY Level 3 (clocked up to 104 MHz) system side interface. POS frames are built by inserting the flags, control escape characters and the FCS fields. Either the CRC-CCITT or CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

No line rate clocks are required directly by the S/UNI-2488 as it synthesizes the transmit clock and recovers the receive clock using a 155.52 MHz reference clock. The S/UNI-2488 outputs a differential PECL line data (TXD+/-).

The S/UNI-2488 is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The S/UNI-2488 also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-2488 is implemented in low power, +1.8 Volt, CMOS technology. It has TTL compatible digital inputs and TTL/CMOS compatible digital outputs. High speed inputs and outputs support 3.3V compatible pseudo-ECL (PECL). The S/UNI-2488 is packaged in a 416 pin UBGA package.

8 PIN DIAGRAMS

TBD

9 SDPIN DESCRIPTION

9.1 Serial Line Side Interface Signals (7)

Pin Name	Type	Pin No.	Function
REFCLK+ REFCLK-	Differential PECL Input	AK10 AK9	The differential **reference clock** inputs (REFCLK+/-) provides a jitter-free 155.52 MHz reference clock for both the clock recovery and the clock synthesis circuits. The 8kHz frame pulse, APSIFP is sampled upon a rising edge transition of REFCLK+/- (i.e. APSIFP is phase-synchronous with REFCLK+/-). APSOFP is updated upon a rising edge transition of REFCLK+/- (i.e. APSOFP is phase-synchronous with REFCLK+/-). Please refer to the Operation section for a discussion of PECL interfacing issues.
RXD+ RXD-	Differential PECL Input	AK16 AK15	The **receive differential data** PECL inputs (RXD+/-) contain the NRZ bit serial receive stream. The receive clock is recovered from the RXD+/- bit stream. Please refer to the Operation section for a discussion of PECL interfacing issues.
SD	TTL Input	AH24	The receive **signal detect** TTL input (SD) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A logic high indicates the presence of valid data. A logic low indicates a loss of signal. Please refer to the Operation section for a discussion of interfacing issues
TXD+ TXD-	Differential PECL Output	AK13 AK12	The **transmit differential data** PECL outputs (TXD+/-) contain the 2488.32 Mbit/s transmit stream. The TXD+/- outputs are driven using the synthesized clock from the CSU. Please refer to the Operation section for a discussion of PECL interfacing issues.

9.2 Clocks and Alarms (7)

Pin Name	Type	Pin No.	Function
PGMRCLK	Output	AK25	The **programmable receive clock** (PGMRCLK) signal provides timing reference for the receive line interface. PGMRCLK is a divided version of the recovered clock. When PGMRCLKSEL register bit is set low, PGMRCLK is a nominal 19.44 MHz, 50% duty cycle clock. When PGMRCLKSEL register bit is set to high, PGMRCLK is a nominal 8 KHz, 50% duty cycle clock. The PGMRCLK output can be disabled and held low by programming the PGMRCLKEN bit in the SRLI PGM Clock Configuration register.
RCLK	Output	AG23	The **receive clock** (RCLK) signal provides timing reference for the receive interface. RCLK is a nominal 77.76 MHz 50% duty cycle clock. The RCLK output can be disabled and held low by programming the RCLKEN bit in the SRLI Clock Configuration register. OOF and SALM are updated on the rising edge of RCLK.
PGMTCLK	Output	AH23	The **programmable transmit clock** (PGMTCLK) signal provides timing reference for the transmit line interface. PGMTCLK is a divided version of the recovered clock. When PGMTCLKSEL register bit is set low, PGMTCLK is a nominal 19.44 MHz, 50% duty cycle clock. When PGMTCLKSEL register bit is set to high, PGMTCLK is a nominal 8 KHz, 50% duty cycle clock. The PGMTCLK output can be disabled and held low by programming the PGMTCLKEN bit in the STLI PGM Clock Configuration register.
TCLK	Output	AJ24	The **transmit clock** (TCLK) signal provides timing reference for the transmit interface. TCLK is a nominal 77.76MHz 50% duty cycle clock. The TCLK output can be disabled and held low by programming the TCLKEN bit in the STLI PGM Clock Configuration register.

Pin Name	Type	Pin No.	Function
OOF	Output	AH27	The active high **out of frame** (OOF) signal indicates when an out of frame condition is declared by the framing block. OOF is set high while the framing block is out of frame. An out of frame condition is declared when four consecutive errored framing patterns (A1 and A2 bytes) have been detected. OOF is set low while the framing block is in frame. OOF is updated on the rising edge of RCLK.
SALM	Output	AG26	The **section alarm** (SALM) signal is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the S/UNI-2488 SARC Section SALM Enable registers. SALM is set low when none of the enabled alarms are active. SALM is updated on the rising edge of RCLK.
RALM	Output	AK28	The **Receive Alarm** (RALM) signal is a multiplexed output of individual alarms of the receive path. Each alarm represents the logical OR of the SALM, LOP-P, AIS-P, RDI-P, ERDI-P, LOPC-P, PAISC-P, UNEQ-P, PSLU, PSLM, PDI-P, TIU-P, TIM-P status of the path. The selection of alarms to be reported is controlled by the S/UNI-2488 SARC Path RALM Enable registers. RALM is updated on the falling edge of ROHCLK. Please refer to the individual alarm interrupt descriptions and Functional Description Section for more details on each alarm.
CSUCLKO	Output	AG22	This clock is used for PMC test purposes only. It must be left as a no connect (NC) during the normal mode of operation.
CSUCLKI	Input	AK24	This clock is used for PMC test purposes only. It must be tied to VSS during the normal mode of operation.
CRUCLKO	Output	AJ23	This clock is used for PMC test purposes only. It must be left as a no connect (NC) during the normal mode of operation.

9.3 Receive Section/Line/Path Overhead Extraction Signals (6)

Pin Name	Type	Pin No.	Function
ROHCLK	Output	V30	The **receive overhead clock** (ROHCLK) signal provides timing for the receive section, line and path overhead extraction. ROHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. ROHCLK has a 33% high duty cycle. ROHFP, RTOH, RPOH, RPOHEN, B3E are updated on the falling edge of ROHCLK.
ROHFP	Output	U27	The **receive overhead frame pulse** (ROHFP) signal provides timing for the receive section, line and path overhead extraction. ROHFP is used to indicate the most significant bit (MSB) on RTOH, RPOH and the first possible path BIP error on B3E. ROHFP can be sample on the rising edge of ROHCLK. ROHFP is updated on the falling edge of ROHCLK.
RTOH	Output	V29	The **receive transport overhead** (RTOH) signal contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) extracted from the incoming stream. RTOH is updated on the falling edge of ROHCLK.
RPOH	Output	V27	The **receive path overhead** (RPOH) signal contains the received path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the STS-48c/STM16c SONET/SDH path overhead The RPOHEN signal is set high to indicate valid path overhead bytes on RPOH. RPOH is updated on the falling edge of ROHCLK.

Pin Name	Type	Pin No.	Function
RPOHEN	Output	V28	The **receive path overhead enable** (RPOHEN) signal indicates valid path overhead bytes on RPOH When RPOHEN signal is set high, the corresponding path overhead byte presented on RPOH is valid. When RPOHEN is set low, the corresponding path overhead byte presented on RPOH is invalid. RPOHEN is updated on the falling edge of ROHCLK.
B3E	Output	W29	The **bit interleaved parity error** (B3E) signal carries the path BIP-8 errors detected for the STS-48c SONET payload. B3E is set high for one ROHCLK clock cycle for each path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, B3E is set high for one ROHCLK clock cycle for up to eight path BIP-8 errors detected (up to one error per path per frame). Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. B3E is updated on the falling edge of ROHCLK.

9.4 Transmit Section/Line/Path Overhead Insertion Signals (7)

Pin Name	Type	Pin No.	Function
TOHCLK	Output	AJ27	The **transmit overhead clock** (TOHCLK) signal provides timing for the transmit section, line and path overhead insertion. TOHCLK is a nominal 20.736MHz clock generated by gapping a 25.92MHz clock. TOHCLK has a 33% high duty cycle. TOHFP and TPOHRDY are updated on the falling edge of TOHCLK. TTOH, TTOHEN, TPOH and TPOHEN are sampled on the rising edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TOHFP	Output	AG25	The **transmit overhead frame pulse** (TOHFP) signal provides timing for the transmit section, line and path overhead insertion. TOHFP is used to indicate the most significant bit (MSB) on TTOH and TPOH. TOHFP is set high when the MSB of the: First A1 byte should be present on TTOH. First J1 byte should be present on TPOH. TOHFP can be sampled on the rising edge of TOHCLK. TOHFP is updated on the falling edge of TOHCLK.
TTOH	Input	AK27	The **transmit transport overhead** (TTOH) signal contains the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) to be transmitted and the error masks to be applied on B1, B2, H1 and H2. TTOH is sampled on the rising edge of TOHCLK.
TTOHEN	Input	AJ26	The **transmit transport overhead insert enable** (TTOHEN) signal controls the insertion of the transmit transport overhead data which is inserted in the outgoing stream. When TTOHEN is high during the most significant bit of a TOH byte on TTOH, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). When TTOHEN is low during the most significant bit of a TOH byte on TTOH, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. When TTOHEN is high during the most significant bit of the H1, H2, B1 or B2 TOH byte positions on TTOH, the sampled TOH byte is logically XOR'ed with the associated incoming byte to force bit errors on the outgoing byte. A logic low bit in the TTOH byte allows the incoming bit to go through while a bit set to logic high will toggle the outgoing bit. A low level on TTOHEN during the MSB of the TOH byte disables the error forcing for the entire byte. TTOHEN is sampled on the rising edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TPOH	Input	AH25	The **transmit path overhead** (TPOH) signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) to be transmitted in the STS-48c SONET path overhead and the error masks to be applied on B3 and H4. A path overhead byte is accepted for transmission when the external source indicates a valid byte (TPOHEN set high) and the S/UNI-2488 indicates ready (TPOHRDY set high). The S/UNI-2488 will ignore the byte on TPOH when TPOHEN is set low. The TPOHRDY is set low to indicate the S/UNI-2488 is not ready, and the byte must be re-presented at the next opportunity. TPOH is sampled on the rising edge of TOHCLK.
TPOHRDY	Output	AJ25	The **transmit path overhead insert ready** (TPOHRDY) signal indicates if the S/UNI-2488 is ready to accept the byte currently on TPOH. TPOHRDY is set high during the most significant bit of a POH byte to indicate readiness to accept the byte on the TPOH input. This byte will be accepted if TPOHEN is also set high. If TPOHEN is set low, the byte is invalid and is ignored. TPOHRDY is set low to indicate that the S/UNI-2488 is unable to accept the byte on TPOH, and expects the byte to be re-presented at the next opportunity. TPOHRDY is updated on the falling edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TPOHEN	Input	AK26	The **transmit path overhead insert enable** (TPOHEN) signal controls the insertion of the transmit path overhead data which is inserted in the outgoing stream. TPOHEN shall be set high during the most significant bit of a POH byte to indicate valid data on the TPOH input. This byte will be accepted for transmission if TPOHRDY is also set high. If TPOHRDY is set low, the byte is rejected and must be re-presented at the next opportunity. Accepted bytes sampled on TPOH are inserted into the corresponding path overhead byte positions (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). The byte on TPOH is ignored when TPOHEN is set low during the most significant bit position. When the byte at the B3 or H4 byte position on TPOH is accepted, it is used as an error mask to modify the corresponding transmit B3 or H4 path overhead byte, respectively. The accepted error mask is XOR'ed with the corresponding B3 or H4 byte before it is transmitted. TPOHEN is sampled on the rising edge of the TOHCLK.

9.5 System Side Utopia and POS Signals (84)

Pin Name	Type	Pin No.	Function
POSL3_ UL3B	Input	B19	The **Utopia/POS interface select (POSL3/UL3B)** selects between Utopia Level 3 and POS-PHY Level 3 mode for the system side interface. When POSL3/UL3B is low, the Utopia Level 3 interface is selected. When high, the POS-PHY Level 3 interface is selected.
RFCLK	Input	E28	The UTOPIA **receive FIFO read clock** (RFCLK) signal is used to read ATM cells from the receive cell FIFO. RFCLK is expected to cycle at 104 MHz.
			The POS-PHY **receive FIFO read clock (RFCLK**) signal is used to read packet data from the 256 byte packet FIFO. RFCLK is expected to cycle at 104 MHz.
RPRTY	Output	P29	The UTOPIA **receive parity** (RPRTY) RPRTY signal indicates the parity of the RDAT bus. The RPRTY signal indicates the parity on the RDAT[31:0] bus. Either odd or even parity selection can be selected. RPRTY is updated on the rising edge of RFCLK.
			The POS-PHY **receive parity (RPRTY)** signal indicates the parity of the RDAT bus. Either odd or even parity can be selected. RPRTY is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RDAT[31] RDAT[30] RDAT[29] RDAT[28] RDAT[27] RDAT[26] RDAT[25] RDAT[24] RDAT[23] RDAT[22] RDAT[21] RDAT[20] RDAT[19] RDAT[18] RDAT[17] RDAT[16] RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Output	D30 E29 F28 G27 E30 F29 G28 H27 F30 H28 J27 G30 H29 J28 H30 J29 K28 L27 J30 L28 M27 K30 L29 M28 L30 N27 M29 N28 M30 P27 N30 P28	The UTOPIA **receive cell data** (RDAT[31:0]) bus carries the ATM cell octets that are read from the receive FIFO. RDAT[31:0] is updated on the rising edge of RFCLK. The POS-PHY **receive packet data** (RDAT[31:0]) bus carries the POS packet octets that are read from the receive FIFO. The RDAT[31:0] signals are valid when RVAL and RENB are asserted. RDAT[31:0] is updated on the rising edge of RFCLK.
RENB	Input	U28	The UTOPIA **receive read enable** (RENB) signal is used to initiate reads from the receive FIFO. The system may de-assert RENB at any time if it is unable to accept more data. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RENB (continued	Input	U28	The POS-PHY **receive read enable** (RENB) signal is used to initiate reads from the receive FIFO. During a data transfer, RVAL must be monitored since it will indicate if the data is valid. The system may deassert RENB at any time if it is unable to accept more data. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.
RSOC	Output	R28	The UTOPIA **receive start of cell** (RSOC) signal marks the start of a cell structure on the RDAT[31:0] bus. The first word of the cell structure is present on the RDAT[31:0] bus when RSOC is high. RSOC is updated on the rising edge of RFCLK.
RSOP			The POS-PHY **receive start of packet** (RSOP) signal indicates the start of a packet on the RDAT[31:0] bus. RSOP is set high for the first word of a packet on RDAT[31:0]. RSOP is updated on the rising edge of RFCLK
RCA	Output	U30	The UTOPIA **receive cell available** (RCA) signal provides direct status indication of when a cell is available in the receive FIFO. RCA can be configured to de-assert when either zero or four words remain in the FIFO. RCA will thus transition low on the rising edge of RFCLK after **payload word** 12 or 7 is output on the RDAT[31:0] bus depending on the configuration. RCA is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RVAL	Output	U30	The POS-PHY **receive data valid** (RVAL) signal indicates the validity of the receive data signals. When RVAL is high, the receive signals RDAT[31:0], RPRTY, RSOP, REOP, RMOD[1:0], and RERR are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will be high when valid data is on the RDAT[31:0] bus. RVAL will transition low when the FIFO is empty. RVAL will remain low until a programmable minimum number of bytes exist in the receive FIFO. The threshold is configurable. RVAL is updated on the rising edge of RFCLK.
RERR			The POS-PHY **receive error** (RERR) signal indicates that the current packet is invalid due to an error such as invalid FCS, excessive length or received abort. RERR may only assert when REOP is asserted marking the last word of the packet. RERR is only used in POS mode and is updated on the rising edge of RFCLK.
REOP	Output	P30	The POS-PHY **receive end of packet** (REOP) signal marks the end of packet on the RDAT[31:0] bus. It is legal for RSOP to be high at the same time REOP is high. REOP is set high to mark the last word of the packet presented on the RDAT[31:0] bus. When REOP is high, RMOD[1:0] specifies if the last word has 1, 2, 3, or 4 valid bytes of data. REOP is only used for POS operation and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RMOD[1] RMOD[0]	Output	T28 T29	The POS-PHY **transmit word modulo** (RMOD[1:0]) bus indicates the size of the current word when configured for packet mode. During a packet transfer, every word on RDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by RMOD[1:0]. RMOD[1:0] = "00" RDAT[31:0] valid RMOD[1:0] = "01" RDAT[31:8] valid RMOD[1:0] = "10" RDAT[31:16] valid RMOD[1:0] = "11" RDAT[31:24] valid RMOD[1:0] is considered valid only when RVAL is asserted. RMOD[1:0] is only used for POS operation and is updated on the rising edge of RFCLK.
RSX	Output	R29	The POS-PHY **receive start of transfer** (RSX) signal is used to indicate the start of a packet transfer. When RSX is high, the channel number being transferred is given on RDAT[31:0]. RSX is only used for POS operation and is updated on the rising edge of RFCLK.
TFCLK	Input	B18	The UTOPIA **transmit FIFO write clock** (TFCLK) signal is used to write ATM cells to the transmit FIFO. TFCLK is expected to cycle at a 104 MHz rate.
TFCLK (continued)	Input	B18	The POS-PHY **transmit FIFO write clock** (TFCLK) signal is used to write packet data into the 256 byte packet FIFO. TFCLK is expected to cycle at a 104 MHz rate.

Pin Name	Type	Pin No.	Function
TDAT[31] TDAT[30] TDAT[29] TDAT[28] TDAT[27] TDAT[26] TDAT[25] TDAT[24] TDAT[23] TDAT[22] TDAT[21] TDAT[20] TDAT[19] TDAT[18] TDAT[17] TDAT[16] TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	B5 D7 A5 B6 C7 D8 A6 B7 D9 A7 B8 C9 A8 B9 C10 D11 B10 C11 D12 A10 C12 A11 D13 B12 C13 A12 B13 D14 C14 B14 A14 C15	The UTOPIA **transmit cell data** (TDAT[31:0]) bus carries the ATM cell octets that are written to the transmit FIFO. TDAT[31:0] is considered valid only when TENB is simultaneously asserted. TDAT[31:0] is sampled on the rising edge of TFCLK. The POS-PHY **transmit packet data** (TDAT[31:0]) bus carries the POS packet octets that are written to the transmit FIFO. TDAT[31:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[31:0] is sampled on the rising edge of TFCLK.
TPRTY	Input	B15	The UTOPIA **transmit bus parity** (TPRTY) signal indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are still inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TPRTY (continued)	Input	B15	The POS-PHY **transmit bus parity** (TPRTY) signal indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Packets with parity errors are still inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
TSOC	Input	D16	The UTOPIA **transmit start of cell** (TSOC) signal marks the start of a cell structure on the TDAT[31:0] bus. The first word of the cell structure is present on the TDAT[31:0] bus when TSOC is high. TSOC must be present for each cell. TSOC is considered valid only when TENB is simultaneously asserted. TSOC is sampled on the rising edge of TFCLK.
TSOP			The POS-PHY **transmit start of packet** (TSOP) signal indicates the start of a packet on the TDAT[31:0] bus. TSOP is required to be present at all instances for proper operation. TSOP must be set high for the first word of a packet on TDAT[31:0]. TSOP is considered valid only when TENB is simultaneously asserted. TSOP is sampled on the rising edge of TFCLK.
TENB	Input	A19	The UTOPIA **transmit write enable** (TENB) signal is an active low input which is used to initiate writes to the transmit FIFO. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY and TSOC signals are invalid. When TENB is sampled low, the information sampled on the TDAT[31:0], TPRTY and TSOC signals are valid and are written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TENB			The POS-PHY **transmit write enable** (TENB) signal is an active low input which is used to initiate writes to the transmit FIFO's. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY, TSOP, TEOP, TMOD[1:0], and TERR signals are invalid. When TENB is sampled low, the information sampled on the TDAT[31:0], TPRTY, TSOP, TEOP, TMOD[1:0], and TERR signals are valid and are written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.
TCA	Output	D17	The UTOPIA **transmit cell available** (TCA) signal provides direct status indication of when cell space is available in the transmit FIFO. When set high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. TCA is set low to either indicate that the transmit FIFO is near full or that the transmit FIFO is full. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be configured. Note that regardless of what fill level TCA is set to indicate "full" at, the transmit cell processors still have the full capacity of its FIFO to store cells. TCA will transition low one TFCLK cycle after the payload word 7 or 11 (depending of the configuration) is sampled on the TDAT[31:0] bus. TCA is updated on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
DTPA	Output	D17	The POS-PHY **direct transmit packet available** (DTPA) signal provides status indication on the fill status of the transmit FIFO. Note that regardless of what fill level DTPA is set to indicate "full" at, the transmit packet processors still have the full capacity of its FIFO to store cells. When DTPA transitions high, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. When DTPA transitions low, it indicates that the transmit FIFO is either full or near full as configured. DTPA is updated on the rising edge of TFCLK.
TEOP	Input	B16	The POS-PHY **transmit end of packet** (TEOP) signal marks the end of packet on the TDAT[31:0] bus when configured for packet data. The TEOP signal marks the last word of a packet on the TDAT[31:0] bus. The TMOD[1:0] signal indicates how many bytes are in the last word. It is legal to set TSOP high at the same time as TEOP high in order to support one, two, three, or four byte packets. TEOP is only valid when TENB is simultaneously asserted. TEOP is only used for POS operation and is sampled on the rising edge of TFCLK.
TERR	Input	A17	The POS-PHY **transmit error** (TERR) signal is used to indicate that the current packet must be aborted. Packets marked with TERR will have the abort sequence appended when transmitted. TERR should only be asserted during the last word of the packet being transferred on TDAT[31:0]. TERR is only considered valid when TENB and TEOP are simultaneously asserted. TERR is ignored for the UTOPIA mode of operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TMOD[1:0]	Input	B17 A18	The POS-PHY **transmit word modulo** (TMOD[1:0]) bus indicates the size of the current word when configured for packet mode. During a packet transfer, every word on TDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by TMOD[1:0] TMOD[1:0] = "00" TDAT[31:0] valid TMOD[1:0] = "01" TDAT[31:8] valid TMOD[1:0] = "10" TDAT[31:16] valid TMOD[1:0] = "11" TDAT[31:24] valid TMOD[1:0] is considered valid only when TENB is simultaneously asserted. TMOD[1:0] is only used for POS operation and is sampled on the rising edge of TFCLK.

9.6 APS Serial Data Interface (20)

Pin Name	Type	Pin No.	Function
APSI+[4] APSI-[4]	Analog LVDS Input	Y4 Y3	The differential **APSI** input (APSI+/-[4:1]) serial data links carries SONET/SDH OC-48 frame data from a mate in bit serial format. Each differential pair carries a constituent OC-12 of the data stream. Data on APSI+/-[4:1] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. When in working mode as set using the APSMODE input and the MODE[1:0] register bits in the S/UNI-2488 Master Reset, Configuration and Loopback register, the APSI+/-[4:1] signals carry the receive data from the protect mate. When in protect mode, the APSI+/-[4:1] signals carry the transmit data from the working mate. The four differential pairs in APSI+/-[4:1] are frequency locked but not phase locked. APSI+/-[4:1] are nominally 777.6 Mbps data streams.
APSI+[3] APSI-[3]		Y2 Y2	
APSI+[2] APSI-[2]		AA3 AA2	
APSI+[1] APSI-[1]		AB4 AB3	

Pin Name	Type	Pin No.	Function
APSIFP	Input	P2	The **APS input frame pulse** signal (APSIFP) provides system timing of the APS input serial interface. APSIFP is set high once every 9720 APSIFPCLK cycles, or multiple thereof, to indicate that the J0 frame boundary 8B/10B character has been delivered on the differential LVDS bus (APSI+/-[4:1]). APSIFP is sampled on the rising edge of APSIFPCLK+/-.
APSO+[4] APSO-[4] APSO+[3] APSO-[3] APSO+[2] APSO-[2] APSO+[1] APSO-[1]	Analog LVDS Output	U1 U2 V3 V4 V1 V2 W2 W3	The differential **APS output** (APSO+/-[4:1]) serial data links carries SONET/SDH OC-48 frame data to a mate in bit serial format. Each differential pair carries a constituent OC-12 of the data stream. Data on APSO+/-[4:1] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is received first and the bit 'j' is received last. When in working mode as set using the APSMODE input, the APSO+/-[4:1] signals carry the transmit data to the protect mate. When in protect mode, the APSO+/-[4:1] signals carry the receive data to the working mate. The four differential pairs in APSO+/-[4:1] are frequency locked but not phase locked. APSO+/-[4:1] are nominally 777.6 Mbps data streams.
APSOFP	Output	P1	The **APS output frame pulse** signal (APSOFP) provides system timing of the APS output serial interface. APSOFP is set high once every 9720 APSIFPCLK cycles, or multiple thereof, to indicate that the J0 frame boundary 8B/10B character has been delivered on the differential LVDS bus (APSO+/-[4:1]). APSOFP is updated on the rising edge of APSIFPCLK +/-.
APSIFPCLK	Input	P3	The **APS input frame pulse clock** (APSIFPCLK) provides a jitter-free reference clock with which the APS input frame pulse (APSIFP) is sampled. Also, the 777.76 MHz Clock Synthesis Unit of the APS Port uses this clock as its reference. APSIFPCLK is expected to cycle at a 77.76 MHz rate, and must be a derivative of REFCLK+/- to ensure that APSIFPCLK is an exact divide-by-two in frequency compared to REFCLK+/-.

9.7 Microprocessor Interface Signals (37)

Pin Name	Type	Pin No.	Function
CSB	Input	F4	The active low **chip select** (CSB) signal is low during S/UNI-2488 register accesses. Note that when not being used, CSB must be tied low. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	D2	The active low **read enable** (RDB) signal is low during a S/UNI-2488 read access. The S/UNI-2488 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	C1	The active low **write strobe** (WRB) signal is low during a S/UNI-2488 register write access. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	N1 P4 N2 M1 M2 N4 L1 M3 L2 K1 M4 K2 J1 K3 J2 H1	The bi-directional **data bus**, D[15:0], is used during S/UNI-2488 read and write accesses.
A[13]/TRS	Input	D28	The **test register select** signal (TRS) selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS may be tied low.

Pin Name	Type	Pin No.	Function
A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	J3 H2 J4 H3 G2 F1 H4 G3 F2 E1 G4 E2 D1	The **address** bus (A[12:0]) selects specific registers during S/UNI-2488 register accesses.
RSTB	Schmidt TTL Input	E4	The active low **reset** (RSTB) signal provides an asynchronous S/UNI-2488 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.
ALE	Input	E3	The **address latch enable** (ALE) is an active-high signal and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-2488 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
INTB	OD Output	D3	The active low **interrupt** (INTB) is set low when a S/UNI-2488 enabled interrupt source is active. The S/UNI-2488 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

9.8 JTAG Test Access Port (TAP) Signals (5)

Pin Name	Type	Pin No.	Function
TCK	Input	C30	The **test clock** (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	E27	The **test mode select** (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
TDI	Input	F27	When the S/UNI-2488 is configured for JTAG operation, the **test data input** (TDI) signal carries test data into the S/UNI-2488 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	D18	The **test data output** (TDO) signal carries test data out of the S/UNI-2488 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Schmidt TTL Input	D28	The active low **test reset** (TRSTB) signal provides an asynchronous S/UNI-2488 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

9.9 Analog Miscellaneous Signals (10)

Pin Name	Type	Pin No.	Function
ATP[3] ATP[2] ATP[1] ATP[0]	Analog	AJ18 AK18 AG2 AF3	Four **analog test ports** (ATP[0], ATP[1], ATP[2], ATP[3]) are provided for production testing only. These pins must be tied to analog ground (AVS) during normal operation. ATP[1] and ATP[0] are the test ports for the 2488 Mbps analog circuitry, while ATP[3] and ATP[2] are the test ports for the 777.76 MHz LVDS analog circuitry.
C0 C1	Analog	AH18 AG18	The analog **C0** and **C1** pins are provided for applications that must meet SONET/SDH jitter tolerance specifications. A 47nF non-polarized capacitor is attached across C0 and C1 for these applications. When the capacitor is used, the RTYPE bit in the CRSI must be set to logic one for proper operation. When the capacitance is not used, these pins are left floating and the RYPE register must be set to logic zero for proper operation.
C2 C3	Analog	AJ20 AK20	The analog **C2** and **C3** pins are provided for applications that must meet SONET/SDH jitter transfer specifications. A 4.7nF non-polarized capacitor is attached across C2 and C3 for these applications. When the capacitance is not used, these pins are left floating.

Pin Name	Type	Pin No.	Function
RES RESK	Analog	AE4 AG1	**Reference Resistor Connection.** An off-chip 4.75kΩ ±1% resistor is connected between the positive resistor reference pin RES and a Kelvin ground contact RESK for the APS port LVDS reference. An on-chip negative feedback path will force the 1.20V VREF voltage onto RES, therefore forcing 252µA of current to flow through the resistor. RESK is electrically connected to AVSS within the block, but should not be connected to AVSS, either on-chip or off-chip.

9.10 Analog Power and Ground (107)

Pin Name	Pin Type	PIN No.	Function
AVDH (24)	Analog Power	AH20 AH17 AH14 AH10 AH9 AG9 AJ9 AJ10 AJ14 AJ17 AJ19 AK19 AG20 AG8	The **analog power** (AVDH) pins for the analog core. The AVDH pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.

Pin Name	Pin Type	PIN No.	Function
AVDL(17)	Analog Power	AG5 AG6 AG7 AH5 AH6 AH7 AJ5 AJ6 AJ7 AK5 AK6 AK7 AG21 AH21 AJ21 AK21	The **analog power** (AVDL) pins for the analog core. The AVDL pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.

9.11 Digital Power and Ground

Pin Name	Pin Type	PIN No.	Function
VDDDC	Digital Core Power	D29 G29 K29 N29 U29 W30 AA28 AH26 AG24 T2 R4 N3 L3 G1 F3 C6 C8 A9 B11 A13 C16 C17 C18 A21 D21 B29 C28 D27 D10 D15 D20	The digital core power (VDDDC) pins should be connected to a well-decoupled +1.8V digital power supply.

Pin Name	Pin Type	PIN No.	Function
VDDDC (Cont.)	Digital Core Power	L4 T4 B2 C3 D4 AG27 AH28 AJ29 K27 R27 Y27	The digital core power (VDDDC) pins should be connected to a well-decoupled +1.8V digital power supply.

Pin Name	Pin Type	PIN No.	Function
VSS (52)	Digital Ground	A1 B1 C2 R1 T1 W1 AA1 AC1 AC2 AC3 AD1 AD2 AE1 AH1 AK1 AJ2 AK2 AK14 AG15 AH15 AJ15 AG16 AH16 AJ16 AK17 AK22 AK23 AJ28 AK29 B28 A16 A15 B3 A2	The digital ground (VSS) pins should be connected to the digital ground of the digital power supply.

Pin Name	Pin Type	PIN No.	Function
VSS (52) (Continued)	Digital Ground	AH3 AJ3 AK3 AG4 AH4 AJ4 AK4 AJ8 AK8 AG11 AH11 AJ11 AK11 AG12 AH12 AJ12 AG13 AH13 AJ13 AK30 AJ30 AH29 T30 R30 C29 B30 A30 A29	The digital ground (VSS) pins should be connected to the digital ground of the digital power supply.

Notes on Pin Description:

1. All S/UNI-2488 inputs and bidirectionals present minimum capacitive loading and operate at CMOS/TTL logic levels except: the REFCLK+/-, RXD+/-, TXD+/-, APSI+/-[4:1], APSO+/-[4:1] pins which operate at pseudo-ECL (PECL) logic levels.

2. The S/UNI-2488 digital outputs and bidirectionals which have 2 mA drive capability are: TBD

   The S/UNI-2488 digital outputs and bidirectionals which have 4 mA drive capability are: TBD

   The S/UNI-2488 digital outputs and bidirectionals which have 6 mA drive capability are: TBD

3. The S/UNI-2488 digital outputs are 3.3V tolerant.

4. Inputs ALE, RSTB, TMS, TDI and TRSTB have internal pull-up resistors.

5. The single ended pseudo-ECL inputs and outputs should be terminated in a passive network and interface at PECL levels as described in the Operations section.

6. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.

7. It is mandatory that every digital power pin (VDD) be connected to the printed circuit board power plane to ensure reliable device operation.

8. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to the Operations sections.

9. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.

10. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.

11. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

12. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

13. Ensure that all digital power is applied simultaneously, and applied before or simultaneously with the analog power. Refer to the Power Sequencing description in the Operations section.

10 FUNCTIONAL DESCRIPTION

10.1 Receive Line Interface

The Receive Line Interface allows direct interface of the S/UNI-2488 to optical modules (ODLs) or other medium interfaces. This block performs clock and data recovery on the incoming 2488.32 Mbit/s data stream and SONET A1/A2 pattern framing.

The clock recovery unit recovers the clock from the incoming bit serial data stream and is compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit continues to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit utilizes a 155.52 MHz reference clock. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference and also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially upon start-up, the PLL locks to the reference clock, REFCLK. When the frequency of the recovered clock is within TBD ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in TBD bit periods or if the recovered clock drifts beyond TBD ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK reference accuracy in the case of a loss of signal condition. To meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/- TBD ppm. When not loop timed, the REFCLK accuracy may be relaxed to +/- TBD ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance specified for SONET equipment by GR-253-CORE. Please refer to the figure below.

Figure 7: Typical STS-48c (STM-16c) Jitter Tolerance

TBD

The Serial to Parallel Converter converts the received bit serial stream to a 16 bit word serial stream.

10.2 SONET/SDH Receive Line Interface (SRLI)

The SONET/SDH receive line interface block performs byte and frame alignment on the incoming 2488 Mbit/s data stream based on the SONET/SDH A1/A2 framing pattern.

While out of frame, the SRLI monitors the receive data stream for an occurrence of the A1/A2 framing pattern. The SRLI adjusts its byte and frame alignment when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SRLI informs the RRMP framer block when the framing pattern has been detected to reinitialize to the new transport frame alignment. While in frame, the SRLI maintains the same byte and frame alignment until the RRMP declares out of frame.

10.3 Receive Regenerator and Multiplexor Processor (RRMP)

The Receive Regenerator and Multiplexor Processor (RRMP) block extracts and process the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with an upstream pattern detector (SRLI) that searches for occurrences of the A1/A2 framing pattern. Once the SRLI has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when the 12 A1 and the 12 A2 bytes are seen error-free in the first STS-12 (STM-4) of the STS-48c (STM-16-16c) stream. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) when only the last A1 byte and the first four bits of the first A2 byte are seen error-free in the first STS-12 (STM-4) of the STS-48c (STM-16c) . Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes or 12 framing bits are examined for bit errors in the framing pattern.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment the performance of each algorithm is dominated by the alignment algorithm used in the SRLI which always examines 3 A1 and 3 A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an out of frame (OOF) condition exists for a total period of 3ms during which there is no continuous in frame period of 3 ms. LOF output is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the

intervening time (one frame) there are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after de-scrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally de-scrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after de-scrambling. Any difference indicates a line BIP-8 error. The RRMP accumulates line BIP-8 errors in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP errors can be accumulated.

The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when twelve consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes must be done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

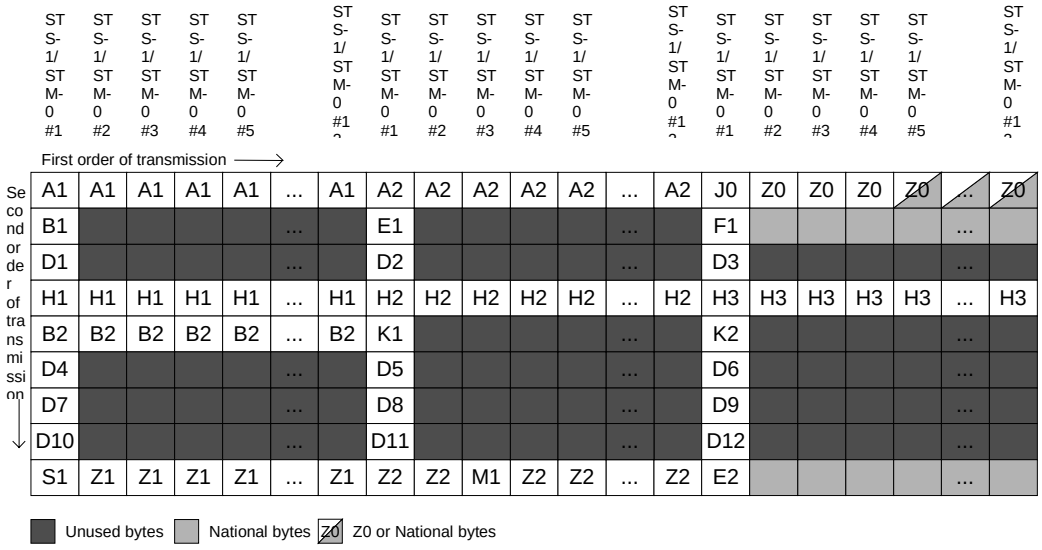
The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

RRMP optionally inserts line alarm indication signal (AIS-L).

The RRMP extracts and serially outputs all the transport overhead (TOH) bytes on the RTOH output. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, B1,

E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). RTOHCLK is the generated output clock used to provide timing for the RTOH output. RTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RTOHFP high with the rising edge of RTOHCLK identifies the MSB of the first A1 byte.

Figure 8: STS-48c (STM-16-16c) on RTOH



A maskable interrupt is activated to indicate any change in the status of out of frame (OOF), loss of frame (LOF), loss of signal (LOS), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS) and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8 and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the RHPP.

10.4 Receive Tail Trace Processor (RTTP)

The Receive Tail Trace Processor (RTTP) block monitors the tail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. Three tail trace algorithms are defined.

The first algorithm is BELLCORE compliant. The algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64 byte tail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected tail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the tail trace message is all zeros.

The second algorithm is ITU compliant. The algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64 byte tail trace message. The current tail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes on the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent tail trace message is declared when an identical message is receive for 3 or 5 consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A TIU defect is declared when one or more erroneous bytes are detected in a total of 8 messages without any persistent message in between. A TIU defect is removed when a persistent message is received.

A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match tail trace message when the accepted message is all zeros.

The third algorithm is not BELLCORE/ITU compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous tail trace byte. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16 byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames. A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM).

10.5 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring.

10.5.1 Pointer Interpreter

The pointer interpreter extracts and validates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and the synchronous payload envelop bytes (SPE) of the constituent STS-48c (VC-16-16c) payloads. The pointer interpreter is a time multiplexed finite state machine that can process the STS-48c (AU-16-16c) pointer. Within the pointer interpretation algorithm three states are defined as shown below:

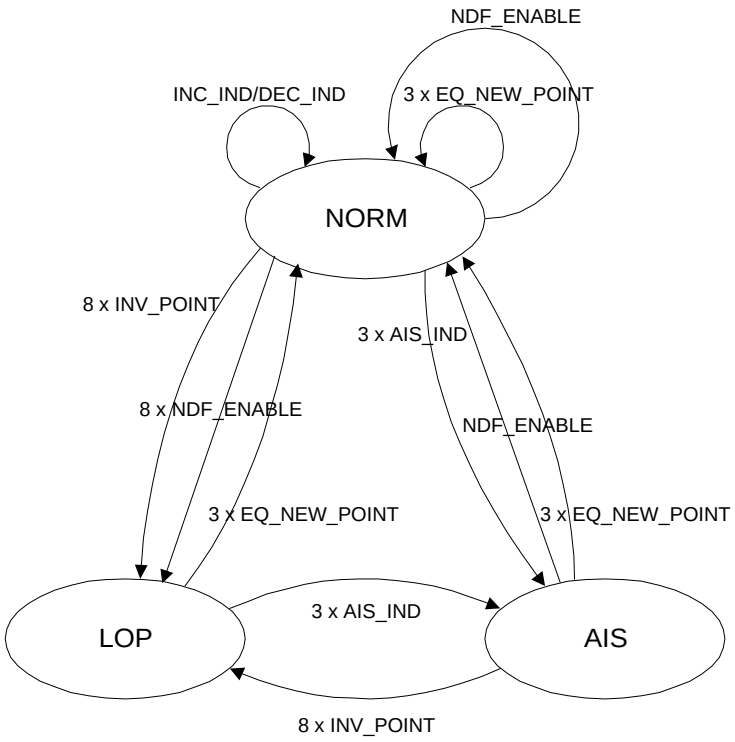
NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 9: Pointer interpretation state diagram



The following events (indications) are defined:

NORM_POINT: disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: H1 = FFh + H2 = FFh.

INC_IND:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.
DEC_IND:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.
INV_POINT:	not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).
NEW_POINT:	disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Note 1:	active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
Note 2:	enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.
Note 3:	disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100 and 0111.
Note 4:	the remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.
Note 5:	ss bits are unspecified in SONET and have bit pattern 10 in SDH.
Note 6:	the use of ss bits in definition of indications may be optionally disabled.
Note 7:	the requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.
Note 8:	NEW_POINT is also an INV_POINT.
Note 9:	the requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.
Note 10:	LOP is not declared if all the following conditions exist: - the received pointer is out of range (>782), - the received pointer is static, - the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.

- When the received pointer returns to an in-range value, the S/UNI-2488 will interpret it correctly.

Note 11: LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: three consecutive equal NEW_POINT indications

NDF_ENABLE: single NDF_ENABLE indication

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

8 x NDF_ENABLE eight consecutive NDF_ENABLE indications

Note 1: the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

Note 2: 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.

Note 3: all three offset values received in 3 x EQ_NEW_POINT must be identical.

Note 4: "consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).

Note 5 "consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications

PAIS is declared on entry to the AIS_state after three consecutive AIS indications

10.5.2 Concatenation pointer interpreter state machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. Within the pointer interpretation algorithm three states are defined as shown below.

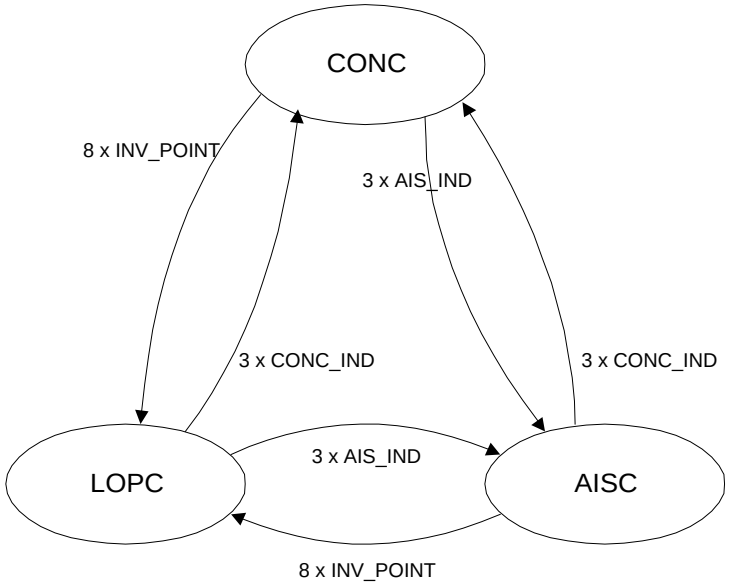
CONC_state (CONC)

AISC_state (AISC)

LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), e.g. three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behaviour is stable and insensitive to low BER.

Figure 10: Concatenation pointer interpretation state diagram



The following events (indications) are defined:

CONC_IND: enabled NDF + dd + “1111111111”

AIS_IND: H1 = FFh + H2 = FFh

INV_POINT: not any of the above (i.e.: not CONC_IND and not AIS_IND)

Note 1: enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

Note 2: the remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, 1111) result in an INV_POINT indication.

Note 3: dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows:

3 X CONC_IND: three consecutive CONC indications

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

Note 1: "consecutive event counters" are reset to zero on a change of state.

LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications

PAISC is declared on entry to the AISC_state after three consecutive AIS indications

10.5.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the SONET (SDH) payloads. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of the STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3 and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block block REI errors can be accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive

frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is increment every time the received PSL differs from the previously received PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 1. PLM-P is removed when the accepted PSL match the expected PSL according to Table 1. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. The PDI-P defect is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 2 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 1: PLM-P, UNEQ-P and PDI-P defects declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive

		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	=expPDI	Match	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	= expPSL	Match	Inactive	Inactive
				!=expPSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	=expPDI	Match	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive

Table 2: Expected PDI defect based on PDI and PDI range values

PDI register value	PDI range register value	Exp PDI	PDI register value	PDI range register value	Exp PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB

	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6 and 7 of the path status byte (G1) to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

The RHPP extracts and serially outputs all the path overhead (POH) bytes on the time multiplexed RPOH port. The POH bytes are output in the same order that they are received (J1, B3, C2, G1, F2, H4, Z3, Z4 and N1). RPOHCLK is the generated output clock used to provide timing for the RPOH port. RPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RPOHFP high with the rising edge of RPOHCLK identifies the MSB of the first J1 byte.

10.6 SONET/SDH Virtual Container Aligner (SVCA)

The SONET (SDH) Virtual Container Aligner (SVCA) block aligns the payload data from an incoming SONET (SDH) data stream to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

10.6.1 Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff

opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Analogously, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

10.6.2 Pointer Generator

The Pointer Generator generates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelope bytes (SPE) of the STS-48c (VC16-16c) payloads. Within the pointer generator algorithm, five states are defined as shown below:

NORM_state (NORM)

AIS_state (AIS)

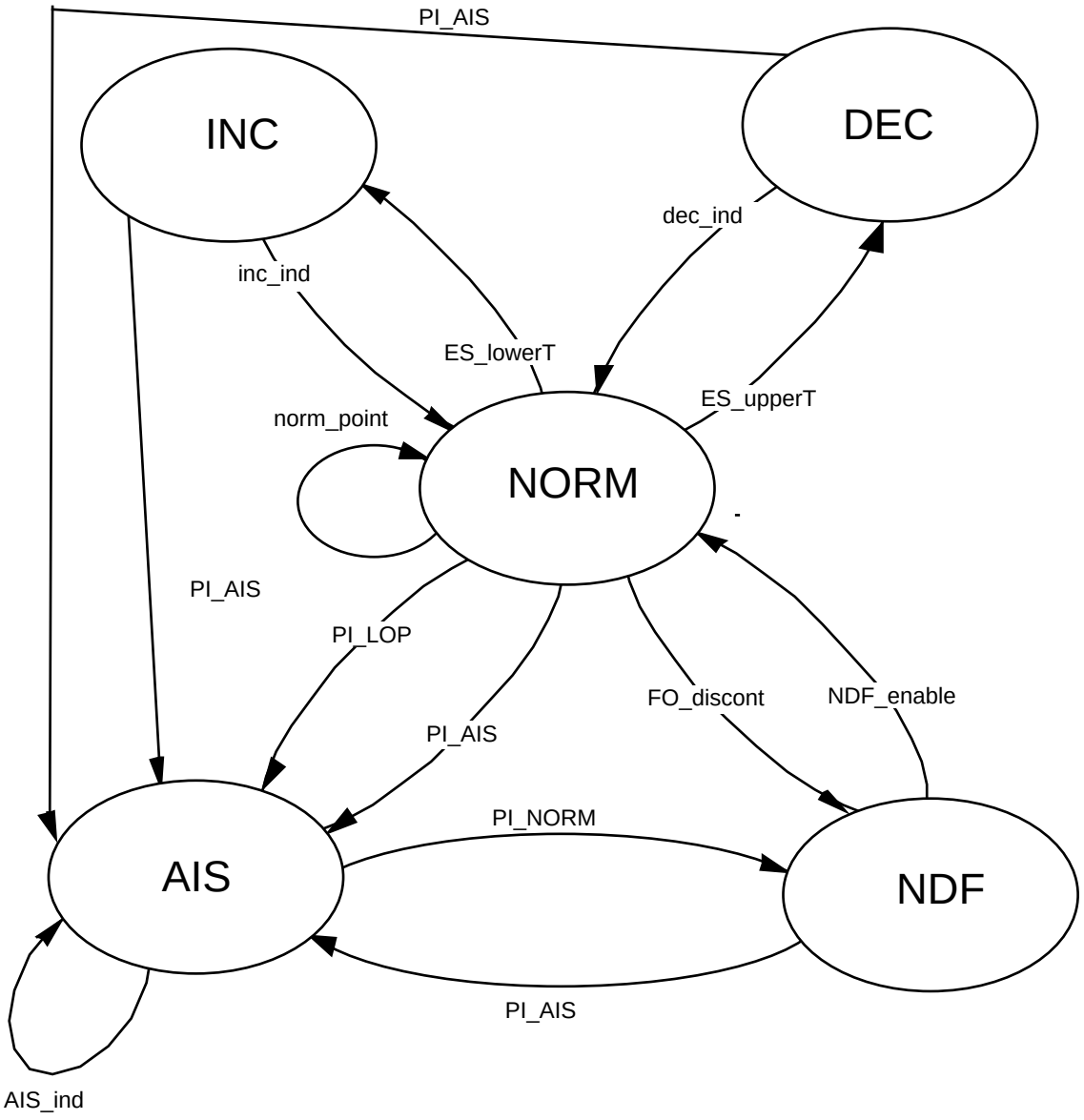
NDF_state (NDF)

INC_state (INC)

DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store block. The transition to/from the AIS state are controlled by the pointer interpreter in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 11: Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont:	frame offset discontinuity
PI_AIS:	PI in AIS state
PI_LOP:	PI in LOP state
PI_NORM:	PI in NORM state
Note 1	A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind:	transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.
dec_ind:	transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.
NDF_enable:	accept new offset as active offset, transmit the pointer with NDF enabled and new offset.
norm_point:	transmit the pointer with NDF disabled and active offset.
AIS_ind:	active offset is undefined, transmit an all-1's pointer and payload.
Note 1	active offset is defined as the phase of the SPE (VC).
Note 2	the ss bits are undefined in SONET, and has bit pattern 10 in SDH
Note 3	enabled NDF is defined as the bit pattern 1001.
Note 4	disabled NDF is defined as the bit pattern 0110.

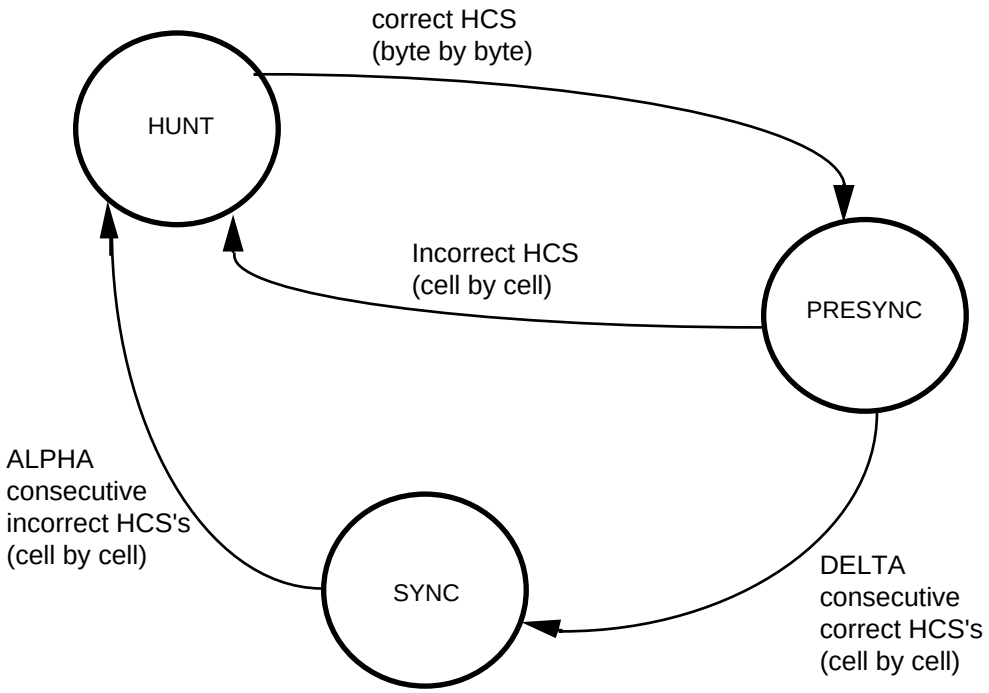
10.7 Receive Cell and Frame Processor (RCFP)

The Receive Cell and Frame Processor (RCFP) performs both ATM and PPP processing. It has the capability to process a single STS-48c (STM-16c) channel.

10.7.1 ATM Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in below.

Figure 12: Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 2 μs for the STS-48c (STM-16c) rate.

10.7.2 ATM Descrambler

The self-synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

10.7.3 ATM Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RCFP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the corrected header contents match the pattern contained in the RCFP Idle Cell Header and Mask register. Idle cell filtering is accomplished by writing the appropriate cell header pattern into the RCFP Idle Cell Header and Mask Pattern register. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RCFP Idle Cell Header and Mask register allows filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RCFP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result. **ATM Performance Monitor**

The Performance Monitor consists of two 16-bit saturating HCS error event counters and a 32-bit saturating receive cell counter. The first error counter accumulates uncorrectable HCS errors. A 32-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss any counted events.

10.7.5 POS Overhead Removal

The overhead removal consists of stripping SONET/SDH overhead bytes from the data stream. Once overhead bytes are removed, the data stream consists of PPP/HDLC frame octets that can be fed directly to the descrambler or the PPP/HDLC Frame Delineation block.

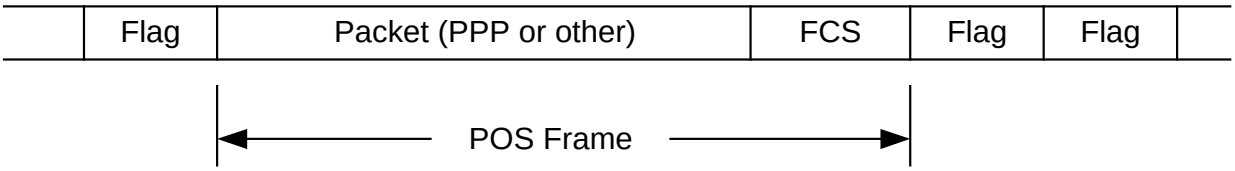
10.7.6 POS Descrambler

When enabled, the self-synchronous descrambler operates on the PPP Frame data, descrambling the data with the polynomial $x^{43}+1$. Descrambling is performed on the raw data stream, before any PPP frame delineation or byte destuffing is performed. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

10.7.7 POS PPP/HDLC Frame Delineation

The PPP/HDLC Frame Delineation is performed on the descrambled data and consists of arranging the framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag and Idle Sequences and passes the data onto the Byte Destuffing block. The PPP/HDLC Frame format is shown in the figure below.

Figure 13: PPP/HDLC Over SONET Frame Format



In the event of a FIFO overflow caused by the FIFO being full while a packet is being received, the packet is marked with an error so it can be discarded by the system. Subsequent bytes associated with this now aborted frame are discarded. Reception of PPP/HDLC data resumes when a Start of Packet is encountered and the FIFO level is below a programmable Reception Initialization Level.

10.7.8 POS Byte Destuffing

The byte destuffing algorithm searches the Control Escape character (0x7D). These characters, listed in the table below are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XORed with 0x20. Therefore, any escaped data byte will be processed properly by the S/UNI-2488.

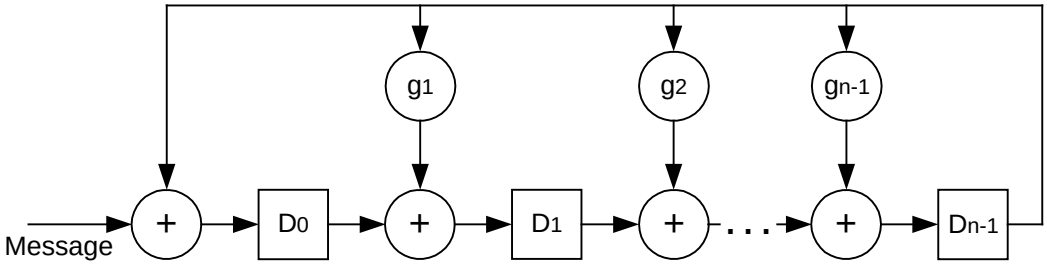
Table 3: Byte Destuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Aborted Packet	7D-7E

10.7.9 POS FCS Check

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, after byte destuffing and data descrambling scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. . Packets with FCS errors are marked as such and should be discarded by the system.

Figure 14: CRC Decoder



10.7.10 POS Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters, one 32-bit saturating received good packet counter, and one 40-bit counter for accumulating packet bytes. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 32-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

The RCFP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but still written into the FIFO. Malformed packets, that is packets that do not at least contain four bytes, are discarded and will be counted as a minimum packet size violation. When the packet size exceeds MAXPL[16:0] the packet is marked with an error and the bytes beyond the maximum count are discarded.

10.8 Receive Scalable Data Queue (RXSDQ)

The RXSDQ provides a FIFO to separate the line-side timing from the higher layer ATM/POS link layer timing. The RXSDQ has two modes of operations, ATM and POS.

10.8.1 Receive ATM FIFO

The RXSDQ is responsible for holding up to 48 cells until they are read by the Receive System Interface.

Receive FIFO management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions. Upon detection of an overrun, the FIFO discards the current cell and discards the incoming cells until there is room in the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit and are considered a system error.

10.8.2 Receive POS FIFO

The RXSDQ contains 48 sixteen byte blocks for FIFO storage, along with management circuitry for reading and writing the FIFO. The receive FIFO provides for the separation of the physical layer timing from the system timing.

Receive FIFO management functions include filling the receive FIFO, indicating when packets or bytes are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun, the FIFO aborts the current packet and discards the current incoming bytes until there is room in the FIFO. Once enough room is available, as defined by the BT[7:0] register bit settings, the RXSDQ will wait for the next start of packet before writing any data into the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit and are considered a system error. A FIFO underrun is caused when the System Interface tries to read more data words while the FIFO is empty. This action will be detected and reported through the FUDRI interrupt, but it is not considered a system error. The system will continue to operate normally. In that situation, RVAL can be used by the Link Layer device to find out if valid or invalid data is provided on the System Interface.

10.9 Receive Phy Interface (RXPHY)

The S/UNI-2488 receive system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides a 32-bit Receive UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI-2488. When configured for POS applications, the system interface provides either a 32-bit POS-PHY Level 3 compliant bus for the transfer of ATM cells and data packets between the link layer device and the S/UNI-2488. The link layer device can implement various protocols, including PPP and HDLC.

10.9.1 Receive UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a read clock (RFCLK) and read enable signal (RENB). The interface indicates the start of a cell (RSOC) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA signal indicates when a cell is available for transfer on the receive data bus RDAT[31:0]. The RPRTY signal reports the parity on the RDAT[31:0] bus (selectable as odd or even parity). This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA is deasserted will output invalid data.

10.9.2 Receive POS-PHY Level 3

The interface accepts a read clock (RFCLK) and read enable signal (RENB) when data is read from the receive FIFO (using the rising edge of the RFCLK). The start of packet RSOP marks the first byte of receive packet data on the RDAT[31:0]. The RPRTY signal determine the parity on the RDAT[31:0] bus (selectable as odd or even parity). The end of a packet is indicated by the REOP signal. Signal RERR is provided to indicate that an error in the received packet has occurred (the error may have several causes include an abort sequence or an FCS error). The RVAL signal is used to indicate when RSOP, REOP, RERR and RDAT[31:0] are valid. Read accesses while RVAL is logic 0 are ignored and will output invalid data. RSX indicates the start of a transfer and marks the clock cycle where the in-band channel address is given on the RDAT bus. The RXPHY performs the polling procedure to select which PHY address is serviced.

10.10 Transmit Line Interface

The Transmit Line Interface allows the S/UNI-2488 to directly interface with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion of the incoming outgoing 2488.32 Mbit/s data stream.

The transmit clock is synthesized from a 155.52. MHz reference. The transfer function yields a typical low pass corner of **TBD** MHz above which reference jitter is attenuated at **TBD** dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free 155.52MHz reference, the intrinsic jitter is typically less than **TBD** UI RMS when measured using a high pass filter with a **TBD** cutoff frequency.

The REFCLK reference should be within ±20 ppm to meet the SONET free-run accuracy requirements specified in GR-253-CORE.

The Parallel to Serial Converter (PISO) converts the transmit byte serial stream to a bit serial stream. The transmit bit serial stream appears on the TXD+/- PECL outputs.

10.11 SONET/SDH Transmit Line Interface (STLI)

The SONET/SDH transmit line interface block properly formats the outgoing 2488 Mbit/s data stream. This block interfaces the TRMP to the Tx Line Interface block.

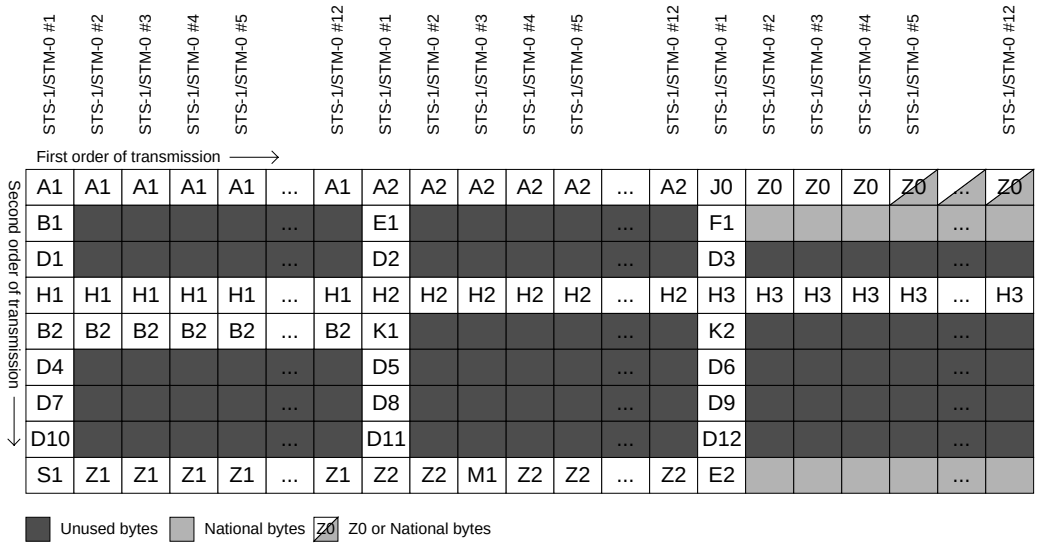
10.12 Transmit Regenerator Multiplexor Processor (TRMP)

The Transmit Regenerator and Multiplexor Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream.

The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two line BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-L and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated. For STS-48c (STM-16c), the maximum single BIP-8 error count is 0xFF while the maximum block BIP-24 error count is 0x10.

The TRMP serially inputs all the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). TTOHCLK is the generated output clock used to provide timing for the TTOH port. TTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TTOHFP high with the rising edge of TTOHCLK identifies the MSB of the first A1 byte. TTOHEN port is used to validate the byte insertion on a byte per byte basis. When TTOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TTOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

Figure 15: STS-48c (STM-16-16c) on TTOH



Note, only the overhead from the first STS-12 (STM-4) of the STS-48c (STM-16c) can be sourced. Overhead from the other three STS-12s (STM-4s) are internally generated assigned or are assigned default values as described below.

The TRMP also inserts most of the transport overhead bytes from internal registers. Since there is multiple sources for the same overhead byte, the TOH bytes must be prioritised according to Table 4 before being inserted into the data stream.

Table 4: TOH insertion priority

BYTE	HIGHEST priority				LOWEST priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)	A1 pass through
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)	A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGEN=1)	TTOH (TTOHEN=1)	J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN=1)	TTOH (TTOHEN=1)	Z0 pass through
B1				Calculated B1 xor TTOH (TTOHEN=1 & B1MASKEN=1)	Calculated B1 xor B1MASK
				TTOH (TTOHEN=1 & B1MASKEN=0)	
E1			E1V (E1REGEN=1)	TTOH (TTOHEN=1)	E1 pass through
F1			F1V	TTOH	F1 pass through

			(F1REGEN=1)	(TTOHEN=1)	
D1-D3			D1D3V (D1D3REGEN=1)	TTOH (TTOHEN=1)	D1-D3 pass through
H1				H1 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)	H1 pass through xor H1MASK
				TTOH (TTOHEN=1 & HMASKEN=0)	
H2				H2 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)	H2 pass through xor H2MASK
				TTOH (TTOHEN=1 & HMASKEN=0)	
H3				TTOH (TTOHEN=1)	H3 pass through
B2				Calculated B2 xor TTOH (TTOHEN=1 & B2MASKEN=1)	Calculated B2 xor B2MASK
				TTOH (TTOHEN=1 & B2MASKEN=0)	
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGEN=1)	TTOH (TTOHEN=1)	K1 pass through
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGEN=1)	TTOH (TTOHEN=1)	K2 pass through
D4-D12			D4D12V (D4D12REGEN=1)	TTOH (TTOHEN=1)	D4-D12 pass through
S1			S1V (S1REGEN=1)	TTOH (TTOHEN=1)	S1 pass through
Z1			Z1V (Z1REGEN=1)	TTOH (TTOHEN=1)	Z1 pass through
Z2			Z2V (Z2REGEN=1)	TTOH (TTOHEN=1)	Z2 pass through
M1			LREI[7:0] (LREIEN=1)	TTOH (TTOHEN=1)	M1 pass through
E2			E2V (E2REGEN=1)	TTOH (TTOHEN=1)	E2 pass through
National			NATIONALV (NATIONALEN=1)	TTOH (TTOHEN=1)	National pass through
Unused			UNUSEDV (UNUSEDEN=1)	TTOH (TTOHEN=1)	Unused pass through
PLD					PLD pass through

The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to BELLCORE.

Table 5: Z0/National growth bytes definition for row #1

TRMP mode	Type	Z0DEF = 1	Z0DEF = 0
STS-48c (STM-16) slave mode	Z0	From STS-1/STM-0 #1 to #4	From STS-1/STM-0 #1 to #12
	National	From STS-1/STM-0 #5 to #12	None

The H1, H2, B1 and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1 and B2 bytes depending on the HMASK, B1MASK and B2MASK register bits of the TRMP Error Insertion register. When the HMASK, B1MASK or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is xor with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI must be inserted, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling. The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

10.13 Transmit Tail Trace Processor (TTTP)

The Transmit Tail Trace Processor (TTTP) block generates the tail trace messages to be transmitted. The TTTP can generate a 16 or 64 byte tail trace message. The message is source from an internal RAM and must have been previously written by an external micro processor. Optionally, the tail trace message can be reduced to a single continuous tail trace byte.

The tail trace message must include synchronisation because the TTTP does not add synchronisation. The synchronisation mechanism is different for a 16 bytes message and for a 64 bytes message. When the message is 16 bytes, the synchronisation is based on the MSB of the tail trace byte. Only one of the 16 bytes has is MSB set high. The byte with its MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronisation is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of tail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP forces the message to all zeros while the microprocessor updates the internal RAM.

10.14 Transmit High Order Path Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are returned to the far end as path remote error indication (REI-P) during the next transmit frame. Because the RHPP and the THPP are in two different clock domains, none, one or two path BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated.

The THPP serially inputs all the path overhead (POH) bytes from the TPOH port. The POH bytes must be input in the same order that they are transmitted (J1, B3, C2, G1, F2, H4, F3, K3 and N1). TOHCLK is the generated output clock used to provide timing for the TPOH port. TOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TPOHRDY high with the rising edge of TOHCLK identifies the MSB of the first J1 byte. TPOHEN port is used to validate the byte insertion on a byte per byte basis. When TPOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TPOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B3 byte of the following frame.

10.15 Transmit Cell and Frame Processor (TCFP)

The Transmit Cell and Frame Processor (TCFP) performs both ATM and PPP processing. It has the capability to process a single STS-48c (STM-16c) channel. In ATM mode, the TCFP performs provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. In POS mode, the TCFP provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs packet data scrambling, and provides performance monitoring functions.

10.15.1 ATM Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

10.15.2 ATM Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler (x^{43} + 1 polynomial) described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

10.15.3 ATM HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

10.15.4 POS PPP/HDLC Frame Generator

The PPP/HDLC Frame Generator runs off of the SONET sequencer to create the POS frames to be transmitted. Flags are inserted whenever the Transmit FIFO is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packets from the Transmit FIFO and transmits them. In addition, FCS generation, error insertion, byte stuffing, and scrambling can be optionally enabled.

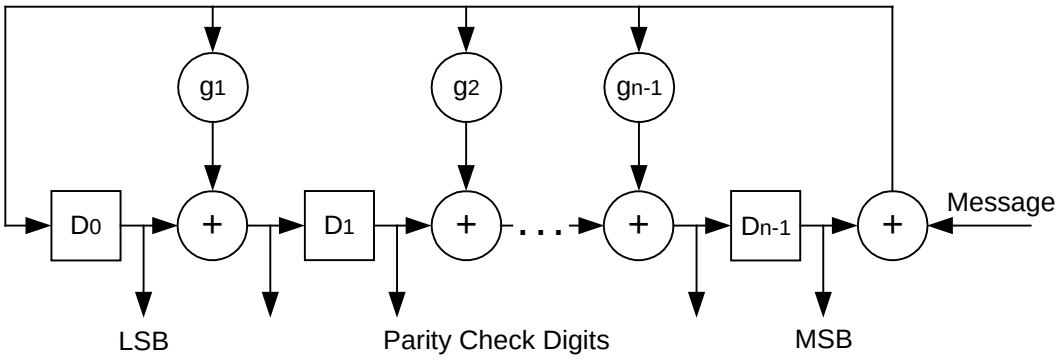
In the event of a FIFO underflow caused by the FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The PPP Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with the Flag Sequence in the outgoing data stream. If an overflow occurs, the packet being transmitted will also be aborted and the same abort sequence will be added. Transmission of data resumes when a Start of Packet is encountered in the FIFO data stream.

The POS Frame Generator also performs Inter Packet Gapping. This operation consists of inserting a programmable number of Flag and Idle Sequence characters between each PPP/HDLC Frame transmission. This feature allows one to control the system effective data transmission rate if required.

10.15.5 POS FCS Generator

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the one's complement of the CRC register after calculation ends. FCS calculation and insertion can be disabled.

Figure 16: CRC Generator



An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting the resulting FCS value, before transmission. This should cause an FCS Error at the far end.

10.15.6 POS Byte Stuffing

The PPP Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are being escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is being escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 6: Byte Stuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Abort Sequence	7D-7E

10.15.7 Data Scrambling

The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. On reset, the scrambler is set to all ones to ensure scrambling on start-up. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

10.16 Transmit Scalable Data Queue (TXSDQ)

The TXSDQ provides a FIFO to separate the line-side timing from the higher layer ATM/POS link layer timing. The TXSDQ has two modes of operations, ATM and POS.

10.16.1 Transmit ATM FIFO

The TXSDQ is responsible for holding up to 48 cells until they can be read and transmitted. The cells are written in with a single 32-bit data bus running off TFCLK and are read out at the channel rate. Internal read and write pointers track the cells and indicate the fill status of the Transmit FIFO. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing (TFCLK).

10.16.2 Transmit POS FIFO

The TXSDQ contains 48 sixteen byte blocks for FIFO storage, along with management circuitry for reading and writing the FIFO. Octets are written in with a single 32-bit data bus running off TFCLK and are read out with a single 32-bit data bus. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing.

Internal read and write pointers track the insertion and removal of octets, and indicate the fill status of the Transmit FIFO. These status indications are used to detect underrun and overrun conditions, abort packets as appropriate on both System and Line sides, control flag insertion and to generate the DTPA output.

10.17 Transmit Phy Interfaces (RXPHY and TXPHY)

The S/UNI-2488 transmit system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides a 32-bit transmit UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI-2488. When configured for POS applications, the system interface provides either a 32-bit POS-PHY Level 3 compliant bus for the transfer of ATM cells and data packets between the link layer device and the S/UNI-2488. The link layer device can implement various protocols, including PPP and HDLC.

10.17.1 Transmit UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). To reduce FIFO latency, the FIFO depth at which TCA indicates “full” can be configured from the TXSDQ. If the programmed depth is less than the TXSDQ FIFO capacity, more than one cell may be written after TCA is deasserted as the TXSDQ FIFO still allows the “maximum” cells to be stored in its FIFO. The interface provides the transmit cell available status (TCA) which can transition from "available" to "unavailable" when the transmit FIFO is near full or when the FIFO is full and can accept no more writes. The TCFP cell processor automatically transmit idle cells until a full cell is available to be transmitted.

10.17.2 Transmit POS-PHY Level 3 Interface

The POS-PHY Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of packet (TSOP) indication, the end of packet (TEOP) indication, errored packet (TERR) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). The TPA signal notifies that the transmit FIFO is not full (the POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or the entire packet is in the FIFO). The TMOD signal (Transmit Mod) is provided to indicate whether 1, 2, 3, or 4 bytes are valid of the final word transfer (TEOP is asserted). A packet may be aborted by asserting the TERR signal at the end of the packet. The interface also indicates FIFO overruns via a maskable interrupt and register bits. The TCFP HDLC processor automatically transmits idle flag characters until sufficient data is available in the transmit TXSDQ to start transmission.

10.18 SONET/SDH Bit Error Rate Monitor (SBER)

The SBER block provides two independent bit error rate monitoring circuits (BERM block). It is used to monitor the Multiplexer Section BIP (B1) with one BERM block dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarm can then be used to control system level features such as Automatic Protection Switching (APS).

The BERM block utilizes a sliding window based algorithm.

10.19 SONET/SDH Alarm Reporting Controller (SARC)

The SARC block receives all the section, line, and path defects detected by the receive overhead processors and, according to user specific configuration, generates consequent action indications.

Receive section alarm (RSALM) indication: RSALM is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

Receive line AIS insertion (RLAISINS) indication: RLAISINS is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration register allow the user to remove any defect from the previous enumeration.

Transmit line RDI insertion (TLRDIINS) indication: TLRDIINS is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration register allow the user to remove any defect from the previous enumeration.

Receive path alarm (RPALM) indication: RPALM is asserted when a RSALM, MSRSALM, AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

Receive path alarm insertion (RPAISINS) indication: RPAISINS is asserted when a RLAISINS, MSRLAISINS, AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

Transmit path ERDI insertion (TPERDIINS[2:0]) indication: TPERDIINS[2:0] is updated when a PLU-P, PLM-P, TIU-P, TIM-P, UNEQ-P, LOP-P or a AIS-P defect is detected in the receive data stream. Configuration register allow the user to remove any defect from the previous enumeration.

10.20 SONET/SDH Inband Error Report Processor (SIRP)

The SIRP block is used for error reporting from a remote APS protect mate when operating as the working mate under a failure condition. When in the failure condition, the remote protect mate performs section, line and path termination and passes the expected P-REI and P-RDI indications back to the working mate in-band in the G1 byte via its output APS port. The SIRP block processes remote alarm indications in the SONET/SDH data stream from the Input APS port. The SIRP in the companion working mate can be configured to extract remote defect indications (RDI) and remote error indications (REI) from a STS-48c (STM-4c) incoming data stream. Accumulated remote error indications and remote defect indications are reported to the THPP block. Both RDI and extended RDI modes are available. The RDI report can be configured to be maintained asserted for at least 10 frames or 20 frames.

10.21 APS Serial Data Interface

The APS Serial Data Interface consists of a input and output 777.76 Mbps serial TeleCombus used to communicate between a working and protect mate for APS applications.

10.21.1 Output APS Serial Data Interface (D8E, APISO, TXLV)

The Output APS Serial Data Interface uses the four sets of D8E, APISO and TXLV blocks to transmit a SONET (SDH) stream to a working or protect mate. The SONET (SDH) OC-48 stream is selected from either the THPP or SVCA block and serialized on a 777.76 Mbps serial TeleCombus. When the S/UNI-2488 is configured as the working mate, the Output APS Serial Data Interface selects the transmit path processed SONET (SDH) stream from the THPP block and transmits it through the 4 differential LVDS pairs, APSO+/-[4:1] to the protect mate where the stream is line and section processed. When the S/UNI-2488 is configured as the protect mate, the Output APS Serial Data Interface selects receive path terminated SONET (SDH) stream from the SVCA block and transmit it through the 4 differential LVDS pairs, APSO+/-[4:1] to the working mate. The working mate will then process the SONET (SDH) payload (ATM or POS) and pass the results to the system via the UTOPIA Level 3 or POSPHY Level 3 interface.

There are four sets of DE8, APISO and TXLV blocks. Each set implements one of four serial streams that make up the output serial TelecomBus. The D8E block takes a SONET (SDH) stream and 8B/10B encodes it. The APISO block performs a parallel to serial conversion. The TXLV block is a differential LVDS transmitter.

10.21.2 Input APS Serial Data Interface (RXLV, DRU, R8TB)

The Input APS Serial Data Interface uses the four sets of RXLV, DRU and R8TB blocks to receive a SONET (SDH) stream from a working or protect mate via a serial TelecomBus. The received SONET (SDH) OC-48 stream is passed to either the RCFP or TRMP block for further processing. When the S/UNI-2488 is configured as the working mate and when a failure condition exists, a receive path processed SONET (SDH) stream is expected from the protect mate on the 4 differential LVDS pairs, APSI+/-[4:1]. The S/UNI-2488 will pass this received stream to the RCFP for ATM or POS payload processing. When the S/UNI-2488 is configured as the protect mate and when a failure condition exists, a transmit path processed SONET (SDH) stream is expected from the working mate on the 4 differential LVDS pairs, APSI+/-[4:1]. The S/UNI-2488 will pass this received stream to the TRMP for SONET line and section insertion before it is transmitted.

There are four sets of RXLV, DRU and R8TB blocks. Each set implements one of four serial streams that make up the input serial TelecomBus. The RXLV block is a differential LVDS receiver. The DRU recovers the 777.76 Mbps 8B/10B encoded serial stream and deserializes it for the R8TB block. The R8TB block converts the deserialized 8B/10B stream into the a SONET (SDH) stream.

10.21.3 LVDS Transmit Reference (TXREF)

The TXLVREF provides an on-chip bandgap voltage reference (1.20V ±5%) and a precision current to the TXLVs. The reference voltage is used to control the common-mode level of the TXLV output, while the reference current is used to control the output amplitude. The precision currents are generated by forcing the reference voltage across an external, off-chip 4.75kΩ (±1%) resistor. The resulting current is then mirrored through several individual reference current outputs, so each TXLV receives its own reference current.

10.21.4 Clock Synthesis Unit (CSU)

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 777.6 MHz for the usage by the transmitter.

10.22 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-2488 identification code is 053810CD hexadecimal.

10.23 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the S/UNI-2488. The normal mode registers are used during normal operation to configure and monitor the S/UNI-2488. The test mode registers are used to enhance the testability of the S/UNI-2488. The register set is accessed as shown below. The corresponding memory map address is identified by the address column of the table. Addresses that are not shown are not used and must be treated as Reserved.

Table 7: Register Memory Map

Address	Register Description
0000	S/UNI-2488 Identity, and Global Performance Monitor Update
0001	S/UNI-2488 Master Reset, Configuration, and Loopback
0002	S/UNI-2488 Reserved
0003	S/UNI-2488 Clock Monitors
0004	S/UNI-2488 Master Interrupt Status #1
0005	S/UNI-2488 Master Interrupt Status #2
0006	S/UNI-2488 Master Interrupt Status #3
0007	S/UNI-2488 Master Interrupt Status #4
0008	S/UNI-2488 Master Interrupt Status #5
0009	S/UNI-2488 Master Interrupt Status #6
000A	S/UNI-2488 Master Interrupt Status #8
000B	Unused

Address	Register Description
000C	S/UNI-2488 APS Input TeleCombus Synchronization Delay
000D	S/UNI-2488 APS Output TeleCombus Synchronization Delay
000E	S/UNI-2488 Diagnostics
000F	S/UNI-2488 FREE Register
0010-001F	Rx2488 Analog Reserved
0020-002F	Tx2488 Analog Reserved
0030	SRLI Clock Configuration
0031	SRLI PGM Clock Configuration
0032-0037	SRLI Reserved
0038	STLI Clock Configuration
0039	STLI PGM Clock Configuration
003A-003F	STLI Reserved
0040	RRMP Configuration
0041	RRMP Status
0042	RRMP Interrupt Enable
0043	RRMP Interrupt Status
0044	RRMP Received APS
0045	RRMP Received SSM
0046	RRMP AIS enable
0047	RRMP Section BIP Error Counter
0048	RRMP Line BIP Error Counter (LSB)
0049	RRMP Line BIP Error Counter (MSB)
004A	RRMP Line REI Error Counter (LSB)
004B	RRMP Line REI Error Counter (MSB)
004C-004FH	RRMP Reserved 1
0050-005FH	RRMP Reserved 2
0060-006FH	RRMP Reserved 3
0070-007FH	RRMP Reserved 4
0080	TRMP Configuration
0081	TRMP Register Insertion
0082	TRMP Error Insertion
0083	TRMP Transmit J0 and Z0
0084	TRMP Transmit E1 and F1
0085	TRMP Transmit D1D3 and D4D12
0086	TRMP Transmit K1 and K2
0087	TRMP Transmit S1 and Z1
0088	TRMP Transmit Z2 and E2

Address	Register Description
0089	TRMP H1 and H2 Mask
008A	TRMP B1 and B2 Mask
008B-009F	TRMP Reserved 1
00A0	TRMP Aux2 Configuration
00A1	TRMP Reserved 2
00A2	TRMP Aux2 Error Insertion
00A3-00BF	TRMP Reserved 2
00C0	TRMP Aux3 Configuration
00C1	TRMP Reserved 3
00C2	TRMP Aux3 Error Insertion
00C3-00DF	TRMP Reserved 3
00E0	TRMP Aux4 Configuration
00E1	TRMP Reserved 4
00E2	TRMP Aux4 Error Insertion
00E3-00FF	TRMP Reserved 4
0100-010F	S/UNI-2488 Reserved
0110	SBER Configuration
0111	SBER Status
0112	SBER Interrupt Enable
0113	SBER Interrupt Status
0114	SBER SF BERM Accumulation Period (LSB)
0115	SBER SF BERM Accumulation Period (MSB)
0116	SBER SF BERM Saturation Threshold (LSB)
0117	SBER SF BERM Saturation Threshold (MSB)
0118	SBER SF BERM Declaring Threshold (LSB)
0119	SBER SF BERM Declaring Threshold (MSB)
011A	SBER SF BERM Clearing Threshold (LSB)
011B	SBER SF BERM Clearing Threshold (MSB)
011C	SBER SD BERM Accumulation Period (LSB)
011D	SBER SD BERM Accumulation Period (MSB)
011E	SBER SD BERM Saturation Threshold (LSB)
011F	SBER SD BERM Saturation Threshold (MSB)
0120	SBER SD BERM Declaring Threshold (LSB)
0121	SBER SD BERM Declaring Threshold (MSB)
0122	SBER SD BERM Clearing Threshold (LSB)
0123	SBER SD BERM Clearing Threshold (MSB)
0124-012F	SBER Reserved

Address	Register Description
0130	RTTP SECTION Indirect Address
0131	RTTP SECTION Indirect Data
0132	RTTP SECTION Trace Unstable Status
0133	RTTP SECTION Trace Unstable Interrupt Enable
0134	RTTP SECTION Trace Unstable Interrupt Status
0135	RTTP SECTION Trace Mismatch Status
0136	RTTP SECTION Trace Mismatch Interrupt Enable
0137	RTTP SECTION Trace Mismatch Interrupt Status
0138	TTTP SECTION Indirect Address
0139	TTTP SECTION Indirect Data
013A-013B	TTTP SECTION Reserved
013C-01FF	S/UNI-2488 Reserved
0200	RHPP STS-1/STM-0 #1 through #12 Indirect Address
0201	RHPP STS-1/STM-0 #1 through #12 Indirect Data
0202-0207	RHPP Reserved
0208	RHPP STS-1/STM-0 #1 Pointer Interpreter Status
0209	RHPP STS-1/STM-0 #1 Pointer Interpreter Interrupt Enable
020A	RHPP STS-1/STM-0 #1 Pointer Interpreter Interrupt Status
020B	RHPP STS-1/STM-0 #1 Error Monitor Status
020C	RHPP STS-1/STM-0 #1 Error Monitor Interrupt Enable
020D	RHPP STS-1/STM-0 #1 Error Monitor Interrupt Status
020E	RHPP STS-1/STM-0 #1 Path BIP Error Counter
020F	RHPP STS-1/STM-0 #1 Path REI Error Counter
0210	RHPP STS-1/STM-0 #2 Pointer Interpreter Status
0211	RHPP STS-1/STM-0 #2 Pointer Interpreter Interrupt Enable
0212	RHPP STS-1/STM-0 #2 Pointer Interpreter Interrupt Status
0213-0217	RHPP Reserved
0218	RHPP STS-1/STM-0 #3 Pointer Interpreter Status
0219	RHPP STS-1/STM-0 #3 Pointer Interpreter Interrupt Enable
021A	RHPP STS-1/STM-0 #3 Pointer Interpreter Interrupt Status
021B-021F	RHPP Reserved
0220	RHPP STS-1/STM-0 #4 Pointer Interpreter Status
0221	RHPP STS-1/STM-0 #4 Pointer Interpreter Interrupt Enable
0222	RHPP STS-1/STM-0 #4 Pointer Interpreter Interrupt Status
0223-0227	RHPP Reserved
0228	RHPP STS-1/STM-0 #5 Pointer Interpreter Status
0229	RHPP STS-1/STM-0 #5 Pointer Interpreter Interrupt Enable

Address	Register Description
022A	RHPP STS-1/STM-0 #5 Pointer Interpreter Interrupt Status
022B-022F	RHPP Reserved
0230	RHPP STS-1/STM-0 #6 Pointer Interpreter Status
0231	RHPP STS-1/STM-0 #6 Pointer Interpreter Interrupt Enable
0232	RHPP STS-1/STM-0 #6 Pointer Interpreter Interrupt Status
0233-0237	RHPP Reserved
0238	RHPP STS-1/STM-0 #7 Pointer Interpreter Status
0239	RHPP STS-1/STM-0 #7 Pointer Interpreter Interrupt Enable
023A	RHPP STS-1/STM-0 #7 Pointer Interpreter Interrupt Status
023B-023F	RHPP Reserved
0240	RHPP STS-1/STM-0 #8 Pointer Interpreter Status
0241	RHPP STS-1/STM-0 #8 Pointer Interpreter Interrupt Enable
0242	RHPP STS-1/STM-0 #8 Pointer Interpreter Interrupt Status
0243-0247	RHPP Reserved
0248	RHPP STS-1/STM-0 #9 Pointer Interpreter Status
0249	RHPP STS-1/STM-0 #9 Pointer Interpreter Interrupt Enable
024A	RHPP STS-1/STM-0 #9 Pointer Interpreter Interrupt Status
024B-024F	RHPP Reserved
0250	RHPP STS-1/STM-0 #10 Pointer Interpreter Status
0251	RHPP STS-1/STM-0 #10 Pointer Interpreter Interrupt Enable
0252	RHPP STS-1/STM-0 #10 Pointer Interpreter Interrupt Status
0253-0257	RHPP Reserved
0258	RHPP STS-1/STM-0 #11 Pointer Interpreter Status
0259	RHPP STS-1/STM-0 #11 Pointer Interpreter Interrupt Enable
025A	RHPP STS-1/STM-0 #11 Pointer Interpreter Interrupt Status
025B-025F	RHPP Reserved
0260	RHPP STS-1/STM-0 #12 Pointer Interpreter Status
0261	RHPP STS-1/STM-0 #12 Pointer Interpreter Interrupt Enable
0262	RHPP STS-1/STM-0 #12 Pointer Interpreter Interrupt Status
0263-027F	RHPP Reserved
0280	RHPP STS-1/STM-0 #13 through #24 Indirect Address
0281	RHPP STS-1/STM-0 #13 through #24 Indirect Data
0282-0287	RHPP Reserved
0288	RHPP STS-1/STM-0 #13 Pointer Interpreter Status
0289	RHPP STS-1/STM-0 #13 Pointer Interpreter Interrupt Enable
028A	RHPP STS-1/STM-0 #13 Pointer Interpreter Interrupt Status
028B-028F	RHPP Reserved

Address	Register Description
. . . . .	. . . . .
02E0	RHPP STS-1/STM-0 #24 Pointer Interpreter Status
02E1	RHPP STS-1/STM-0 #24 Pointer Interpreter Interrupt Enable
02E2	RHPP STS-1/STM-0 #24 Pointer Interpreter Interrupt Status
02E3-02FF	RHPP Reserved
0300	RHPP STS-1/STM-0 #25 through #36 Indirect Address
0301	RHPP STS-1/STM-0 #25 through #36 Indirect Data
0302-0307	RHPP Reserved
0308	RHPP STS-1/STM-0 #25 Pointer Interpreter Status
0309	RHPP STS-1/STM-0 #25 Pointer Interpreter Interrupt Enable
030A	RHPP STS-1/STM-0 #25 Pointer Interpreter Interrupt Status
030B-030F	RHPP Reserved
. . . . .	. . . . .
0360	RHPP STS-1/STM-0 #36 Pointer Interpreter Status
0361	RHPP STS-1/STM-0 #36 Pointer Interpreter Interrupt Enable
0362	RHPP STS-1/STM-0 #36 Pointer Interpreter Interrupt Status
0363-036F	RHPP Reserved
0380	RHPP STS-1/STM-0 #37 through #48 Indirect Address
0381	RHPP STS-1/STM-0 #37 through #48 Indirect Data
0382-0387	RHPP Reserved
0388	RHPP STS-1/STM-0 #37 Pointer Interpreter Status
0389	RHPP STS-1/STM-0 #37 Pointer Interpreter Interrupt Enable
038A	RHPP STS-1/STM-0 #37 Pointer Interpreter Interrupt Status
038B-038F	RHPP Reserved
. . . . .	. . . . .
03E0	RHPP STS-1/STM-0 #48 Pointer Interpreter Status
03E1	RHPP STS-1/STM-0 #48 Pointer Interpreter Interrupt Enable
03E2	RHPP STS-1/STM-0 #48 Pointer Interpreter Interrupt Status
03E3-03FF	RHPP Reserved
0400	THPP STS-1/STM-0 #1 through #12 Indirect Address
0401	THPP STS-1/STM-0 #1 through #12 Indirect Data
0402	THPP Payload Configuration
0402-047F	THPP Reserved 1
0480	THPP STS-1/STM-0 #13 through #24 Indirect Address
0481	THPP STS-1/STM-0 #13 through #24 Indirect Data
0482-04FF	THPP Reserved 2
0500	THPP STS-1/STM-0 #25 through #36 Indirect Address

Address	Register Description
0501	THPP STS-1/STM-0 #25 through #36 Indirect Data
0502-057F	THPP Reserved 3
0580	THPP STS-1/STM-0 #37 through #48 Indirect Address
0581	THPP STS-1/STM-0 #37 through #48 Indirect Data
0582-05FF	THPP Reserved 4
0600	RSVCA Indirect Address
0601	RSVCA Indirect Data
0602	RSVCA Payload Configuration
0603	RSVCA Positive Justification Interrupt Status
0604	RSVCA Negative Justification Interrupt Status
0605	RSVCA FIFO Overflow Interrupt Status
0606	RSVCA FIFO Underflow Interrupt Status
0607-061F	RSVCA Reserved 1
0620-063F	RSVCA Reserved 2
0640-065F	RSVCA Reserved 3
0660-067F	RSVCA Reserved 4
0680	TSVCA Indirect Address
0681	TSVCA Indirect Data
0682	TSVCA Payload Configuration
0683	TSVCA Positive Justification Interrupt Status
0684	TSVCA Negative Justification Interrupt Status
0685	TSVCA FIFO Overflow Interrupt Status
0686	TSVCA FIFO Underflow Interrupt Status
0687-069F	TSVCA Reserved 1
06A0-06BF	TSVCA Reserved 2
06C0-06DF	TSVCA Reserved 3
06E0-06FF	TSVCA Reserved 4
0700	RTTP PATH Indirect Address
0701	RTTP PATH Indirect Data
0702	RTTP PATH Trace Unstable Status
0703	RTTP PATH Trace Unstable Interrupt Enable
0704	RTTP PATH Trace Unstable Interrupt Status
0705	RTTP PATH Trace Mismatch Status
0706	RTTP PATH Trace Mismatch Interrupt Enable
0707	RTTP PATH Trace Mismatch Interrupt Status
0708	TTTP PATH Indirect Address
0709	TTTP PATH Indirect Data

Address	Register Description
070A-070B	TTTP PATH Reserved
070C-071F	S/UNI-2488 Reserved
0720	SARC Indirect Address
0721	SARC Reserved
0722	SARC Section Configuration
0723	SARC Section SALM
0724	SARC Section RLAISINS Enable
0725	SARC Section TLAISINS Enable
0726-0727	SARC Reserved
0728	SARC Path Configuration
0729	SARC Path RALM Enable
072A	SARC Path RPAISINS Enable
072B-072F	SARC Reserved
0730	SARC LOP Pointer Status
0731	SARC LOP Pointer Interrupt Enable
0732	SARC LOP Pointer Interrupt Status
0733	SARC AIS Pointer Status
0734	SARC AIS Pointer Interrupt Enable
0735	SARC AIS Pointer Interrupt Status
0736-073F	SARC Reserved
0740	RCFP Configuration
0741	RCFP Interrupt Enable
0742	RCFP Interrupt Indication and Status
0743	RCFP Minimum Packet Length
0744	RCFP Maximum Packet Length
0745	RCFP LCD Count Threshold
0746	RCFP Idle Cell Header and Mask
0747	RCFP Receive Byte/Idle Cell Counter (LSB)
0748	RCFP Receive Byte/Idle Cell Counter
0749	RCFP Receive Byte/Idle Cell Counter (MSB)
074A	RCFP Packet/Cell Counter (LSB)
074B	RCFP Receive Packet/ATM Cell Counter (MSB)
074C	RCFP Receive Erred FCS/HCS Counter
074D	RCFP Receive Aborted Packet Counter
074E	RCFP Receive Minimum Length Packet Error
074F	RCFP Receive Maximum Length Packet Error Counter
0750	TCFP Configuration

Address	Register Description
0751	TCFP Interrupt Indication
0752	TCFP Idle/Unassigned ATM Cell Header
0753	TCFP Diagnostics
0754	TCFP Transmit Cell/Packet Counter (LSB)
0755	TCFP Transmit Cell/Packet Counter (MSB)
0756	TCFP Transmit Byte Counter (LSB)
0757	TCFP Transmit Byte Counter
0758	TCFP Transmit Byte Counter (MSB)
0759	TCFP Aborted Packet Counter
075A-075F	TCFP Reserved
0760	RXSDQ FIFO Reset
0761	RXSDQ FIFO Interrupt Enable
0762	RXSDQ Reserved
0763	RXSDQ FIFO Overflow Port and Interrupt Indication
0764	RXSDQ FIFO SOP Error Port and Interrupt Indication
0765	RXSDQ FIFO EOP Error Port and Interrupt Indication
0766	RXSDQ Reserved
0767	RXSDQ Reserved
0768	RXSDQ FIFO Indirect Address
0769	RXSDQ FIFO Indirect Configuration
076A	RXSDQ FIFO Indirect Data Available Threshold
076B	RXSDQ FIFO Indirect Cells and Packets Count
076C	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
076D	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
076E	RXSDQ FIFO Cells and Packets Dropped Aggregate Count
076F	RXSDQ Reserved
0770	TXSDQ FIFO Reset
0771	TXSDQ FIFO Interrupt Enable
0772	TXSDQ Reserved
0773	TXSDQ FIFO Overflow Port and Interrupt Indication
0774	TXSDQ FIFO SOP Error Port and Interrupt Indication
0775	TXSDQ FIFO EOP Error Port and Interrupt Indication
0776	TXSDQ Reserved
0777	TXSDQ Reserved
0778	TXSDQ FIFO Indirect Address
0779	TXSDQ FIFO Indirect Configuration
077A	TXSDQ FIFO Indirect Data and Buffer Available Thresholds

Address	Register Description
077B	TXSDQ FIFO Indirect Cells and Packets Count
077C	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
077D	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
077E	TXSDQ FIFO Cells and Packets Dropped Aggregate count
077F	TXSDQ Reserved
0780	RXPHY Configuration
0781	RXPHY Interrupt Status
0782	RXPHY Interrupt Enable
0783	RXPHY Indirect Burst Size
0784	RXPHY Calendar Length
0785	RXPHY Calendar Indirect Address Data
0786	RXPHY Data Type Field
0787	RXPHY Reserved
0788	TXPHY Configuration
0789	TXPHY Interrupt Status
078A	TXPHY Interrupt Enable
078B	TXPHY Data Type Field
078C-078F	TXPHY Reserved
0790	SIRP Configuration Timeslot
0791-079B	SIRP Reserved 1
079C	SIRP Configuration
079D-079F	SIRP Reserved 1
07A0-07AF	SIRP Reserved 2
07B0-07BF	SIRP Reserved 2
07C0-07CF	SIRP Reserved 2
07D0-07FF	S/UNI-2488 Reserved
0800	PRGM Indirect Address
0801	PRGM Indirect Data
0802	PRGM Generator Payload Configuration
0803	PRGM Monitor Payload Configuration
0804	PRGM Monitor Byte Error Interrupt Status
0805	PRGM Monitor Byte Error Interrupt Enable
0806	PRGM Monitor B1/E1 Bytes Interrupt Status
0807	PRGM Monitor B1/E1 Bytes Interrupt Enable
0808	PRGM Monitor B1/E1 Bytes Status
0809	PRGM Monitor Synchronization Interrupt Status
080A	PRGM Monitor Synchronization Interrupt Enable

Address	Register Description
080B	PRGM Monitor Synchronization Status
080C	PRGM Reserved
080D-080F	PRGM Reserved
0810	PRGM Aux2 Indirect Address
0811	PRGM Aux2 Indirect Data
0812	PRGM Aux2 Generator Payload Configuration
0813	PRGM Aux2 Monitor Payload Configuration
0814	PRGM Aux2 Monitor Byte Error Interrupt Status
0815	PRGM Aux2 Monitor Byte Error Interrupt Enable
0816-0818	PRGM Aux2 Reserved
0819	PRGM Aux2 Monitor Synchronization Interrupt Status
081A	PRGM Aux2 Monitor Synchronization Interrupt Enable
081B	PRGM Aux2 Monitor Synchronization Status
081C-081F	PRGM Aux2 Reserved
0820	PRGM Aux3 Indirect Address
0821	PRGM Aux3 Indirect Data
0822	PRGM Aux3 Generator Payload Configuration
0823	PRGM Aux3 Monitor Payload Configuration
0824	PRGM Aux3 Monitor Byte Error Interrupt Status
0825	PRGM Aux3 Monitor Byte Error Interrupt Enable
0826-0828	PRGM Aux3 Reserved
0829	PRGM Aux3 Monitor Synchronization Interrupt Status
082A	PRGM Aux3 Monitor Synchronization Interrupt Enable
082B	PRGM Aux3 Monitor Synchronization Status
082C-082F	PRGM Aux3 Reserved
0830	PRGM Aux3 Indirect Address
0831	PRGM Aux3 Indirect Data
0832	PRGM Aux4 Generator Payload Configuration
0833	PRGM Aux4 Monitor Payload Configuration
0834	PRGM Aux4 Monitor Byte Error Interrupt Status
0835	PRGM Aux4 Monitor Byte Error Interrupt Enable
0836-0838	PRGM Aux4 Reserved
0839	PRGM Aux4 Monitor Synchronization Interrupt Status
083A	PRGM Aux4 Monitor Synchronization Interrupt Enable
083B	PRGM Aux4 Monitor Synchronization Status
083C-083F	PRGM Aux4 Reserved
0840	R8TD APS0 Control and Status

Address	Register Description
0841	R8TD APS0 Interrupt Status
0842	R8TD APS0 Line Code Violation Count
0843	R8TD APS0 Analog Control 1
0844	R8TD APS0 Analog Control 2
0845-0847	R8TD APS0 Reserved
0848	R8TD APS1 Control and Status
0849	R8TD APS1 Interrupt Status
084A	R8TD APS1 Line Code Violation Count
084B	R8TD APS1 Analog Control 1
084C	R8TD APS1 Analog Control 2
084D-084F	R8TD APS1 Reserved
0850	R8TD APS2 Control and Status
0851	R8TD APS2 Interrupt Status
0852	R8TD APS2 Line Code Violation Count
0853	R8TD APS2 Analog Control 1
0854	R8TD APS2 Analog Control 2
0855-0857	R8TD APS2 Reserved
0858	R8TD APS3 Control and Status
0859	R8TD APS3 Interrupt Status
085A	R8TD APS3 Line Code Violation Count
085B	R8TD APS3 Analog Control 1
085C	R8TD APS3 Analog Control 2
085D-085F	R8TD APS3 Reserved
0860	T8TE APS0 Control and Status
0861	T8TE APS0 Interrupt Status
0862	T8TE APS0 TeleCombus Mode #1
0863	T8TE APS0 TeleCombus Mode #2
0864	T8TE APS0 Test Pattern
0865	T8TE APS0 Analog Control
0866	T8TE APS0 DTB Bus
0867	T8TE APS0 Reserved
0868	T8TE APS1 Control and Status
0869	T8TE APS1 Interrupt Status
086A	T8TE APS1 TeleCombus Mode #1
086B	T8TE APS1 TeleCombus Mode #2
086C	T8TE APS1 Test Pattern
086D	T8TE APS1 Analog Control

Address	Register Description
086E	T8TE APS1 DTB Bus
086F	T8TE APS1 Reserved
0870	T8TE APS2 Control and Status
0871	T8TE APS2 Interrupt Status
0872	T8TE APS2 TeleCombus Mode #1
0873	T8TE APS2 TeleCombus Mode #2
0874	T8TE APS2 Test Pattern
0875	T8TE APS2 Analog Control
0876	T8TE APS2 DTB Bus
0877	T8TE APS2 Reserved
0878	T8TE APS3 Control and Status
0879	T8TE APS3 Interrupt Status
087A	T8TE APS3 TeleCombus Mode #1
087B	T8TE APS3 TeleCombus Mode #2
087C	T8TE APS3 Test Pattern
087D	T8TE APS3 Analog Control
087E	T8TE APS3 DTB Bus
087F	T8TE APS3 Reserved
0880-0883	RFCLK DLL Reserved
0884-0887	TFCLK DLL Reserved
0888	CSTR Control
0889	CSTR Interrupt Enable and CSU Lock Status
088A	CSTR CSU Lock Interrupt Indication
088B	CSTR Reserved
088C-088F	S/UNI-2488 Reserved
0890-0897	S/UNI-2488 Rx STSI Reserved
0898-089F	S/UNI-2488 Tx STSI Reserved
08A0-1FFF	S/UNI-2488 Reserved
2000-2FFF	S/UNI-2488 Test

Notes on Register Memory Map:

1. For all register accesses, CSB must be low.

2. Addresses that are not shown must be treated as Reserved.

3. A[13] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-2488. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-2488 to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-2488 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-2488 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Register 0000H: S/UNI-2488 Identity, and Global Performance Monitor Update

Bit	Type	Function	Default
Bit 15	R	TIP	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R	TYPE[4]	0
Bit 7	R	TYPE[3]	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision number of the S/UNI-2488 to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI-2488.

In addition, writing to this register performs a global performance monitor update by simultaneously loading all the performance meter registers in the RHPP, RRMP, RCFP, RXSDQ, TXSDQ, TCFP, R8TD, and T8TE blocks.

ID[3:0]:

The ID bits can be read to provide a binary S/UNI-2488 revision number.

TYPE[4:0]:

The TYPE bits can be read to distinguish the S/UNI-2488 from the other members of the family of devices. The TYPE[4:0] register for the PM5381 S/UNI-2488 is 00010.

TIP:

The TIP bit is set to a logic one when the performance meter registers are being loaded. Writing to this register with DRESET equal to logic 0 initiates an accumulation interval transfer and loads all the performance meter registers in the S/UNI-2488.
TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Register 0001H: S/UNI-2488 Master Reset, Configuration, and Loopback

Bit	Type	Function	Default
Bit 15	R/W	DRESET	0
Bit 14	R/W	ARESET	0
Bit 13	R/W	TXDINV	0
Bit 12	R/W	RXDINV	0
Bit 11	R/W	DISCOR	1
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PL3EN	0
Bit 5	R/W	MODE[1]	0
Bit 4	R/W	MODE[0]	0
Bit 3	R/W	LOOPT	0
Bit 2	R/W	PDLE	0
Bit 1	R/W	SDLE	0
Bit 0	R/W	SLLE	0

This register allows the configuration of S/UNI-2488 features.

SLLE:

The SLLE bit enables the S/UNI-2488 line loopback mode when the device is configured for 2488.32 Mbit/s serial line interface mode of operation. When SLLE is a logic one, the recovered data from the receive serial RXD+/- differential inputs is mapped to the TXD+/- differential outputs. The SDLE and the SLLE bits should not be set high simultaneously.

SDLE:

The SDLE bit enables the serial diagnostic loopback. When SDLE is a logic one, the transmit serial stream on the TXD+/- differential outputs is internally connected to the received serial RXD+/- differential inputs. The SDLE and the SLLE bits should not be set high simultaneously.

PDLE:

The Parallel Diagnostic Loopback, PDLE bit enables the S/UNI-2488 diagnostic loopback where the TRMP block is directly connected to its RRMP block. When PDLE is logic one, loopback is enabled. Under this operating condition, the S/UNI-2488 continues to operates

normally in the transmit direction. When PDLE is logic zero, the S/UNI-2488 operates normally.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the channel. When LOOPT is a logic zero, the transmitter timing is derived from input REFCLK (Clock Synthesis Unit). When LOOPT is a logic one, the transmitter timing is derived from the recovered clock (Clock Recovery Unit).

The S/UNI-2488 cannot be configured for loop time operation if operating with a mate device unless both the received clocks are frequency locked.

MODE[1:0]:

The MODE bits selects one of the four operating mode of the S/UNI-2488 as illustrated below:

MODE[1:0]	Description
00	Normal operation. The S/UNI-2488 is configured in this mode when not using the APS ports. When using the APS ports, the S/UNI-2488 is configured in this mode if a failover condition does not exist. Under this mode of operation, the S/UNI-2488 receives data from RXD+/- and outputs this data though its POS-PHY Level 3 interface and transmits data from its POS-PHY Level 3 interface out through TXD+/-.
01	Reserved
10	APS Working Mate under a failed condition. The S/UNI-2488 can be configured in this mode when operating as the working device in a APS failover condition. Under this mode of operation, the S/UNI-2488 receives a SONET stream from a protect mate via the Input APS port and presents the payload out through the POS-PHY Level 3 interface. The S/UNI-2488 transmits data from its POS-PHY Level 3 interface out thorough its Output APS port to a mate device. It is assumed that the mate device will transmit the data onto the line.
11	APS Protect Mate. The S/UNI-2488 is always configured in this mode as a protect device. Under this mode of operation, the Input APS port is expected to contain a bridged transmit SONET stream from a working mate device. In addition, the S/UNI-2488 will output a received SONET stream out the Output APS port to the same mate device.

PL3EN:

The POS-PHY Level 3 Select bit (POSL3) is OR'ed with the POSL3_UL3B pin to select POS-PHY Level 3 mode on the system interface. When POSL3 or POSL3_UL3B are logic 1, the system bus operates in POS-PHY Level 3 mode. When both POSL3 and POSL3_UL3B are logic 0, the bus operates as a UTOPIA Level 3 bus. Reading this bit gives the mode of the bus, (ie, the OR of the pin and the bit). The default state of this register bit is logic 0.

DISCOR:

The DISCOR bit is used to globally disable ATM single-bit HCS error correction. When DISCOR is set to logic 1, HCS error correction is globally disabled. When DISCOR is set to logic 0, HCS error correction is dependent on the RCFP Configuration register. By default, HCS error correction is enabled in the RCFP.

RXDINV:

The receive inversion RXDINV bit controls the polarity of the receive data. When RXDINV is set high, the polarity of the RXD+/- is inverted. When RXDINV is set low, the RXD+/- inputs operate normally.

TXDINV:

The transmit inversion TXDINV bit controls the polarity of the transmit data. When TXDINV is set high, the polarity of the TXD+/- is inverted. When TXDINV is set low, the TXD+/- outputs operate normally.

ARESET:

The ARESET bit allows the analog circuitry in the S/UNI-2488 to be reset under software control. If the ARESET bit is a logic one, all the S/UNI-2488 analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-2488 out of reset. Holding the S/UNI-2488 in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET bit, thus negating the analog software reset.

DRESET:

The DRESET bit allows the digital circuitry in the S/UNI-2488 to be reset under software control. If the DRESET bit is a logic one, all the S/UNI-2488 digital circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-2488 out of reset A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register 0003H: S/UNI-2488 Clock Monitors

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	TCLKA	X
Bit 3	R	RCLKA	X
Bit 2	R	RFCLKA	X
Bit 1	R	TFCLKA	X
Bit 0	R	REFCLKA	X

REFCLKA:

The REFCLK active (REFCLKA) bit monitors for low to high transitions on the REFCLK reference clock input. REFCLKA is set high on a rising edge of REFCLK, and is set low when this register is read.

TFCLKA:

The TFCLK active (TFCLKA) bit monitors for low to high transitions on the TFCLK transmit FIFO clock input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

RFCLKA:

The RFCLK active (RFCLKA) bit monitors for low to high transitions on the RFCLK receive FIFO clock input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

RCLKA:

The RCLK active (RCLKA) bit monitors for low to high transitions on the RCLK output. RCLKA is set high on a rising edge of RCLK, and is set low when this register is read.

TCLKA:

The TCLK active (TCLKA) bit monitors for low to high transitions on the TCLK output. TCLKA is set high on a rising edge of TCLK, and is set low when this register is read.

Register 0004H: S/UNI-2488 Master Interrupt Status #1

Bit	Type	Function	Default
Bit 15	R/W	INTE[1]	0
Bit 14	R	TSTSII	X
Bit 13	R	Unused	X
Bit 12	R	TPRGMI[1]	X
Bit 11	R	TSVCAI[1]	X
Bit 10	R	RSTSII	X
Bit 9	R	RPRGMI[1]	X
Bit 8	R	SARCI[1]	X
Bit 7	R	RSVCAI[1]	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	PATHRTTPI[1]	X
Bit 3	R	RHPPI[1]	X
Bit 2	R	SBERI[1]	X
Bit 1	R	RTTPI[1]	X
Bit 0	R	RRMPI[1]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[1]…TSTSI:

The RRMPI[1] to TSTSI are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[1]:

The interrupt enable (INTE[1]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[1], the RRMP[1]…ASTSI pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[1], the RRMP[1]…TSTSI pending interrupt will not assert the interrupt (INTB) output.

Register 0005H: S/UNI-2488 Master Interrupt Status #2

Bit	Type	Function	Default
Bit 15	R/W	INTE[2]	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	TPRGMI[2]	X
Bit 11	R	TSVCAI[2]	X
Bit 10	R	Unused	X
Bit 9	R	RPRGMI[2]	X
Bit 8	R	SARCI[2]	X
Bit 7	R	RSVCAI[2]	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RHPPI[2]	X
Bit 2	R	SBERI[2]	X
Bit 1	R	RTTPI[2]	X
Bit 0	R	RRMPI[2]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[2]…TPRGMI[2]:

The RRMPI[2] to TPRGMI[2] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[2]:

The interrupt enable (INTE[2]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[2], the RRMP[2]…TPRGM[2] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[2], the RRMP[2]…TPRGM[2] pending interrupt will not assert the interrupt (INTB) output.

Register 0006H: S/UNI-2488 Master Interrupt Status #3

Bit	Type	Function	Default
Bit 15	R/W	INTE[3]	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	TPRGMI[3]	X
Bit 11	R	TSVCAI[3]	X
Bit 10	R	Unused	X
Bit 9	R	RPRGMI[3]	X
Bit 8	R	SARCI[3]	X
Bit 7	R	RSVCAI[3]	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RHPPI[3]	X
Bit 2	R	SBERI[3]	X
Bit 1	R	RTTPI[3]	X
Bit 0	R	RRMPI[3]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[3]…TPRGMI[3]:

The RRMPI[3] to TPRGMI[3] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[3]:

The interrupt enable (INTE[3]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[3], the RRMP[3]…TPRGM[3] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[3], the RRMP[3]…TPRGM[3] pending interrupt will not assert the interrupt (INTB) output.

Register 0007H: S/UNI-2488 Master Interrupt Status #4

Bit	Type	Function	Default
Bit 15	R/W	INTE[4]	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	TPRGMI[4]	X
Bit 11	R	TSVCAI[4]	X
Bit 10	R	Unused	X
Bit 9	R	RPRGMI[4]	X
Bit 8	R	SARCI[4]	X
Bit 7	R	RSVCAI[4]	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RHPPI[4]	X
Bit 2	R	SBERI[4]	X
Bit 1	R	RTTPI[4]	X
Bit 0	R	RRMPI[4]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[4]…TPRGMI[4]:

The RRMPI[4] to TPRGMI[4] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[4]:

The interrupt enable (INTE[4]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[4], the RRMP[4]…TPRGM[4] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[4], the RRMP[4]…TPRGM[4] pending interrupt will not assert the interrupt (INTB) output.

Register 0008H: S/UNI-2488 Master Interrupt Status #5

Bit	Type	Function	Default
Bit 15	R/W	INTE[5]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	RXPHYI	X
Bit 8	R	RXSDQI	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	RCFPI	X

This register is used to indicate interrupts generated from blocks associated with the receive UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

RCFPI:

The RCFP interrupt event indication (RCFPI) transitions to logic 1 when a hardware interrupt event is sourced from RCFP #***x*** block. This bit is cleared to logic 0 when the interrupt is cleared.

RXSDQI:

The RXSDQ interrupt event indication (RXSDQI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system FIFO RXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

RXPHYI:

The RXPHY interrupt event indication (RXPHYI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system UTOPIA/POS-PHY interface RXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

INTE[5]:

The interrupt enable (INTE[5]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[5], the RCFPI, RXSDQI or RXPHYI pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[5], the RCFPI, RXSDQI or RXPHYI pending interrupt will not assert the interrupt (INTB) output.

Register 0009H: S/UNI-2488 Master Interrupt Status #6

Bit	Type	Function	Default
Bit 15	R/W	INTE[6]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	TXPHYI	X
Bit 8	R	TXSDQI	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TCFPI	X

This register is used to indicate interrupts generated from blocks associated with the transmit UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

TCFPI:

The RCFP interrupt event indication (TCFPI) transitions to logic 1 when a hardware interrupt event is sourced from TCFP block. This bit is cleared to logic 0 when the interrupt is cleared.

TXSDQI:

The TXSDQ interrupt event indication (TXSDQI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system FIFO TXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

TXPHYI:

The RXPHY interrupt event indication (TXPHYI) transitions to logic 1 when a hardware interrupt event is sourced from the transmit system UTOPIA/POS-PHY interface TXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

INTE[6]:

The interrupt enable (INTE[6]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[6], the TCFPI, TXSDQI or TXPHYI pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[6], the TCFPI, TXSDQI or TXPHYI pending interrupt will not assert the interrupt (INTB) output.

Register 000AH: S/UNI-2488 Master Interrupt Status #7

Bit	Type	Function	Default
Bit 15	R/W	INTE[7]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	CRSTI	X
Bit 11	R	T8TE4I	X
Bit 10	R	T8TE3I	X
Bit 9	R	T8TE2I	X
Bit 8	R	T8TE1I	X
Bit 7	R	TxANALOGI	X
Bit 6	R	RXANALOGI	X
Bit 5	R	DLL_TFCLKI	X
Bit 4	R	DLL_RFCLKI	X
Bit 3	R	R8TD4I	X
Bit 2	R	R8TD3I	X
Bit 1	R	R8TD2I	X
Bit 0	R	R8TD1I	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

TSB1, TSB2 etc…..:

The interrupt event indications transition to logic 1 when a hardware interrupt event is sourced from the corresponding block. The corresponding bit is cleared to logic 0 when the interrupt is cleared.

Register 000BH: Unused

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register is unused

Register 000CH: APS Input TeleCombus Synchronization Delay

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	AIJ0DLY[13]	0
Bit 12	R/W	AIJ0DLY[12]	0
Bit 11	R/W	AIJ0DLY[11]	0
Bit 10	R/W	AIJ0DLY[10]	0
Bit 9	R/W	AIJ0DLY[9]	0
Bit 8	R/W	AIJ0DLY[8]	0
Bit 7	R/W	AIJ0DLY[7]	0
Bit 6	R/W	AIJ0DLY[6]	0
Bit 5	R/W	AIJ0DLY[5]	0
Bit 4	R/W	AIJ0DLY[4]	0
Bit 3	R/W	AIJ0DLY[3]	0
Bit 2	R/W	AIJ0DLY[2]	0
Bit 1	R/W	AIJ0DLY[1]	0
Bit 0	R/W	AIJ0DLY[0]	0

This register controls the delay from the APSIFP input signal to the time when the S/UNI-2488 may safely process the J0 characters delivered by the APS Input serial data links (APSI+/-[4:1]).

AIJ0DLY[13:0]:

The APS Input transport frame delay bits (AIJ0FP[13:0]) controls the delay, in REFCLK cycles, inserted by the S/UNI-2488 before processing the J0 characters delivered by the APS Input serial data links (APSI+/-[4:1]). AIJ0DLY is set such that after the specified delay, all active APS Input links would have delivered the J0 character. The relationships of AIJ0FP, AIJ0DLY[13:0] and the system configuration are described in the Functional Timing section.

Valid values of AIJ0DLY[13:0] are 0000H to 25F7H.

Register 000DH: APS Output TeleCombus Synchronization Delay

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	AOJ0REFDLY[13]	0
Bit 12	R/W	AOJ0REFDLY[12]	0
Bit 11	R/W	AOJ0REFDLY[11]	0
Bit 10	R/W	AOJ0REFDLY[10]	0
Bit 9	R/W	AOJ0REFDLY[9]	0
Bit 8	R/W	AOJ0REFDLY[8]	0
Bit 7	R/W	AOJ0REFDLY[7]	0
Bit 6	R/W	AOJ0REFDLY[6]	0
Bit 5	R/W	AOJ0REFDLY[5]	0
Bit 4	R/W	AOJ0REFDLY[4]	0
Bit 3	R/W	AOJ0REFDLY[3]	0
Bit 2	R/W	AOJ0REFDLY[2]	0
Bit 1	R/W	AOJ0REFDLY[1]	0
Bit 0	R/W	AOJ0REFDLY[0]	0

This register controls the delay from the APSIFP input signal to the time when the S/UNI-2488 produces the J0 pulse on the APS Output serial data links (APSO+/-[4:1]).

AOJ0REFDLY[13:0]:

The APS Output transport frame delay bits (AOJ0REFDLY [13:0]) control the delay, in REFCLK cycles, inserted by the S/UNI-2488 between receiving a reference J0 frame pulse on APSIFP, and presenting the outgoing J0 character on APSO+/-[4:1]. The relationships of APSIFP, AOJ0REFDLY [13:0] and the system configuration are described in the Functional Timing section.

Valid values of AOJ0REFDLY [13:0] are 0000H to 25F7H.

Register 000EH: S/UNI-2488 Diagnostics

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	TSVCA_ESDIS	0
Bit 4	R/W	RSVCA_ESDIS	0
Bit 3	R/W	TLD_VAL	0
Bit 2	R/W	TSLD_VAL	0
Bit 1	R/W	DS	0
Bit 0	R/W	DD	0

DD:

The Disable Descrambling (DD) bit is used to disable SONET descrambling perfomed by the RRMP block. When set to a logic 1, SONET descrambling is disabled. When set to a logic 0, SONET descrambling is enabled. For normal operation, this bit should be set to a logic zero.

DS:

The Disable Scrambling (DS) bit is used to disable SONET scrambling perfomed by the TRMP block. When set to a logic 1, SONET scrambling is disabled. When set to a logic 0, SONET scrambling is enabled. For normal operation, this bit should be set to a logic zero.

TSLD_VAL:

The TSLD value (TSLD_VAL) bit is used to set the value optionally inserted into the section or line DCC in the transmit data stream as configured using the TSLDEN bit in the TRMP Configuration register. When set to a logic 1, ones are inserted. When set to a logic 0, zeros are inserted.

TLD_VAL:

The TLD value (TLD_VAL) bit is used to set the value optionally inserted into the section or line DCC in the transmit data stream as configured using the TLDEN bit in the TRMP Configuration register. When set to a logic 1, ones are inserted. When set to a logic 0, zeros are inserted.

RSVCA_ESDIS:

The RSVCA elastic store disable (RSVCA_ESDIS) bit is used to disable the elastic store. This bit should normally be set to 0.

TSVCA_ESDIS:

The TSVCA elastic store disable (TSVCA_ESDIS) bit is used to disable the elastic store. This bit should normally be set to 0.

Register 000FH: S/UNI-2488 FREE Register

Bit	Type	Function	Default
Bit 15	R/W	FREE[15]	0
Bit 14	R/W	FREE[14]	0
Bit 13	R/W	FREE[13]	0
Bit 12	R/W	FREE[12]	0
Bit 11	R/W	FREE[11]	0
Bit 10	R/W	FREE10]	0
Bit 9	R/W	FREE[9]	0
Bit 8	R/W	FREE[8]	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

FREE[7:0]:

The FREE[7:0] field may be freely modified by firmware.

Register 0010H: Rx2488 Analog Interrupt Control/Status

Bit	Type	Function	Default
Bit 15	R	PRBS_SYNC_I	0
Bit 14	R	PRBS_ERR_I	0
Bit 13	R	FIFO_OVRF_I	0
Bit 12	R	FIFO_UNDF_I	0
Bit 11	R	LOS_I	0
Bit 10	R	DOOL_I	0
Bit 9	R	ROOL_I	0
Bit 8		UNUSED	X
Bit 7		UNUSED	X
Bit 6	R/W	PRBS_SYNC_EN	0
Bit 5	R/W	PRBS_ERR_EN	0
Bit 4	R/W	FIFO_OVRF_EN	0
Bit 3	R/W	FIFO_UNDF_EN	0
Bit 2	R/W	LOS_EN	0
Bit 1	R/W	DOOL_EN	0
Bit 0	R/W	ROOL_EN	0

The Interrupt Control/Status register is provided at RCS_2488 read/write address 0100.

ROOL_EN:

The Reference Out Of Lock Enable bit connects the ROOL_I status bit to the ECBI_INTB pin of the RCS_2488. When ROOL_EN is set to logic one, an interrupt on the ECBI_INTB is generated upon assertion of the ROOL_I register bit. When ROOL_EN is set low, a change in the ROOL_I status does not generate an interrupt.

DOOL_EN:

The Data Out Of Lock Enable bit connects the DOOL_I status bit to the ECBI_INTB pin of the RCS_2488. When DOOL_EN is set to logic one, an interrupt on the ECBI_INTB is generated upon assertion of the DOOL_I register bit. When DOOL_EN is set low, a change in the DOOL_I status does not generate an interrupt.

LOS_EN:

The Loss of Signal Enable bit connects the LOS_I status bit to the ECBI_INTB pin of the RCS_2488. When LOS_EN is set to logic one, an interrupt on the ECBI_INTB is generated upon assertion of the LOS_I register bit. When LOS_EN is set low, a change in the LOS_I status does not generate an interrupt.

FIFO_UNDF_EN:

The FIFO Underflow Enable bit connects the FIFO_UNDF_I status bit to the ECBI_INTB pin of the RCS_2488. When FIFO_UNDF_EN is set to logic one, an interrupt on the ECBI_INTB

is generated upon assertion of the FIFO_UNDF_I register bit. When FIFO_UNDF_EN is set low, a change in the FIFO_UNDF_I status does not generate an interrupt.

FIFO_OVRF_EN:

The FIFO Overflow Enable bit connects the FIFO_OVRF_I status bit to the ECBI_INTB pin of the RCS_2488. When FIFO_OVRF_EN is set to logic one, an interrupt on the ECBI_INTB is generated upon assertion of the FIFO_OVRF_I register bit. When FIFO_OVRF_EN is set low, a change in the FIFO_OVRF_I status does not generate an interrupt.

PRBS_ERR_EN:

The PRBS Error Enable bit connects the PRBS_ERR_I status bit to the ECBI_INTB pin of the RCS_2488. When PRBS_ERR_EN is set to logic one, an interrupt on the ECBI_INTB is generated upon assertion of the PRBS_ERR_I register bit. When PRBS_ERR_EN is set low, a change in the PRBS_ERR_I status does not generate an interrupt.

PRBS_SYNC_EN:

The PRBS Synchronized Enable bit connects the PRBS_SYNC_I status bit to the ECBI_INTB pin of the RCS_2488. When PRBS_SYNC_EN is set to logic one, an interrupt on the ECBI_INTB is generated upon assertion of the PRBS_SYNC_I register bit. When PRBS_SYNC_EN is set low, a change in the PRBS_SYNC_I status does not generate an interrupt.

ROOL_I:

The recovered reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK. ROOL_I is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the REFCLK frequency. At startup, ROOL_I may remain at logic 1 for several hundred millisecond while the PLL obtains lock. This bit is only cleared by over-writing with a ‘1’.

DOOL_I:

The recovered data out of lock status indicates the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOL_I is a logic one if the divided down recovered clock frequency is not within 488 ppm of the REFCLK frequency of if no transitions have occurred on the RXD input for more than LOS_COUNT[4:0] bits. This bit is only cleared by over-writing with a ‘1’.

LOS_I:

The loss of signal status indicates the receive signal is lost or at least LOS_COUNT[4:0] consecutive ones or zeros have been received. LOS_I is a logic zero if the SDI input is high or less than LOS_COUNT[4:0] consecutive ones or zeros have been received. LOS_I is a logic one if the SDI input is low or LOS_COUNT[4:0] consecutive ones or zeros have been received. This bit is only cleared by over-writing with a ‘1’.

FIFO_UNDF_I:

The FIFO Underflow bit provides a status indication of an underflow condition in the Rx data slip-buffer. When FIFO_UNDF_I is set to ‘1’ the data written to the slip-buffer has underflowed and data invalid data has been read from the FIFO. This bit is only cleared by over-writing with a ‘1’.

FIFO_OVRF_I:

The FIFO Overflow bit provides a status indication of an overflow condition in the Rx data slip-buffer. When FIFO_OVRF_I is set to ‘1’ the data written to the slip-buffer has overflowed and data has been lost. This bit is only cleared by over-writing with a ‘1’.

PRBS_ERR_I:

The PRBS Bit Error bit provides a status indication that a bit error has been detected in the comparison between the incoming data and the locally generated data. The PRBS_ERR_I is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected. This bit is only cleared by over-writing with a ‘1’.

PRBS_SYNC_I:

The PRBS Synchronization bit indicates that a change in the status of PRBS Monitor has occurred. the comparison between the incoming data and the PRBS pattern generated locally. The PRBS_SYNC_I is set high when the monitor is in the synchronized state and has received four consecutive errored bytes forcing the PRBS monitor to resynchronize. This bit is only cleared by over-writing with a ‘1’.

Register 0011H: Rx2488 Analog CRU Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R/W	CRU_RESET	0
Bit 13	R/W	CSU_RESET	0
Bit 12	R/W	RX2488_ENABLE	1
Bit 11	R/W	CRU_ENABLE	1
Bit 10		Unused	X
Bit 9	R/W	IDDQ_ENABLE	0
Bit 8	R/W	CSU_CLOCK	0
Bit 7	R/W	CRU_MODE[7]	0
Bit 6	R/W	CRU_MODE[6]	0
Bit 5	R/W	CRU_MODE[5]	1
Bit 4	R/W	CRU_MODE[4]	0
Bit 3	R/W	CRU_MODE[3]	1
Bit 2	R/W	CRU_MODE[2]	0
Bit 1	R/W	CRU_MODE[1]	0
Bit 0	R/W	CRU_MODE[0]	1

The CRU Control register is provided at RCS_2488 read/write address 0101.

CRU_MODE[7:0]:

The CRU Mode control bits are used to place the CRU is one of the following modes:

Table 8 CRU Mode Control

MODE BITS	Description
7	Override Lock to Data. When high forces the CRU to remain locked to the reference clock. When low the CRU state machine controls the CRU.
6:5	Loop Filter Modes: 00 = 1.25 K ohm 01 = 2.5 K ohm 10 = 5.0 K ohm 11 = 10 K ohm The default is 2.5 K ohm
4	Disable Narrow-banding feature (i.e. current offset). Active High
3	Enable CSU Narrow-banding and disable on-board ICO current offset. Active High
2	Override Lock to Reference. When high forces the CRU to remain locked to the data. When low the CRU state machine controls the CRU.
1:0	Rate Select Bits: 00 = OC3 01 = OC48 10 = OC12 11 = OC48

CSU_CLOCK:

The Clock Source Unit Reference Clock selection bit is used to select the source of the CSU clock. If CSU_CLOCK is set to logic 1 the clock for CSUCLKI input Pin is used as the reference. If CSU_CLOCK is set to logic 0 than the reference clock is obtained from the CRU.

IDDQ_ENABLE:

The IDDQ_ENABLE bit activates the IDDQ (Quiescent Current) test mode. When set to '1' all Analog Circuits are disabled and the IDDQ of the digital circuits can be measured. When this bit is set to '0' all analog circuits operate normally. This bit is only used during production testing.

CRU_ENABLE:

The Clock Recovery Unit Enable provides a global power down of the CRU Analog Block Circuit. When set to '0' this bit forces the ABC to a low power state and functionality is disabled. When set to '1' the ABC operates in the normal mode of operation.

RX2488_ENABLE:

The 2.488GHz Receiver Enable provides a global power down of the RX2488 Analog Block Circuit. When set to ‘0’ this bit forces the ABC to a low power state and functionality is disabled. When set to ‘1’ the ABC operates in the normal mode of operation.

CSU_RESET:

The Clock Source Unit Reset provides a complete reset of the CRU Analog Block Circuit. When set to ‘0’ this bit forces the ABC to a known initial state. While the bit is set to ‘1’ the functionality of the block is disabled. When set to ‘0’ the ABC operates in the normal mode of operation. This bit is not self-clearing. Therefore a ‘0’ must writing to the bit to remove the reset condition.

CRU_RESET:

The Clock Recovery Unit Reset provides a complete reset of the CRU Analog Block Circuit. When set to ‘0’ this bit forces the ABC to a known initial state. While the bit is set to ‘1’ the functionality of the block is disabled. When set to ‘0’ the ABC operates in the normal mode of operation. This bit is not self-clearing. Therefore a ‘0’ must writing to the bit to remove the reset condition.

Register 0012H: Rx2488 Analog CRU Clock Training Configuration and Status

Bit	Type	Function	Default
Bit 15	R/W	LOS_COUNT[4]	1
Bit 14	R/W	LOS_COUNT[3]	0
Bit 13	R/W	LOS_COUNT[2]	0
Bit 12	R/W	LOS_COUNT[1]	0
Bit 11	R/W	LOS_COUNT[0]	0
Bit 10	R/W	FILL_LEVEL[5]	1
Bit 9	R/W	FILL_LEVEL[4]	1
Bit 8	R/W	FILL_LEVEL[3]	0
Bit 7	R/W	FILL_LEVEL[2]	0
Bit 6	R/W	FILL_LEVEL[1]	0
Bit 5	R/W	FILL_LEVEL[0]	0
Bit 4	R	TRAIN	0
Bit 3	R/W	OUTLOCK	0
Bit 2	R/W	OUTDATA	0
Bit 1	R/W	INLOCK	1
Bit 0	R/W	INDATA	1

The CRU Clock Training Configuration register is provided at RCS_2488 read/write address 2.

INDATA:

The clock difference detector DATA TO LOCK transition configuration bit determines the number of times the clock difference detector must pass before the CRU control state machine transitions from the LOCKED TO REFERENCE state to the DATA IN RANGE state. When INDATA is a logic zero, the clock difference detector must pass once before the state transition can occur. When INDATA is a logic one, the clock difference detector must pass 39 consecutive times before the state transition can occur.

INLOCK:

The clock difference detector LOCKING TO DATA transition configuration bit determines the number of times the clock difference detector must pass before the CRU control state machine transitions from the DATA IN RANGE state to the LOCKED TO DATA state. When INLOCK is a logic zero, the clock difference detector must pass once before the state transition can occur. When INLOCK is a logic one, the clock difference detector must pass 39 consecutive times before the state transition can occur.

OUTDATA:

The clock difference detector DROPPING OUT OF LOCK transition configuration bit determines the number of times the clock difference detector must fail before the CRU control state machine transitions from the DATA IN RANGE state to the LOCKED TO REFERENCE state. When OUTDATA is a logic zero, the clock difference detector must fail once before the

state transition can take place. When OUTDATA is a logic one, the clock difference detector must fail 39 consecutive times before the state transition can occur.

OUTLOCK:

The clock difference detector DROPPING OUT OF DATA transition configuration bit determines the number of times the clock difference detector must pass before the CRU control state machine transitions from the LOCKED TO DATA state to the DATA IN RANGE state. When OUTLOCK is a logic zero, the clock difference detector must fail once before the state transition can occur. When OUTLOCK is a logic one, the clock difference detector must fail 39 consecutive times before the state transition can occur.

TRAIN:

The CRU reference training status indicates if the CRU is locking to the reference clock or the locking to the receive data as described in TBD. TRAIN is a logic one if the CRU is locking or locked to the reference clock. TRAIN is a logic zero if the CRU is locking or locked to the receive data. TRAIN is invalid if the CRU is not used.

FILL_LEVEL[3:0]:

The FIFO Fill level sets the amount of data that must be accumulated in the FIFO before valid data is output to the system. The level ensures that enough data is in the FIFO to prevent an underflow condition caused by jitter on the input clock. The default value is set to 48 or one half of the FIFO's total capacity of 96 words.

LOS_COUNT[3:0]:

The Loss of signal 1's/0's transition detector count. This field sets the value for the number of consecutive all-zeros or all-ones pattern that will force the CRU out of the LOCK TO DATA state. Each bit in the binary count represents 8 ones or zeros in the pattern. I.e. to set the consecutive all-ones or all-zeros pattern to 128 the LOS_COUNT should be set to "10000"b. The default value for this field is 128.

Register 0013H: Rx2488 Analog PRBS Control

Bit	Type	Function	Default
Bit 15	R	PRBS_ERR_CNT[7]	0
Bit 14	R	PRBS_ERR_CNT[6]	0
Bit 13	R	PRBS_ERR_CNT[5]	0
Bit 12	R	PRBS_ERR_CNT[4]	0
Bit 11	R	PRBS_ERR_CNT[3]	0
Bit 10	R	PRBS_ERR_CNT[2]	0
Bit 9	R	PRBS_ERR_CNT[1]	0
Bit 8	R	PRBS_ERR_CNT[0]	0
Bit 7	W	LATCH_ERR_CNT	X
Bit 6		UNUSED	X
Bit 5	R/W	INV_DATA	0
Bit 4	R/W	FIFO_CLOCK	0
Bit 3	R	SYNC_STAT	0
Bit 2	R/W	PRBS_FPATT	0
Bit 1	R/W	PRBS_ENABLE	0
Bit 0	R/W	RESYNC	0

The CRU Clock Training Configuration register is provided at RCS_2488 read/write address 3.

RESYNC:

Forces the monitor to re-initialize the PRBS sequence. When set high, the monitor's state machine will be forced in the Out-Of-Sync state and automatically tries to resynchronize to the incoming stream. This bit is cleared once the monitor enters the In-Sync state.

PRBS_ENABLE:

This bit enables the PRBS monitor of the RCS_2488. When low, the PRBS monitor is disabled. When high the PRBS monitor is enabled and will check the incoming data stream for errors.

PRBS_FPATT:

This bit determines whether the RCS_2488 is monitoring a PRBS data stream or a fixed pattern. When low, the data stream contains PRBS bytes, and when high the fixed pattern written into the PATTERN[15:0] Register is monitored.

SYNC_STAT:

The Monitor Synchronization Status bit reflects the state of the monitor's state machine. When SYNC_STAT is set low, the monitor has lost synchronization. When SYNC_STAT is high, the monitor is in synchronization.

FIFO_CLOCK:

The FIFO Clock source selection bit is used to select the source of the FIFO output. If FIFO_CLOCK is set to logic 1 the clock for CRU output clock is used as the reference. If FIFO_CLOCK is set to logic 0 than the FIFO clock is obtained from the CSU.

INV_DATA:

The Serial Data Inversion INV_DATA controls the polarity of the received data. When INV_DATA is set to '1' the polarity of the RXD+/- input pins invert. When INV_DATA is set to '0' the RXD+/- inputs operate normally.

LATCH_ERR_CNT:

The Latch Error Count bit loads the PRBS byte error count value. When a logic 1 is written to this bit the PRBS byte error count register is loaded into the LATCH_ERR_CNT[7:0] register and the PRBS byte error count is reset to zero. This bit is write only and is cleared immediately after the write is complete.

PRBS_ERR_CNT[7:0]:

The ERR_CNT[7:0] register, is the number of errors in the PRBS bytes detected during the monitoring. Errors are accumulated only when the monitor is in the synchronized state. Even if there is multiple errors within one PRBS byte, only one error is counted. The transfer of the error counter to this holding register is trigger by writing to the LATCH_ERR_CNT bit or by pulsing high the LCLK signal. This PRBS_ERR_CNT[7:0] is cleared after it is read. The actual PRBS error counter is cleared immediately after a logic 1 is written to the LATCH_ERR_CNT bit. The error counter will not wrap around after reaching FFh, it will saturate to this value.

Register 0014H: Rx2488 Analog Pattern Register

Bit	Type	Function	Default
Bit 15	R/W	FPATT[15]	0
Bit 14	R/W	FPATT[14]	0
Bit 13	R/W	FPATT[13]	0
Bit 12	R/W	FPATT[12]	0
Bit 11	R/W	FPATT[11]	0
Bit 10	R/W	FPATT[10]	0
Bit 9	R/W	FPATT[9]	0
Bit 8	R/W	FPATT[8]	0
Bit 7	R/W	FPATT[7]	0
Bit 6	R/W	FPATT[6]	0
Bit 5	R/W	FPATT[5]	0
Bit 4	R/W	FPATT[4]	0
Bit 3	R/W	FPATT[3]	0
Bit 2	R/W	FPATT[2]	0
Bit 1	R/W	FPATT[1]	0
Bit 0	R/W	FPATT[0]	0

The Pattern register is provided at RCS_2488 read/write address 4.

FPATT[15:0]:

The FPATT[15:0] provides the fixed pattern that will be monitored for when the PRBS_FPATT bit is set to a logic 1. If PRBS_FPATT is set to logic 0 this register is not used.

Register 0030H: SRLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	ROTATEEN	1
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	DISFRM4	0
Bit 8	R/W	DISFRM3	0
Bit 7	R/W	DISFRM2	0
Bit 6	R/W	DISFRM1	0
Bit 5	R/W	DISFRM	0
Bit 4	R/W	RCLK4EN	0
Bit 3	R/W	RCLK3EN	0
Bit 2	R/W	RCLK2EN	0
Bit 1	R/W	RCLK1EN	0
Bit 0		Unused	

The Clock Configuration Register is provided at SRLI r/w address 0030H.

RCLK1EN:

The receive clock enable (RCLK1EN) bit controls the gating of the RCLK1 output clock. When RCLK1EN is set to logic 1, the RCLK1 output clock operates normally. When RCLK1EN is set to logic 0, the RCLK1 output clock is held low.

RCLK2EN:

The receive clock enable (RCLK2EN) bit controls the gating of the RCLK2 output clock. When RCLK2EN is set to logic 1, the RCLK2 output clock operates normally. When RCLK2EN is set to logic 0, the RCLK2 output clock is held low.

RCLK3EN:

The receive clock enable (RCLK3EN) bit controls the gating of the RCLK3 output clock. When RCLK3EN is set to logic 1, the RCLK3 output clock operates normally. When RCLK3EN is set to logic 0, the RCLK3 output clock is held low.

RCLK4EN:

The receive clock enable (RCLK4EN) bit controls the gating of the RCLK4 output clock. When RCLK4EN is set to logic 1, the RCLK4 output clock operates normally. When RCLK4EN is set to logic 0, the RCLK4 output clock is held low.

DISFRM:

The disable framing (DISFRM) bit disables the framing algorithm and resets the bit alignment on the RD[15:0] input bus to none. When DISFRM is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM1:

The disable framing (DISFRM1) bit disables the framing algorithm and resets the bit alignment on the RD1[7:0] input bus to none. When DISFRM1 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM1 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM2:

The disable framing (DISFRM2) bit disables the framing algorithm and resets the bit alignment on the RD2[7:0] input bus to none. When DISFRM2 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM2 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM3:

The disable framing (DISFRM3) bit disables the framing algorithm and resets the bit alignment on the RD3[7:0] input bus to none. When DISFRM3 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM3 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM4:

The disable framing (DISFRM4) bit disables the framing algorithm and resets the bit alignment on the RD4[7:0] input bus to none. When DISFRM4 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM4 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

ROTATEEN:

The TSI rotate enable (ROTATEEN) bit controls the TSI rotation matrix. When ROTATEEN is set to logic 1, the TSI rotation matrix is active and the bytes on the RD[15:0] output bus are re ordered. When ROTATEEN is set to logic 0, the TSI rotation matrix is inactive.

Register 0031H: SRLI PGM Clock Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PGMRCLKSRC[1]	0
Bit 2	R/W	PGMRCLKSRC[0]	0
Bit 1	R/W	PGMRCLKSEL	0
Bit 0	R/W	PGMRCLKEN	0

The PGM Clock Configuration Register is provided at SRLI r/w address 0031H.

PGMRCLKEN:

The programmable receive clock enable (PGMRCLKEN) bit controls the gating of the PGMRCLK output clock. When PGMRCLKEN is set to logic one, the PGMRCLK output clock operates normally. When PGMRCLKEN is set to logic zero, the PGMRCLK output clock is held low.

PGMRCLKSEL

The programmable receive clock frequency selection (PGMRCLKSEL) bit selects the frequency of the PGMRCLK output clock. When PGMRCLKSEL is set high, PGMRCLK is a nominal 8 KHz clock. When PGMRCLKSEL is set to logic zero, PGMRCLK is a nominal 19.44 MHz clock.

PGMRCLKSRC[1:0]:

The programmable receive clock source (PGMRCLKSRC[1:0]) bits select the source of the PGMRCLK output clock when the S/UNI-2488 is in quad STS-12 (STM-4) mode. When the SP2488 is in STS-48 (STM-16) mode, RDCLK is the source of the PGMRCLK output clock.

PGMRCLKSRC[1:0]	Source
00	PICLK1
01	PICLK2
10	PICLK3
11	PICLK4

Register 0038H: STLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TDCLKOEN	0

TDCLKOEN:

The transmit clock enable (TDCLKOEN) bit controls the gating of the internal parallel transmit clock. When TDCLKOEN is set to logic 1, the TDCLKO output clock operates normally. When TDCLKOEN is set to logic 0, the TDCLKO output clock is held low. This register bit should be set to loic 1 for normal operation.

Register 0039H: STLI PGM Clock Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	PGMTCLKSEL	0
Bit 0	R/W	PGMTCLKEN	0

PGMTCLKEN:

The programmable transmit clock enable (PGMTCLKEN) bit controls the gating of the PGMTCLK output clock. When PGMTCLKEN is set to logic one, the PGMTCLK output clock operates normally. When PGMTCLKEN is set to logic zero, the PGMTCLK output clock is held low.

PGMTCLKSEL

The programmable transmit clock frequency selection (PGMTCLKSEL) bit selects the frequency of the PGMTCLK output clock. When PGMTCLKSEL is set high, PGMTCLK is a nominal 8 KHz clock. When PGMTCLKSEL is set to logic zero, PGMTCLK is a nominal
Register 0040H: RRMP Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R/W	LREIBLK	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	LBIPEACCBLK	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBIPEACCBLK	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	LRDI3	0
Bit 2	R/W	LAIS3	0
Bit 1	R/W	ALGO2	0
Bit 0	W	FOOF	X

FOOF:

The force out of frame (FOOF) bit forces out of frame condition. When a logic 1 is written to FOOF, the framer block is forced out of frame at the next frame boundary regardless of the framing pattern value. The OOF event initiates re framing in an upstream frame detector.

ALGO2:

The ALGO2 bit selects the framing pattern used to determine and maintain the frame alignment. When ALGO2 is set to logic 1, the framing pattern consist of the 8 bits of the first A1 framing bytes and the first 4 bits of the last A2 framing bytes (12 bits total). This algorithm examines only 12 framing bits; all other framing bits are ignored. When ALGO2 is set to logic 0, the framing patterns consist of 12 A1 framing bytes and 12 A2 framing bytes.

LAIS3:

The line alarm indication signal detection (LAIS3) bit selects the Line AIS detection algorithm. When LAIS3 is set to logic 1, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LAIS3 is set to logic 0, Line AIS is

declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

LRDI3:

The line remote defect indication detection (LRDI3) bit selects the Line RDI detection algorithm. When LRDI3 is set to logic 1, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LRDI3 is set to logic 0, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

SBIPEACCBLK:

The section BIP error accumulation block (SBIPEACCBLK) bit controls the accumulation of section BIP errors. When SBIPEACCBLK is set to logic 1, the section BIP accumulation represents BIP-8 block errors (a maximum of 1 error per frame). When SBIPEACCBLK is set to logic 0, the section BIP accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

LBIPEACCBLK:

The line BIP error accumulation block (LBIPEACCBLK) bit controls the accumulation of line BIP errors. When LBIPEACCBLK is set to logic 1, the line BIP accumulation represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEACCBLK is set to logic 0, the line BIP accumulation represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LREIBLK

The line REI block (LREIBLK) bit controls the extraction of line REI errors from the M1 byte. When LREIBLK is set to logic 1, the extracted line REI are interpreted as block BIP-24 errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the extracted line REI are interpreted as BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

BUSY:

The BUSY (BUSY) bit reports the status of the transfer of section BIP, line BIP and line REI error counters to the holding registers. BUSY is set to logic 1 upon writing to the holding register addresses or by a low to high transition on LCK. BUSY is set to logic 0, upon completion of the transfer. This bit should be polled to determine when new data is available in the holding registers.

Register 0041H: RRMP Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	APSBFV	X
Bit 4	R	LRDIV	X
Bit 3	R	LAISV	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit reflects the current status of the out of frame defect. The OOF defect is declared when four consecutive frames have one or more bit error in their framing pattern. The OOF defect is cleared when two error free framing pattern are found.

LOFV:

The LOFV bit reflects the current status of the loss of frame defect. The LOF defect is declared when an out of frame condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. The LOF defect is cleared when an in frame condition exists for a continuous period of 3 ms.

LOSV:

The LOSV bit reflects the current status of the loss of signal defect. The LOS defect is declared when 20 µs of consecutive all zeros pattern is detected. The LOS defect is cleared when two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern.

LAISV:

The LAISV bit reflects the current status of the line alarm indication signal defect. The AIS-L defect is declared when the 111 pattern is detected in bits 6,7 and 8 of the K2 byte for three or five consecutive frames. The AIS-L defect is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

LRDIV:

The LRDIV bit reflects the current status of the line remote defect indication signal defect. The RDI-L defect is declared when the 110 pattern is detected in bits 6, 7, and 8 of the k2 byte for three or five consecutive frames. The RDI-L defect is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

APSBFV:

The APSBF bit reflects the current status of the APS byte failure defect. The APS byte failure defect is declared when no three consecutive identical K1 bytes are received in the last twelve consecutive frames starting with the last frame containing a previously consistent byte. The APS byte failure defect is cleared when three consecutive identical K1 bytes are received.

Register 0042H: RRMP Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R/W	LREIEE	0
Bit 9	R/W	LBIPEE	0
Bit 8	R/W	SBIPEE	0
Bit 7	R/W	COSSME	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	APSBFE	0
Bit 4	R/W	LRDIE	0
Bit 3	R/W	LAISE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE, LOFE, LOSE, LAISE, LRDIE, APSBFE, COAPSE, COSSME, SBIPEE, LBIPEE, LREIEE:

The interrupt enable bits controls the activation of the interrupt (INTB) output. When the interrupt enable bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the interrupt enable bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0043H: RRMP Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R	LREIEI	X
Bit 9	R	LBIPEI	X
Bit 8	R	SBIPEI	X
Bit 7	R	COMMSI	X
Bit 6	R	COAPSI	X
Bit 5	R	APSBFI	X
Bit 4	R	LRDII	X
Bit 3	R	LAISI	X
Bit 2	R	LOSI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI:

The out of frame interrupt status (OOFI) bit is an event indicator. OOFI is set to logic 1 to indicate any change in the status of OOFV. The interrupt status bit is independent of the interrupt enable bit. OOFI is cleared to logic 0 when this register is read.

LOFI:

The loss of frame interrupt status (LOFI) bit is an event indicator. LOFI is set to logic 1 to indicate any change in the status of LOFV. The interrupt status bit is independent of the interrupt enable bit. LOFI is cleared to logic 0 when this register is read.

LOSI:

The loss of signal interrupt status (LOSI) bit is an event indicator. LOSI is set to logic 1 to indicate any change in the status of LOSV. The interrupt status bit is independent of the interrupt enable bit. LOSI is cleared to logic 0 when this register is read.

LAISI:

The line alarm indication signal interrupt status (LAISI) bit is an event indicator. LAISI is set to logic 1 to indicate any change in the status of LAISV. The interrupt status bit is independent of the interrupt enable bit. LAISI is cleared to logic 0 when this register is read.

LRDII:

The line remote defect indication interrupt status (LRDII) bit is an event indicator. LRDII is set to logic 1 to indicate any change in the status of LRDIV. The interrupt status bit is independent of the interrupt enable bit. LRDII is cleared to logic 0 when this register is read.

APSBFI:

The APS byte failure interrupt status (APSBFI) bit is an event indicator. APSBFI is set to logic 1 to indicate any change in the status of APSBFV. The interrupt status bit is independent of the interrupt enable bit. APSBFI is cleared to logic 0 when this register is read.

COAPSI:

The change of APS bytes interrupt status (COAPSI) bit is an event indicator. COAPSI is set to logic 1 to indicate a new APS bytes. The interrupt status bit is independent of the interrupt enable bit. COAPSI is cleared to logic 0 when this register is read.

COSSMI:

The change of SSM message interrupt status (COSSMI) bit is an event indicator. COSSMI is set to logic 1 to indicate a new SSM message. The interrupt status bit is independent of the interrupt enable bit. COSSMI is cleared to logic 0 when this register is read.

SBIPEI:

The section BIP error interrupt status (SBIPEI) bit is an event indicator. SBIPEI is set to logic 1 to indicate a section BIP error. The interrupt status bit is independent of the interrupt enable bit. SBIPEI is cleared to logic 0 when this register is read.

LBIPEI:

The line BIP error interrupt status (LBIPEI) bit is an event indicator. LBIPEI is set to logic 1 to indicate a line BIP error. The interrupt status bit is independent of the interrupt enable bit. LBIPEI is cleared to logic 0 when this register is read.

LREIEI:

The line REI error interrupt status (LREIEI) bit is an event indicator. LREIEI is set to logic 1 to indicate a line REI error. The interrupt status bit is independent of the interrupt enable bit. LREIEI is cleared to logic 0 when this register is read.

Register 0044H: RRMP Receive APS

Bit	Type	Function	Default
Bit 15	R	K1V[7]	X
Bit 14	R	K1V[6]	X
Bit 13	R	K1V[5]	X
Bit 12	R	K1V[4]	X
Bit 11	R	K1V[3]	X
Bit 10	R	K1V[2]	X
Bit 9	R	K1V[1]	X
Bit 8	R	K1V[0]	X
Bit 7	R	K2V[7]	X
Bit 6	R	K2V[6]	X
Bit 5	R	K2V[5]	X
Bit 4	R	K2V[4]	X
Bit 3	R	K2V[3]	X
Bit 2	R	K2V[2]	X
Bit 1	R	K2V[1]	X
Bit 0	R	K2V[0]	X

K1V[7:0]/K2V[7:0]:

The APS K1/K2 bytes value (K1V[7:0]/K2V[7:0]) bits represent the extracted K1/K2 APS bytes. K1V/K2V is updated when the same K1 and K2 bytes (forming a single entity) are received for three consecutive frames.

Register 0045H: RRMP Receive SSM

Bit	Type	Function	Default
Bit 15	R/W	BYTESSM	0
Bit 14	R/W	FLTRSSM	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	SSMV[7]	X
Bit 6	R	SSMV[6]	X
Bit 5	R	SSMV[5]	X
Bit 4	R	SSMV[4]	X
Bit 3	R	SSMV[3]	X
Bit 2	R	SSMV[2]	X
Bit 1	R	SSMV[1]	X
Bit 0	R	SSMV[0]	X

SSMV[7:0]:

The synchronization status message value (SSMV[7:0]) bits represent the extracted S1 nibble (or byte). When filtering is enabled via the FLTRSSM register bit, SSMV is updated when the same S1 nibble (or byte) is received for eight consecutive frames. When filtering is disable, SSMV is updated every frame.

FLTRSSM:

The filter synchronization status message (FLTRSSM) bit enables the filtering of the SSM nibble (or byte). When FLTRSSM is set to logic 1, the SSM value is updated when the same SSM is received for eight consecutive frames. When FLTRSSM is set to logic 0, the SSM value is updated every frame.

BYTESSM:

The byte synchronization status message (BYTESSM) bit extends the SSM from a nibble to a byte. When BYTESSM is set to logic 1, the SSM is a byte and bits 1 to 8 of the S1 byte are considered. When BYTESSM is set to logic 0, the SSM is a nibble and only bits 5 to 8 of the S1 byte are considered.

Register 0046H: RRMP AIS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4	R/W	K2AIS	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	RLOHAISEN	0
Bit 0	R/W	RSOHAISEN	0

RSOHAISEN:

The receive section overhead AIS enable (RSOHAISEN) bit enables AIS insertion on RTOH when carrying section overhead bytes. When RSOHAISEN is set to logic 1, all ones are forced on the section overhead bytes when a LOF or LOS condition exists. When RSOHAISEN is set to logic 0, no AIS are forced on the section overhead bytes regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLOHAISEN:

The receive line overhead AIS enable (RLOHAISEN) bit enables AIS insertion on RTOH, when carrying line overhead bytes. When RLOHAISEN is set to logic 1, all ones are forced on the line overhead bytes when a LOF or LOS condition exists. When RLOHAISEN is set to logic 0, no AIS are forced on the line overhead bytes regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLAISEN:

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the outgoing data stream. When RLAISEN is set to logic 1, line AIS is inserted in the outgoing data stream when a LOF or LOS condition exists. When RLAISEN is set to logic 0, no line AIS is inserted regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLAISINS:

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the receive SONET data stream. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed.

K2AIS:

The K2 line AIS (K2AIS) bit restricts line AIS to the K2 byte. When K2AIS is set to logic 1, line AIS is only inserted in bits 6, 7 and 8 of the K2 byte. When K2AIS is set to logic 0, line AIS is inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes).

Register 0047H: RRMP Section BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	SBIPE[15]	X
Bit 14	R	SBIPE[14]	X
Bit 13	R	SBIPE[13]	X
Bit 12	R	SBIPE[12]	X
Bit 11	R	SBIPE[11]	X
Bit 10	R	SBIPE[10]	X
Bit 9	R	SBIPE[9]	X
Bit 8	R	SBIPE[8]	X
Bit 7	R	SBIPE[7]	X
Bit 6	R	SBIPE[6]	X
Bit 5	R	SBIPE[5]	X
Bit 4	R	SBIPE[4]	X
Bit 3	R	SBIPE[3]	X
Bit 2	R	SBIPE[2]	X
Bit 1	R	SBIPE[1]	X
Bit 0	R	SBIPE[0]	X

SBIPE[15:0]:

The section BIP error (SBIPE[15:0]) bits represent the number of section BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI-2488 Identity, and Global Performance Monitor Update register.

Register 0048H: RRMP Line BIP Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LBIPE[15:0]	XXXX

Register 0049H: RRMP Line BIP Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LBIPE[23:16]	XX

LBIPE[23:0]:

The line BIP error (LBIPE[23:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI-2488 Identity, and Global Performance Monitor Update register.

Register 004AH: RRMP Line REI Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LREIE[15:0]	XXXX

Register 004BH: RRMP Line REI Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LREIE[23:16]	XX

LREIE[23:0]:

The line REI error (LREIE[23:0]) bits represent the number of line REI errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI-2488 Identity, and Global Performance Monitor Update register.

Register 0080H: TRMP Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	LREIBLK	0
Bit 10	R/W	LREIEN	1
Bit 9	R/W	APSEN	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	TLDEN	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	TSLDEN	1
Bit 3	R/W	TRACEEN	1
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

A1A2EN:

The A1A2 framing enable (A1A2EN) bit controls the insertion of the framing bytes in the data stream. When A1A2EN is set to logic 1, F6h and 28h are inserted in the A1 and A2 bytes according to the priority of Table 4. When A1A2EN is set to logic 0, the framing bytes are not inserted.

For normal operation, the A1A2EN bits in the TRMP Aux1 Configuration register, the TRMP Aux2 Configuration register and the TRMP Aux3 Configuration register must be set to the same value as the A1A2EN bit.

Z0DEF:

The Z0 definition (Z0DEF) bit defines the Z0 growth bytes. When Z0DEF is set to logic 1, the Z0 bytes are defined according to ITU. The Z0 bytes are located in STS-1/STM-0 #2 to #12. When Z0DEF is set to logic 0, the Z0 bytes are defined according to BELLCORE. The Z0 bytes are located in STS-1/STM-0 #2 to #48.

For normal operation, the Z0DEF bits in the TRMP Aux1 Configuration register, the TRMP Aux2 Configuration register and the TRMP Aux3 Configuration register must be set to the same value as the Z0DEF bit.

J0Z0INCEN:

The J0 and Z0 increment enable (J0Z0INCEN) bit controls the insertion of an incremental pattern in the section trace and Z0 growth bytes. When J0ZOINCEN is set to logic 1, the corresponding STS-1/STM-0 path # is inserted in the J0 and Z0 bytes according to the priority of Table 4. When J0Z0INCEN is set to logic 0, no incremental pattern is inserted.

For normal operation, the J0Z0INCEN bits in the TRMP Aux1 Configuration register, the TRMP Aux2 Configuration register and the TRMP Aux3 Configuration register must be set to the same value as the J0Z0INCEN bit.

TRACEEN:

The section trace enable (TRACEEN) bit controls the insertion of section trace in the data stream. When TRACEEN is set to logic 1, the section trace from the Section TTTP block is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 4. When TRACEEN is set to logic 0, the section trace from the J0[7:0] input port is not inserted.

TSLDEN:

The TSLD enable (TSLDEN) bit controls the insertion of section or line DCC in the data stream. When TSLDEN is set to logic 1, the S/UNI-2488 inserts all ones or all zeros as selected using the TSLD_VAL bit in the S/UNI-2488 Diagnostic register into the D1-D3 bytes or D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When TSLDEN is set to logic 0, the section or line DCC is not inserted.

TLDEN:

The TLD enable (TLDEN) bit controls the insertion of line DCC in the data stream. When TLDEN is set to logic 1, the S/UNI-2488 inserts all ones or all zeros as selected using the TLD_VAL bit in the S/UNI-2488 Diagnostic register into in the D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When TLDEN is set to logic 0, an all ones pattern is not inserted.

APSEN:

The APS enable (APSEN) bit controls the insertion of automatic protection switching in the data stream. When APSEN is set to logic 1, the APS bytes from the RRMP are inserted in the K1/K2 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When APSEN is set to logic 0, the APS bytes from the RRMP are not inserted.

LREIEN:

The line REI enable (LREIEN) bit controls the insertion of line remote error indication in the data stream. When LREIEN is set to logic 1, the line REI from the RRMP is inserted in the M1 byte of STS-1/STM-0 #3 according to the priority of Table 4. When LREIEN is set to logic 0, the line REI from the RRMP is not inserted.

LREIBLK:

The line REI block error (LREIBLK) bit controls the generation of line remote error indication. When LREIBLK is set to logic 1, the line REI inserted in the M1 byte represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the line REI inserted in the M1 byte represents BIP-8 errors (a maximum of 8 error per STS-1/STM-0 per frame).

Register 0081H: TRMP Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	NATIONALV	0
Bit 12	R/W	NATIONALEN	0
Bit 11		Unused	
Bit 10	R/W	E2REGEN	0
Bit 9	R/W	Z2REGEN	0
Bit 8	R/W	Z1REGEN	0
Bit 7	R/W	S1REGEN	0
Bit 6	R/W	D4D12REGEN	0
Bit 5	R/W	K1K2REGEN	0
Bit 4	R/W	D1D3REGEN	0
Bit 3	R/W	F1REGEN	0
Bit 2	R/W	E1REGEN	0
Bit 1	R/W	Z0REGEN	0
Bit 0	R/W	J0REGEN	0

J0REGEN:

The J0 register enable (J0REGEN) bit controls the insertion of section trace in the data stream. When J0REGEN is set to logic 1, the section trace from the TRMP Transmit J0 and Z0 register is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 4. When J0REGEN is set to logic 0, the section trace from the TRMP Transmit J0 and Z0 register is not inserted.

Z0REGEN:

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is inserted in the Z0 bytes according to the priority of Table 4. When Z0REGEN is set to logic 0, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRMP Configuration register bit defines the Z0 bytes.

E1REGEN:

The E1 register enable (E1REGEN) bit controls the insertion of section order wire in the data stream. When E1REGEN is set to logic 1, the section order wire from the TRMP Transmit E1 and F1 register is inserted in the E1 byte of STS-1/STM-0 #1 according to the priority of Table 4. When E1REGEN is set to logic 0, the section order wire from the TRMP Transmit E1 and F1 register is not inserted.

F1REGEN:

The F1 register enable (F1REGEN) bit controls the insertion of section user channel in the data stream. When F1REGEN is set to logic 1, the section user channel from the TRMP Transmit E1 and F1 register is inserted in the F1 byte of STS-1/STM-0 #1 according to the priority of Table 4. When F1REGEN is set to logic 0, the section user channel from the TRMP Transmit E1 and F1 register is not inserted.

D1D3REGEN:

The D1 to D3 register enable (D1D3REGEN) bit controls the insertion of section data communication channel in the data stream. When D1D3REGEN is set to logic 1, the section DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When D1D3REGEN is set to logic 0, the section DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

K1K2REGEN:

The K1K2 register enable (K1K2REGEN) bit controls the insertion of automatic protection switching in the data stream. When K1K2REGEN is set to logic 1, the APS bytes from the TRMP Transmit K1 and K2 register are inserted in the K1, K2 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When K1K2REGEN is set to logic 0, the APS bytes from the TRMP Transmit K1 and K2 register are not inserted.

D4D12REGEN:

The D4 to D12 register enable (D4D12REGEN) bit controls the insertion of line data communication channel in the data stream. When D4D12REGEN is set to logic 1, the line DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When D4D12REGEN is set to logic 0, the line DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

S1REGEN:

The S1 register enable (S1REGEN) bit controls the insertion of the synchronization status message in the data stream. When S1REGEN is set to logic 1, the SSM from the TRMP Transmit S1 and Z1 register is inserted in the S1 byte of STS-1/STM-0 #1 according to the priority of Table 4. When S1REGEN is set to logic 0, the SSM from the TRMP Transmit S1 and Z1 register is not inserted.

Z1REGEN:

The Z1 register enable (Z1REGEN) bit controls the insertion of Z1 growth bytes in the data stream. When Z1REGEN is set to logic 1, the Z1 byte from the TRMP Transmit S1 and Z1 register is inserted in the Z1 bytes according to the priority of Table 4. When Z1REGEN is set to logic 0, the Z1 byte from the TRMP Transmit S1 and Z1 register is not inserted.

Z2REGEN:

The Z2 register enable (Z2REGEN) bit controls the insertion of Z2 growth bytes in the data stream. When Z2REGEN is set to logic 1, the Z2 byte from the TRMP Transmit Z2 and E2 register is inserted in the Z2 bytes according to the priority of Table 4. When Z2REGEN is set to logic 0, the Z2 byte from the TRMP Transmit Z2 and E2 register is not inserted.

E2REGEN:

The E2 register enable (E2REGEN) bit controls the insertion of line order wire in the data stream. When E2REGEN is set to logic 1, the line order wire from the TRMP Transmit Z2 and E2 register is inserted in the E2 byte of STS-1/STM-0 #1 according to the priority of Table 4. When E2REGEN is set to logic 0, the line order wire from the TRMP Transmit Z2 and E2 register is not inserted.

NATIONALEN:

The national enable (NATIONALEN) bit controls the insertion of national bytes in the data stream. When NATIONALEN is set to logic 1, an all one or an all zero pattern is inserted in the national bytes according to the priority of Table 4. When NATIONALEN is set to logic 0, no pattern is inserted. The Z0DEF bit in the TRMP Configuration register defines the national bytes of ROW #1.

NATIONALV:

The national value (NATIONALV) bit controls the value inserted in the national bytes. When NATIONALV is set to logic 1, an all one pattern is inserted in the national bytes if enable via the NATIONALEN register bit. When NATIONALV is set to logic 0, an all zero pattern is inserted in the national bytes if enable via the NATIONALEN register bit.

UNUSEDEN:

The unused enable (UNUSEDEN) bit controls the insertion of unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the unused bytes according to the priority of Table 4. When UNUSEDEN is set to logic 0, no pattern is inserted.

UNUSEDV:

The unused value (UNUSEDV) bit controls the value inserted in the unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the unused bytes if enable via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the unused bytes if enable via the UNUSEDEN register bit.

Register 0082H: TRMP Error Insertion

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	LRDIINS	0
Bit 3	R/W	A1ERR	0
Bit 2	R/W	HMASKEN	1
Bit 1	R/W	B2MASKEN	1
Bit 0	R/W	B1MASKEN	1

B1MASKEN:

The B1 mask enable (B1MASKEN) bit selects the used of the B1 byte extracted from the TTOH port. When B1MASKEN is set to logic 1, the B1 byte extracted from the TTOH port is used as a mask to toggle bits in the calculated B1 byte (the B1 byte extracted from the TTOH port is xor with the calculated B1 byte). When B1MASKEN is set to logic 0, the B1 byte extracted from the TTOH port is inserted instead of the calculated B1 byte.

B2MASKEN:

The B2 mask enable (B2MASKEN) bit selects the used of the B2 bytes extracted from the TTOH port. When B2MASKEN is set to logic 1, the B2 bytes extracted from the TTOH port are used as a mask to toggle bits in the calculated B2 bytes (the B2 bytes extracted from the TTOH port are xor with the calculated B2 bytes). When B2MASKEN is set to logic 0, the B2 bytes extracted from the TTOH port are inserted instead of the calculated B2 bytes.

HMASKEN:

The H1/H2 mask enable (HMASKEN) bit selects the used of the H1/H2 bytes extracted from the TTOH port. When HMASKEN is set to logic 1, the H1/H2 bytes extracted from the TTOH port are used as a mask to toggle bits in the H1/H2 path payload pointer bytes (the H1/H2 bytes extracted from the TTOH port are xor with the path payload pointer bytes). When

HMASKEN is set to logic 0, the H1/H2 bytes extracted from the TTOH port are inserted instead of the path payload pointer bytes.

A1ERR:

The A1 error insertion (A1ERR) bit is used to introduce framing errors in the A1 bytes. When A1ERR is set to logic 1, 76h instead of F6h is inserted in all of the A1 bytes of the STS-12/STM-4 #1 according to the priority of Table 4. When A1ERR is set to logic 0, no framing errors are introduced.

LRDIINS:

The line RDI insertion (LRDIINS) bit is used to force a line remote defect indication in the data stream. When LRDIINS is set to logic 1, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1/STM-0 #1 to force a line RDI condition. When LRDIINS is set to logic 0, the line RDI condition is removed.

LAISINS:

The line AIS insertion (LAISINS) bit is used to force a line alarm indication signal in the data stream. When LAISINS is set to logic 1, all ones are inserted in the line overhead and in the payload (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When LAISINS is set to logic 0, the line AIS condition is removed. Line AIS is inserted/removed on frame boundary before scrambling.

Note, this bit must be set to the same value as the other LAISINS bits in the TRMP Aux2 Error Insertion, TRMP Aux3 Error Insertion and TRMP Aux4 Error Insertion registers.

LOSINS:

The LOS insertion (LOSINS) bit is used to force a loss of signal condition in the data stream. When LOSINS is set to logic 1, the data steam is set to all zero (after scrambling) to force a loss of signal condition. When LOSINS is set to logic 0, the loss of signal condition is removed.

Note, this bit must be set to the same value as the other LOSINS bits in the TRMP Aux2 Error Insertion, TRMP Aux3 Error Insertion and TRMP Aux4 Error Insertion registers.

Register 0083H: TRMP Transmit J0 and Z0

Bit	Type	Function	Default
Bit 15	R/W	J0V[7]	0
Bit 14	R/W	J0V[6]	0
Bit 13	R/W	J0V[5]	0
Bit 12	R/W	J0V[4]	0
Bit 11	R/W	J0V[3]	0
Bit 10	R/W	J0V[2]	0
Bit 9	R/W	J0V[1]	0
Bit 8	R/W	J0V[0]	0
Bit 7	R/W	Z0V[7]	0
Bit 6	R/W	Z0V[6]	0
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	0
Bit 2	R/W	Z0V[2]	0
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

Z0V[7:0]:

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted in the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN bit in the TRMP Register Insertion register. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

J0V[7:0]:

The J0 byte value (J0V[7:0]) bits hold the section trace to be inserted in the data stream. The J0V[7:0] value is inserted in the J0 byte of STS-1/STM-0 #1 if the insertion is enabled via the J0REGEN bit in the TRMP Register Insertion register.

Register 0084H: TRMP Transmit E1 and F1

Bit	Type	Function	Default
Bit 15	R/W	E1V[7]	0
Bit 14	R/W	E1V[6]	0
Bit 13	R/W	E1V[5]	0
Bit 12	R/W	E1V[4]	0
Bit 11	R/W	E1V[3]	0
Bit 10	R/W	E1V[2]	0
Bit 9	R/W	E1V[1]	0
Bit 8	R/W	E1V[0]	0
Bit 7	R/W	F1V[7]	0
Bit 6	R/W	F1V[6]	0
Bit 5	R/W	F1V[5]	0
Bit 4	R/W	F1V[4]	0
Bit 3	R/W	F1V[3]	0
Bit 2	R/W	F1V[2]	0
Bit 1	R/W	F1V[1]	0
Bit 0	R/W	F1V[0]	0

F1V[7:0]:

The F1 byte value (F1V[7:0]) bits hold the section user channel to be inserted in the data stream. The F1V[7:0] value is inserted in the F1 byte of STS-1/STM-0 #1 if the insertion is enabled via the F1REGEN bit in the TRMP Register Insertion register.

E1V[7:0]:

The E1 byte value (E1V[7:0]) bits hold the section order wire to be inserted in the data stream. The E1V[7:0] value is inserted in the E1 byte of STS-1/STM-0 #1 if the insertion is enabled via the E1REGEN bit in the TRMP Register Insertion register.

Register 0085H: TRMP Transmit D1D3 and D4D12

Bit	Type	Function	Default
Bit 15	R/W	D1D3V[7]	0
Bit 14	R/W	D1D3V[6]	0
Bit 13	R/W	D1D3V[5]	0
Bit 12	R/W	D1D3V[4]	0
Bit 11	R/W	D1D3V[3]	0
Bit 10	R/W	D1D3V[2]	0
Bit 9	R/W	D1D3V[1]	0
Bit 8	R/W	D1D3V[0]	0
Bit 7	R/W	D4D12V[7]	0
Bit 6	R/W	D4D12V[6]	0
Bit 5	R/W	D4D12V[5]	0
Bit 4	R/W	D4D12V[4]	0
Bit 3	R/W	D4D12V[3]	0
Bit 2	R/W	D4D12V[2]	0
Bit 1	R/W	D4D12V[1]	0
Bit 0	R/W	D4D12V[0]	0

D4D12V[7:0]:

The D4D12 byte value (D4D12V[7:0]) bits hold the line data communication channel to be inserted in the data stream. The D4D12V[7:0] value is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D4D12REGEN bit in the TRMP Register Insertion register.

D1D3V[7:0]:

The D1D3 byte value (D1D3V[7:0]) bits hold the section data communication channel to be inserted in the data stream. The D1D3V[7:0] value is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D1D3REGEN bit in the TRMP Register Insertion register.

Register 0086H: TRMP Transmit K1 and K2

Bit	Type	Function	Default
Bit 15	R/W	K1V[7]	0
Bit 14	R/W	K1V[6]	0
Bit 13	R/W	K1V[5]	0
Bit 12	R/W	K1V[4]	0
Bit 11	R/W	K1V[3]	0
Bit 10	R/W	K1V[2]	0
Bit 9	R/W	K1V[1]	0
Bit 8	R/W	K1V[0]	0
Bit 7	R/W	K2V[7]	0
Bit 6	R/W	K2V[6]	0
Bit 5	R/W	K2V[5]	0
Bit 4	R/W	K2V[4]	0
Bit 3	R/W	K2V[3]	0
Bit 2	R/W	K2V[2]	0
Bit 1	R/W	K2V[1]	0
Bit 0	R/W	K2V[0]	0

K1V[7:0], K2V[7:0]:

The K1, K2 bytes value (K1V[7:0], K2V[7:0]) bits hold the APS bytes to be inserted in the data stream. The K1V[7:0], K2V[7:0] values are inserted in the K1, K2 bytes of STS-1/STM-0 #1 if the insertion is enabled via the K1K2REGEN bit in the TRMP Register Insertion register.

Register 0087H: TRMP Transmit S1 and Z1

Bit	Type	Function	Default
Bit 15	R/W	S1V[7]	0
Bit 14	R/W	S1V[6]	0
Bit 13	R/W	S1V[5]	0
Bit 12	R/W	S1V[4]	0
Bit 11	R/W	S1V[3]	0
Bit 10	R/W	S1V[2]	0
Bit 9	R/W	S1V[1]	0
Bit 8	R/W	S1V[0]	0
Bit 7	R/W	Z1V[7]	0
Bit 6	R/W	Z1V[6]	0
Bit 5	R/W	Z1V[5]	0
Bit 4	R/W	Z1V[4]	0
Bit 3	R/W	Z1V[3]	0
Bit 2	R/W	Z1V[2]	0
Bit 1	R/W	Z1V[1]	0
Bit 0	R/W	Z1V[0]	0

Z1V[7:0]:

The Z1 byte value (Z1V[7:0]) bits hold the Z1 growth byte to be inserted in the data stream. The Z1V[7:0] value is inserted in the Z1 byte if the insertion is enabled via the Z1REGEN bit in the TRMP Register Insertion register.

S1V[7:0]:

The S1 byte value (S1V[7:0]) bits hold the synchronization status message to be inserted in the data stream. The S1V[7:0] value is inserted in the S1 byte of STS-1/STM-0 #1 if the insertion is enabled via the S1REGEN bit in the TRMP Register Insertion register.

Register 0088H: TRMP Transmit Z2 and E2

Bit	Type	Function	Default
Bit 15	R/W	Z2V[7]	0
Bit 14	R/W	Z2V[6]	0
Bit 13	R/W	Z2V[5]	0
Bit 12	R/W	Z2V[4]	0
Bit 11	R/W	Z2V[3]	0
Bit 10	R/W	Z2V[2]	0
Bit 9	R/W	Z2V[1]	0
Bit 8	R/W	Z2V[0]	0
Bit 7	R/W	E2V[7]	0
Bit 6	R/W	E2V[6]	0
Bit 5	R/W	E2V[5]	0
Bit 4	R/W	E2V[4]	0
Bit 3	R/W	E2V[3]	0
Bit 2	R/W	E2V[2]	0
Bit 1	R/W	E2V[1]	0
Bit 0	R/W	E2V[0]	0

E2V[7:0]:

The E2 byte value (E2[7:0]) bits hold the line order wire to be inserted in the data stream. The E2V[7:0] value is inserted in the E2 byte of STS-1/STM-0 #1 if the insertion is enabled via the E2REGEN bit in the TRMP Register Insertion register.

Z2V[7:0]:

The Z2 byte value (Z2V[7:0]) bits hold the Z2 growth byte to be inserted in the data stream. The Z2V[7:0] value is inserted in the Z2 byte if the insertion is enabled via the Z2REGEN bit in the TRMP Register Insertion register.

Register 0089H: TRMP Transmit H1 and H2 Mask

Bit	Type	Function	Default
Bit 15	R/W	H1MASK[7]	0
Bit 14	R/W	H1MASK[6]	0
Bit 13	R/W	H1MASK[5]	0
Bit 12	R/W	H1MASK[4]	0
Bit 11	R/W	H1MASK[3]	0
Bit 10	R/W	H1MASK[2]	0
Bit 9	R/W	H1MASK[1]	0
Bit 8	R/W	H1MASK[0]	0
Bit 7	R/W	H2MASK[7]	0
Bit 6	R/W	H2MASK[6]	0
Bit 5	R/W	H2MASK[5]	0
Bit 4	R/W	H2MASK[4]	0
Bit 3	R/W	H2MASK[3]	0
Bit 2	R/W	H2MASK[2]	0
Bit 1	R/W	H2MASK[1]	0
Bit 0	R/W	H2MASK[0]	0

H2MASK[7:0]:

The H2 mask (H2MASK[7:0]) bits hold the H2 path payload pointer errors to be inserted in the data stream. The H2MASK[7:0] is xored with the path payload pointer already in the data stream.

H1MASK[7:0]:

The H1 mask (H1MASK[7:0]) bits hold the H1 path payload pointer errors to be inserted in the data stream. The H1MASK[7:0] is xored with the path payload pointer already in the data stream.

Register 008A: TRMP Transmit B1 and B2 Mask

Bit	Type	Function	Default
Bit 15	R/W	B1MASK[7]	0
Bit 14	R/W	B1MASK[6]	0
Bit 13	R/W	B1MASK[5]	0
Bit 12	R/W	B1MASK[4]	0
Bit 11	R/W	B1MASK[3]	0
Bit 10	R/W	B1MASK[2]	0
Bit 9	R/W	B1MASK[1]	0
Bit 8	R/W	B1MASK[0]	0
Bit 7	R/W	B2MASK[7]	0
Bit 6	R/W	B2MASK[6]	0
Bit 5	R/W	B2MASK[5]	0
Bit 4	R/W	B2MASK[4]	0
Bit 3	R/W	B2MASK[3]	0
Bit 2	R/W	B2MASK[2]	0
Bit 1	R/W	B2MASK[1]	0
Bit 0	R/W	B2MASK[0]	0

B2MASK[7:0]:

The B2 mask (B2MASK[7:0]) bits hold the B2 BIP-8 errors to be inserted in the data stream. The B2MASK[7:0] is xored with the calculated B2 before insertion in the B2 byte.

B1MASK[7:0]:

The B1 mask (B1MASK[7:0]) bits hold the B1 BIP-8 errors to be inserted in the data stream. The B1MASK[7:0] is xored with the calculated B1 before insertion in the B1 byte.

Register 00A0H: TRMP Aux2 Configuration

Register 00C0H: TRMP Aux3 Configuration

Register 00E0H: TRMP Aux4 Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved TSLDEN	1
Bit 3	R/W	Reserved	1
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

All reserved bits in this register should be set to logic 0 for normal operation.

A1A2EN:

For normal operation, the A1A2EN should be set to the same value as the A1A2EN bit in the TRMP Configuration register.

Z0DEF:

For normal operation, the Z0DEF should be set to the same value as the Z0DEF bit in the TRMP Configuration register.

J0Z0INCEN:

For normal operation, the J0Z0INCEN should be set to the same value as the J0Z0INCEN bit in the TRMP Configuration register.

Register 00A2H: TRMP Aux2 Error Insertion

Register 00C2H: TRMP Aux3 Error Insertion

Register 00E2H: TRMP Aux4 Error Insertion

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

All reserved bits in this register should be set to logic 0 for normal operation.

LAISINS:

For normal operation, the LAISINS should be set to the same value as the LAISINS bit in the TRMP Error Insertion register.

LOSINS:

For normal operation, the LOSINS should be set to the same value as the LOSINS bit in the TRMP Error Insertion register.

Register 0110H: SBER Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	SFBERTEN	0
Bit 4	R/W	SFSMODE	0
Bit 3	R/W	SFCMODE	0
Bit 2	R/W	SDBERTEN	0
Bit 1	R/W	SDSMODE	0
Bit 0	R/W	SDCMODE	0

SDCMODE:

The SDCMODE alarm bit selects the Signal Degrade BERM window size to use for clearing alarms. When SDCMODE is a logic 0 the SD BERM will clear an alarm using the same window size used for declaration. When SDCMODE is a logic 1 the SD BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SD BERM Accumulation Period register.

SDSMODE:

The SDSMODE bit selects the Signal Degrade BERM saturation mode. When SDSMODE is a logic 0 the SD BERM will saturate the BIP count on a per frame basis using the SBER SD Saturation Threshold register value. When SDSMODE is a logic 1 the SD BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SDBERTEN:

The SDBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Degrade BERM. When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SD BERM configuration registers should be set up before the monitoring is enabled.

SFCMODE:

The SFCMODE alarm bit selects the Signal Failure BERM window size to use for clearing alarms. When SFCMODE is a logic 0 the SF BERM will clear an alarm using the same window size used for declaration. When SFCMODE is a logic 1 the SF BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SF BERM Accumulation Period register.

SFSMODE:

The SFSMODE bit selects the Signal Failure BERM saturation mode. When SFSMODE is a logic 0 the SF BERM will saturate the BIP count on a per frame basis using the SBER SF Saturation Threshold register value. When SFSMODE is a logic 1 the SF BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure BERM. When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SF BERM configuration registers should be set up before the monitoring is enabled.

Register 0111H: SBER Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R	SFBERV	X
Bit 0	R	SDBERV	X

SDBERV:

The SDBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SDBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SDBERV is a logic zero) when the clearing threshold has been reached.

SFBERV:

The SFBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SFBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SFBERV is a logic zero) when the clearing threshold has been reached.

Register 0112H: SBER Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	SFBERE	0
Bit 0	R/W	SDBERE	0

SDBERE:

The SDBERE bit is the interrupt enable for the SDBER alarm. When SDBERE set to logic 1, the pending interrupt in the SBER Interrupt Status register, SDBERI, will assert the interrupt (INTB) output. When SDBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

SFBERE:

The SFBERE bit is the interrupt enable for the SFBER alarm. When SFBERE set to logic 1, the pending interrupt in the SBER Interrupt Status Register, SFBERI, will assert the interrupt (INTB) output. When SFBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Register 0113H: SBER Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R	SFBERI	X
Bit 0	R	SDBERI	X

SDBERI:

The SDBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SDBERV. This interrupt status bit is independent of the SDBERE interrupt enable bits. The SDBERI bit is cleared to logic 0 when the SBER Interrupt Status register is read.

SFBERI:

The SFBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SFBERV. This interrupt status bit is independent of the SFBERE interrupt enable bits. The SFBERI bit is cleared to logic 0 when the SBER Interrupt Status register is read.

Register 0114H: SBER SF BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[15:0]	0000

Register 0115H: SBER SF BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[31:16]	0000

SFSAP[31:0]:

The SFSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for the recommended settings..

Register 0116H: SBER SF BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[15:0]	0000

Register 0117H: SBER SF BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[31:16]	0000

SFSATH[31:0]:

The SFSTH[31:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFFFF disables the saturation functionality. Refer to the Operations section for the recommended settings..

Register 0118H: SBER SF BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[15:0]	0000

Register 0119H: SBER SF BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[31:16]	0000

SFDECTH[31:0]:

The SFDECTH[31:0] register represent the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operations section for the recommended settings..

Register 011AH: SBER SF BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[15:0]	0000

Register 011BH: SBER SF BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[31:16]	0000

SFCLRTH[31:0]:

The SFCLRTH[31:0] register represent the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operations section for the recommended settings..

Register 011CH: SBER SD BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[15:0]	0000

Register 011DH: SBER SD BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[31:16]	0000

SDSAP[31:0]:

The SDSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for the recommended settings..

Register 011EH: SBER SD BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSTH[15:0]	0000

Register 011FH: SBER SD BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSTH[31:16]	0000

SDSTH[31:0]:

The SDSTH[31:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFFFF disables the saturation functionality. Refer to the Operations section for the recommended settings..

Register 0120H: SBER SD BERM Declaration Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[15:0]	0000

Register 0121H: SBER SD BERM Declaration Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[31:16]	0000

SDDECTH[31:0]:

The SDDECTH[31:0] register represent the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operations section for the recommended settings..

Register 0122H: SBER SD BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[15:0]	0000

Register 0123H: SBER SD BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[31:16]	0000

SDCLRTH[31:0]:

The SDCLRTH[31:0] register represent the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operations section for the recommended settings.

Register 0130H: RTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	SECTION[3]	0
Bit 2	R/W	SECTION[2]	0
Bit 1	R/W	SECTION[1]	0
Bit 0	R/W	SECTION[0]	0

SECTION[3:0]:

The STS-1/STM-0 section (SECTION[3:0]) bits select which STS-1/STM-0 section is accessed by the current indirect transfer. This register should only be set to 0001 since only the STS-1/STM-0 #1 section byte is valid.

IADDR[7:0]:

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB:

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY:

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0131H: RTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 0132H: RTTP SECTION Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserve	X
Bit 9	R	Reserve	X
Bit 8	R	Reserve	X
Bit 7	R	Reserve	X
Bit 6	R	Reserve	X
Bit 5	R	Reserve	X
Bit 4	R	Reserve	X
Bit 3	R	Reserve	X
Bit 2	R	Reserve	X
Bit 1	R	Reserve	X
Bit 0	R	TIUV[1]	X

TIUV[1]:

The trace identifier unstable status (TIUV[1]) bit indicates the current status of the TIU defect.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 tail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous tail trace byte. BYTE_TIUV is set to logic 0 when the same tail trace byte is received for 48 consecutive frames.

Register 0133H: RTTP SECTION Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TIUE[1]	0

TIUE[1]:

The trace identifier unstable interrupt enable (TIUE[1]) bit controls the activation of the interrupt (INTB) output. When the bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0134H: RTTP SECTION Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserve	X
Bit 9	R	Reserve	X
Bit 8	R	Reserve	X
Bit 7	R	Reserve	X
Bit 6	R	Reserve	X
Bit 5	R	Reserve	X
Bit 4	R	Reserve	X
Bit 3	R	Reserve	X
Bit 2	R	Reserve	X
Bit 1	R	Reserve	X
Bit 0	R	TIUI[1]	X

TIUI[1]:

The trace identifier unstable interrupt status (TIUI[1]) bit is an event indicator. TIUI[1] is set to logic 1 to indicate any changes in the status of TIUV[1] (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit. TIUI[1] is cleared to logic 0 when this register is read.

Register 0135H: RTTP SECTION Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIMV[1]	X

TIMV[1]:

The trace identifier mismatch status (TIMV[1]) bit indicates the current status of the TIM defect.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 0136H: RTTP SECTION Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserve	0
Bit 10	R/W	Reserve	0
Bit 9	R/W	Reserve	0
Bit 8	R/W	Reserve	0
Bit 7	R/W	Reserve	0
Bit 6	R/W	Reserve	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserve	0
Bit 3	R/W	Reserve	0
Bit 2	R/W	Reserve	0
Bit 1	R/W	Reserve	0
Bit 0	R/W	TIME[1]	0

TIME[1]:

The trace identifier mismatch interrupt enable (TIME[1]) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0137H: RTTP SECTION Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserve	X
Bit 9	R	Reserve	X
Bit 8	R	Reserve	X
Bit 7	R	Reserve	X
Bit 6	R	Reserve	X
Bit 5	R	Reserve	X
Bit 4	R	Reserve	X
Bit 3	R	Reserve	X
Bit 2	R	Reserve	X
Bit 1	R	Reserve	X
Bit 0	R	TIMI[1]	X

TIMI[1]:

The trace identifier mismatch interrupt status (TIMI[1]) bit is an event indicator. TIMI[1] is set to logic 1 to indicate any changes in the status of TIMV[1] (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit. TIMI[1] is cleared to logic 0 when this register is read.

Indirect Register 00H: RTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]:

The tail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the tail trace message.

ALGO[1:0]	Tail trace algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the tail trace algorithms are disable. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16:

The message length (LENGTH16) bit selects the length of the tail trace message use by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

NOSYNC:

The synchronization disable (NOSYNC) bit disables the synchronization of the tail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the tail trace message. The bytes of the tail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the tail trace message. When LENGTH16 is set to logic 1, the tail trace message is synchronize on the MSB of the tail trace message. The byte with its MSB set high is placed in the first byte location of the captured page. When LENGTH16 is set to logic 0, the tail trace message is synchronize on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the tail trace message. The byte following the CR/LF bytes is placed in the first byte location of the captured page.

PER5:

The message persistency (PER5) bit selects the number of multi-frames a tail trace message must be received in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same tail trace message must be receive for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same tail trace message must be received for 3 consecutive multi frame to be declared persistent.

ZEROEN:

The all zero message enable (ZEROEN) bit selects if the all zero message are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

Indirect Register 40H to 7FH: RTTP SECTION Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

The RTTP SECTION Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]:

The captured tail trace message (CTRACE[7:0]) bits contain the currently received tail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronize. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP SECTION Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

The RTTP SECTION Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]:

The accepted tail trace message (ATRACE[7:0]) bits contain the persistent tail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same tail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same tail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same tail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP SECTION Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The RTTP SECTION Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]:

The expected tail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validated the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 0138H: TTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	SECTION[3]	0
Bit 2	R/W	SECTION[2]	0
Bit 1	R/W	SECTION[1]	0
Bit 0	R/W	SECTION[0]	0

SECTION[3:0]:

The STS-1/STM-0 section (SECTION[3:0]) bits select which STS-1/STM-0 is accessed by the current indirect transfer. SECTION[3:0] should be set to 0001.

IADDR[6:0]:

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB:

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY:

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0139H: TTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0138H: TTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16:

The message length (LENGTH16) bit selects the length of the tail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

BYTEEN:

The single byte message enable (BYTEEN) bit enables the single byte tail trace message. When BYTEEN is set to logic 1, the length of the tail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the tail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN:

The all zero message enable (ZEROEN) bit enables the transmission of an all zero tail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero tail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP SECTION Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]:

The tail trace message (TRACE[7:0]) bits contain the tail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Register 0200H: RHPP STS-1/STM-0 #1 through #12 Indirect Address
Register 0280H: RHPP STS-1/STM-0 #13 through #24 Indirect Address
Register 0300H: RHPP STS-1/STM-0 #25 through #36 Indirect Address
Register 0380H: RHPP STS-1/STM-0 #37 through #48 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]:

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001	Path #(1, 13, 25 or 37)
0010	Path #(2, 14, 26 or 38)
0011	Path #(3, 15, 27 or 39)
0100	Path #(4, 16, 28 or 40)
0101	Path #(5, 17, 29 or 41)
0110	Path #(6, 18, 30 or 42)
0111	Path #(7, 19, 31 or 43)
1000	Path #(8, 20, 32 or 44)
1001	Path #(9, 21, 33 or 45)
1010	Path #(10, 22, 34 or 46)

1011	Path #(11, 23, 35 or47)
1100	Path #(12, 24, 36 or 48)
1101-1111	Invalid path

IADDR[2:0]:

The address location (IADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address **IADDR[2:0]**	**Indirect Data**
000	Pointer Interpreter Configuration
001	Error Monitor Configuration
010	Pointer Value and ERDI
011	Captured and Accepted PSL
100	Expected PSL and PDI
101	GPO and status
101 to 111	Unused

RWB:

The active high read and active low write (RWB) bit selects if the current access to a internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY:

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0201H: RHPP STS-1/STM-0 #1 through #12 Indirect Data
Register 0281H: RHPP STS-1/STM-0 #13 through #24 Indirect Data
Register 0301H: RHPP STS-1/STM-0 #25 through #36 Indirect Data
Register 0381H: RHPP STS-1/STM-0 #37 through #48 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 0208H, 0210H, 0218H, 0220H, 0228H, 0230H, 0238H, 0240H, 0248H, 0250H, 0258H, 0260H
Register 0288H, 0290H, 0298H, 02A0H, 02A8H, 02B0H, 02B8H, 02C0H, 02C8H, 02D0H, 02D8H, 02E0H
Register 0308H, 0310H, 0318H, 0320H, 0328H, 0330H, 0338H, 0340H, 0348H, 0350H, 0358H, 0360H
Register 0388H, 0390H, 0398H, 03A0H, 03A8H, 03B0H, 03B8H, 03C0H, 03C8H, 03D0H, 03D8H, 03E0H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	
Bit 0		Unused	

PLOPV:

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

This bit is only valid for RHPP STS-1/STM0 #1.

PAISV:

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

This bit is only valid for RHPP STS-1/STM0 #1.

PLOPCV:

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

This bit is only valid for RHPP STS-1/STM0 #2-48.

PAISCV:

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the LOPC_state.

This bit is only valid for RHPP STS-1/STM0 #2-48.

Register 0209H, 0211H, 0219H, 0221H, 0229H, 0231H, 0239H, 0241H, 0249H, 0251H, 0259H, 0261H
Register 0289H, 0291H, 0299H, 02A1H, 02A9H, 02B1H, 02B9H, 02C1H, 02C9H, 02D1H, 02D9H, 02E1H
Register 0309H, 0311H, 0319H, 0321H, 0329H, 0331H, 0339H, 0341H, 0349H, 0351H, 0359H, 0361H
Register 0389H, 0391H, 0399H, 03A1H, 03A9H, 03B1H, 03B9H, 03C1H, 03C9H, 03D1H, 03D9H, 03E1H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Pointer Interpreter Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	
Bit 0	R/W	PTRJEE	0

PTRJEE:

The pointer justification event interrupt enable (PTRJEE) bit control the activation of the interrupt (INTB) output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt (INTB) output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #1.

PLOPE:

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt (INTB) output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt (INTB) output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #1.

PAISE:

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt (INTB) output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt (INTB) output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #1.

PLOPCE:

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt (INTB) output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt (INTB) output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #2-48.

PAISCE:

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt (INTB) output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt (INTB) output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #2-48.

Register 020AH, 0212H, 021AH, 0222H, 022AH, 0232H, 023AH, 0242H, 024AH, 0252H, 025AH, 0262H
Register 028AH, 0292H, 029AH, 02A2H, 02AAH, 02B2H, 02BAH, 02C2H, 02CAH, 02D2H, 02DAH, 02E2H
Register 030AH, 0312H, 031AH, 0322H, 032AH, 0332H, 033AH, 0342H, 034AH, 0352H, 035AH, 0362H
Register 038AH, 0392H, 039AH, 03A2H, 03AAH, 03B2H, 03BAH, 03C2H, 03CAH, 03D2H, 03DAH, 03E2H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Pointer Interpreter Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

NJEI:

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared to logic 0 when this register is read.

This bit is only valid for RHPP STS-1/STM0 #1.

PJEI:

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared to logic 0 when this register is read.

This bit is only valid for RHPP STS-1/STM0 #1.

PLOPI:

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read.

This bit is only valid for RHPP STS-1/STM0 #1.

PAISI:

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared to logic 0 when this register is read.

This bit is only valid for RHPP STS-1/STM0 #1.

PLOPCI:

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. PLOPCI is cleared to logic 0 when this register is read.

This bit is only valid for RHPP STS-1/STM0 #2-48.

PAISCI:

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. PAISCI is cleared to logic 0 when this register is read.

This bit is only valid for RHPP STS-1/STM0 #2-48.

Register 020B: RHPP STS-1/STM-0 #1 Error Monitor Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0		Unused	

PPLUV:

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously received PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV:

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 1, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to Table 1, the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 1, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 1, the expected PSL.

PUNEQV:

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect. PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 1, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). An PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 1, for 3 or 5 consecutive frames.

PPDIV:

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a PDI that does not match, according to Table 1, the expected PDI for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is a PDI that matches, according to Table 1, the expected PDI for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a PDI that does not match, according to Table 1, the expected PDI. PPDI is set to logic 0 when the accepted PSL is a PDI that matches, according to Table 1, the expected PDI.

PRDIV:

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV:

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

Register 020C: RHPP STS-1/STM-0 #1 Error Monitor Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

COPSLE:

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt (INTB) output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt (INTB) output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt (INTB) output.

PPLUE:

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt (INTB) output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt (INTB) output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt (INTB) output.

PPLME:

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt (INTB) output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt (INTB) output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt (INTB) output.

PUNEQE:

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt (INTB) output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt (INTB) output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt (INTB) output.

PPDIE:

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt (INTB) output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt (INTB) output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt (INTB) output.

PRDIE:

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt (INTB) output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt (INTB) output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt (INTB) output.

PERDIE:

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt (INTB) output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt (INTB) output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt (INTB) output.

COPERDIE:

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt (INTB) output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt (INTB) output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt (INTB) output.

PBIPEE:

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt (INTB) output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt (INTB) output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt (INTB) output.

PREIEE:

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt (INTB) output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt (INTB) output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt (INTB) output.

Register 020D: RHPP STS-1/STM-0 #1 Error Monitor Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

COPSLI:

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. COPSLI is cleared to logic 0 when this register is read. ALGO2 register bit has no effect on COPSLI.

PPLUI:

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. PPLUI is cleared to logic 0 when this register is read.

PPLMI:

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. PPLMI is cleared to logic 0 when this register is read.

PUNEQI:

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. PUNEQI is cleared to logic 0 when this register is read.

PPDII:

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PPDII is cleared to logic 0 when this register is read.

PRDII:

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PRDII is cleared to logic 0 when this register is read.

PERDII:

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PERDII is cleared to logic 0 when this register is read.

COPERDII:

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. COPERDII is cleared to logic 0 when this register is read.

PBIPEI:

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. PBIPEI is cleared to logic 0 when this register is read.

PREIEI:

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. PREIEI is cleared to logic 0 when this register is read.

Register 020E: RHPP STS-1/STM-0 #1 Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

PBIPE[15:0]:

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to this register or the SUNI-2488 Identity, and Global Performance Monitor Update register.

Register 020F: RHPP STS-1/STM-0 #1 Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

PREIE[15:0]:

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to this register or the SUNI-2488 Identity, and Global Performance Monitor Update register.

Indirect Register 00H: RHPP Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3EN	0
Bit 1	R/W	SSEN	0
Bit 0	R/W	PTRCDIS	0

PTRCDIS:

The concatenation pointer processing disable (PTRCDIS) bit disables the path concatenation pointer interpreter state machine. When PTRCDIS is set to logic 1, the path concatenation pointer interpreter state-machine is disabled and excluded from the LOPC-P, AISC-P and ALLAISC-P defect declaration. When PTRCDIS is set to logic 0, the path concatenation pointer interpreter state-machine is enabled and included in the LOPC-P, AISC-P and ALLAISC-P defect declaration.

This bit should be set to logic 1 for RHPP STS-1/STM0 #1 and logic 0 for all other RHPP STS-1/STM0 #N.

SSEN:

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3EN:

The “justification more than 3 frames ago enable” (JUST3EN) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart

to be considered valid. When JUST3EN is set to logic 1, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3EN is set to logic 0, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

This bit is only valid for RHPP STS-1/STM0 #1.

RELAYPAIS:

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

This bit is only valid for RHPP STS-1/STM0 #1.

INVCNT:

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 X NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 X NEW_POINT indications.

This bit is only valid for RHPP STS-1/STM0 #1.

NDFCNT:

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + ss. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + ss + offset value in the range 0 to 782 (764 in TU-3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

This bit is only valid for RHPP STS-1/STM0 #1.

Indirect Register 01H: RHPP Error Monitor Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R/W	Reserved	0
Bit 11	R/W	B3EONRPOH	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLK	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	PBIPBLKACC	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

ALGO2:

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the BELLCORE compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions.

This bit is only valid for RHPP STS-1/STM0 #1.

PSL5:

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

This bit is only valid for RHPP STS-1/STM0 #1.

PLMEND:

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

This bit is only valid for RHPP STS-1/STM0 #1.

PRDI10:

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

This bit is only valid for RHPP STS-1/STM0 #1.

PBIPBLKACC:

The path block BIP-8 errors accumulation (PBIPBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

This bit is only valid for RHPP STS-1/STM0 #1.

B3EBLK:

The serial path block BIP-8 errors (B3EBLK) bit controls the indication of path BIP-8 errors on the B3E serial output. When B3EBLK is set to logic 1, B3E outputs block BIP-8 errors (a maximum of 1 error per frame). When B3EBLK is set to logic 0, B3E outputs BIP-8 errors (a maximum of 8 errors per frame).

This bit is only valid for RHPP STS-1/STM0 #1.

PREIBLK:

The path block REI errors (PREIBLK) bit controls the extraction of path REI errors from the path status (G1) byte. When PREIBLK is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

This bit is only valid for RHPP STS-1/STM0 #1.

IBER

The inband error reporting (IBER) bit controls the inband regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

This bit is only valid for RHPP STS-1/STM0 #1. When operating as the protect mate, this bit should be set to logic 1.

IPREIBLK

The inband path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

This bit is only valid for RHPP STS-1/STM0 #1.

B3EONRPOH

The B3E On RPOH bit controls whether the normal B3 output on RPOH should be replaced by the BIP-8 Error byte. When set to logic zero, B3 is output normally. When set to logic one, B3 in replaced by the BIP-8 error code.

This bit is only valid for RHPP STS-1/STM0 #1.

Indirect Register 02H: RHPP Pointer value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12		Unused	
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

PTRV[9:0]:

The path pointer value (PTRV[9:0]) bits represent the current STS (AU or TU3) pointer being process by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]:

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]:

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

These bits are only valid for RHPP STS-1/STM0 #1.

Indirect Register 03H: RHPP captured and accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

This register is only used by the STS-1/STM-0 #1 slice. For all other slices, this register is invalid.

APSLV[7:0]:

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit). ALGO2 register bit has no effect on APSLV[7:0]

CPSLV[7:0]:

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 04H: RHPP Expected PSL and PDI

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This register is only used by the STS-1/STM-0 #1 slice. For all other slides, this register is invalid.

EPSL[7:0]:

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 1.

PDI[4:0], PDIRANGE:

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication according to Table 2. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 1.

Indirect Register 05H: RHPP GPO and other status

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R	NDF	0
Bit 7	R	ILLPTR	0
Bit 6	R	INVNDF	0
Bit 5	R	DISCOPA	0
Bit 4	R	CONCAT	0
Bit 3	R	ILLJREQ	0
Bit 2	R	NEWPTR	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

NEWPTR:

The new pointer (NEWPTR) signal is set high when an incoming pointer satisfying the new_point indication is received.

This bit is only valid for RHPP STS-1/STM0 #1.

ILLJREQ:

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

This bit is only valid for RHPP STS-1/STM0 #1.

CONCAT:

The CONCAT bit is set high if the H1, H2 pointer byte received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA:

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

This bit is only valid for RHPP STS-1/STM0 #1.

INVNDF:

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

This bit is only valid for RHPP STS-1/STM0 #1.

ILLPTR:

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 782 . Pointer justification requests (inc_req, dec_req) and AIS indications (AIS_ind) are not considered illegal.

This bit is only valid for RHPP STS-1/STM0 #1.

NDF:

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating an pointer adjustment (NDF_enabled indication).

This bit is only valid for RHPP STS-1/STM0 #1.

Register 0400H: THPP STS-1/STM-0 #1 through #12 Indirect Address Register 0480H: THPP STS-1/STM-0 #13 through #24 Indirect Address Register 0500H: THPP STS-1/STM-0 #25 through #36 Indirect Address Register 0580H: THPP STS-1/STM-0 #37 through #48 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	IADDR[3]	0
Bit 7	R/W	IADDR[2]	0
Bit 6	R/W	IADDR[1]	0
Bit 5	R/W	IADDR[0]	0
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]:

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001	Path #(1, 13, 25 or 37)
0010	Path #(2, 14, 26 or 38)
0011	Path #(3, 15, 27 or 39)
0100	Path #(4, 16, 28 or 40)
0101	Path #(5, 17, 29 or 41)
0110	Path #(6, 18, 30 or 42)
0111	Path #(7, 19, 31 or 43)
1000	Path #(8, 20, 32 or 44)
1001	Path #(9, 21, 33 or 45)
1010	Path #(10, 22, 34 or 46)

1011	Path #(11, 23, 35 or47)
1100	Path #(12, 24, 36 or 48)
1101-1111	Invalid path

IADDR[3:0]:

The address location (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[3:0]	Indirect Register
0000	THPP Control Register
0001	THPP Source and Pointer Control
0010	THPP Current Pointer
0011	THPP Arbitrary Pointer
0100	THPP B3 Mask and Fixed stuff byte
0101	THPP Transmit C2 and J1
0110	THPP Transmit H4 Mask and G1
0111	THPP Transmit F2 and Z3
1000	THPP Transmit Z4 and Z5
1001 to 1111	Unused

RWB:

The active high read and active low write (RWB) bit selects if the current access to a internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY:

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0401H: THPP STS-1/STM-0 #1 through #12 Indirect Data
Register 0481H: THPP STS-1/STM-0 #13 through #24 Indirect Data
Register 0501H: THPP STS-1/STM-0 #25 through #36 Indirect Data
Register 0581H: THPP STS-1/STM-0 #37 through #48 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 0402: THPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	FIXPTR	0
Bit 11	R/W	ENESB	0
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Indirect Register 00H: THPP Control Register

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PAIS	0

PAIS:

The PAIS bit controls the insertion of the path alarm indication signal. This register bit value is logically ORed with the results form the SARC block. When a logic 1 is written to this bit position, the complete SPE/VC-x, and the the pointer bytes (H1, H2) and stuffing opportunity bytes (H3) are overwritten with the all ones pattern. When a logic 0 is written to this bit position, the pointer bytes and the SPE/VC-n are processed normally. Upon de-activation of path AIS, a new data flag accompanies the first valid pointer.

This bit should be consistent for all THPP STS-1/STM0 #N.

PREIEBLK:

The path REI block error (PREIEBLK) bit controls the extraction of path REI errors in the PREI monitoring block of the STS/AU pointer. When PREIEBLK is set to logic 1, the path REI extracted represents BIP-8 block errors (a maximum of 1 error per frame). When PREIEBLK is set to logic 0, the path REI extracted represents BIP-8 errors (a maximum of 8 errors per frame).

This bit is only valid for THPP STS-1/STM0 #1.

FSBEN:

When the FSBEN register bit is logic one, THPP overwrites the fixed stuff byte .

This bit should be consistent for all THPP STS-1/STM0 #1 through #48.

Indirect Register 01H: THPP Source and Pointer Control Register

Bit	Type	Function	Default
Bit 15			0
Bit 14		Unused	
Bit 13	R/W	H4MASK	0
Bit 12	R/W	B3MASK	0
Bit 11	R/W	ENG1REC	0
Bit 10	R/W	ENH4MASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCREI	0
Bit 3	R/W	SRCRDI	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

IBER:

When the IBER register bit is set to logic one, the G1 byte is generated by the SIRP block. The THPP overwrites the LSB of the pass-through G1 with a zero logic value. When IBER is set to logic zero, the G1 byte can be modified by one of the PIBEN:

This bit is only valid for THPP STS-1/STM0 #1.

SRCJ1, SRCC2, SRCF2, SRCZ3, SRCZ4, SRCZ5:

The SRCnn bits are used to determine the source for the path overhead bytes. For example, when a logic 1 is written to SRCJ1, the J1 byte inserted can be found in the THPP Transmit C2 and J1 register. When a logic 0 is written to SRCJ1, the J1 byte source can either be the TPOH input or the TTTP PATH depending on the value of the PTBJ1 register bit that can be found in this register.

These bits are only valid for THPP STS-1/STM0 #1.

SRCREI:

The valid high SRCREI register bit enables the THPP to overwrite the G1 byte with the REI field in the THPP Transmit H4 Mask and G1 register. When SRCREI is set to logic zero, the REI source is other than the THPP Transmit H4 Mask and G1 register.

These bits are only valid for THPP STS-1/STM0 #1.

SRCRDI:

The valid high SRCRDI register bit enables the THPP to overwrite the G1 byte with the RDI field in the THPP Transmit H4 Mask and G1 register. When SRCREI is set to logic zero, the RDI source is other than the THPP Transmit H4 Mask and G1 register.

These bits are only valid for THPP STS-1/STM0 #1.

PTBJ1:

The PTBJ1 or Path Trace Buffer J1 byte register bit is used to determine the origin of the path trace byte to be inserted. When PTBJ1 is high, the J1 byte is sourced from the TTTP PATH block; otherwise, the J1 byte is either sourced from the TPOH input or not inserted at all as controlled using the SRCJ1 bit.

These bits are only valid for THPP STS-1/STM0 #1.

ENH4MASK:

When ENH4MASK is logic high, the H4[7:0] byte in THPP Transmit H4 Mask and G1 register is used as an error mask on the H4 byte. When ENH4MASK is logic low, the H4[7:0] byte in THPP Transmit H4 Mask and G1 register is inserted as the H4 byte.

These bits are only valid for THPP STS-1/STM0 #1.

ENG1REC:

The valid high ENG1REC register bit enables the insertion of the PRDI[2:0] and PREI[3:0] of the G1 byte from the SARC block. When ENG1REC is set to logic low, the G1 byte source is other than the SARC block.

B3MASK:

When B3MASK is logic high, the byte received via the TPOH (valid only if TPOHEN is logic high) bit serial stream is to be used as a mask for an internally generated B3. When B3MASK is logic low, the byte received on TPOH (valid only if TPOHEN is logic high) will be inserted in the B3 byte if the path overhead source priority is TPOH.

H4MASK:

When H4MASK is logic high, the byte received via the TPOH (valid only if TPOHEN is logic high) bit serial stream is to be used as a mask for the H4 byte. When H4MASK is logic low, the byte received on TPOH (valid only if TPOHEN is logic high) will be inserted in the H4 byte only if the path overhead source priority is TPOH.

Indirect Register 02H: THPP Current Pointer Register

Bit	Type	Function	Default
Bit 15	R	NDF[3]	0
Bit 14	R	NDF[2]	0
Bit 13	R	NDF[1]	0
Bit 12	R	NDF[0]	0
Bit 11	R	S[1]	0
Bit 10	R	S[0]	0
Bit 9	R	CPTR[9]	0
Bit 8	R	CPTR[8]	0
Bit 7	R	CPTR[7]	0
Bit 6	R	CPTR[6]	0
Bit 5	R	CPTR[5]	0
Bit 4	R	CPTR[4]	0
Bit 3	R	CPTR[3]	0
Bit 2	R	CPTR[2]	0
Bit 1	R	CPTR[1]	0
Bit 0	R	CPTR[0]	0

CPTR[9:0]:

The CPTR[9:0] bits in the THPP Current Pointer Register reflect the value of the current payload pointer being inserted. This field can be used to verify the user programmable pointer when FIXPTR is logic one.

S[1:0]:

The S[1:0] bits in the THPP Current Pointer Register reflect the ss bits being inserted. This field can be used by the to verify the ss field in the user programmable pointer when FIXPTR is logic one.

NDF[3:0]:

The NDF[3:0] bits in the THPP Current Pointer Register reflect the NDF bit field being inserted. This field can be used to verify the NDF field in the user programmable pointer when FIXPTR is logic one.

Indirect Register 03H: THPP Arbitrary Pointer Register

Bit	Type	Function	Default
Bit 15	R/W	NDF[3]/CONCAT[15]	0
Bit 14	R/W	NDF[2]/CONCAT[14]	0
Bit 13	R/W	NDF[1]/CONCAT[13]	0
Bit 12	R/W	NDF[0]/CONCAT[12]	0
Bit 11	R/W	S[1]/CONCAT[11]	0
Bit 10	R/W	S[0]/CONCAT[10]	0
Bit 9	R/W	APTR[9]/CONCAT[9]	0
Bit 8	R/W	APTR[8]/CONCAT[8]	0
Bit 7	R/W	APTR[7]/CONCAT[7]	0
Bit 6	R/W	APTR[6]/CONCAT[6]	0
Bit 5	R/W	APTR[5]/CONCAT[5]	0
Bit 4	R/W	APTR[4]/CONCAT[4]	0
Bit 3	R/W	APTR[3]/CONCAT[3]	0
Bit 2	R/W	APTR[2]/CONCAT[2]	0
Bit 1	R/W	APTR[1]/CONCAT[1]	0
Bit 0	R/W	APTR[0]/CONCAT[0]	0

APTR[9:0]:

The APTR[9:0] bits are used to set an arbitrary payload pointer value. The arbitrary pointer value is transferred by writing a logic one to the PLD bit in the THPP Control Register. A legal value (i.e. 0- 782) results in the THPP forcing a shifting to the corresponding byte position. If the FTPTR bit is a logic 1, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) continueously.

These bits are only valid for THPP STS-1/STM0 #1.

S[1:0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions in the payload pointer.

These bits are only valid for THPP STS-1/STM0 #1.

NDF[3:0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions of a pointer.

These bits are only valid for THPP STS-1/STM0 #1.

CONCAT[15:0]:

The CONCAT[15:0] bits contain the value inserted in the H1 and H2 bit positions of a pointer.

These bits are only valid for THPP STS-1/STM0 #2-#48.

Indirect Register 05H: THPP B3 Mask and Fixed Stuff Byte

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]:

When the FSBEN bit in the THPP Control register is logic one, the THPP replaces the fixed bytes with the byte from this register.

This field should be consistent for all THPP STS-1/STM0 #1 through #48.

B3MASK[7:0]:

The calculated B3 parity byte is always XORed with this register bit to allow the user to insert errors in B3.

This field is only valid for THPP STS-1/STM0 #1.

Indirect Register 06H: THPP Transmit C2 and J1

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]:

The J1[7:0] bits are inserted in the J1 byte position when the SRCJ1 bit of the THPP Source & Pointer Control Register is logic 0 and TPOHEN is low during the path trace bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position when the SRCC2 bit of the THPP Source & Pointer Control Register is logic 0 and TPOHEN is low during the path signal lable bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

Indirect Register 07H: THPP Transmit H4 Mask and G1

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]:

The G1[7:0] bits are inserted in the G1 byte position when the SRCREI and SRCRDI bits of the Source and Pointer Control Register are high and TPOHEN is low during the path status bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

H4[7:0]:

The H4[7:0] bits are inserted in the H1 byte position when the ENH4MASK bit of the Source and Pointer Control Register is high and TPOHEN is low during the path multiframe bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

Indirect Register 08H: THPP Transmit F2 and Z3

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

Z3[7:0]:

The Z3[7:0] bits are inserted in the Z3 byte position when the SRCZ3 bit of the THPP Source & Pointer Control Register is logic 0 and input TPOHEN is low during the path Z3 growth bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

F2[7:0]:

The F2[7:0] bits are inserted in the F2 byte position when the SRCF2 bit of the THPP Source & Pointer Control Register is logic 0 and input TPOHEN is low during the path User Channel bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

Indirect Register 09H: THPP Transmit Z4 and Z5

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z5[7:0]:

The Z5[7:0] bits are inserted in the Z5 byte position when the SRCZ5 bit of the THPP Source & Pointer Control Register is logic 0 and input TPOHEN is low during the path Z5 growth bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

Z4[7:0]:

The Z4[7:0] bits are inserted in the Z4 byte position when the SRCZ4 bit of the THPP Source & Pointer Control Register is logic 0 and input TPOHEN is low during the path Z4 growth bit positions in the path overhead input stream, TPOH.

This field is only valid for THPP STS-1/STM0 #1.

Register 0600H: RSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

IADDR[2:0]:

The address location (IADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[2:0]	Indirect Register
000	RSVCA Pointer Justification Interrupt Enable
001	RSVCA FIFO Interrupt Enable
010	RSVCA Positive Justification Performance Monitor
011	RSVCA Negative Justification Performance Monitor
100	RSVCA Diagnostic/Configuration
101 to 111	Unused

RWB:

The active high read and active low write (RWB) bit selects if the current access to a internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write

access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY:

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0601H: RSVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the

data from DATA[15:0] will be transferred to the register. The indirect Data register must contain

Register 0603H: RSVCA Positive Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved[3]	X
Bit 14	R/W	Reserved[2]	X
Bit 13	R/W	Reserved[1]	X
Bit 12	R/W	Reserved[0]	X
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	PPJI[1]	0

PPJI[1]:

The positive pointer justification interrupt status (PPJI[1]) bit indicates a positive pointer adjustment in the STS-48c/STM-4-4c stream. PPJI[1] is set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. This interrupt status bit is independent of the interrupt enable bit. PPJI[1] is cleared to logic 0 when this register is read.

Register 0604H: RSVCA Negative Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved[3]	X
Bit 14	R/W	Reserved[2]	X
Bit 13	R/W	Reserved[1]	X
Bit 12	R/W	Reserved[0]	X
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	NPJI[1]	0

NPJI[1]:

The negative pointer justification interrupt status (NPJI[1]) bit indicates a negative pointer adjustment in the STS-48c/STM-4-4c stream. NPJI[1] is set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. This interrupt status bit is independent of the interrupt enable bit. NPJI[1] is cleared to logic 0 when this register is read.

Register 0605H: RSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	FOVRI[1]	0

FOVRI[1]:

The FIFO overflow event interrupt status (FOVRI[1]) bit indicates a FIFO overflow in the SVCA. FOVRI[1] is set to logic 1 to indicate a FIFO overflow event. This interrupt status bit is independent of the interrupt enable bit. FOVRI[1] is cleared to logic 0 when this register is read.

Register 0606H: RSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	FUDRI[1]	0

FUDRI[1]:

The FIFO underflow event interrupt status (FUDRI[1]) bit indicates a FIFO underflow in the SVCA. FUDRI[1] is set to logic 1 to indicate a FIFO underflow event. This interrupt status bit is independent of the interrupt enable bit. FUDRI[1] is cleared to logic 0 when this register is read.

Indirect Register 00H: RSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PJIEN[1]	0

PJIEN[1]:

The pointer justification event interrupt enable (PJIEN[1]) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Indirect Register 01H: RSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	FIEN[1]	0

FIEN[1]:

The FIFO event interrupt enable (FIEN[1]) bit controls the activation of the interrupt (INTB) output due to a FIFO overflow or a FIFO underflow. When set to logic 1, the corresponding pending interrupts will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupts will not assert the interrupt (INTB) output.

Indirect Register 02H: RSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

PJPMON[12:0]:

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 3 TCLK cycles after a transfer is triggered by writing a logic one to the PMONXFER bit of the SVCA Diagnostic/Configuration Register or by writing to the S/UNI-2488 Identity, and Global Performance Monitor Update register.

Indirect Register 03H: RSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

NJPMON[12:0]:

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 3 TCLK cycles after a transfer is triggered by writing a logic one to the PMONXFER bit of the SVCA Diagnostic/Configuration Register or by writing to the S/UNI-2488 Identity, and Global Performance Monitor Update register.

Indirect Register 04H: RSVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	X
Bit 14	R/W	PTR_RST	X
Bit 13	W	PMONXFER	X
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		unused	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Diag_FifoAISDis	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Diag_LOP	0
Bit 1	R/W	Diag_NegJust	0
Bit 0	R/W	Diag_PosJust	1

Diag_PosJust :

The Diag_PosJust bit forces the SVCA to generate outgoing positive justification event. When set to 1, the SVCA generates positive justification events at the rate of one every four frames regardless of the current level of the internal fifo. Prolonged application may cause the FIFO to overflow.

Note : Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_NegJust :

The Diag_NegJust bit forces the SVCA to generate outgoing negative justification events. When set to 1, the SVCA generates negative justification events at the rate of one every four frames regardless of the current level of the internal fifo. Prolonged application may cause the FIFO to underflow.

Note : Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_LOP :

When set high, the Diag_LOP bit forces the SVCA to invert the outgoing NDF field of the payload (selected path(s)) pointer causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

Diag_PAIS :

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_FifoAISDis :

When set high, the Diag_FifoAISDis bit forces the SVCA not to insert path AIS upon FIFO overflow/underflow detection. When set low (normal operation), detection of FIFO overflow/underflow causes path AIS to be inserted in the outgoing stream for at least three consecutive frames.

PMON_XFER :

When set high, Negative and Positive Performance Monitors are transferred to a stable readable register.

PTR_RST:

When set high, incoming and outgoing pointers are reset to their default values. This bit is level sensitive.

Register 0680H: TSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

IADDR[2:0]:

The address location (IADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[2:0]	Indirect Register
000	TSVCA Pointer Justification Interrupt Enable
001	TSVCA FIFO Interrupt Enable
010	TSVCA Positive Justification Performance Monitor
011	TSVCA Negative Justification Performance Monitor
100	TSVCA Diagnostic/Configuration
101 to 111	Unused

RWB:

The active high read and active low write (RWB) bit selects if the current access to a internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write

access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY:

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0601H: TSVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 0603H: TSVCA Positive Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved[3]	X
Bit 14	R/W	Reserved[2]	X
Bit 13	R/W	Reserved[1]	X
Bit 12	R/W	Reserved[0]	X
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	PPJI[1]	0

PPJI[1]:

The positive pointer justification interrupt status (PPJI[1]) bit indicates a positive pointer adjustment in the STS-48c/STM-4-4c stream. PPJI[1] is set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. This interrupt status bit is independent of the interrupt enable bit. PPJI[1] is cleared to logic 0 when this register is read.

Register 0604H: TSVCA Negative Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved[3]	X
Bit 14	R/W	Reserved[2]	X
Bit 13	R/W	Reserved[1]	X
Bit 12	R/W	Reserved[0]	X
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	NPJI[1]	0

NPJI[1]:

The negative pointer justification interrupt status (NPJI[1]) bit indicates a negative pointer adjustment in the STS-48c/STM-4-4c stream. NPJI[1] is set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. This interrupt status bit is independent of the interrupt enable bit. NPJI[1] is cleared to logic 0 when this register is read.

Register 0605H: TSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	FOVRI[1]	0

FOVRI[1]:

The FIFO overflow event interrupt status (FOVRI[1]) bit indicates a FIFO overflow in the SVCA. FOVRI[1] is set to logic 1 to indicate a FIFO overflow event. This interrupt status bit is independent of the interrupt enable bit. FOVRI[1] is cleared to logic 0 when this register is read.

Register 0606H: TSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	FUDRI[1]	0

FUDRI[1]:

The FIFO underflow event interrupt status (FUDRI[1]) bit indicates a FIFO underflow in the SVCA. FUDRI[1] is set to logic 1 to indicate a FIFO underflow event. This interrupt status bit is independent of the interrupt enable bit. FUDRI[1] is cleared to logic 0 when this register is read.

Indirect Register 00H: TSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PJIEN[1]	0

PJIEN[1]:

The pointer justification event interrupt enable (PJIEN[1]) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Indirect Register 01H: TSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	FIEN[1]	0

FIEN[1]:

The FIFO event interrupt enable (FIEN[1]) bit controls the activation of the interrupt (INTB) output due to a FIFO overflow or a FIFO underflow. When set to logic 1, the corresponding pending interrupts will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupts will not assert the interrupt (INTB) output.

Indirect Register 02H: TSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

PJPMON[12:0]:

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 3 TCLK cycles after a transfer is triggered by writing a logic one to the PMONXFER bit of the SVCA Diagnostic/Configuration Register or by writing to the S/UNI-2488 Identity, and Global Performance Monitor Update register.

Indirect Register 03H: TSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

NJPMON[12:0]:

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 3 TCLK cycles after a transfer is triggered by writing a logic one to the PMONXFER bit of the SVCA Diagnostic/Configuration Register or by writing to the S/UNI-2488 Identity, and Global Performance Monitor Update register.

Indirect Register 04H: TSVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	X
Bit 14	R/W	PTR_RST	X
Bit 13	W	PMONXFER	X
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		unused	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Diag_FifoAISDis	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Diag_LOP	0
Bit 1	R/W	Diag_NegJust	0
Bit 0	R/W	Diag_PosJust	1

Diag_PosJust :

The Diag_PosJust bit forces the SVCA to generate outgoing positive justification event. When set to 1, the SVCA generates positive justification events at the rate of one every four frames regardless of the current level of the internal fifo. Prolonged application may cause the FIFO to overflow.

Note : Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_NegJust :

The Diag_NegJust bit forces the SVCA to generate outgoing negative justification events. When set to 1, the SVCA generates negative justification events at the rate of one every four frames regardless of the current level of the internal fifo. Prolonged application may cause the FIFO to underflow.

Note : Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_LOP :

When set high, the Diag_LOP bit forces the SVCA to invert the outgoing NDF field of the payload (selected path(s)) pointer causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

Diag_PAIS :

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_FifoAISDis :

When set high, the Diag_FifoAISDis bit forces the SVCA not to insert path AIS upon FIFO overflow/underflow detection. When set low (normal operation), detection of FIFO overflow/underflow causes path AIS to be inserted in the outgoing stream for at least three consecutive frames.

PMON_XFER :

When set high, Negative and Positive Performance Monitors are transferred to a stable readable register.

PTR_RST:

When set high, incoming and outgoing pointers are reset to their default values. This bit is level sensitive.

Register 0700H: RTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]:

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. This register should only be set to 0001 since only the STS-1/STM-0 #1 path byte is valid.

IADDR[7:0]:

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB:

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY:

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0701H: RTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 0702H: RTTP PATH Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserve	X
Bit 9	R	Reserve	X
Bit 8	R	Reserve	X
Bit 7	R	Reserve	X
Bit 6	R	Reserve	X
Bit 5	R	Reserve	X
Bit 4	R	Reserve	X
Bit 3	R	Reserve	X
Bit 2	R	Reserve	X
Bit 1	R	Reserve	X
Bit 0	R	TIUV[1]	X

TIUV[1]:

The trace identifier unstable status (TIUV[1]) bit indicates the current status of the TIU defect.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 tail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous tail trace byte. BYTE_TIUV is set to logic 0 when the same tail trace byte is received for 48 consecutive frames.

Register 0703H: RTTP PATH Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserve	0
Bit 10	R/W	Reserve	0
Bit 9	R/W	Reserve	0
Bit 8	R/W	Reserve	0
Bit 7	R/W	Reserve	0
Bit 6	R/W	Reserve	0
Bit 5	R/W	Reserve	0
Bit 4	R/W	Reserve	0
Bit 3	R/W	Reserve	0
Bit 2	R/W	Reserve	0
Bit 1	R/W	Reserve	0
Bit 0	R/W	TIUE[1]	0

TIUE[1]:

The trace identifier unstable interrupt enable (TIUE[1]) bit controls the activation of the interrupt (INTB) output. When the bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0704H: RTTP PATH Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserve	X
Bit 9	R	Reserve	X
Bit 8	R	Reserve	X
Bit 7	R	Reserve	X
Bit 6	R	Reserve	X
Bit 5	R	Reserve	X
Bit 4	R	Reserve	X
Bit 3	R	Reserve	X
Bit 2	R	Reserve	X
Bit 1	R	Reserve	X
Bit 0	R	TIUI[1]	X

TIUI[1]:

The trace identifier unstable interrupt status (TIUI[1]) bit is an event indicator. TIUI[1] is set to logic 1 to indicate any changes in the status of TIUV[1] (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit. TIUI[1] is cleared to logic 0 when this register is read.

Register 0705H: RTTP PATH Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserve	X
Bit 9	R	Reserve	X
Bit 8	R	Reserve	X
Bit 7	R	Reserve	X
Bit 6	R	Reserve	X
Bit 5	R	Reserve	X
Bit 4	R	Reserve	X
Bit 3	R	Reserve	X
Bit 2	R	Reserve	X
Bit 1	R	Reserve	X
Bit 0	R	TIMV[1]	X

TIMV[1]:

The trace identifier mismatch status (TIMV[1]) bit indicates the current status of the TIM defect.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 0706H: RTTP PATH Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserve	0
Bit 10	R/W	Reserve	0
Bit 9	R/W	Reserve	0
Bit 8	R/W	Reserve	0
Bit 7	R/W	Reserve	0
Bit 6	R/W	Reserve	0
Bit 5	R/W	Reserve	0
Bit 4	R/W	Reserve	0
Bit 3	R/W	Reserve	0
Bit 2	R/W	Reserve	0
Bit 1	R/W	Reserve	0
Bit 0	R/W	TIME[1]	0

TIME[1]:

The trace identifier mismatch interrupt enable (TIME[1]) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0707H: RTTP PATH Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserve	X
Bit 10	R	Reserve	X
Bit 9	R	Reserve	X
Bit 8	R	Reserve	X
Bit 7	R	Reserve	X
Bit 6	R	Reserve	X
Bit 5	R	Reserve	X
Bit 4	R	Reserve	X
Bit 3	R	Reserve	X
Bit 2	R	Reserve	X
Bit 1	R	Reserve	X
Bit 0	R	TIMI[1]	X

TIMI[1]:

The trace identifier mismatch interrupt status (TIMI[1]) bit is an event indicator. TIMI[1] is set to logic 1 to indicate any changes in the status of TIMV[1] (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit. TIMI[1] is cleared to logic 0 when this register is read.

Indirect Register 00H: RTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]:

The tail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the tail trace message.

ALGO[1:0]	Tail trace algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the tail trace algorithms are disable. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16:

The message length (LENGTH16) bit selects the length of the tail trace message use by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

NOSYNC:

The synchronization disable (NOSYNC) bit disables the synchronization of the tail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the tail trace message. The bytes of the tail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the tail trace message. When LENGTH16 is set to logic 1, the tail trace message is synchronize on the MSB of the tail trace message. The byte with its MSB set high is placed in the first byte location of the captured page. When LENGTH16 is set to logic 0, the tail trace message is synchronize on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the tail trace message. The byte following the CR/LF bytes is placed in the first byte location of the captured page.

PER5:

The message persistency (PER5) bit selects the number of multi-frames a tail trace message must be received in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same tail trace message must be receive for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same tail trace message must be received for 3 consecutive multi frame to be declared persistent.

ZEROEN:

The all zero message enable (ZEROEN) bit selects if the all zero message are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

Indirect Register 40H to 7FH: RTTP PATH Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

The RTTP PATH Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]:

The captured tail trace message (CTRACE[7:0]) bits contain the currently received tail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronize. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP PATH Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

The RTTP PATH Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]:

The accepted tail trace message (ATRACE[7:0]) bits contain the persistent tail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same tail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same tail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same tail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP PATH Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The RTTP PATH Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]:

The expected tail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validated the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 0708H: TTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]:

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. PATH[3:0] should be set to 0001.

IADDR[6:0]:

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB:

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY:

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0709H: TTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16:

The message length (LENGTH16) bit selects the length of the tail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

BYTEEN:

The single byte message enable (BYTEEN) bit enables the single byte tail trace message. When BYTEEN is set to logic 1, the length of the tail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the tail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN:

The all zero message enable (ZEROEN) bit enables the transmission of an all zero tail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero tail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP PATH Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]:

The tail trace message (TRACE[7:0]) bits contain the tail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Register 0720H: SARC Indirect Address

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]:

This field should be set ot 1H

Register 0722H: SARC Section Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	LRDI22	0
Bit 0	R/W	Reserved	0

LRDI22:

The line remote defect indication (LRDI22) bit selects the line RDI persistence when line RDI is asserted as a result of received defects. When LRDI22 is set to logic 1, a new line RDI-L indication is transmitted for at least 22 frames. When LRDI22 is set to logic 0, a new line RDI indication is transmitted for at least 12 frames.

Register 0723H: SARC Section SALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	GROWTH[1]	0
Bit 10	R/W	GROWTH[0]	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN:

The OOF enable bit allows the out of frame defect to be ORed into the SALM output. When the OOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the OOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOFEN:

The LOF enable bit allows the loss of frame defect to be ORed into the SALM output. When the LOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the LOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOSEN:

The LOS enable bit allows the loss of signal defect to be ORed into the SALM output. When the LOSEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the LOSEN bit is set low, the corresponding defect indication does not affect the SALM output.

LAISEN:

The LAIS enable bit allows the line alarm indication signal defect to be ORed into the SALM output. When the LAISEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the LAISEN bit is set low, the corresponding defect indication does not affect the SALM output.

LRDIEN:

The LRDI enable bit allows the line remote defect indication defect to be ORed into the SALM output. When the LRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the LRDIEN bit is set low, the corresponding defect indication does not affect the SALM output.

APSBFEN:

The APSBF enable bit allows the APS byte failure defect to be ORed into the SALM output. When the APSBFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the APSBFEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIUEN:

The STIU enable bit allows the section trace identifier unstable defect to be ORed into the SALM output. When the STIUEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the STIUEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIMEN:

The STIM enable bit allows the section trace identifier mismatch defect to be ORed into the SALM output. When the STIMEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the STIMEN bit is set low, the corresponding defect indication does not affect the SALM output.

SDBEREN:

The SDBER enable bit allows the signal degrade BER defect to be ORed into the SALM output. When the SDBEREN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the SDBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

SFBEREN:

The SFBER enable bit allows the signal failure BER defect to be ORed into the SALM output. When the SFBEREN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the SFBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

GROWTHEN[1:0]:

The GROWTH enable bit allows the growth defect to be ORed into the SALM output. When the GROWTHEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the GROWTHEN bit is set low, the corresponding defect indication does not affect the SALM output.

Register 0724H: SARC Section RLAISINS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	GROWTH[1]	0
Bit 10	R/W	GROWTH[0]	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN, LOFEN, LOSEN, LAISEN, LRDIEN, APSBFEN, STIUEN, STIMEN, SDBEREN, SFBEREN, GROWTHEN[1:0]:

The above enable bits allows for the auto assertion of receive LAIS based on the following conditions:

- out of frame defect
- loss of frame defect
- loss of signal defect
- line alarm indication signal defect
- line remote defect indication defect
- APS byte failure defect
- section trace identifier unstable defect
- section trace identifier mismatch defect
- signal degrade BER defect
- signal failure BER defect
- growth defect

When the bit is set high, the corresponding defect indication is ORed with other defect indications and the result forces receive LAIS. Under receive LAIS, a all ones pattern is written into the receive line overhead and SPE bytes. When the bit is set low, the corresponding defect indication does not affect the assertion of receive LAIS.

Register 0725H: SARC Section TLRDIINS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	GROWTH[1]	0
Bit 10	R/W	GROWTH[0]	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN, LOFEN, LOSEN, LAISEN, LRDIEN, APSBFEN, STIUEN, STIMEN, SDBEREN, SFBEREN, GROWTHEN[1:0]:

The above enable bits allows for the auto assertion of transmit LAIS based on the following conditions:

- out of frame defect
- loss of frame defect
- loss of signal defect
- line alarm indication signal defect
- line remote defect indication defect
- APS byte failure defect
- section trace identifier unstable defect
- section trace identifier mismatch defect
- signal degrade BER defect
- signal failure BER defect
- growth defect

When the bit is set high, the corresponding defect indication is ORed with other defect indications and the result forces transmit LAIS. Under transmit LAIS, an all ones pattern is written into the transmit line overhead and SPE bytes. When the bit is set low, the corresponding defect indication does not affect the assertion of transmit LAIS.

Register 0728H: SARC Path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI22	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLOPTREND	0
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG[0]	0

PLOPTRCFG[1:0]:

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits define the LOP-P defect. When PLOPTRCFG[1:0] is set to 00b, an LOP-P defect is declared when the pointer is in the LOP state and an LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG[1:0] is set to 01b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG[1:0] is set to 10b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state.

PAISPTRCFG[1:0]:

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the AIS-P defect. When PAISPTRCFG[1:0] is set to 00b, an AIS-P defect is declared when the pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When PAISPTRCFG[1:0] is set to 01b, an AIS-P defect is declared when the pointer or any of the concatenated pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG[1:0] is set to 10b, an AIS-P defect is declared when the pointer and all the concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state.

PLOPTREND:

The path loss of pointer removal (PLOPTREND) bit controls the removal of a LOP-P defect when an AIS-P defect is declared. When PLOPTREND is set to logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

PERDI22:

The path enhance remote defect indication (PERDI22) bit selects the path ERDI persistence. When PERDI22 is set to logic 1, a new path ERDI indication is transmitted by the THPP for at least 22 frames. When PERDI22 is set to logic 0, a new path ERDI indication is transmitted transmitted by the THPP for at least 12 frames.

PRDIEN:

The path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI code and the 3 bits ERDI code. When PRDIEN is set to logic 1, the 1 bit RDI code is transmitted transmitted by the THPP. When PRDIEN is set to logic 0, the 3 bit ERDI code is transmitted transmitted by the THPP.

Register 0729H: SARC Path RALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PGROWTH[1]	0
Bit 12	R/W	PGROWTH[0]	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RSALMEN	0

SALMEN, PLOPTREN, PAISPTREN, PPLUEN, PPLMEN, PUNEQEN, PPDIEN, PRDIEN, PERDIEN, PTIUEN, PTIMEN, PGROWTHEN[1:0]:

The above enable bits allows for the generation of the RALM output based on the following conditions:

- section alarm (register 06A3H)
- path loss of pointer defect
- path AIS pointer defect
- path payload label unstable defect
- path payload label mismatch defect
- path unequipped defect
- path payload defect indication defect
- path remote defect indication defect
- path enhanced remote defect indication defect
- path trace identifier unstable defect
- path trace identifier mismatch defect
- path growth defect

When the bit is set high, the corresponding defect indication is ORed with other defect indications to generate RALM. When the bit is set low, the corresponding defect indication does not affect RALM.

Register 072A: SARC Path RPAISINS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PGROWTH[1]	0
Bit 12	R/W	PGROWTH[0]	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RLAISINSEN	0

RLAISINSEN, PLOPTREN, PAISPTREN, PPLUEN, PPLMEN, PUNEQEN, PPDIEN, PRDIEN, PERDIEN, PTIUEN, PTIMEN, PGROWTHEN[1:0]:

The above enable bits allows for the generation of receive path AIS (AIS-P) based on the following conditions:

- receive LAIS (register 06A4H)
- path loss of pointer defect
- path AIS pointer defect
- path payload label unstable defect
- path payload label mismatch defect
- path unequipped defect
- path payload defect indication defect
- path remote defect indication defect
- path enhanced remote defect indication defect
- path trace identifier unstable defect
- path trace identifier mismatch defect
- path growth defect

When the bit is set high, the corresponding defect indication is ORed with other defect indications to generate receive AIS-P. When under receive AIS-P, a all ones pattern is inserted into the receive SPE bytes. When the bit is set low, the corresponding defect indication does not affect the assertion of AIS-P.

Register 0730H: SARC LOP Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PLOPTRV	X

PLOPTRV:

The path loss of pointer status (PLOPTRV) bit indicates the current status of the LOP-P defect for STS-1/STM-0. When PLOPTRCFG register bits are set to 00b, PLOPTRV is asserted when the pointer is in the LOP state and PLOPTRV is negated when the pointer is not in the LOP state. When PLOPTRCFG register bits are set to 01b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG register bits are set to 10b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state. When the PLOPTREND register bit is set to one, PLOPPTRV is negated when a AIS-P defect is detected.

Register 0731H: SARC LOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PLOPTRE[1]	0

PLOPTRE:

The path loss of pointer interrupt enable (PLOPTRE) bit controls the activation of the interrupt (INTB) output. When this bit is set to logic 1, the pending interrupt will assert the interrupt (INTB) output. When this bit is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Register 0732H: SARC LOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PLOPTRI[1]	X

PLOPTRI:

The path loss of pointer interrupt status (PLOPTRI) bit is an event indicator for the STS-1/STM-0 path #1. PLOPTRI is set to logic 1 to indicate any changes in the status of PLOPTRV. This interrupt status bit is independent of the interrupt enable bit. PLOPTRI is cleared to logic 0 when this register is read.

Register 0733H: SARC AIS Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PAISPTRV[1]	X

PAISPTRV:

The path AIS pointer status (PAISPTRV) bit indicates the current status of the AIS-P defect for STS-1/STM-0 #1. When PAISPTRCFG register bits are set to 00b, PAISPTRV is asserted when the pointer is in the AIS state and PAISPTRV is negated when the pointer is not in the AIS state. When PAISPTRCFG register bits are set to 01b, PAISPTRV is asserted when the pointer or any of the concatenated pointers is in the AIS state and PAISPTRV is negated when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG register bits are set to 10b, PAISPTRV is asserted when the pointer and all the concatenated pointers are in the AIS state and PAISPTRV is negated when the pointer or any of the concatenation pointers are not in the AIS state.

Register 0734H: SARC AIS Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PAISPTRE	0

PAISPTRE:

The path AIS signal pointer interrupt enable (PAISPTRE) bit controls the activation of of the interrupt (INTB) output. When this bit is set to logic 1, the pending interrupt will assert the interrupt (INTB) output. When this bit is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Register 0735H: SARC AIS Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PAISPTRI	X

PAISPTRI:

The path AIS pointer interrupt status (PAISPTRI) bit is an event indicators for STS-1/STM-0 paths #1. PAISPTRI is set to logic 1 to indicate any changes in the status of PAISPTRV. These interrupt status bits are independent of the interrupt enable bits. PAISPTRI is cleared to logic 0 when this register is read.

Register 0740H: RCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	POS_SEL	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	STRIP_SEL	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	IDLEPASS	0
Bit 5	R/W	CRCPASS	0
Bit 4	R/W	CRC_SEL[1]	1
Bit 3	R/W	CRC_SEL[0]	1
Bit 2	R/W	RXOTYP	0
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

PROV:

The processor provision bit (PROV) is used to enable the RCFP. When PROV is logic 0, the RCFP ATM and packet processors are disabled and will not transfer any valid data to the Receive FIFO interface. When PROV is logic 1, the RCFP ATM or packet processor is enabled and will process data presented to it and transfer data to the Receive FIFO (RXSDQ).

DESCRMBL:

The DESCRMBL bit controls the descrambling of the packet or ATM cell payload with the polynomial $x^{43} + 1$. When DESCRMBL is set to logic 0, frame or cell payload descrambling is disabled. When DESCRMBL is set to logic 1, payload descrambling is enabled.

RXOTYP:

The RXOTYP bit determines if an incoming alarm signal (from IPAIS[x]) will stop a packet by simply asserting EOP, (RXOTYP set to logic 0), or by asserting both EOP and ERR, (RXOTYP set to logic 1). When RXOTYP is set to logic 0, premature termination of the packet will result in that packet failing a FCS check.

This bit is only valid when in POS mode. In ATM mode the RCFP will finish processing any cell in progress and then stop until the alarm signal is cleared.

CRC_SEL[1:0]:

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, after byte destuffing and descrambling.

Table 9: Functionality of the CRC_SEL[1:0] register bits

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS verification
01	Reserved	Reserved
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

CRCPASS:

The CRCPASS bit controls the dropping of cells and packets based on the detection of a CRC error.

When in ATM mode and when CRCPASS is a logic 0, cells containing an uncorrectable HCS error are dropped and the HCS verification state machine transitions to the 'Detection Mode'.

Cells containing a correctable HCS error have the error fixed (if HCS error correction is enabled), and the state machine transitions to the 'Detection Mode'.
When CRCPASS is logic 1, cells are passed to the external FIFO interface regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine will never lose cell delineation.

Regardless of the programming of this bit, ATM cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the DELINDIS bit in this register is set to logic 1.
When in POS mode and CRCPASS is logic 1, then packets with FCS errors are not marked as such and are passed to the external FIFO interface as if no FCS error occurred. When CRCPASS is logic 0, then packets with FCS errors are marked with ERR.

IDLEPASS:

The IDLEPASS bit controls the function of the ATM Idle Cell filter. It is only valid when in ATM mode. When IDLEPASS is written with logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is enabled, the Idle Cell Header Pattern and Mask register bits are ignored. The default state of this bit and the bits in the RCFP Idle Cell Header and Mask Register enable the dropping of Idle cells.

STRIP_SEL:

The frame check sequence stripping bit (STRIP_SEL) selects the CRC stripping mode of the RCFP. When STRIP_SEL is logic 1, CRC stripping is enabled. When STRIP_SEL is logic 0, CRC stripping is disabled. Note that CRC_SEL[1:0] must not equal "00", (no CRC) for stripping to be enabled. When stripping is enabled the received packet FCS or ATM cell HCS byte(s) are not passed to the RXSDQ FIFO. When STRIP is disabled the received packet FCS are transferred over the FIFO interface. When DELINDIS is enabled, packets and cells are not delineated therefore the value of STRIP_SEL is ignored. **The STRIP_SEL bit must be set to logic 1 if working in ATM mode.**

INVERT:

The data inversion bit (INVERT) configures the processor to logically invert the incoming stream before processing it. When INVERT is set to logic 1, the stream is logically inverted before processing. When INVERT is set to logic 0, the stream is not inverted before processing.

POS_SEL:

The Packet Over SONET (POS_SEL) bit selects the data type mode of the RCFP. When POS_SEL is logic 1, POS mode is selected. When POS_SEL is logic 0, ATM mode is selected.

Reserved:

All Reserved bits must be set to their default values for proper operation.

Register 0741H: RCFP Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	OOFV	X
Bit 8	R	LOFV	X
Bit 7	R/W	MINLE	0
Bit 6	R/W	MAXLE	0
Bit 5	R/W	ABRTE	0
Bit 4	R/W	XFERE	0
Bit 3	R/W	CCRCE	0
Bit 2	R/W	UCRCE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOFE	0

LOFE:

The LOFE bit enables the generation of an interrupt due to a change in the ATM LCD state. When LOFE is set to logic 1, the interrupt is enabled.

OOFE:

The OOFE bit enables the generation of an interrupt due to a change in ATM cell delineation state or packet Idle state. When OOFE is set to logic 1, the interrupt is enabled.

UCRCE

The UCRCE bit enables the generation of an interrupt due to the detection of an uncorrectable ATM HCS or packet FCS error. When UCRCE is set to logic 1, the interrupt is enabled.

Reserved:

The Reserved bit should be set to logic 0 for proper operation.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RCFP performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

ABRTE:

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE:

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE:

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set to logic 1, the interrupt is enabled.

LOFV:

The LOFV bit gives the ATM Loss of Cell Delineation state. When LOFV is logic 1, an out of cell delineation (LOF) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LOFV is logic 0, the RCFP has been in cell delineation for the number of cells specified in the RCFP LCD Count Threshold register. The cell time period can be varied by using the LCDC[10:0] register bits in the RCFP LCD Count Threshold register.

OOFV:

The OOFV bit indicates the ATM cell delineation or packet out of frame alignment state. When OOFV is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries or the packet processor is in Idle state. When OOFV is logic 0, the cell delineation state machine is in the 'SYNC' state (either Correction or Detection mode) and cells are passed through the receive FIFO or the packet processor is not in Idle state.

Register 0742H: RCFP Interrupt Indication and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	MINLI	X
Bit 6	R	MAXLI	X
Bit 5	R	ABRTI	X
Bit 4	R	XFERI	X
Bit 3	R	Reserved	X
Bit 2	R	UCRCI	X
Bit 1	R	OOFI	X
Bit 0	R	LOFI	X

LOFI:

The LOFI bit is set to logic 1 when there is a change in the loss of cell delineation (LCD) state. The current value of the LCD state is available through the LOF bit in this register. This bit is set to logic 0 immediately after a read to this register. This interrupt can be masked using LOFE.

OOFI:

The OOFI bit is set to logic 1 when the RCFP ATM cell processor enters or exits the SYNC state or the packet processor enters or exits the frame alignment state. The OOFI bit is set to logic 0 immediately after a read to this register. This interrupt can be masked using OOFE.

UCRCI:

The UCRCI bit is set to logic 1 when an uncorrectable ATM HCS or packet FCS error is detected. This bit is set to logic 0 immediately after a read to this register. This interrupt can be masked using UCRCE.

Reserved:

This bit is not used.

XFERI:

The XFERI bit indicates that a transfer of accumulated counter data has occurred. Logic 1 in this bit position indicates that the RCFP performance monitor counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by writing to address 0000H. XFERI is set to logic 0 after this register is read. This interrupt can be masked using XFERE.

ABRTI:

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE. ABRTI is set to logic 0 after this register is read.

MAXLI:

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE. MAXLI is set to logic 0 after this register is read.

MINLI:

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. This interrupt can be masked using MINLE. MINLI is set to logic 0 after this register is read.

Register 0743H: RCFP Minimum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	0
Bit 10	R/W	MINPL[2]	1
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RBY_MODE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

Reserved:

The Reserved bits should be set to their default values for proper operation.RBY_MODE:

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[39:0] counters work. When RBY_MODE is logic 0, RBY_IC[39:0] will count all bytes in received packets (including FCS and Abort bytes) after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[39:0] will count all bytes in received packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid when working in POS mode.

MINPL[7:0]:

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame after destuffing but including the FCS. The default minimum packet length is 4 octets. Values smaller than 4 should not be used.

Register 0744H: RCFP Maximum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

MAXPL[16:1]:

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum packet length. MAXPL[0] is automatically set to logic 0. Packets larger than this length are marked with an error. This Maximum Packet Length defaults to 1.5 Kbytes. The packet length used here is defined as the number of bytes encapsulated into the POS frame excluding byte stuffing but including the FCS. The default maximum packet length is 1536 octets. The maximum packet length allowed is 128 Kbytes.

Register 0745H: RCFP LCD Count Threshold

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]:

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to the following:

Table 10: Average STS-x cell period versus LCD integration period

Format	Average cell period	Default LCD integration period
STS-48c	176.9 ns	63.8 µs
STS-12c	707.5 ns	254.7 µs

Register 0746H: RCFP Idle Cell Header and Mask

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[3]	0
Bit 10	R/W	PTI[2]	0
Bit 9	R/W	PTI[1]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to this register to select the bits included in the cell filter. Logic 1 in this bit position enables the CLP bit in the pattern register to be compared. Logic 0 causes the masking of the CLP bit. The default enables the register bit comparison.

MPTI[3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. Logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. Logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bit. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

Note that an all-zeros pattern must be present in the VPI and VCI fields of the Idle cell.

Register 0747H: RCFP Receive Byte/Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RBY_IC[15:0]	XXXX

Register 0748H: RCFP Receive Byte/Idle Cell Counter

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RBY_IC[31:16]	XXXX

Register 0749H: RCFP Receive Byte/Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	R	Unused	XXXX
Bit 7 to Bit 0	R	RBY_IC[39:32]	XXXX

RBY_IC[39:0]:

When POS mode is selected, the RBY_IC[39:0] bits indicate the number of bytes received within POS frames during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes in the count is controlled by the RBY_MODE register bit. HDLC flags are not counted.

When ATM mode is selected, the RBY_IC[39:0] bits indicate the number of Idle cells received and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP performance monitor counter registers loads the registers with the current counter value and resets the internal 40 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

Register 074AH: RCFP Packet/Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RP_RC[15:0]	XXXX

Register 074BH: RCFP Receive Packet/ATM Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RP_RC[31:16]	XXXX

RP_RC[31:0]:

When POS mode is selected, the RP_RC[31:0] bits indicate the number of received good packets passed to the FIFO interface during the last accumulation interval.

When ATM mode is selected, the RP_RC[31:0] bits indicate the number of received ATM cells and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP performance monitor Counter registers loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

Register 074CH: RCFP Receive Erred FCS/HCS Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]	X
Bit 14	R	EFCS[14]	X
Bit 13	R	EFCS[13]	X
Bit 12	R	EFCS[12]	X
Bit 11	R	EFCS[11]	X
Bit 10	R	EFCS[10]	X
Bit 9	R	EFCS[9]	X
Bit 8	R	EFCS[8]	X
Bit 7	R	EFCS[7]/UHCS[7]	X
Bit 6	R	EFCS[6]/UHCS[6]	X
Bit 5	R	EFCS[5]/UHCS[5]	X
Bit 4	R	EFCS[4]/UHCS[4]	X
Bit 3	R	EFCS[3]/UHCS[3]	X
Bit 2	R	EFCS[2]/UHCS[2]	X
Bit 1	R	EFCS[1]/UHCS[1]	X
Bit 0	R	EFCS[0]/UHCS[0]	X

EFCS[15:0]:

When POS mode is selected, the EFCS[15:0] bits indicate the number of received FCS errors during the last accumulation interval.

UHCS[7:0]:

When ATM mode is selected, the UHCS[7:0] bits indicate the number of uncorrectable HCS errors received in the last accumulation interval.

Register 074DH: RCFP Receive Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	RABR[15]	X
Bit 14	R	RABR[14]	X
Bit 13	R	RABR[13]	X
Bit 12	R	RABR[12]	X
Bit 11	R	RABR[11]	X
Bit 10	R	RABR[10]	X
Bit 9	R	RABR[9]	X
Bit 8	R	RABR[8]	X
Bit 7	R	RABR[7]	X
Bit 6	R	RABR[6]	X
Bit 5	R	RABR[5]	X
Bit 4	R	RABR[4]	X
Bit 3	R	RABR[3]	X
Bit 2	R	RABR[2]	X
Bit 1	R	RABR[1]	X
Bit 0	R	RABR[0]	X

RABR[15:0]:

When POS mode is selected, the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Aborted Packet Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

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Register 074EH: RCFP Receive Minimum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

RMINL[15:0]:

When POS mode is selected, the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Minimum Length Packet Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

Register 074FH: RCFP Receive Maximum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

RMAXL[15:0]:

When POS mode is selected, the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Maximum Length Packet Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

Register 0750H: TCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	FIFO_ERRE	0
Bit 14	R/W	FIFO_UDRE	0
Bit 13	R/W	XFERE	0
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	POS_SEL	0
Bit 7	R/W	CRC_SEL[1]	1
Bit 6	R/W	CRC_SEL[0]	1
Bit 5	R/W	FLAG[3]	0
Bit 4	R/W	FLAG[2]	0
Bit 3	R/W	FLAG[1]	0
Bit 2	R/W	FLAG[0]	0
Bit 1	R/W	SCRMBL	1
Bit 0	R/W	PROV	0

PROV:

The processor provision bit (PROV) is used to enable the TCFP. When PROV is logic 0, the TCFP ATM and packet processors are disabled and will not request data from the TXSDQ FIFO interface and will respond to data requests with all 1's data. When PROV is logic 1, the TCFP ATM or packet processor is enabled and will respond to data requests with valid data after requesting and processing data from the TXSDQ FIFO interface.

SCRMBL:

The SCRMBL bit controls the scrambling of the packet data stream or ATM cell payload. When SCRMBL is a logic 1, scrambling is enabled. When SCRMBL is a logic 0, scrambling is disabled.

FLAG[3:0]:

The flag insertion control (FLAG[3:0]) configures the minimum number of flag bytes the packet processor inserts between packets. The minimum number of flags (01111110) inserted between packets is shown in the table below. FLAG[3:0] are used only in POS mode.

Table 11: Selection of the number of Flag Bytes

FLAG[3:0]	Minimum Number of FLAG Bytes

0000	1 flag
0001	2 flags
0010	4 flags
0011	8 flags
0100	16 flags
0101	32 flags
0110	64 flags
0111	128 flags
1000	256 flags
1001	512 flags
1010	1024 flags
1011	2048 flags
1100	4096 flags
1101	8192 flags
1110	16384 flags
1111	32768 flags

CRC_SEL[1:0]:

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, before byte stuffing and scrambling.

Table 12: CRC Mode Selection

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS inserted
01	Reserved	No FCS inserted
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

POS_SEL:

The POS_SEL bit enables the POS HDLC frame processing mode. When POS_SEL is set to logic 1, POS processing will occur. When POS_SEL is set to logic 0, ATM mode is selected.

Reserved:

The Reserved bits should be set to logic 0 for proper operation.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the transmitted packet/cell counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

FIFO_UDRE:

The FIFO_UDRE bit enables the generation of an interrupt due to a FIFO underrun. When FIFO_UDRE is set to logic 1, the interrupt is enabled the signal INTB will be set to logic 0 whenever FIFO_UNRI is set to logic 1.

FIFO_ERRE:

The FIFO_ERRE bit enables the generation of an interrupt due to a FIFO error. When FIFO_ERRE is set to logic 1, the interrupt is enabled and the signal INTB will be set to logic 0 whenever FIFO_ERRI is set to logic 1.

Register 0751H: TCFP Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	FIFO_ERRI	0
Bit 14	R	FIFO_UDRI	0
Bit 13	R	XFERI	0
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

XFERI:

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the transmitted cell/packet counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the TCFP counter register locations, or initiating a global performance monitor update by writing to register 0000H. XFERI is set to logic 0 when this register is read.

FIFO_UDRI:

The FIFO_UDRI bit is set high when an attempt is made to read from the FIFO while it is empty. This is considered a system error. This bit is set to logic 0 immediately after a read to this register.

FIFO_ERRI:

This bit is set to one when an error is detected on the read side of the FIFO. This error can be caused by an abnormal sequence of TSOP and TEOP signals or the assertion of FIFO_ERR. This can normally be caused by a previous FIFO overrun or underrun condition or a user asserted error from the POS-PHY L3 interface. This bit is reset immediately after a read to this register.

Register 0752H: TCFP Idle/Unassigned ATM Cell Header

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]:

The PAYLD[7:0] (Idle Cell Payload) value reflects the payload bytes which will be inserted into the ATM Idle cell generated by the TCFP.

CLP:

The CLP (Cell Loss Priority) bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

PTI[2:0]:

The PTI[2:0] (Payload Type) bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

GFC[3:0]:

The GFC[3:0] (Generic Flow Control) bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TCFP detects that no outstanding cells are available from the FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode. The all zeros pattern is transmitted in the VCI and VPI fields of the idle/unassigned cell.

Register 0753H: TCFP Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	DCRC[7]	0
Bit 14	R/W	DCRC[6]	0
Bit 13	R/W	DCRC[5]	0
Bit 12	R/W	DCRC[4]	0
Bit 11	R/W	DCRC[3]	0
Bit 10	R/W	DCRC[2]	0
Bit 9	R/W	DCRC[1]	0
Bit 8	R/W	DCRC[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TX_BYTE_MODE	0
Bit 4	R/W	XOFF	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved:

The Reserved bits should be set to their default values for proper operation.

INVERT:

The data inversion bit (INVERT) configures the ATM or packet processor to logically invert the outgoing data stream. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0.

XOFF:

The XOFF serves as a transmission enable bit. When XOFF is set to logic 0, ATM cells or packets are transmitted normally. When XOFF is set to logic 1, the cell or packet currently being transmitted is completed and then transmission is suspended. When XOFF is set to logic 1, the TCFP will not request data from the FIFO. ATM Idle cells or HDLC flags will be sent on the TCFP egress interface.

TX_BYTE_MODE:

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[39:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS and Abort bytes) before the byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[39:0] will count all bytes in

transmitted packets (including FCS, Abort, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in POS mode.

DCRC[7:0]:

The diagnostic CRC word (DCRC[7:0]) configures the ATM or packet processor to logically invert bits in the inserted CRC on the outgoing data stream for diagnostic purposes. When any bit in DCRC[7:0] is set to logic 1, the corresponding bit in the FCS value inserted by the POS processor or the HCS value inserted by the ATM processor is logically inverted. DCRC[7:0] is ignored when no FCS is inserted. Each DCRC[x] bit will cause a bit error in each byte of the 2 byte or 4 byte FCS.

Register 0754H: TCFP Transmit Cell/Packet Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_CELL[15:0]	XXXX

Register 0755H: TCFP Transmit Cell/Packet Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_CELL[31:16]	XXXX

TX_CELL[31:0]:

The TX_CELL[31:0] bits indicate the number of cells or **non-aborted** packets transmitted to the TCFP egress stream during the last accumulation interval. ATM Idle cells, HDLC flags, and HDLC Abort bytes inserted into the transmission stream are not counted.

A write to any one of the TCFP Transmit Cell/Packet Counter registers loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell/Packet Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

Register 0756H: TCFP Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_BYTE[15:0]	XXXX

Register 0757H: TCFP Transmit Byte Counter

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_BYTE[31:16]	XXXX

Register 0758H: TCFP Transmit Byte Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R	TX_BYTE[39:32]	XX

TX_BYTE[39:0]:

The TX_ BYTE[39:0] bits indicate the number of bytes in packets transmitted to the TCFP egress stream during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes is controlled by the TX_BYTE_MODE register bit. HDLC flags are not counted. The TX_BYTE[39:0] counters are only valid when processing packets.

A write to any one of the TCFP Transmit Byte Counter registers loads the registers with the current counter value and resets the internal 40 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Byte Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

Register 0759H: TCFP Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	TX_ABT[15]	X
Bit 14	R	TX_ABT[14]	X
Bit 13	R	TX_ABT[13]	X
Bit 12	R	TX_ABT[12]	X
Bit 11	R	TX_ABT[11]	X
Bit 10	R	TX_ABT[10]	X
Bit 9	R	TX_ABT[9]	X
Bit 8	R	TX_ABT[8]	X
Bit 7	R	TX_ABT[7]	X
Bit 6	R	TX_ABT[6]	X
Bit 5	R	TX_ABT[5]	X
Bit 4	R	TX_ABT[4]	X
Bit 3	R	TX_ABT[3]	X
Bit 2	R	TX_ABT[2]	X
Bit 1	R	TX_ABT[1]	X
Bit 0	R	TX_ABT[0]	X

TX_ABT[15:0]:

The TX_ ABT[15:0] bits indicate the number aborted packets transmitted to the TCFP egress stream during the last accumulation interval. These counters are only valid when processing packets.

A write to any one of the TCFP Transmit Byte Counter registers loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Byte Counter registers. The counter should be polled regularly to avoid saturating.

To allow for synchronization update with all other blocks, register 0000H can be written to initiate a global performance counter update.

Register 0760H: RXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	RXSDQTIP	X
Bit 0	R/W	SDQRST	1

SDQRST:

This bit is used to reset the RXSDQ. The RXSDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

RXSDQTIP:

The RXSDQTIP bit indicates that the RXSDQ counters are in the process of being transferred to their holding registers. A transfer is initialized by writing to the S/UNI-2488 Identity, and Global Performance Monitor Update register (0000H).

Register 0761H: RXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	EOPE	0
Bit 1	R/W	SOPE	0
Bit 0	R/W	OFLE	0

OFLE:

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

SOPE:

When this bit is set to 1, bad SOP signals cause the INTB output to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

EOPE:

When this bit is set to 1, bad EOP signals cause the INTB output to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

Reserved:

This bit should be set to logic 0 for proper operation.

Register 0763H: RXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	OFLI	X

OFLI:

This bit is set when there is a FIFO overflow condition. This bit is cleared when read by the user.

OFL_FIFO[5:0]:

These bits are used to indicate the FIFO identity. This field should contain the same number as the FIFO_NUMBER [5:0] field in RXSDQ FIFO Indirect Configuration register; otherwise, an system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0764H: RXSDQ FIFO SOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	SOP_FIFO[5]	X
Bit 12	R	SOP_FIFO[4]	X
Bit 11	R	SOP_FIFO[3]	X
Bit 10	R	SOP_FIFO[2]	X
Bit 9	R	SOP_FIFO[1]	X
Bit 8	R	SOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	SOPI	X

SOPI:

This bit is set when two SOPs arrive consecutively on the FIFO without being separated by a EOP. This bit is cleared when read by the user.

SOP_FIFO[5:0]:

These bits are used to indicate the FIFO identity. This field should contain the same number as the FIFO_NUMBER [5:0] field in RXSDQ FIFO Indirect Configuration register; otherwise, an system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0765H: RXSDQ FIFO EOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	EOP_FIFO[5]	X
Bit 12	R	EOP_FIFO[4]	X
Bit 11	R	EOP_FIFO[3]	X
Bit 10	R	EOP_FIFO[2]	X
Bit 9	R	EOP_FIFO[1]	X
Bit 8	R	EOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	EOPI	X

EOPI:

This bit is set when two EOPs arrive consecutively on the FIFO without being separated by a SOP. This bit is cleared when read by the user.

EOP_FIFO[5:0]:

These bits are used to indicate the FIFO identity. This field should contain the same number as the FIFO_NUMBER [5:0] field in RXSDQ FIFO Indirect Configuration register; otherwise, an system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0768H: RXSDQ FIFO Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	0
Bit 12	R	EMPTY	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

This is an indirect register that is used to specify the address of the FIFO that the user is setting up or reading the setup for. A FIFO needs to be configured according to a set of rules defined in the Operations section. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information.

PHYID[5:0]:

This is a 6-bit number that is used to describe the current FIFO being addressed by the rest of the FIFO setup registers – the RXSDQ FIFO Indirect Configuration, RXSDQ FIFO Buffer Available Threshold, RXSDQ FIFO Data Available Threshold and RXSDQ FIFO Cells and Packets Count. This field should be set to all zeros.

EMPTY:

This read-only bit indicates if the requested FIFO is empty. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty.

FLUSH:

This is a write-only bit used to discard all the current data in a specified FIFO. This should typically be used if a non-empty FIFO needs to be reconfigured.

RWB:

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers RXSDQ FIFO Indirect Configuration, RXSDQ FIFO Indirect Buffer Available Threshold, RXSDQ FIFO Indirect Data Available Threshold, and RXSDQ FIFO Indirect Cells and Packets Count. When this bit is set to 0, the user is writing the configuration of a FIFO.

BUSY:

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the information for the FIFO is now available in the accessed register.

Register 0769H: RXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	1
Bit 5		Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

BLOCK_PTR[4:0]:

This is a 5-bit number that is calculated and programmed by the user based on the number of PHYs, the size of each FIFO, and total number of FIFOs required by the system. The rules governing this calculation are in the Operations Section.

FIFO_BS[1:0]:

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the RXSDQ FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY. The values to be programmed are given in the operations section.

FIFO_NUMBER[5:0]:

This is a 6-bit internal FIFO number that is used to associate a given PHY ID with a FIFO. This allows the user to flexibly use the SDQ to map any FIFO of any size to any PHY ID. The values to be programmed are given in the operations section.

POS_SEL:

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs.

ENABLE:

Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but continues to assert Data Available internally until it is drained completely. In order to reconfigure FIFOs during operation, they need to be disabled first.

Register 076AH: RXSDQ FIFO Indirect Data Available Threshold

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register is used to set the Data Available Threshold for a FIFO. This threshold is explained in the Operations Section. A FIFO does not need to be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again.

Reserved:

The Reserved bits should be set to their default values for proper operation.

DT[7:0]:

These bits specify the Data Available threshold for the FIFO selected by the RXSDQ FIFO Indirect Address register's PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO. The absolute maximum value is DT[7:0] +1 = 16. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number should be set to a value of DT[7:0] = 3 (ATM cells are 4 Blocks long).

Register 076BH: RXSDQ FIFO Indirect Cells and Packets Count

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

COUNT[3:0]:

These read-only bits hold the last sampled count for the FIFO requested for in the RXSDQ FIFO Indirect Address register's PHYID[5:0] bits. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over. This register is for internal diagnostics only.

Register 076CH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[15:0]	X

Register 076DH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[31:16]	X

ACOUNT[31:0]:

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the RXSDQ. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it holds the value, and does not roll over.

Register 076EH: RXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]:

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the RXSDQ due to FIFO overflows. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it holds the value, and does not roll over.

Register 0770H: TXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	TXSDQTIP	X
Bit 0	R/W	SDQRST	1

SDQRST:

This bit is used to reset the TXSDQ. The TXSDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

TXSDQTIP:

The TXSDQTIP bit indicates that the TXSDQ counters are in the process of being transferred to their holding registers. A transfer is initialized by writing to the S/UNI-2488 Identity, and Global Performance Monitor Update register (0000H).

Register 0771H: TXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	EOPE	0
Bit 1	R/W	SOPE	0
Bit 0	R/W	OFLE	0

OFLE:

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

SOPE:

When this bit is set to 1, bad SOP signals cause the INTB output to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

EOPE:

When this bit is set to 1, bad EOP signals cause the INTB output to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

Reserved:

This bit should be set to logic 0 for proper operation.

Register 0773H: TXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	OFLI	X

OFLI:

This bit is set when there is a FIFO overflow condition. This bit is cleared when read by the user.

OFL_FIFO[5:0]:

These bits are used to indicate the FIFO identity. This field should contain the same number as the FIFO_NUMBER [5:0] field in TXSDQ FIFO Indirect Configuration register; otherwise, an system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0774H: TXSDQ FIFO SOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	SOP_FIFO[5]	X
Bit 12	R	SOP_FIFO[4]	X
Bit 11	R	SOP_FIFO[3]	X
Bit 10	R	SOP_FIFO[2]	X
Bit 9	R	SOP_FIFO[1]	X
Bit 8	R	SOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	SOPI	X

SOPI:

This bit is set when two SOPs arrive consecutively on the FIFO without being separated by a EOP. This bit is cleared when read by the user.

SOP_FIFO[5:0]:

These bits are used to indicate the FIFO identity. This field should contain the same number as the FIFO_NUMBER [5:0] field in TXSDQ FIFO Indirect Configuration register; otherwise, an system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0775H: TXSDQ FIFO EOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	EOP_FIFO[5]	X
Bit 12	R	EOP_FIFO[4]	X
Bit 11	R	EOP_FIFO[3]	X
Bit 10	R	EOP_FIFO[2]	X
Bit 9	R	EOP_FIFO[1]	X
Bit 8	R	EOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	EOPI	X

EOPI:

This bit is set when two EOPs arrive consecutively on the FIFO without being separated by a SOP. This bit is cleared when read by the user.

EOP_FIFO[5:0]:

These bits are used to indicate the FIFO identity. This field should contain the same number as the FIFO_NUMBER [5:0] field in TXSDQ FIFO Indirect Configuration register; otherwise, an system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0778H: TXSDQ FIFO Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	0
Bit 12	R	EMPTY	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

This is an indirect register that is used to specify the address of the FIFO that the user is setting up or reading the setup for. A FIFO needs to be configured according to a set of rules defined in the Operations section. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information.

PHYID[5:0]:

This is a 6-bit number that is used to describe the current FIFO being addressed by the rest of the FIFO setup registers – the TXSDQ FIFO Indirect Configuration, TXSDQ FIFO Buffer Available Threshold, TXSDQ FIFO Data Available Threshold and TXSDQ FIFO Cells and Packets Count. This field should be set to all zeros.

EMPTY:

This read-only bit indicates if the requested FIFO is empty. When this bit is rad as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty.

FLUSH:

This is a write-only bit used to discard all the current data in a specified FIFO. This should typically be used if a non-empty FIFO needs to be reconfigured.

RWB:

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers RXSDQ FIFO Indirect Configuration, RXSDQ FIFO Indirect Buffer Available Threshold, RXSDQ FIFO Indirect Data Available Threshold, and RXSDQ FIFO Indirect Cells and Packets Count. When this bit is set to 0, the user is writing the configuration of a FIFO.

BUSY:

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the information for the FIFO is now available in the accessed register.

Register 0779H: TXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	1
Bit 5		Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

BLOCK_PTR[4:0]:

This is a 5-bit number that is calculated and programmed by the user based on the number of PHYs, the size of each FIFO, and total number of FIFOs required by the system. The rules governing this calculation are in the Operations Section.

FIFO_BS[1:0]:

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the TXSDQ FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY. The values to be programmed are given in the operations section.

FIFO_NUMBER[5:0]:

This is a 6-bit internal FIFO number that is used to associate a given PHY ID with a FIFO. This allows the user to flexibly use the SDQ to map any FIFO of any size to any PHY ID. The values to be programmed are given in the operations section.

POS_SEL:

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs.

ENABLE:

Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but continues to assert Data Available internally until it is drained completely. In order to reconfigure FIFOs during operation, they need to be disabled first.

Register 077AH: TXSDQ FIFO Indirect Data and Buffer Available Thresholds

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	BT[4]	0
Bit 3	R/W	BT[3]	0
Bit 2	R/W	BT[2]	0
Bit 1	R/W	BT[1]	1
Bit 0	R/W	BT[0]	1

This register is used to set the Data and Buffer Available Thresholds for a FIFO. These thresholds are explained in the Operations Section. A FIFO does not need to be enabled to set this threshold. In order to change a value for a FIFO, the user should first disable it, write in the new value, and enable it again.

BT[4:0]:

These bits specify the Buffer Available threshold for the FIFO specified in PHYID[5:0] bits in the TXSDQ FIFO Indirect Address register. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to BT[4:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is BT[4:0] +1 = 32. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number should be et to a value of BT[4:0] = 3 since ATM cells are 4 bytes in size.

DT[7:0]:

These bits specify the Data Available threshold for the FIFO selected by the TXSDQ FIFO Indirect Address register PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is DT[7:0] +1 = 192. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number should be set to a value of DT[7:0] = 3 (ATM cells are 4 Blocks long).

The DT[7:0] threshold sets the level at which the cell/packet processors (TCFP) blocks can begin transmission of a cell or packet. Once transmission of a cell or packet begins, it cannot be stopped so this threshold should be set to a value which guarantees that the Utopia/POS-PHY interface can write to the FIFO in due time to prevent FIFO underruns. For packet data, it is recommended that DT[7:0] be set to a larger value about equal to 1/2 or 2/3 the size of the FIFO.

Register 077BH: TXSDQ FIFO Indirect Cells and Packets Count

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

COUNT[3:0]:

These read-only bits hold the last sampled count for the FIFO requested for in TXSDQ FIFO Indirect Address register PHYID[5:0] bits. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it rolls over. This register is for internal diagnostics only.

Register 077CH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[15:0]	X

Register 077DH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[31:16]	X

ACOUNT[31:0]:

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the TXSDQ. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it holds the value, and does not roll over.

Register 077EH: TXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]:

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the TXSDQ due to FIFO overflows. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches it's maximum count, it holds the value, and does not roll over.

Register 0780H: RXPHY Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	RXPRST	1

RXPRST:

The RXPRST bit is used to reset the RXPHY circuitry. When RXPRST is set to logic zero, the RXPHY operates normally. When RXPRST is set to logic one, the RXPHY ignores all pin inputs but the register bits may be accessed for purposes of initialization. The RXPHY deasserts all outputs until a logic zero is written to RXPRST.

ODDPARITY:

The ODDPARITY bit is used to set the type of parity that is generated by the RXPHY for the UL3 or POS L3 interface. When set to logic 1, odd parity is generated. When set to logic 0, even parity is generated.

Reserved:

The Reserved bits must be set to logic 0 for proper operation.

Register 0781H: RXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

In UTOPIA, the RENB was detected as being deasserted before appropriate time at end of the cell transfer. The cell will continue to be transferred as per the Utopia Level 3 specification, but this indicates that there may be a configuration mismatch between the RXPHY and the downstream device. A possible cause is the incorrect setting of the size of the cell expected by this interface. The RUNTCELLI bit is cleared when it is read.

Register 0782H: RXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RUNTCELLE	0

RUNTCELLE

The RUNTCELLE bit is used to enable RUNTCELLI signal to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Register 0783H: RXPHY Indirect Burst Size

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CONFIG_RWB	0
Bit 13	R/W	PHY_ADDR[5]	0
Bit 12	R/W	PHY_ADDR[4]	0
Bit 11	R/W	PHY_ADDR[3]	0
Bit 10	R/W	PHY_ADDR[2]	0
Bit 9	R/W	PHY_ADDR[1]	0
Bit 8	R/W	PHY_ADDR[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	BURST_SIZE[3]	0
Bit 2	R/W	BURST_SIZE[2]	0
Bit 1	R/W	BURST_SIZE[1]	1
Bit 0	R/W	BURST_SIZE[0]	1

The RXPHY Indirect Burst Size register is an indirect address and data register. The register is used only in POS mode of operation.

BURST_SIZE[3:0]

The BURST_SIZE data register is provided to program the allowable burst size for the PHY. The size of a burst is BURST_SIZE + 1. For example, a BURST_SIZE[3:0] = “0000” indicates a burst size of one block. A block is equal to 16 bytes and takes 4 clocks to transfer. The 4 bits of Burst Size allow the maximum burst to be 16 blocks (256 bytes), per PHY. This register is used only in POS-PHY L3 mode.

PHY_ADDR[5:0]

The PHY_ADDR bits are an indirect address that is used with BURST_SIZE data. The two allow indirect address reads and writes using a small amount of external address space. The PHY_ADDR is used with CONFIG_RWB and BUSY to command reads and writes. Valid values for PHY_ADDR[5:0] are from 0 to 2FH. For the S/UNI-2488, PHY_ADDR[5:0] must be set to zero.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of ‘1’ means that a read is to be performed on the data

for PHY_ADDR and will be placed in the BURST_SIZE register. A value of '0' means that a write of the information in BURST_SIZE will be performed for PHY channel address PHY_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0784H: RXPHY Calendar Length

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	CALENDAR_LENGTH[6]	0
Bit 5	R/W	CALENDAR_LENGTH[5]	0
Bit 4	R/W	CALENDAR_LENGTH[4]	0
Bit 3	R/W	CALENDAR_LENGTH[3]	0
Bit 2	R/W	CALENDAR_LENGTH[2]	0
Bit 1	R/W	CALENDAR_LENGTH[1]	0
Bit 0	R/W	CALENDAR_LENGTH[0]	0

CALENDAR_LENGTH[6:0]

The CALENDAR_LENGTH register is provided to program the length of calendar used for servicing up to a maximum of 128 entries. Please see the RXPHY Calendar Indirect Address Data register. The number of entries is equal to CALENDAR_LENGTH + 1. For the S/UNI-2488, this register should be set to all zeros.

Register 0785H: RXPHY Calendar Indirect Address Data

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CALENDAR_ADDR[6]	0
Bit 13	R/W	CALENDAR_ADDR[5]	0
Bit 12	R/W	CALENDAR_ADDR[4]	0
Bit 11	R/W	CALENDAR_ADDR[3]	0
Bit 10	R/W	CALENDAR_ADDR[2]	0
Bit 9	R/W	CALENDAR_ADDR[1]	0
Bit 8	R/W	CALENDAR_ADDR[0]	0
Bit 7	R/W	CONFIG_RWB	0
Bit 6		Unused	X
Bit 5	R/W	CALENDAR_DATA[5]	0
Bit 4	R/W	CALENDAR_DATA[4]	0
Bit 3	R/W	CALENDAR_DATA[3]	0
Bit 2	R/W	CALENDAR_DATA[2]	0
Bit 1	R/W	CALENDAR_DATA[1]	0
Bit 0	R/W	CALENDAR_DATA[0]	0

The RXPHY Calendar Indirect Address Data register is an indirect address and data register. The register is used in POS mode of operation

CALENDAR_DATA[5:0]

The CALENDAR_DATA register is provided to program the PHY address number to be serviced in the calendar sequence. The calendar consists of a maximum of 128 entries where the CALENDAR_ADDR is used to access one of the 128 (or less) entries to either write or read CALENDAR_DATA. CALENDAR_DATA is the PHY address to be serviced during the sequence associated with CALENDAR_ADDR. The length of the calendar is set in the RXPHY Calendar Length register. For the S/UNI-2488, this register should be set to all zeros.

CALENDAR_ADDR[6:0]

The CALENDAR_ADDR register is an indirect address register that is used with CALENDAR_DATA register. The two registers together allow indirect address reads and writes using a small amount of external address space. The CALENDAR_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data at CALENDAR_ADDR and will be placed in the CALENDAR_DATA register. A value of '0' means that a write of the information in CALENDAR_DATA will be performed at address CALENDAR_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0786H: RXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	POS_FIELD[7]	0
Bit 14	R/W	POS_FIELD[6]	0
Bit 13	R/W	POS_FIELD[5]	0
Bit 12	R/W	POS_FIELD[4]	0
Bit 11	R/W	POS_FIELD[3]	0
Bit 10	R/W	POS_FIELD[2]	0
Bit 9	R/W	POS_FIELD[1]	0
Bit 8	R/W	POS_FIELD[0]	1
Bit 7	R/W	ATM_FIELD[7]	0
Bit 6	R/W	ATM_FIELD[6]	0
Bit 5	R/W	ATM_FIELD[5]	0
Bit 4	R/W	ATM_FIELD[4]	0
Bit 3	R/W	ATM_FIELD[3]	0
Bit 2	R/W	ATM_FIELD[2]	0
Bit 1	R/W	ATM_FIELD[1]	0
Bit 0	R/W	ATM_FIELD[0]	0

The RXPHY Data Type Field register is used in POS-PHY L3 mode of operation only and is provided as a means to identify the type of traffic, ATM or packet, being sent over the POS-PHY L3 interface. Selection of ATM and packet PHYs is done using the POS_SEL bits in the RXSDQ FIFO Indirect Configuration register.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cell transfers over the POS-PHY L3 interface. When the outgoing data is an ATM cell, then the ATM_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (ie. when RSX is logic 1).

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data transfers over the POS-PHY L3 interface. When the outgoing data is of type packet, then the POS_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (ie. when RSX is logic 1).

Register 0788H: TXPHY Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6	R/W	INBANDADDR	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PARERREN	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	TXPRST	1

TXPRST:

The TXPRST bit is used to reset the TXPHY circuitry. When TXPRST is set to logic zero, the TXPHY operates normally. When TXPRST is set to logic one, the TXPHY ignores all pin inputs but the registers may be accessed for purposes of initialization. The TXPHY deasserts all outputs until a logic zero is written to TXPRST.

ODDPARITY:

The ODDPARITY bit is used to set the type of parity that is checked by the TXPHY. When set to logic 1, odd parity is expected. When set to logic 0, even parity is expected. This bit is global and affects all PHY channels.

PARERREN:

When set to logic 1, PARERREN will enable the TXPHY to pass an error signal to the TXSDQ upon detection of a parity error. This will cause the packet to be aborted by the cell processor. This bit has no effect on ATM cells with parity errors.

INBANDADDR

The INBANDADDR bit is used only in POS-PHY L3 mode to indicate whether the in-band address is expected on the interface. This bit is useful in single PHY applications where the in-band addressing is optional (address 0 is assumed) and the Link Layer device does not

send an address in band since there is only one PHY. This bit can only be changed when TXPRST is logic 1.

Reserved:

The Reserved bits must be set to logic 0 for proper operation.

Register 0789H: TXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TDTFERRI	X
Bit 1	R	TPARERRI	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

The RUNTCELLI bit indicates that TENB was detected as being deasserted before the end of the cell transfer when operating in Utopia L3 mode. This will result in a partial cell transfer and an erred cell will passed to the TXSDQ. Possible causes are incorrect setting in the size of the cell expected by this interface. The RUNTCELLI bit is cleared when this register is read.

TPARERRI

The TPARERR bit is used to indicate that a Parity Error was observed on the incoming TDAT bus since the last time the interrupt was read. The packet will be marked erred and sent on to the TXSDQ. ATM cell transmission is not affected by parity errors. The TPARERRI bit is cleared when this register is read.

TDTFERRI

The TDTFERR bit is used to indicate that a Data Field mismatch was observed on the incoming TDAT[31:24] bus compared to the ATM/packet selection for that PHY configuration (selection done using the POS_SEL bits in the TXSDQ FIFO Indirect Configuration register). This bit is cleared on microprocessor read.

Register 078AH: TXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	TDTFERRE	X
Bit 1	R/W	TPARERRE	X
Bit 0	R/W	RUNTCELLE	X

RUNTCELLE

The RUNTCELLE bit is used to enable the detection of the runt cell condition (RUNTCELLI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

TPARERRE

The TPARERRE bit is used to enable the detection of a parity error (TPARERRI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

TDTFERRE

The TDTFERRE bit is used to enable the TDFTERRI interrupt status bit to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Register 078BH: TXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	POS_FIELD[7]	0
Bit 14	R/W	POS_FIELD[6]	0
Bit 13	R/W	POS_FIELD[5]	0
Bit 12	R/W	POS_FIELD[4]	0
Bit 11	R/W	POS_FIELD[3]	0
Bit 10	R/W	POS_FIELD[2]	0
Bit 9	R/W	POS_FIELD[1]	0
Bit 8	R/W	POS_FIELD[0]	1
Bit 7	R/W	ATM_FIELD[7]	0
Bit 6	R/W	ATM_FIELD[6]	0
Bit 5	R/W	ATM_FIELD[5]	0
Bit 4	R/W	ATM_FIELD[4]	0
Bit 3	R/W	ATM_FIELD[3]	0
Bit 2	R/W	ATM_FIELD[2]	0
Bit 1	R/W	ATM_FIELD[1]	0
Bit 0	R/W	ATM_FIELD[0]	0

The TXPHY Data Type Field is used in POS-PHY L3 mode of operation only and is provided as a means to identify the type of traffic, ATM or packet, being sent over the POS-PHY L3 interface. Selection of ATM and packet PHYs is done using the POS_SEL bit in the TXSDQ FIFO Indirect Configuration register.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify an ATM cell being transferred over the POS-PHY L3 interface. When the incoming data is of type ATM cell, then the value of TDAT[31:24] at the cycle in which the in-band address is inserted on TDAT[5:0] (ie. when TSX = 1) should match ATM_FIELD[7:0]. Otherwise, an interrupt is signaled to indicate a data type mismatch.

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data being transferred over the POS-PHY L3 interface. When the incoming data is of type packet, then the value of TDAT[31:24] at the cycle in which the in-band address is inserted on TDAT[5:0] (ie. When TSX = 1) should match POS_FIELD[7:0]. Otherwise, an interrupt is signaled to indicate a data type mismatch.

Register 0790H: SIRP Configuration Timeslot

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	TSx_RDI[1]	0
Bit 10	R/W	TSx_RDI[0]	0
Bit 9	R/W	TSx_REI[3]	0
Bit 8	R/W	TSx_REI[2]	0
Bit 7	R/W	TSx_REI[1]	0
Bit 6	R/W	TSx_REI[0]	0
Bit 5	R/W	Tsx_FORCE_LCD	0
Bit 4	R/W	TSx_RDI20F	0
Bit 3	R/W	TSx_ERDI	0
Bit 2	R/W	TSx_RMODE[1]	1
Bit 1	R/W	TSx_RMODE[0]	1
Bit 0	R/W	TSx_PROV	0

TSx_PROV:

When TSx_PROV is logic 0, automatic remote alarm reporting is disabled for the APS In bus into the THPP. When TSx_PROV is logic 1, automatic remote alarm reporting is enabled for the APS In data stream to the THPP.

TSx_RMODE[1:0]:

The TSx_RMODE[1:0] bits identify the mode of reporting STS Path Remote Defect Indications (RDI) as shown in Table 13.

Table 13: SIRP RDI and REI Reporting Modes

TSx_RMODE[1:0]	Error Reporting Mode
00	**Register Mode:** Source REI[3:0] and RDI[1:0] from internal registers TSx_REI[3:0] and TSx_RDI[1:0] respectively. The remote alarm port and LCD indications (which map to a specified 2 bit programmable RDI code) are ignored.
01	**Remote Alarm Input Only Mode:** Source REI[3:0] and RDI[1:0] entirely from the APS In bus.
10	**Remote Alarm Input with Loss of ATM Cell Delineation Input Mode:** Source REI[3:0] from the APS In bus and RDI[1:0] from LCD indications with a specified 2 bit RDI code.
11	**Normal Error Reporting Mode:** Source REI[3:0] from the APS In bus. LCD indications with a specified 2-bit RDI code is compared to incoming RDI[1:0] from the APS In bus. Higher priority RDI takes precedence.

TSx_ERDI:

The TSx_ERDI bit selects between normal and extended RDI encoding. When TSx_ERDI is set high, extended RDI is selected. The RDI output is treated as a 2-bit codepoint. When TSx_ERDI is set low, normal RDI is selected. These selections are summarized in Table 14.

Table 14: SIRP RDI Settings

	TS*x*_RDI[1:0]	ERDI Interpretation
TSx_ERDI = 1	00	No RDI-P defect
	01	ERDI-P payload defect
	10	ERDI-P server defect
	11	ERDI-P connectivity defect
TSx_ERDI = 0	00	No RDI-P defect
	01	No RDI-P defect
	10	RDI-P defect
	11	RDI-P defect

TSx_RDI20F:

The TSx_RDI20F bits specify the configuration of RDI maintenance duration. The standard required duration is 10 frames. The GR-253 objective duration is 20 frames. The two options are specified by the TSx_RDI20F bit are selected as shown in Table 15.

Table 15: SIRP RDI Maintenance

TS*x*_RDI20F	Configuration
0	A particular RDI value for will be maintained for the required 10 frames before changing to a lower priority RDI code.
1	A particular RDI value for will be maintained for the GR-253 objective 20 frames before changing to a lower priority RDI code.

TSx_FORCE_LCD:

The TSx_FORCE_LCD bit is used to force a Loss of ATM Cell Delineation (LCD) event. A logic OR operation is performed on the LCD indication and the TSx_FORCE_LCD bit. When TSx_FORCE_LCD is set high, an LCD event is assumed and RDI[1:0] is sourced entirely from a specified 2 bit RDI code (LCD[1:0]). The TSx_FORCE_LCD bit is ignored when TSx_RMODE[1:0] = b'00 and b'01.

TSx_REI[3:0]:

The TSx_REI[3:0] bits are used to manually transmit an STS path Remote Error Indication (REI) when both TSx_RMODE[1:0] register bits are set low. If TSx_REI[3:0] is 0, far end block errors are automatically reported to the transmit data stream (if TSx_PROV = 1). If TSx_REI[3:0] is set to a value other than 0, then that value will be transmitted at the next opportunity. After the transmission is completed, TSx_REI[3:0] is reset to the value 0.

TSx_RDI[1:0]:

The TSx_RDI[1:0] bits control the value of the RDI output of the data stream selected when both TSx_RMODE[1:0] register bits are set low. When extended RDI is enabled (TSx_ERDI set high), the RDI output is controlled directly by TSx_RDI [1:0] register bits when either register bit is set high. The RDI output reflects the remote alarm status (if TSx_PROV = 1) when both TSx_RDI[1:0] register bits are set low. When extended RDI is disabled (TSx_ERDI set low), and the RDI[0] register bit is set high, the RDI output is forced high regardless of the remote alarm status. When RDI[0] is set low, the RDI output reflects the remote alarm status. When both TSx_RMODE[1:0] register bits are not set low, the TSx_RDI[1:0] bits are ignored.

Register 079CH: SIRP Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RDIPRIHI[1]	0
Bit 4	R/W	RDIPRIHI[0]	0
Bit 3	R/W	RDIPRIMID[1]	0
Bit 2	R/W	RDIPRIMID[0]	0
Bit 1	R/W	LCD[1]	1
Bit 0	R/W	LCD[0]	0

LCD[1:0]:

The LCD[1:0] bits represent the 2 bit programmable RDI code generated when a Loss of ATM Cell Delineation (LCD) event is detected.

RDIPRIMID[1:0]

The RDIPRIMID[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the second highest priority code. These bits combined with the RDIPRIHI bits allow almost any priority scheme to be specified. The bits are interpreted as shown in RDIPRIHI[1:0]
The RDIPRIHI[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the highest priority code. High priority codes will replace low priority codes at the next transmit G1 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed.
Table 16.

RDIPRIHI[1:0]

The RDIPRIHI[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the highest priority code. High priority codes will replace low priority codes at the next transmit G1 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed.

Table 16: SIRP RDI Priority Schemes

RDIPRIHI[1:0]	RDIPRIMID[1:0]	Priority of Codes (3 = highest)	
		Code	Priority
11	01	11	3
		01	2
		10	1
		00	0
11	10	11	3
		10	2
		01	1
		00	0
10	11	10	3
		11	2
		01	1
		00	0
10	01	10	3
		01	2
		11	1
		00	0
01	11	01	3
		11	2
		10	1
		00	0
01	10	01	3
		10	2
		11	1
		00	0
00	00	11	1
		10	1
		01	1
		00	0
Other codes	other codes	Reserved	

Note: When RDIPRIHI[1:0] and RDIPRIMID[1:0] are both equal to b'00, all RDI codes have equal priority except RDI[1:0] = b'00 which always has lowest priority.

Register 0800H: PRGM Indirect Address

Register 0810H: PRGM Aux 2 Indirect Address

Register 0820H: PRGM Aux 3 Indirect Address

Register 0830H: PRGM Aux 4 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]:

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. For the S/UNI-2488, PATH[3:0] should be set to 1H.

IADDR[3:0]:

The internal address bits select which internal register is accessed by the current indirect transfer. Six registers are defined for the monitor while four pages are defined for the generator.

IADDR[3:0]	Register
0000	Monitor - Timeslot Configuration page
0001	Monitor - PRBS[22:7] page
0010	Monitor - PRBS[6:0] page
0011	Monitor - B1/E1 value page

0100	Monitor - Monitor error count page
0101	Monitor - Received B1 and E1
1000	Generator - Timeslot Configuration page
1001	Generator - PRBS[22:7] page
1010	Generator - PRBS[6:0] page
1011	Generator - B1/E1 value page

RWB:

The active high read and active low write (RWB) bit selects if the current access to the internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal register. When RWB is set to logic 1, an indirect read access to the register is initiated. The data from the addressed location in the internal register will be transfer to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the register is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal register.

BUSY:

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0801H: PRGM Indirect Data

Register 0811H: PRGM Aux 2 Indirect Data

Register 0821H: PRGM Aux 3 Indirect Data

Register 0831H: PRGM Aux 4 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]:

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an internal register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal register will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfered to the addressed location in the internal register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which internal register is being accessed.

Register 0802H: PRGM Generator Payload Configuration

Register 0812H: PRGM Aux 2 Generator Payload Configuration

Register 0822H: PRGM Aux 3 Generator Payload Configuration

Register 0832H: PRGM Aux 4 Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	GEN_MSSLEN[2]	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

GEN_MSSLEN[2:0], GEN_STS12C, GEN_STS12CSL:

These bits control the operating mode of the PRGM generators. The bits should be set according to the table below.

PRGM	GEN_STS12C	GEN_STS12CSL	GEN_MSSLEN[2:0]
Master	1	0	011
Aux2 Aux3 Aux4	1	1	011

Register 0803H: PRGM Monitor Payload Configuration register

Register 0813H: PRGM Aux 2 Monitor Payload Configuration

Register 0823H: PRGM Aux 3 Monitor Payload Configuration

Register 0833H: PRGM Aux 4 Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	MON_MSSLEN[2]	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

MON_MSSLEN[2:0], MON_STS12C, MON_STS12CSL:

These bits control the operating mode of the PRGM monitors. The bits should be set according to the table below.

PRGM	MON_STS12C	MON_STS12CSL	MON_MSSLEN[2:0]
Master	1	0	011
Aux2 Aux3 Aux4	1	1	011

Register 0804H: PRGM Monitor Byte Error Interrupt Status

Register 0814H: PRGM Aux 2 Monitor Byte Error Interrupt Status

Register 0824H: PRGM Aux 3 Monitor Byte Error Interrupt Status

Register 0834H: PRGM Aux 4 Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON[N+12]_ERRI	X
Bit 10	R	MON[N+11]_ERRI	X
Bit 9	R	MON[N+10]_ERRI	X
Bit 8	R	MON[N+9]_ERRI	X
Bit 7	R	MON[N+8]_ERRI	X
Bit 6	R	MON[N+7]_ERRI	X
Bit 5	R	MON[N+6]_ERRI	X
Bit 4	R	MON[N+5]_ERRI	X
Bit 3	R	MON[N+4]_ERRI	X
Bit 2	R	MON[N+3]_ERRI	X
Bit 1	R	MON[N+2]_ERRI	X
Bit 0	R	MON[N+1]_ERRI	X

MON**x**_ERRI:

The Monitor Byte Error Interrupt Status registers contain the status of the interrupt generated by each of the 48 STS-1 paths when an error has been detected.

PRGM Monitor Byte Error Interrupt Status register, N = 0.
PRGM Aux2 Monitor Byte Error Interrupt Status register, N = 1.
PRGM Aux3 Monitor Byte Error Interrupt Status register, N = 2.
PRGM Aux4 Monitor Byte Error Interrupt Status register, N = 3.

The MON**x**_ERRI bit is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE, and is cleared after it's been read.

Register 0805H: PRGM Monitor Byte Error Interrupt Enable

Register 0815H: PRGM Aux 2 Monitor Byte Error Interrupt Enable

Register 0825H: PRGM Aux 3 Monitor Byte Error Interrupt Enable

Register 0835H: PRGM Aux 4 Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON[N+12]_ERRE	0
Bit 10	R/W	MON[N+11]_ERRE	0
Bit 9	R/W	MON[N+10]_ERRE	0
Bit 8	R/W	MON[N+9]_ERRE	0
Bit 7	R/W	MON[N+8]_ERRE	0
Bit 6	R/W	MON[N+7]_ERRE	0
Bit 5	R/W	MON[N+6]_ERRE	0
Bit 4	R/W	MON[N+5]_ERRE	0
Bit 3	R/W	MON[N+4]_ERRE	0
Bit 2	R/W	MON[N+3]_ERRE	0
Bit 1	R/W	MON[N+2]_ERRE	0
Bit 0	R/W	MON[N+1]_ERRE	0

MON**x**_ERRE:

The Monitor Byte Error Interrupt Enable registers enable the interrupt for each of the 48 STS-1 paths.

PRGM Monitor Byte Error Interrupt Enable register, N = 0.
PRGM Aux2 Monitor Byte Error Interrupt Enable register, N = 1.
PRGM Aux3 Monitor Byte Error Interrupt Enable register, N = 2.
PRGM Aux4 Monitor Byte Error Interrupt Enable register, N = 3.

When MON**x**_ERRE is set high, the Byte Error Interrupt is allowed to generate an interrupt on INTB.

Register 0806H: Monitor B1/E1 Bytes Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	MON1_B1E1I	X

MON1_B1E1I:

The MON1_B1E1I bit indicates the status of the interrupt generated when a change in the status of the comparison has been detected on the B1/E1 bytes. The MON1_B1E1I is set high when the monitor is in the synchronized state and when the status change is detected on either the B1 or E1 bytes. For example, if a mismatch is detected and the previous comparison was a match, the MON1_B1E1I bit will be set high. But if a mismatch is detected and the previous comparison was a mismatch, the MON1_B1E1I bit will keep its previous value. This bit is independent of MON1_B1E1E, and is cleared after it's been read.

Register 0807H: Monitor B1/E1 Bytes Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON1_ B1E1E	0

MON1_B1E1E:

When MON1_B1E1E is set high, the B1/E1Bytes Interrupt (MON1_B1E1I) is allowed to generate an interrupt on INTB.

Register 0808H: Monitor B1/E1 Bytes Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	MON1_ B1E1V	X

MON1_B1E1V:

The Monitor B1/E1 Bytes Status value bit reflects the status of the previous B1/E1 comparison. When MON1_B1E1V is set high, an error on the previous B1 or E1 bytes has been detected. When MON1_B1E1V is low, the received B1 and E1 bytes were the expected ones.

Register 0809H: PRGM Monitor Synchronization Interrupt Status

Register 0819H: PRGM Aux 2 Monitor Synchronization Interrupt Status

Register 0829H: PRGM Aux 3 Monitor Synchronization Interrupt Status

Register 0839H: PRGM Aux 4 Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON[N+12]_SYNCI	X
Bit 10	R	MON[N+11]_SYNCI	X
Bit 9	R	MON[N+10]_SYNCI	X
Bit 8	R	MON[N+9]_SYNCI	X
Bit 7	R	MON[N+8]_SYNCI	X
Bit 6	R	MON[N+7]_SYNCI	X
Bit 5	R	MON[N+6]_SYNCI	X
Bit 4	R	MON[N+5]_SYNCI	X
Bit 3	R	MON[N+4]_SYNCI	X
Bit 2	R	MON[N+3]_SYNCI	X
Bit 1	R	MON[N+2]_SYNCI	X
Bit 0	R	MON[N+1]_SYNCI	X

MON**x**_SYNCI:

The Monitor Synchronization Interrupt Status registers indicate synchronization interrupts for each of the 48 STS-1 paths.

PRGM Monitor Synchronization Interrupt Status register, N = 0.
PRGM Aux2 Monitor Synchronization Interrupt Status register, N = 1.
PRGM Aux3 Monitor Synchronization Interrupt Status register, N = 2.
PRGM Aux4 Monitor Synchronization Interrupt Status register, N = 3.

The Monitor Synchronization Interrupt Status Interrupt (MON**x**_SYNCI) bit is set high when a change occures in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE, and is cleared after it's been read.

Register 080AH: PRGM Monitor Synchronization Interrupt Enable

Register 081AH: PRGM Aux 2 Monitor Synchronization Interrupt Enable

Register 082AH: PRGM Aux 3 Monitor Synchronization Interrupt Enable

Register 083AH: PRGM Aux 4 Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON[N+12]_SYNCE	0
Bit 10	R/W	MON[N+11]_SYNCE	0
Bit 9	R/W	MON[N+10]_SYNCE	0
Bit 8	R/W	MON[N+9]_SYNCE	0
Bit 7	R/W	MON[N+8]_SYNCE	0
Bit 6	R/W	MON[N+7]_SYNCE	0
Bit 5	R/W	MON[N+6]_SYNCE	0
Bit 4	R/W	MON[N+5]_SYNCE	0
Bit 3	R/W	MON[N+4]_SYNCE	0
Bit 2	R/W	MON[N+3]_SYNCE	0
Bit 1	R/W	MON[N+2]_SYNCE	0
Bit 0	R/W	MON[N+1]_SYNCE	0

MON**x**_SYNCE:

The Monitor Synchronization Interrupt Enable registers enables the synchronization interrupts for each of the 48 STS-1 paths.

PRGM Monitor Synchronization Interrupt Enable register, N = 0.
PRGM Aux2 Monitor Synchronization Interrupt Enable register, N = 1.
PRGM Aux3 Monitor Synchronization Interrupt Enable register, N = 2.
PRGM Aux4 Monitor Synchronization Interrupt Enable register, N = 3.

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INTB. When MON**x**_SYNCE is set high, a change in the synchronization state of the monitor in STS-1 path **x** generates an interrupt on INTB.

Register 080BH: PRGM Monitor Synchronization Status

Register 081BH: PRGM Aux 2 Monitor Synchronization Status

Register 082BH: PRGM Aux 3 Monitor Synchronization Status

Register 083BH: PRGM Aux 4 Monitor Synchronization Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON[N+12]_SYNCV	X
Bit 10	R	MON[N+11]_SYNCV	X
Bit 9	R	MON[N+10]_SYNCV	X
Bit 8	R	MON[N+9]_SYNCV	X
Bit 7	R	MON[N+8]_SYNCV	X
Bit 6	R	MON[N+7]_SYNCV	X
Bit 5	R	MON[N+6]_SYNCV	X
Bit 4	R	MON[N+5]_SYNCV	X
Bit 3	R	MON[N+4]_SYNCV	X
Bit 2	R	MON[N+3]_SYNCV	X
Bit 1	R	MON[N+2]_SYNCV	X
Bit 0	R	MON[N+1]_SYNCV	X

MON**x**_SYNCV:

The Monitor Synchronization Status registers reflects the synchronization state of each STS-1 path.

PRGM Monitor Synchronization Status register, N = 0.
PRGM Aux2 Monitor Synchronization Status register, N = 1.
PRGM Aux3 Monitor Synchronization Status register, N = 2.
PRGM Aux4 Monitor Synchronization Status register, N = 3.

The Monitor Synchronization Status registers reflect the state of the monitor's state machine. When MON**x**_SYNCV is set high, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low, the monitor is out of sync for the STS-1 Path **x**.

Indirect Register 0800H: PRGM Monitor Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

MON_ENA:

Monitor Enable register bit enables the PRBS monitors for the PRGM blocks (all 48). If MON_ENA is set high, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

INV_PRBS:

Sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted else they will be compared unmodified.

RESYNC:

Sets the monitor to re-initialize the PRBS sequence. When set high, the monitor's state machines will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. To force another resynchronization, the bit needs to be set low again before it is set high..

B1E1_ENA:

When high, this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to

the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are monitored.

SEQ_PRBSB:

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload is expected to contain PRBS bytes. When high, the payload is expected to contain a sequential pattern.

Reserved:

The Reserved bit should be set to logic 0 for proper operation.

Indirect Register 0801H: PRGM Monitor PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PRBS[22:7]	0000

Indirect Register 0802H: PRGM Monitor PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 7		Unused	00
Bit 6 to Bit 0	R/W	PRBS[6:0]	00

PRBS[22:0]:

The PRBS[22:0] register contians the state of the LFSR monitor. It is possible to write in this register to change the initial state of the monitor.

Indirect Register 0803H: PRGM Monitor B1/E1 Value Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This indirect register is not valid for PRGM Aux2, Aux3, Aux4.

B1[7:0]:

When enabled, the monitoring of the B1byte in the incoming SONET/SDH frame is a simple comparison to the value in the PRGM Monitor B1/E1 Value Page register. The same value is used for the monitoring of the E1 byte except its complement is used.

Indirect Register 0804H: PRGM Monitor Error Count Page

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

ERR_CNT[15:0]:

The ERR_CNT[15:0] register is the number of error in the PRBS bytes detected during the monitoring. Errors are accumulated only when the monitor is in the synchonized state. Even if there are multiple errors within one PRBS byte, only one error is counted. The transfer of the error counter to this holding register is trigger by an indirect write to this register or writing register 0000H for a global performance monitor update. The error counter will not wrap around after reaching FFFFH. It will saturate to this value.

Indirect Register 0805H: PRGM Monitor Received B1/E1 Bytes Page

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

This indirect register is not valid for PRGM Aux2, Aux3, Aux4.

REC_B1[7:0]:

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame. Every time a B1 byte is received, it is copied in this register.

REC_E1[7:0]:

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame. Every time a E1 byte is received, it is copied in this register.

Indirect Register 0808H: PRGM Generator Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	PRBS_ENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	S[1]	0
Bit 6	R/W	S[0]	0
Bit 5	R/W	PRBS_SEQB	1
Bit 4	R/W	B1E1_ENA	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	X
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

INV_PRBS:

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted; else they will be inserted unmodified.

FORCE_ERR:

The Force Error bit is used to force bit errors in the inserted pattern. When set high, the MSB of the next byte will be inverted, inducing a single bit error. The register will clear itself when the operation is complete. A read operation will always result in a logic ‘0’.

B1E1_ENA:

This bit enables the replacement of the B1 byte in the SONET/SDH frame, by a programmable value. The E1 byte is replaced by the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are replaced in the frame; otherwise they go through the PRGM unaltered.

PRBS_SEQB:

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When high, the payload is filled with PRBS bytes. When low, a sequential pattern is inserted.

S[1:0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions in the payload pointer.

Reserved:

The Reserved bit should be set to logic 0 for proper operation.

PRBS_ENA:

This bit specifies if PRBS overwriting is enabled. If PRBS_ENA is high, PRBS patterns are generated and are used to overwrite the data stream; else no pattern is generated and the data stream is not overwritten.

Reserved:

The Reserved bit should be programmed to logic 0 for proper operation.

Indirect Register 0809H : PRGM Generator PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PRBS[22:7]	0000

Indirect Register 080AH: PRGM Generator PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 7		Unused	00
Bit 6 to Bit 0	R/W	PRBS[6:0]	00

PRBS[22:0]:

The PRBS[22:0] register contians the state of the LFSR generator. It is possible to write in this register to change the initial state of the monitor.

Indirect Register 080BH: PRGM Generator B1/E1 Value Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This indirect register is not valid for PRGM Aux2, Aux3, Aux4.

B1[7:0]:

When enabled, the value in this register is inserted in the B1byte position of the outgoing SONET/SDH frame. The complement of this value is also inserted at the E1 byte position.

Register 0840H: R8TD APS1 Control and Status

Register 0848H: R8TD APS2 Control and Status

Register 0850H: R8TD APS3 Control and Status

Register 0858H: R8TD APS4 Control and Status

Bit	Type	Function	Default
Bit 15	R/W	DLBEN	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	PININV	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	W	FOFA	X
Bit 0	W	FOCA	X

FOCA:

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment circuit on a serial link. A transition from logic zero to logic one in this bit forces the receiver to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA:

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment circuit. A transition from logic zero to logic one in this bit forces the receiver to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV:

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment circuit. OCAV is set high when the receiver is in the out-of-character-alignment state. OCAV is set low when the receiver is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment circuit. OFAV is set high when the receiver is in the out-of-frame-alignment state. OFAV is set low when the receiver is in the in-frame-alignment state.

OCAE:

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment circuit changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE:

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUEO is set low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set high to force high-order AIS signals in the R8TD egress data stream if the R8TD is in the out-of-frame-alignment state. The R8TD egress data stream is left unaffected in the out-of-frame alignment state when the OFFAIS is set low.

PININV

The parallel incoming data invert bit (PININV) controls the active polarity of the incoming data stream. When PININV is set high, the incoming data stream is complemented before further processing by the R8TD. When PININV is set low, the incoming data stream is not complemented.

DLBEN:

The diagnostic loopback enable bit (DLBEN) controls diagnostic loopback operation. When DLBEN is set high, serial TeleCombus diagnostic loopback is enabled. When DLBEN is set low, serial TeleCombus diagnostic loopback is disabled. The loopback involves the complementary R8TD and T8TE blocks. For example, the T8TE which sources APSO[1] will be diagnostically looped back to the R8TD which sinks APSI[1].

Register 0841H: R8TD APS1 Interrupt Status

Register 0849H: R8TD APS2 Interrupt Status

Register 0851H: R8TD APS3 Interrupt Status

Register 0859H: R8TD APS4 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	0
Bit 0		Unused	X

OCAI:

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by

the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

LCVI:

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is set high when this event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events.

Register 0842H: R8TD APS1 Line Code Violation Count

Register 084AH: R8TD APS2 Line Code Violation Count

Register 0852H: R8TD APS3 Line Code Violation Count

Register 085AH: R8TD APS4 Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

LCV[15:0]:

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV registers are polled by writing to this register or to register 0000H, the S/UNI-2488 Identity, and Global Performance Monitor Update. This action transfers the internally accumulated error count to the LCV registers within 5 REFCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0843H: R8TD APS1 Analog Control 1

Register 084BH: R8TD APS2 Analog Control 1

Register 0853H: R8TD APS3 Analog Control 1

Register 085BH: R8TD APS4 Analog Control 1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls internal analog functions.

Reserved[8:0]

The Reserved[8:0] bits must be set to the indicated default value for correct operation of the TSE.

Register 0844H: R8TD APS1 Analog Control 2

Register 084CH: R8TD APS2 Analog Control 2

Register 0854H: R8TD APS3 Analog Control 2

Register 085CH: R8TD APS4 Analog Control 2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls internal analog functions. This register should not be used.

Register 0860H: T8TE APS1 Control and Status

Register 0868H: T8TE APS2 Control and Status

Register 0870H: T8TE APS3 Control and Status

Register 0878H: T8TE APS4 Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	LLBEN	0
Bit 1	W	CENTER	1
Bit 0	R/W	DLCV	0

DLCV:

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the outgoing data stream. When this bit is set high, the transmit encoded data bus is inverted to generate the complementary running disparity.

CENTER:

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

LLBEN:

The line loopback enable bit (LLBEN) controls line loopback operation. When LLBEN is set high, serial line loopback is enabled. When LLBEN is set low, line loopback is disabled.

TPINS:

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the output data stream. When TPINS is set low, no test patterns are generated.

FIFOERRE:

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) controls the FIFO overrun interrupt event. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

Register 0861H: T8TE APS1 Interrupt Status

Register 0869H: T8TE APS2 Interrupt Status

Register 0871H: T8TE APS3 Interrupt Status

Register 0879H: T8TE APS4 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

FIFOERRI:

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when the T8TE Interrupt status register is read. This bit does not cause a hardware interrupt on INTB, unless the FIFOERRE bit is set high.

Register 0862H: T8TE APS1 TeleCombus Mode #1

Register 086AH: T8TE APS2 TeleCombus Mode #1

Register 0872H: T8TE APS3 TeleCombus Mode #1

Register 087AH: T8TE APS4 TeleCombus Mode #1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register is reserved and should be forced to all zeros.

Register 0863H: T8TE APS1 TeleCombus Mode #2

Register 086BH: T8TE APS2 TeleCombus Mode #2

Register 0873H: T8TE APS3 TeleCombus Mode #2

Register 087BH: T8TE APS4 TeleCombus Mode #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register is reserved and should be forced to all zeros.

Register 0864H: T8TE APS1 Test Pattern

Register 086CH: T8TE APS2 Test Pattern

Register 0874H: T8TE APS3 Test Pattern

Register 087CH: T8TE APS4 Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

TP[9:0]:

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the outgoing data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the output data stream.

Register 0865H: T8TE APS1 Analog Control

Register 086DH: T8TE APS2 Analog Control

Register 0875H: T8TE APS3 Analog Control

Register 087DH: T8TE APS4 Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Reserved	0
Bit 9		Reserved	0
Bit 8	R/W	TXLV_ENB	1
Bit 7	R/W	PISO_ENB	1
Bit 6	R/W	ATIN[3]	0
Bit 5	R/W	ATIN[2]	0
Bit 4	R/W	ATIN[1]	0
Bit 3	R/W	ATIN[0]	0
Bit 2	R/W	TXLV_ATMSB	1
Bit 1	R/W	PISO_ATMSB	1
Bit 0	R/W	ARSTB	1

ARSTB:

The analog reset bit (ARSTB) controls the TXLV and PISO operation. When ARSTB is set low, the TXLV and PISO are reset. This bit must be set to logic 1 for normal operation.

PISO_ATMSB:

The PISO analog test mode select bit (PISO_ATMSB) controls the PISO test operation. PISO_ATMSB drives the output PISO_ATMSB pin low to enable test mode in the PISO. This bit must be set to logic 1 for normal operation.

TXLV_ATMSB:

The TXLV analog test mode select bit (TXLV_ATMSB) controls the TXLV test operation. TXLV_ATMSB drives the output TXLV_ATMSB pin low to enable test mode in the TXLV block. This bit must be set to logic 1 for normal operation.

ATIN[3:0]:

The analog test control inputs (ATIN[3:0]) control the PISO and TXLV test circuitry. These bits are not used for normal operation.

PISO_ENB:

The PISO enable bit (PISO_ENB) controls the PISO operation. When set to logic 1, PISO_ENB disables the PISO. When set to logic 0, PISO_ENB enables the PISO.

TXLV_ENB:

The TXLV enable bit (TXLV_ENB) controls the TXLV operation. When set to logic 1, TXLV_ENB disables the TXLV. When set to logic 0, TXLV_ENB enables the TXLV.

Reserved:

The Reserved bits should be set to logic 0 for proper operation.

Register 0866H: T8TE APS1 DTB Bus

Register 086EH: T8TE APS2 DTB Bus

Register 0876H: T8TE APS3 DTB Bus

Register 087EH: T8TE APS4 DTB Bus

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	
Bit 7	R/W	DTBO[0]	0
Bit 6	R/W	DTBO[0]	0
Bit 5	R/W	DTBO[0]	0
Bit 4	R/W	DTBO[0]	0
Bit 3	R	DTBI[3]	0
Bit 2	R	DTBI[2]	0
Bit 1	R	DTBI[1]	0
Bit 0	R	DTBI[0]	0

DTBO[3:0]

The analog wrapper digital test bus output bits (DTB_OUT[3:0]) are used to drive values on the digital test bus (DTB[3:0]). These bits are not used in normal operation.

DTBI[3:0]

The analog wrapper digital test bus input bits (DTB_IN[3:0]) are used to read values from the digital test bus (DTB[3:0]). Thee bits are not used in normal operation.

Register 0880H-0883H: RFCLK DLL Reserved

Register 0884H-0887H: TFCLK DLL Reserved

Register 0888H: CSTR Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11		Unused	X
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	X
Bit 1	R/W	Reserved	X
Bit 0	R/W	Reserved	1

Except for the CSU_ENB register bit, the other register bits are used for manufacturing test purposes only. They are not required for normal operations.

Reserved:

Register 0889H: CSTR Interrupt Enable and CSU Lock Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1	R	CSU_LOCKV	X
Bit 0	R/W	CSU_LOCKE	0

CSU_LOCKE:

The CSU lock interrupt enable bit (CSU_LOCKE) enables the assertion of a hardware interrupt on INTB when the CSU lock status changes. When CSU_LOCKE is logic 1, the hardware interrupt is enabled. When CSU_LOCKE is logic 0, the hardware interrupt is disabled.

CSU_LOCKV:

The CSU lock status (CSU_LOCKV) indicates the current state of the CSU. When CSU_LOCKV is logic 1, the CSU has locked on to the SYSCLK reference and is operating normally. When CSU_LOCKV is logic 0, the CSU has not locked onto the SYSCLK reference and is not in normal operating mode.

Register 088AH: CSTR CSU Lock Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1		Unused	X
Bit 0	R	CSU_LOCKI	X

CSU_LOCKI:

The CSU lock interrupt indication bit (CSU_LOCKI) reports changes in the CSU lock status. CSU_LOCKI is logic 1 when the CSU transitions to or out of lock state. CSU_LOCKI is cleared when this register is read.

Register 088BH: CSTR CSU Lock Interrupt Indication

Register 0890H-0897: S/UNI-2488 Rx STSI Reserved

Register 0898H-089F: S/UNI-2488 Tx STSI Reserved

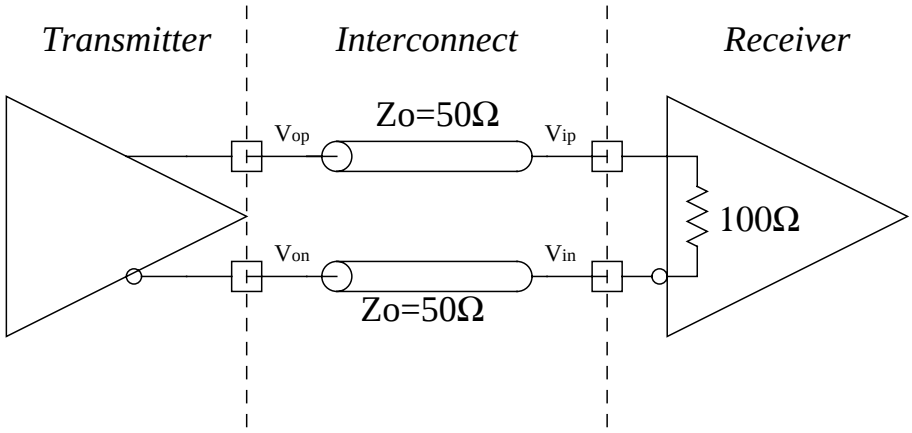
12 OPERATION

12.1.1 LVDS Overview

The LVDS APS Port implements the 777.6 Mb/s LVDS links. A reference clock of 77.76MHz is required (which is generated from the S/UNI-2488 CSU). Four 777.6 Mb/s LVDS form a high-speed serial TeleCombus interface for passing an STS-48 aggregate data stream.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Figure 17: Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Ten-bit parallel data is sampled by the line rate divided-by-10 clock (77.76MHz SYSCLK) and then serialized at the line rate on the LVDS output pins by a 777.6MHz clock synthesized from a divided version of REFCLK. Serial line rate LVDS data is sampled and de-serialized to 10-bit parallel data. Parallel output transfers are synchronized to a gated line rate divided-by-10 clock. The 10-bit data is passed to an 8B/10B decoding block. The gating duty cycle is adjusted such that the throughput of the parallel interface equals the receive input data rate (Line Rate +/- 100ppm). It is expected that the clock source of the transmitter is the same as the clock source of the receiver to ensure the data throughput at both ends of the link are identical.

Data must contain sufficient transition density to allow reliable operation of the data recovery units. 8B/10B block coding and decoding is provided by the T8TE and R8TD blocks.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. Namely, a worst case eye opening of 0.7UI and 100mV differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of backplane connectors and up to 1m of backplane interconnects. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. Due to power constraints, the output differential amplitude is approximately 350mV.

The LVDS system is comprised of the LVDS Receiver (RXLV), Data Recovery Unit (DRU), Receive 8B/10B TeleCombus Decoder (R8TD), Transmit 8B/10B TeleCombus Encoder (T8TE), APS Parallel to Serial converter (APISO), LVDS Transmitter (TXLV) and Transmitter LVDS Reference (TXLVREF), and Clock Synthesis Unit (CSU) blocks.

12.1.2 LVDS Receiver (RXLV)

The RXLV ABC is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Receiver according to the IEEE 1596.3-1996 LVDS Specification.

The RXLV ABC is the receiver accepts up to 777.6 Mb/s LVDS signals from the transmitter, amplifies them, converts them to digital signals and passes them to a data recovery unit (DRU). As per to the IEEE 1596.3-1996 specification, the RXLV has a differential input sensitivity better than 100mV, and includes at least 25mV of hysteresis.

12.1.3 Data Recovery Unit (DRU)

The DRU is a fully integrated data recovery and serial to parallel converter which is used for 777.6 Mb/s NRZ data. An 8B/10B block code is used to guarantee transition density for optimal performance. The DRU recovers data and outputs a 10-bit word synchronized with a line rate divided by 10 gated clock to allow frequency deviations between the data source and the local oscillator. The DRU accumulates 10 data bits and outputs them on the next clock edge.

The DRU provides moderate high frequency jitter tolerance suitable for inter-chip serial link applications. It can support frequency deviations up to ±100ppm.

12.1.4 Receive 8B/10B TeleCombus Decoder (R8TD)

The R8TD works in conjunction with the upstream DRU that packs consecutive bits from an incoming 8B/10B serial link into a 10-bit wide stream with arbitrary alignment to the 8B/10B character boundaries.

The R8TD character alignment block uses the K28.5 control character (Comma control / transport frame alignment) to determine 8B/10B character alignment in the incoming stream. When the R8TD character alignment state machine is in the out-of-character-alignment state, it searches for the K28.5 character in all positions of the incoming stream. Upon detecting the K28.5 character, the R8TD will align its internal character boundary, the character alignment state machine will transition to the in-character-alignment state and cease searching for subsequent K28.5

characters. The character alignment block also monitors for line-code violations (LCV) which are accumulated in an internal register. If 5 or more LCVs are detected within a window of 15 characters, the R8TD will enter the out-of-character-alignment state and begin searching for the K28.5 character afresh.

When operating in FIFO mode, aligned characters are written into a 24-character FIFO that isolates the incoming timing domain from the outgoing timing domain and provides a means of synchronizing multiple R8TDs outputs. Otherwise, the FIFO is bypassed.

In order to allow synchronization with other R8TDs that may have slightly different frame alignment and to allow for frame re-alignment, the R8TD frame alignment block monitors the character aligned data stream for the K28.5. An internal frame counter is maintained based on this character. If the K28.5 is found out of place three times then the frame alignment moves to the out-of-frame-alignment state. When in the out-of-frame-alignment state the first K28.5 will be written to the 0 position of the FIFO. The read pointer is then set by the OJ0FP signal to synchronize the output of the K28.5 characters which ensures that signals leaving the multiple R8TDs will have the same alignment.

The R8TD decodes 8B/10B control characters associated with specific SONET/SDH byte positions in an extended TeleCombus stream. In order to identify more SONET/SDH bytes than the 12 control characters available in the standard set, those control characters with balanced line codes for both positive and negative running disparity (K28.0, K28.4, K38.7, K23.7, K27.7, K29.7 and K30.7) are treated specially, where the positive and negative disparity codes are each associated with a different SONET/SDH byte. The reception of these line-codes will not be considered LCVs due to a mismatch with the running disparity.

The R8TD provides a diagnostic loopback port where the outgoing stream from an associated Transmit 8B/10B Encoder block (T8TE) can be processed in place of the incoming stream.

12.1.5 Transmit 8B/10B TeleCombus Encoder (T8TE)

The T8TE encodes a TeleCombus data stream and encodes it into an extended 8B/10B format for transmission on the serial LVDS links. The T8TE encodes TeleCombus control signals such as transport frame and payload boundaries, pointer justification events and alarm conditions into three levels of extended set of 8B/10B characters as well as performing the IEEE mode conversion on data. In order to identify more TeleCombus bytes and events than the 12 control characters available in the standard set, those control characters with balanced line codes for both positive and negative running disparity (K28.0, K28.4, K28.5, k28.6, k28.7, K23.7, K27.7, K29.7 and K30.7) are treated specially. The positive and negative disparity codes are each associated of a different SONET/SDH byte or event.

The T8TE can be configured to operate in the Loopback mode which allows a line loopback from the associated R8TD block. The T8TE can be configured to use a FIFO to bridge between the incoming data stream and the outgoing data stream clock domains.

12.1.6 APS Parallel to Serial Converter (PISO)

The APISO is a parallel-to-serial converter designed for high-speed transmit operation, supporting up to 777.6 Mb/s.

12.1.7 LVDS Transmitter (TXLV)

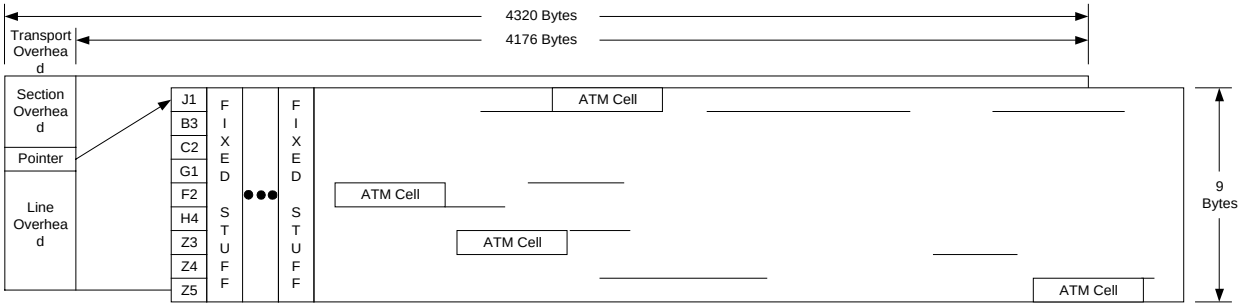
The TXLV is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Transmitter according to the IEEE 1596.3-1996 LVDS Specification. The TXLV accepts 777.6 Mbit/s differential data from the APSIO circuit and transmits the data off-chip as a low voltage differential signal. The TXLV uses the reference current and voltage from the TXLVREF to control the output differential voltage amplitude and the output common-mode voltage.

12.2 SONET/SDH Frame Mappings and Overhead Byte Usage

12.2.1 ATM Mapping

The S/UNI-2488 processes the ATM cell mapping for STS-48c (STM-16c) as shown below in Figure 18. The S/UNI-2488 processes the transport and path overhead required to support ATM UNIs and NNIs. In addition, the S/UNI-2488 provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. In Figure 18, the STS-48c (STM-16c) mapping is shown. In this mapping, fifteen stuff columns are included in the SPE. No other options are provided.

Figure 18 ATM Mapping

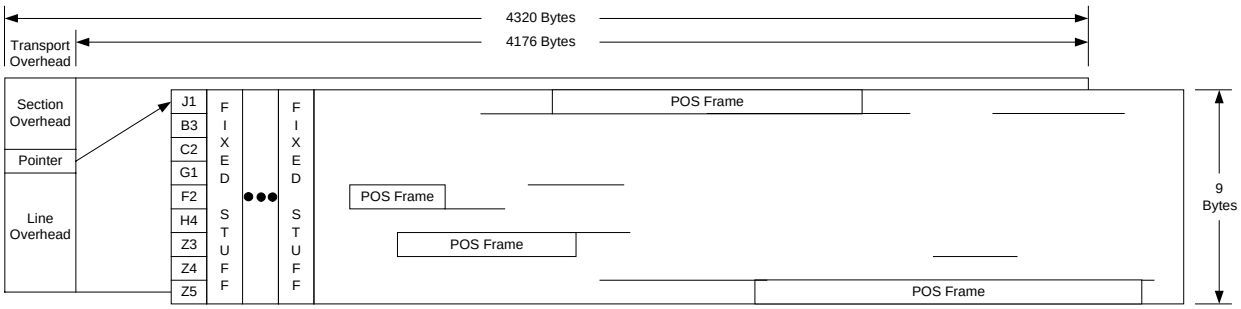


12.2.2 Packet Over SONET Mapping

The S/UNI-2488 processes the Packet Over SONET mapping for STS-48c (STM-16c) as shown below in Figure 19. The S/UNI-2488 processes the transport and path overhead required to support Packet Over SONET applications. In addition, the S/UNI-2488 provides support for the

APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. Figure 19, the STS-48c (STM-16c) mapping is shown. In this mapping, the entire SPE is used for POS Frames.

Figure 19 Packet Over SONET Mapping



12.2.3 Transport and Path Overhead Bytes

Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET frame in the STS-48c (STM-16c) serial stream.

J0 The J0 byte is currently defined as the STS-48c (STM-16c) section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.

Z0: The Z0 bytes are currently defined as the STS-48c (STM-16c) section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the S/UNI-2488 calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling.

In the receive direction, the S/UNI-2488 calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in an error event counter.

D1 - D3: The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.

H1, H2: The pointer value bytes locate the path overhead column in the SONET/SDH frame.

In the transmit direction, the S/UNI-622-POS inserts a fixed pointer value, with a normal new data flag indication in the first H1-H2 pair. The concatenation indication is inserted in the remaining H1-H2 pairs (STS-48c (STM-16c)). Pointer movements can be induced using the THPP registers.

In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the S/UNI-2488 calculates the B2 values. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-2488 calculates the B2 code over the current frame and compares this calculation with the B2 code receive in the following frame. Receive B2 errors are accumulated in an error event counter.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

In the transmit direction, the S/UNI-2488 provides register control for the K1 and K2 bytes.

In the receive direction, the S/UNI-2488 provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined to determine the presence of the line AIS, or the line RDI maintenance signals

D4 - D12: The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.

S1: The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of STS-48c (STM-16c) signal. Bits 1 through 4 are currently undefined.

In the transmit direction, the S/UNI-2488 provides register control for the synchronization status byte.

In the receive direction, the S/UNI-2488 provides register access to the synchronization status byte.

Z1: The Z1 bytes are located in the second and third STS-1's locations of an STS-48c (STM-16c) and are allocated for future growth.

M1: The M1 byte is located in the third STS-1 location of a STS-48c (STM-16c) and provides a line far end block error function for remote performance monitoring.

Z2: The Z2 bytes are located in the first and second STS-1's locations of a STS-12c (STM-4c) and are allocated for future growth.

In the transmit direction, Z2 byte is internally generated. The number of B2 errors detected in the previous interval is inserted.

In the receive direction, a legal Z2 byte value is added to the line FEBE event counter.

Path Overhead Bytes

J1: The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

In the transmit direction, characters can be inserted using the TTTP Path Trace register. The register is the default selection and resets to 0x00 to enable the transmission of NULL characters from a reset state.

In the receive direction, the path trace message is optionally extracted into the 16 or 64 byte path trace message buffer.

B3: The path bit interleaved parity byte provides a path error monitoring function.

In the transmit direction, the S/UNI-2488 calculates the B3 bytes. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-2488 calculates the B3 code and compares this calculation with the B3 byte received in the next frame. B3 errors are accumulated in an error event counter.

C2: The path signal label indicator identifies the equipped payload type. For ATM payloads, the identification code is 0x13. For Packet over SONET (including $X^{43}+1$ payload scrambling), the identification code is 0x16.

G1: The path status byte provides a path RDI function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

In the transmit direction, the S/UNI-2488 provides register bits to control the path RDI (bit 5) and auxiliary path RDI (bit 6) states. For path RDI, the number of B3 errors detected in the previous interval is inserted either automatically or using a register. This path RDI code has 9 legal values, namely 0 to 8 errors.

In the receive direction, a legal path RDI value is accumulated in the path RDI event counter. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers.

H4: The multi-frame indicator byte is a payload specific byte, and is not used for ATM payloads. This byte is forced to 0x00 in the transmit direction, and is ignored in the receive direction.

Z3 - Z5: The path growth bytes provide three unused bytes for future use.

In the transmit direction, the growth bytes may be inserted from the three THPP Path Growth byte registers.

12.2.4 ATM Cell Data Structure

ATM cells may be passed to/from the S/UNI-2488 using a 52 byte cell structure on a 32-bit UTOPIA level 3 compliant interface.

Figure 20 shows the default ATM cell format for the S/UNI-2488 at the UTOPIA Level 3 interface. It is the 13x32-bit word structure with no HCS or UDF bytes.

Bit 31 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first four header octets).

Figure 20: A 52 Byte ATM Data Structure

	Bit 31	Bit 16	Bit 15	Bit 0
Word 1	H1	H2	H3	H4
Word 2	Payload 1	Payload 2	Payload 3	Payload 4
Word 3	Payload 5	Payload 6	Payload 7	Payload 8
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
Word 12	Payload 41	Payload 42	Payload 43	Payload 44
Word 13	Payload 45	Payload 46	Payload 47	Payload 48

12.3 POS/HDLC Data Structure

Packets may be passed to/from the S/UNI-2488 using a 32-bit POS-PHY Level 3 compliant interface.

The 32-bit POS-PHY Level 3 data structure is shown in Figure 21. The packet length of 63 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable. Octets are written in the same order they are to be transmitted or they were received on the SONET line. All words are composed of four octets, except the last word of a packet which can have one, two, three, or four octets. If the Transmit Packet Processor (TCFP) is configured to not insert the FCS field, then these bytes should be included with the packet passed through the POS-PHY L3 interface. Similarly, if the Receive Packet Processor (RCFP) is configured to not strip the FCS field, then these bytes will be included at the end of the packet.

Figure 21: A 63 Byte Packet Data Structure

	Bit 31	Bit 16	Bit 15	Bit 0
Word 1	Byte 1/SOP	Byte 2	Byte 3	Byte 4
Word 2	Byte 5	Byte 6	Byte 7	Byte 8
Word 3	Byte 9	Byte 10	Byte 11	Byte 12
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
Word 15	Byte 57	Byte 58	Byte 59	Byte 60
Word 16	Byte 61	Byte 62	Byte 63/EOP	Unused

Both the start of the packet and the end of the packet must be identified by the TSOP/RSOP and TEOP/REOP signals. When the first section of a packet is transferred over the interface, the

TSOP/RSOP signals will be high for Byte 1 of the packet only. The TMOD[1:0] pins will indicate how many bytes of the final word are valid.

Bits 31 to 24 form the first transmitted byte and bit 31 can be configured to be the bit which is transmitted first. This is the desired set-up for byte-synchronous POS. Bit 24 can also be configured to be the first transmitted bit of this byte. This is the desired set-up for bit-synchronous HDLC.

12.3.1 Limitation when using externally generated FCS in STS-48c Mode

When the S/UNI-2488 is set up in STS-48c POS mode and FCS bytes are passed through the transmit POS-PHY L3 interface, the overall throughput is reduced. The maximum bandwidth throughput will be reduced by a maximum of 2 bytes per packet. The overall effect will depend on the length of the packets + FCS bytes being transferred through the POS-PHY L3 interface. If the packet + FCS length is evenly divisible by 4 bytes, no bandwidth is lost for that packet.

12.3.2 Limitations from Small Packets

The S/UNI-2488 cannot process packets which are smaller than 4 bytes (including FCS). Packets of size 3 bytes or less are discarded by the RCFP packet processor and marked as minimum length violations.

12.4 Setting ATM Mode of Operation

TBD

12.5 Setting Packet Over SONET/SDH Mode of Operation

TBD

12.6 Bit Error Rate Monitor

TBD

12.7 Clocking Operations

TBD

12.8 Loopback Operation

TBD

12.9 Board Design Recommendations

TBD

12.10 Power Supplies

TBD

12.11 Interfacing to ECL or PECL Devices

TBD

13 FUNCTIONAL TIMING

13.1 Serial Line Interface

TBD

13.2 ATM Utopia Level 3 System Interface

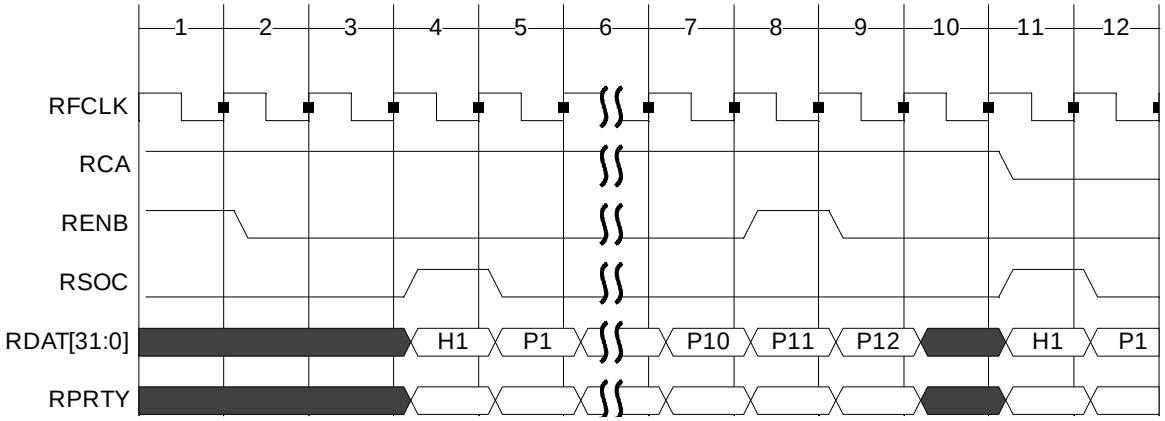
The Receive UTOPIA Level 3 System Interface Timing diagrams Figure 22 and Figure 23 illustrate the operation of the system side receive interface.

The single PHY case shown in Figure 22 illustrates the behaviour of the RCA signal. At the start cycle 3, RENB is sampled low which initiates a cell transfer from the S/UNI-2488. The transfer begins at cycle 4. The response to RENB always occurs on the rising RFCLK edge following the RFCLK edge which samples RENB. Also note that RENB must remain asserted during a cell transfer as specified by the Utopia L3 standard. In Figure 22, this occurs on the rising edge of RFCLK at the start of cycle 9.

RCA is deasserted in cycle 11 coincident with the RSOC assertion indicating that the cell transfer which has just started contains the last cell in the FIFO at this time. RCA may be asserted at any time due to the insertion of a complete cell into the FIFO.

Back-to-back cells can be handled by holding RENB asserted at logic 0 during cycle 8. In this case, cycle 10 for RSOC, RDAT[31:0], and RPRTY will be eliminated and the following cycles will be advanced.

Figure 22 Single-PHY Utopia Level 3 Receive Functional Timing



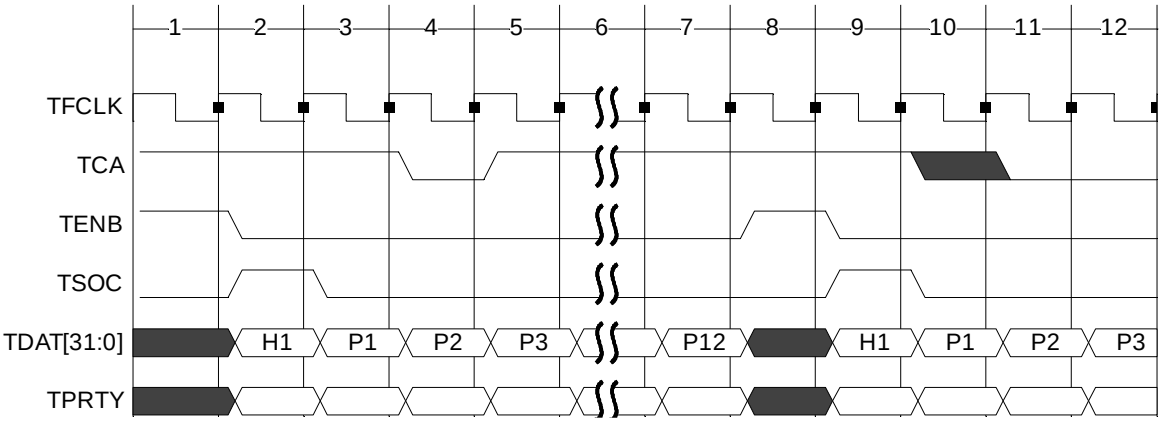
The Transmit UTOPIA Level 3 System Interface Timing diagram (Figure 23) illustrates the operation of the system side transmit UL3 interface. The single PHY case shown Figure 23 illustrates the behaviour of the TCA signal. At the start of cycle 4, there is only enough FIFO buffer space for the cell being transferred so TCA is deasserted. The deassertion occurs on the TFCLK edge **after** TSOC of the cell (cell#1) being written to the FIFO is sampled. This cell will take the last remaining cell buffer space in the FIFO. This TCA behaviour is consistent with the Utopia L3 specification which states that TCA is invalid on the TFCLK edge that initiates the transition of TSOC to logic 1.

On cycle 5, a cell has been read out of the FIFO to the S/UNI-2488 core so it now has room to accomodate the cell currently being transferred (cell#1) plus one additional cell (cell#2). At the start of cycle 8, the transfer of cell#1 is completed. TCA remains high because there is still buffer space for one more cell. At the start of cycle 10, transfer of cell#2 starts. TCA is deasserted at cycle 11 because besides the space for holding cell#2, there is no FIFO space for any more cells.

Note that the single-PHY mode is handled exactly like the multi-PHY mode except that the PHY address is held at the value 0. However, TENB must be set to logic 1 between cell transfers as shown in Figure 23. Back-to-back cell transfers is not allowed.

TSOC must be high during the first byte of the ATM cell structure and must be present for the start of each cell. Thus, TSOC will mark the H1 byte. If TSOC is asserted at the wrong time (not at proper cell boundaries), a corrupted (but complete) cell will be transmitted from the S/UNI-2488. This corrupted cell will contain the bytes from the runt cell transferred through the UL3 interface plus some random bytes to fill the remainder of the ATM cell.

Figure 23 Single-PHY Utopia Level 3 Transmit Functional Timing



13.3 Packet Over SONET/SDH (POS) Level 3 System Interface

The Receive POS Level 3 System Interface Timing diagram (Figure 24) illustrates the operation of the system side receive interface. The SUNI-2488 performs the polling operation internally, selects the PHY for which data is to be transferred, and pushes data to the downstream reader.

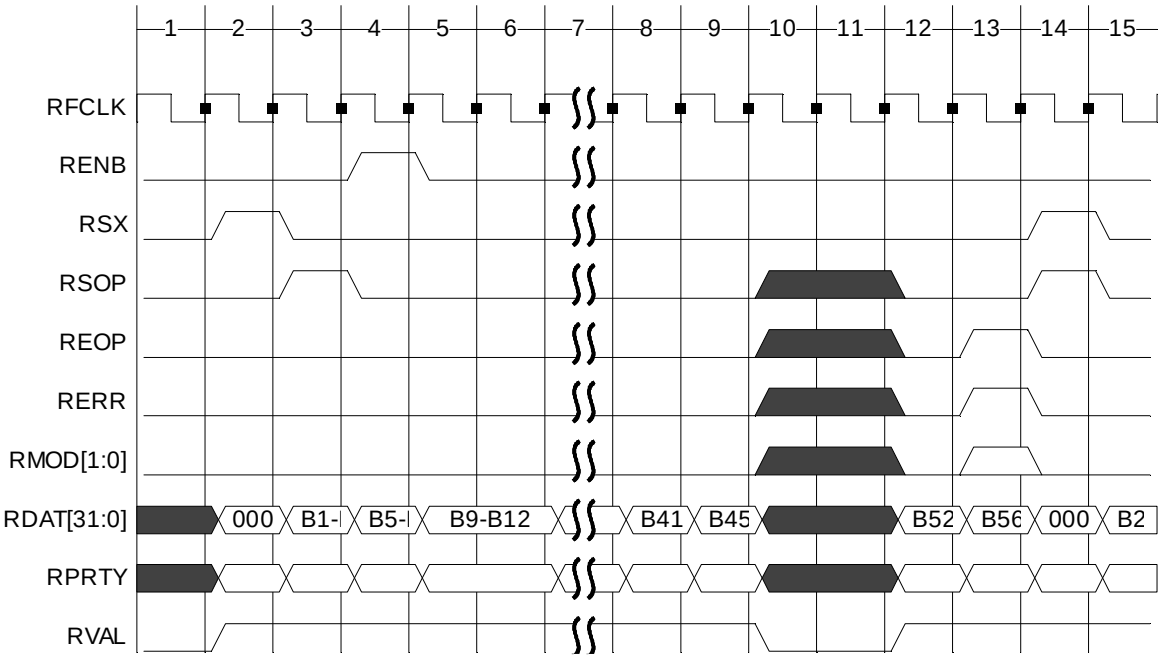
When data is available, the RVAL signal is asserted. RSX is also asserted in cycle 2 to indicate that the PHY address for which data is being transferred is present on RDAT[31:0]. At cycle 3, RSOP is asserted to indicate that the RDAT[31:24] contains the first byte of a packet. RENB is deasserted in cycle 4 because the downstream device wants to pause the data transfer.

Data transfer continues until cycle 10 when RVAL is deasserted. At cycle 12 and 13, the last two transfers for the packet are performed. In cycle 13, REOP signals the last byte of the packet is contained in RDAT[31:0] and the value of RMOD[1:0] indicates which bytes in RDAT[31:0] contain valid data. RERR is asserted along with REOP if errors were detected in this packet (aborted, length violation, FIFO overrun, FCS errors) so the downstream device may discard the packet. In cycle 14, a new transfer is initiated by reasserting RSX and a new PHY address on RDAT[31:0].

The burst length of any transfer can be limited by setting the RXPHY's BURST_SIZE[7:0] register bits. The polling algorithm used for selecting the order in which data from different PHYs are transferred is completely user programmable using the CALENDAR_LENGTH[6:0], CALENDAR_ADDR[6:0] and CALENDAR_DATA[5:0] register bits of the RXPHY.

The FIFO threshold at which data transfer begins is set by the RXSDQ's DT[7:0] register bits. ATM cells can be transferred through the PL3 interface as fixed length packets. The DT[7:0] value should be set so that only complete ATM cells are transferred.

Figure 24 Single PHY POS-PHY Level 3 Receive Functional Timing



The Transmit POS Level 3 System Interface Timing (Figure 25) illustrates the operation of the system side transmit FIFO interface. TENB, TSX, and TDAT[31:0] (which contains the in-band PHY address since TSX = 1) are asserted in cycle 1 to start the transfer. Because the S/UNI-2488 is a single-PHY device, the in-band address must always be set to 0x0000. DTPA responds in cycle 3 to show that there is room in the FIFO (the FIFO fill threshold is user programmable) for PHY address 0. The packet data is transferred on TDAT[31:0] starting at the rising TFCLK edge at the start of cycle 3. TSOP is also asserted at this cycle to indicate the data on TDAT[31:24] contains the start-of-packet byte. TENB is deasserted in cycle 3 by the upstream device to pause the transfer. Data transfer continues in cycle 4. In cycle 6, DTPA is deasserted indicating that the FIFO for PHY address 0 has fallen below the data available threshold (TXSDQ's BT[7:0] register bits). In the example shown here, BT[7:0] is set to the value 1 so that DTPA is deasserted when there is less than 16 bytes of buffer space left in the FIFO. The TXSDQ FIFO status takes 1 clock cycle to propagate to the interface so after the upstream device samples DTPA at the rising TFCLK edge at the start of cycle 7, it can only write one more cycle of TDAT[31:0] before it must stop to avoid overrunning the FIFO. TENB is deasserted before cycle 9 to prevent the overrun.

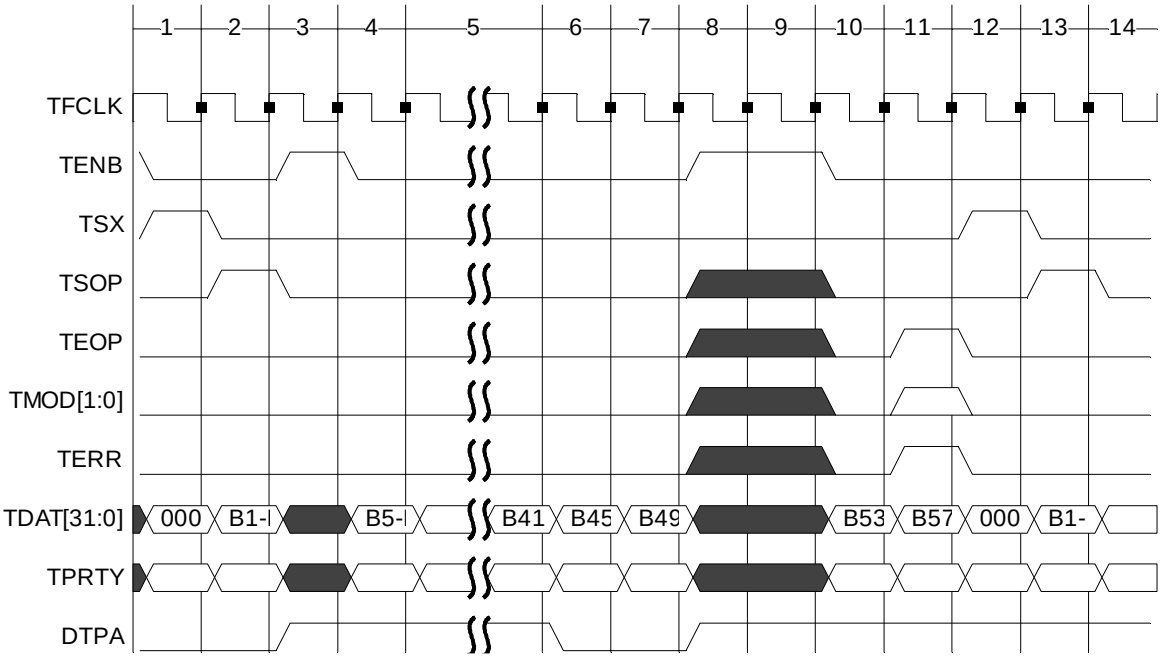
The TXSDQ hysteresis value (GHT[3:0] should be used to prevent the DTPA signal from pulsating on and off while the FIFO is at the BA[7:0] threshold.

Because DTPA is asserted again on cycle 8, transfers can be conducted again. TENB is asserted again before cycle 11 to continue the transfer. In cycle 11, TEOP is asserted to indicate that TDAT[31:0] contains one byte which is the end of the packet. TMOD[1:0] is valid at the same time to indicate which bytes in TDAT[31:0] contain valid data and thus the last byte of the packet can be inferred. TERR is also valid during this cycle to indicate whether or not this packet should be aborted because of an upstream error. If TERR is logic 1, the packet will be aborted by the S/UNI-2488's packet processor.

In cycle 12, TENB is deasserted and TSX is asserted to select a different PHY to transfer data to.

TSOP must be high during transfers which contain the first byte of a packet. TEOP must be high during transfers which contain the last byte of a packet. It is legal to assert TSOP and TEOP at the same time. This case occurs when TDAT[31:0] contain both the SOP and EOP. When TSOP is asserted and the previous transfer was not marked with TEOP, the system interface realigns itself to the new timing, and both the previous packet and the current packet may be corrupted and aborted.

Figure 25 Single PHY POS-PHY Level 3 Transmit Functional Timing



13.4 Section and Line Data Communication Channels

TBD

13.5 S/UNI-2488 Conceptual Regions

The S/UNI-2488 can conceptually be split into 3 regions: line side timeslots, system side timeslots, and system side channels. Each region has its data streams segregated differently and has a transmit half and a receive half.

14 TEST FEATURES DESCRIPTION

15 FUNCTIONAL TIMING

16 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 17: Absolute Maximum Ratings

Case Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	TBD
Voltage on Any Digital Pin	-0.3V to V_{VDD}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

17 D.C. CHARACTERISTICS

T_C = -40°C to +85°C, V_{DD} = $VDD_{typical}$ ± 10%

(Typical Conditions: T_C = 25°C, V_{VDDDC} = 1.8V, V_{VDDAC} = 3.3V, V_{AVDH} = 3.3V +/- 5% only, V_{AVDL} = 1.8V +/- 5% only, V_{QAVD} = 3.3V +/- 5% only)

Table 18: D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDI}	Power Supply	1.62	1.8	1.98	Volts	
V_{VDDO}	Power Supply	2.97	3.3	3.63	Volts	
V_{AVDD}	Power Supply	2.97	3.3	3.63	Volts	
V_{AVDDQ}	Power Supply	2.97	3.3	3.63	Volts	
V_{IL}	Input Low Voltage	0	TBD	0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0	TBD		Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		TBD	0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	TBD		Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		TBD		Volts	Applies to RSTB and TRSTB only.
I_{ILPU}	Input Low Current	TBD	TBD	TBD	µA	V_{IL} = GND. Notes 1 and 3.

I_{IHPU}	Input High Current	TBD	TBD	TBD	µA	$V_{IH} = V_{DD}$. Notes 1 and 3.
I_{IL}	Input Low Current	TBD	TBD	TBD	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$. Notes 2 and 3.
V_{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity			100	mV	
R_{IN}	LVDS Differential Input Impedance	85	100	115	Ω	
V_{LOH}	LVDS Output voltage high		1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025		mV	R_{LOAD}=100Ω ±1%
V_{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	85	110	115	Ω	
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I_{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz

I_{DDOP1}	Operating Current			TBD	mA	V_{DD} = max, Outputs Unloaded
I_{DDOP2}	Operating Current			TBD	mA	V_{DD} = max, Outputs Unloaded
I_{DDOP3}	Operating Current			TBD	mA	V_{DD} = max, Outputs Unloaded
I_{DDOP4}	Operating Current			TBD	mA	V_{DD} = max, Outputs Unloaded

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.

2. Input pin or bi-directional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

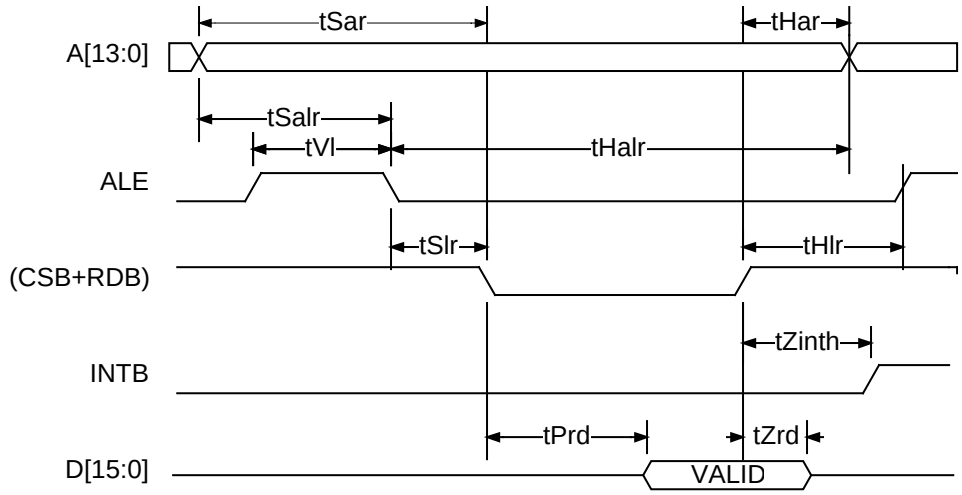
18 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = typical ± 10%)

Table 19: Microprocessor Interface Read Access (Figure 26)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB High		50	ns

Figure 26: Intel Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

5. Parameter tH_{AR} is not applicable if address latching is used.

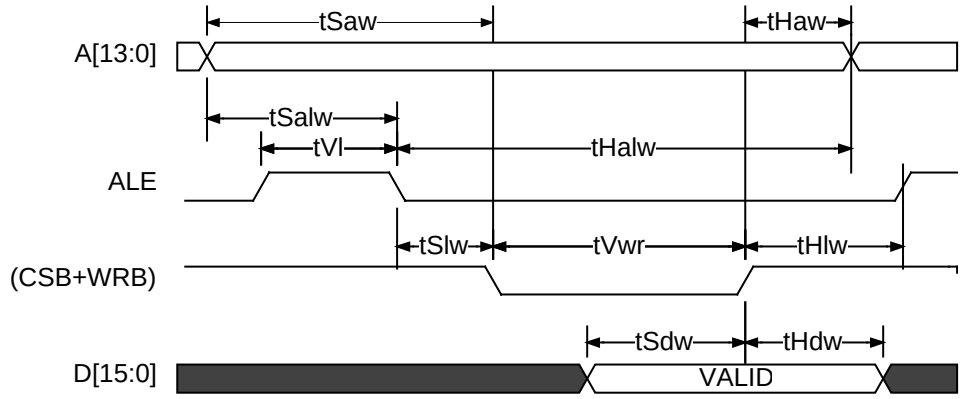
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 20: Microprocessor Interface Write Access (Figure 27)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 27: Intel Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2 In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.

3 Parameter tH_{AW} is not applicable if address latching is used.

4 When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5 When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt

19 A.C. TIMING CHARACTERISTICS

Table 21: Receive System Interface Timing (Figure 28)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	60	104	MHz
tHI_{RFCLK}	RFCLK HI Pulse Width	3.85		ns
tLO_{RFCLK}	RFCLK LO pulse Width	3.85		ns
tS_{RENB}	RENB Set-up time to RFCLK	2		ns
tH_{RENB}	RENB Hold time to RFCLK	0.5		ns
tP_{RVAL}	RFCLK High to RCA/RVAL Valid	1	5	ns
tP_{RSOP}	RFCLK High to RSOC/RSOP Valid	1	5	ns
tP_{REOP}	RFCLK High to REOP Valid	1	5	ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	5	ns
tP_{RERR}	RFCLK High to RERR Valid	1	5	ns
tP_{RSX}	RFCLK High to RSX Valid	1	5	ns
tP_{RDAT}	RFCLK High to RDAT[31:0] Valid	1	5	ns
tP_{RMOD}	RFCLK High to RMOD[1:0] Valid	1	5	ns

Figure 28: Receive System Interface Timing Diagram

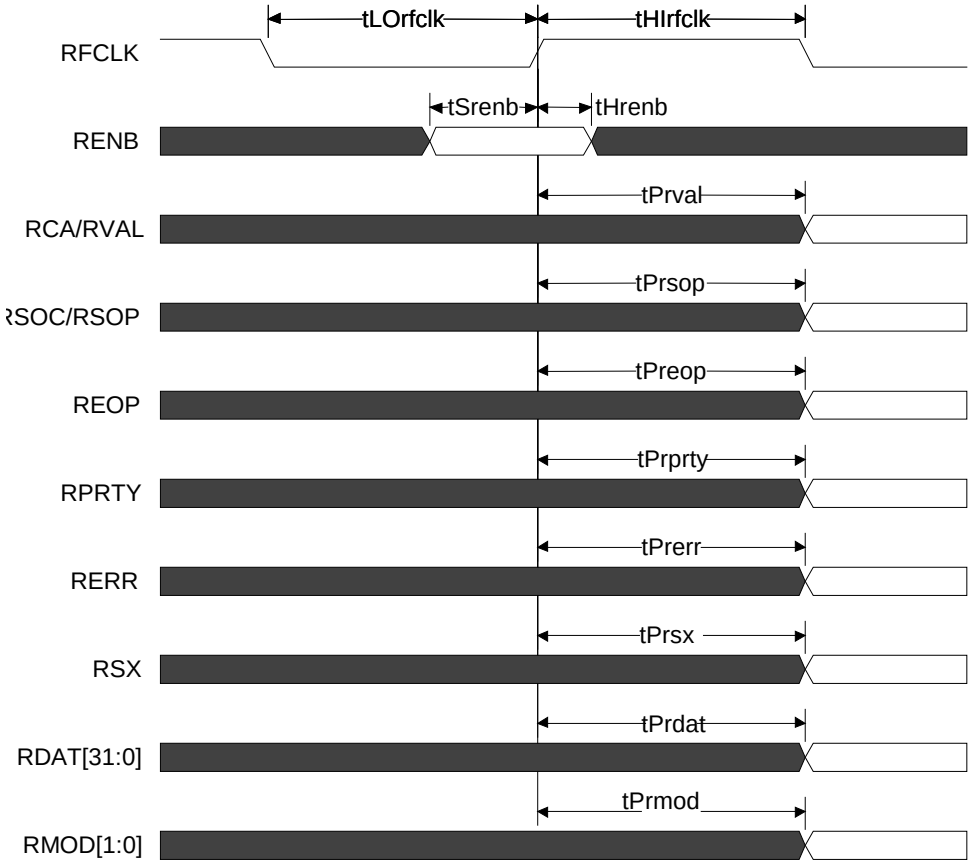
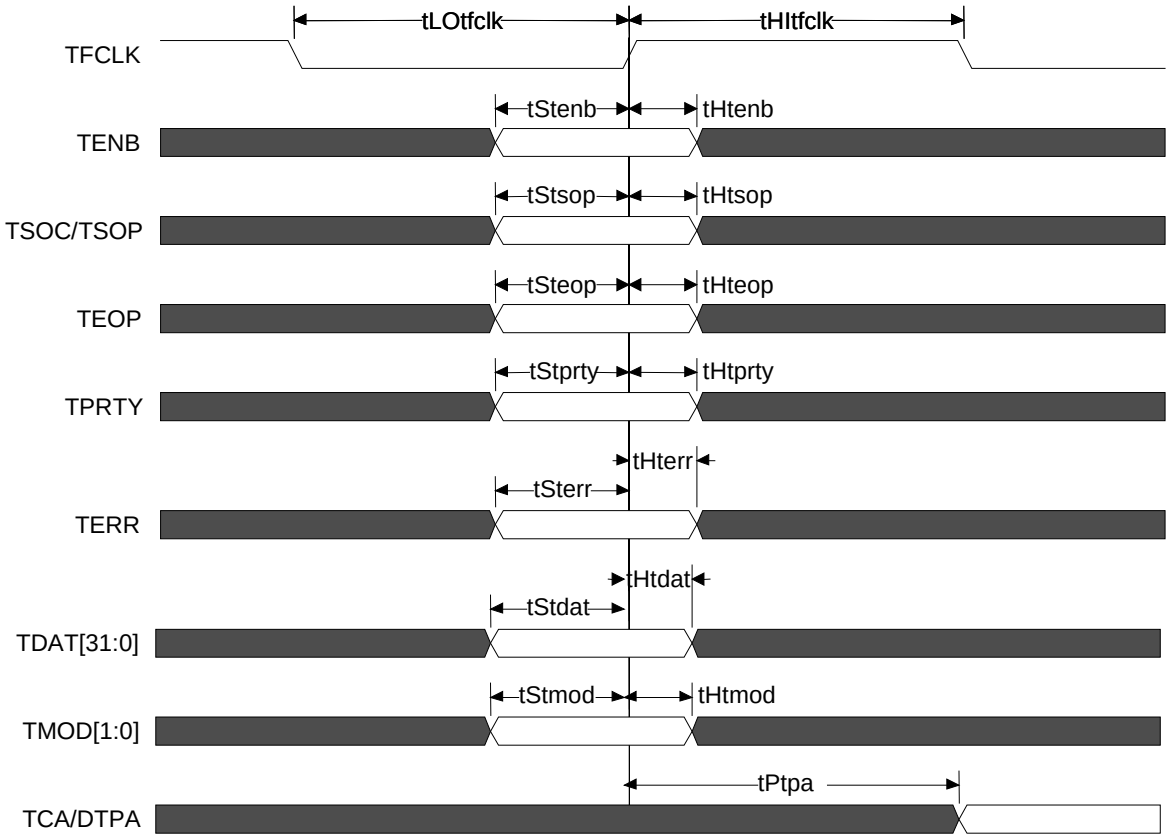


Table 22: Transmit System Interface Timing (Figure 29)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	60	104	MHz
tHI_{TFCLK}	TFCLK HI Pulse Width	3.85		ns
tLO_{TFCLK}	TFCLK LO pulse Width	3.85		ns
tS_{TENB}	TENB Set-up time to TFCLK	2		ns
tH_{TENB}	TENB Hold time to TFCLK	0.5		ns
tS_{TSOP}	TSOC/TSOP Set-up time to TFCLK	2		ns
tH_{TSOP}	TSOC/TSOP Hold time to TFCLK	0.5		ns
tS_{TEOP}	TEOP Set-up time to TFCLK	2		ns
tH_{TEOP}	TEOP Hold time to TFCLK	0.5		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0.5		ns
tS_{TERR}	TERR Set-up time to TFCLK	2		ns
tH_{TERR}	TERR Hold time to TFCLK	0.5		ns
tS_{TDAT}	TDAT[31:0] Set-up time to TFCLK	2		ns
tH_{TDAT}	TDAT[31:0] Hold time to TFCLK	0.5		ns
tS_{TMOD}	TMOD[1:0] Set-up time to TFCLK	2		ns
tH_{TMOD}	TMOD[1:0] Hold time to TFCLK	0.5		ns
tP_{TPA}	TFCLK High to TCA/DTPA Valid	1	5	ns

Figure 29: Transmit System Interface Timing



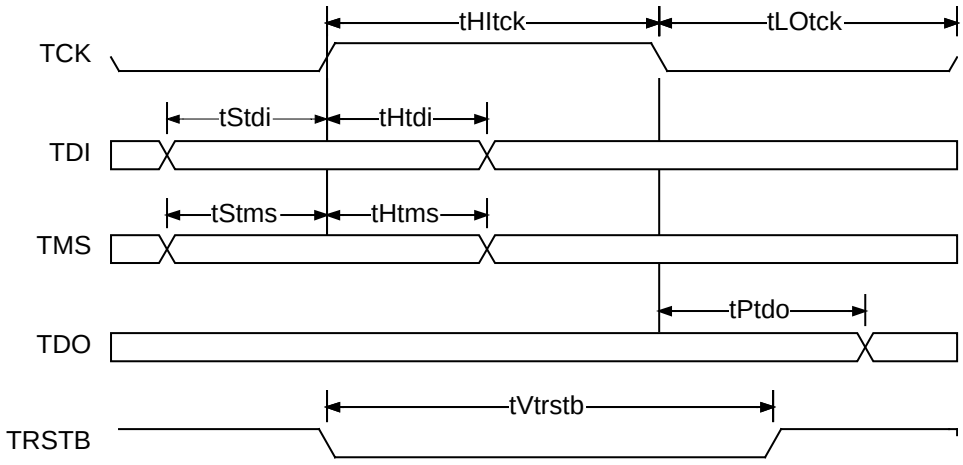
19.1 APS Port Interface

Symbol	Description	Min	Typical	Max	Units
f_{RLVDS}	APSI+/-[4:1], APSO+/-[4:1] Bit Rate	$5f_{SYSCLK}$ - 100ppm	$5f_{SYSCLK}$	$5f_{SYSCLK}$ - 100ppm	Mbps
t_{FALL}	V_{ODM} fall time, 80%-20%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
t_{RISE}	V_{ODM} rise time, 20%-80%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
t_{SKEW}	Differential Skew			50	ps

Table 23: JTAG Port Interface (Figure 30)

Symbol	Description	Min	Max	Units
f_{TCK}	TCK Frequency		4	MHz
t_{HITCK}	TCK HI Pulse Width	100		ns
t_{HITCK}	TCK LO Pulse Width	100		ns
t_{STMS}	TMS Set-up time to TCK	25		ns
t_{HTMS}	TMS Hold time to TCK	25		ns
t_{STDI}	TDI Set-up time to TCK	25		ns
t_{HTDI}	TDI Hold time to TCK	25		ns
t_{PTDO}	TCK Low to TDO Valid	2	25	ns
t_{VTRSTB}	TRSTB Pulse Width	100		ns

Figure 30: JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

20 ORDERING AND THERMAL INFORMATION

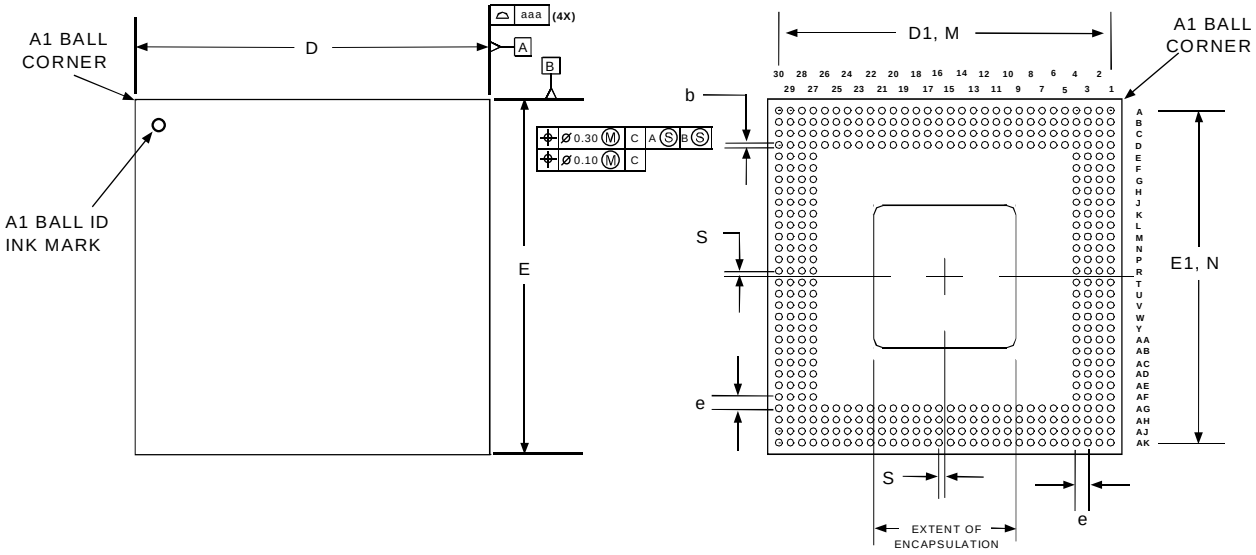
Table 24: Ordering Information

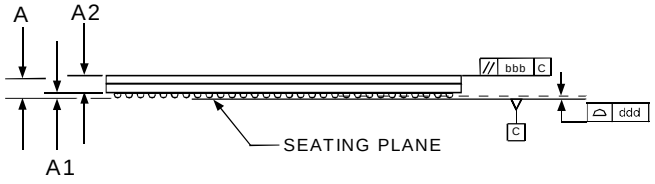
PART NO.	DESCRIPTION
PM5381-BI	416-pin Ultra Ball Grid Array (UBGA)

Table 25: Thermal Information

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM5381-BI	-40°C to 85°C	X °C/W	X °C/W

21 MECHANICAL INFORMATION





NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 416 THERMALLY ENHANCED BALL GRID ARRAY - UBGA															
BODY SIZE : 31 x 31 x 1.47 MM															
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	S	
Min.	1.32	0.40	0.92	30.90	-	30.90	-	-	0.50	-	-	-	-	0.45	
Nom.	1.47	0.50	0.97	31.00	29.00	31.00	29.00	30x30	0.63	1.00	-	-	-	0.50	
Max.	1.62	0.60	1.02	31.10	-	31.10	-	-	0.70	-	0.20	0.25	0.20	0.55	

PMC-2000489 (P1) Ref PMC-991408 (P1) Issue date: March 2000