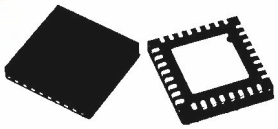
PM6685

DUAL STEP-DOWN CONTROLLER WITH AUXILARY VOLTAGES FOR NOTEBOOK SYSTEM POWER

Preliminary Data

Features

- CONSTANT ON TIME TOPOLOGY ALLOWS VERY FAST LOAD TRANSIENTS
- 6V TO 28V INPUT VOLTAGE RANGE
- FIXED 5V-3.3V OUTPUT VOLTAGES
- 5V AND 3.3V ALWAYS VOLTAGES AVAILABLE DELIVER 100mA PEAK CURRENT
- 1.23V ± 1% REFERENCE VOLTAGE AVAILABLE
- NO R_{SENSE} CURRENT SENSING USING LOW SIDE MOSFETs' $R_{DS(on)}$
- ACCURATE CURRENT SENSE WITH R_{SENSE}
- NEGATIVE CURRENT LIMIT
- SOFT START INTERNALLY FIXED AT 2ms
- SOFT OFF FOR OUTPUT DISCHARGE
- LATCHED OVP AND UVP
- SELECTABLE PULSE SKIPPING AT LIGHT LOADS
- SELECTABLE MINIMUM FREQUECY (25kHz) IN PULSE SKIP MODE
- 4 mW MAXIMUM QUIESCENT POWER
- INDIPENDENT POWER GOOD SIGNALs
- OUTPUT VOLTAGE RIPPLE COMPENSATION



VFQFPN-32 5X5

Description

PM6685 is a dual step-down controller specifically designed to provide extremely high efficiency conversion, with lossless current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation. An embedded integrator control loop compensates the DC voltage error due to the output ripple. Pulse skipping technique increases efficiency at very light load. Moreover a minimum switching frequency of 25kHz is selectable to avoid audio noise issues. The PM6685 provides a selectable switching frequency, allowing either 200kHz/ 300kHz, 300kHz/400Khz or 400kHz/500kHz operation of the 5V/3.3V switching sections...

Applications

- NOTEBOOK COMPUTERS
- TABLET PC OR SLATES
- MOBILE SYSTEM POWER SUPPLY
- 3-4 CELLS Li+ BATTERY POWERED DEVICES

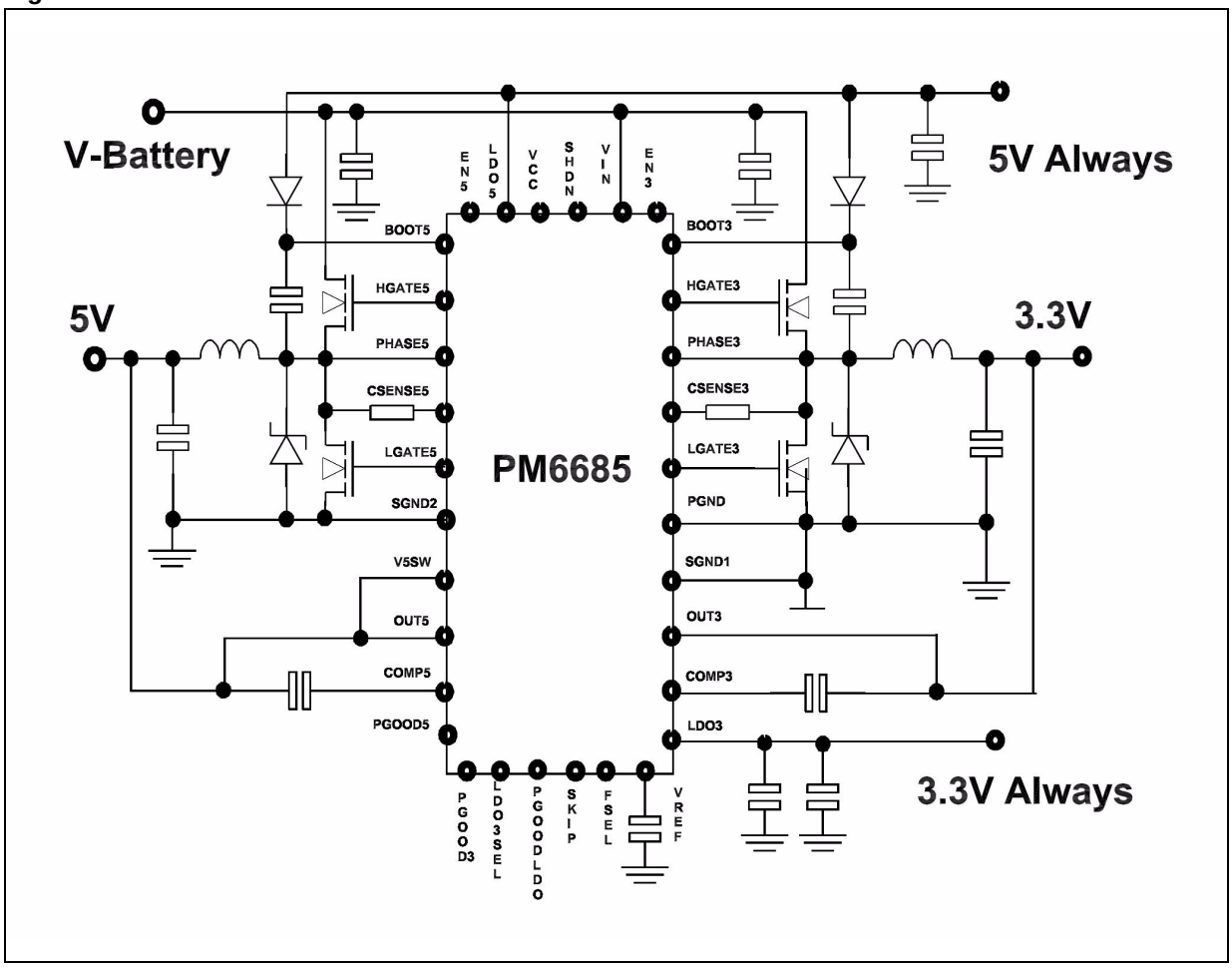
Order codes

Part number	Marking	Package	Packing
PM6685	PM6685	VFQFPN-32 5X5	TAPE & REEL

Contents

1 Typical application circuit

Figure 1. Circuit



2 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
	SGND1 to SGND2	Shorted	
	COMPx, FSEL, LDO3_SEL, VREF, SKIP to SGND1, SGND2	-0.3 to V_{CC} + 0.3	V
	Enx, SHDN, PGOD_LDO3, OUTx, PGOODx, V_{CC} to SGND1, SGND2	-0.3 to 6	
	LDO3 to SGND1, SGND2	-0.3 to LDO5 + 0.3	V
	LGATEx to PGND	-0.3 to LDO5 + 0.3	V
	HGATEx and BOOTx, to PHASEx	-0.3 to 6	V
	PHASEx to PGND	-0.6 to 36	V
	CSENSEx, to PGND	-0.6 to 42	V
	CSENSEx to BOOTx	-6 to 0.3	V
	V5SW, LDO5 to PGND	-0.3 to 0.6	V
	VIN to PGND	-0.3 to 36	V
	PGND to SGND1, SGND2	-0.3 to 0.3	V
	Power dissipation at T_{amb} = 25°C	2	W

Table 2. Thermal data

Symbol	Description	Value	Unit
R_{thJA}	Thermal Resistance Junction to ambient (mounted on demoboard)	45	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction operating temperature range	-10 to 125	°C

3 Block & pin connection diagrams

Figure 2. Pin connection diagram (top view)

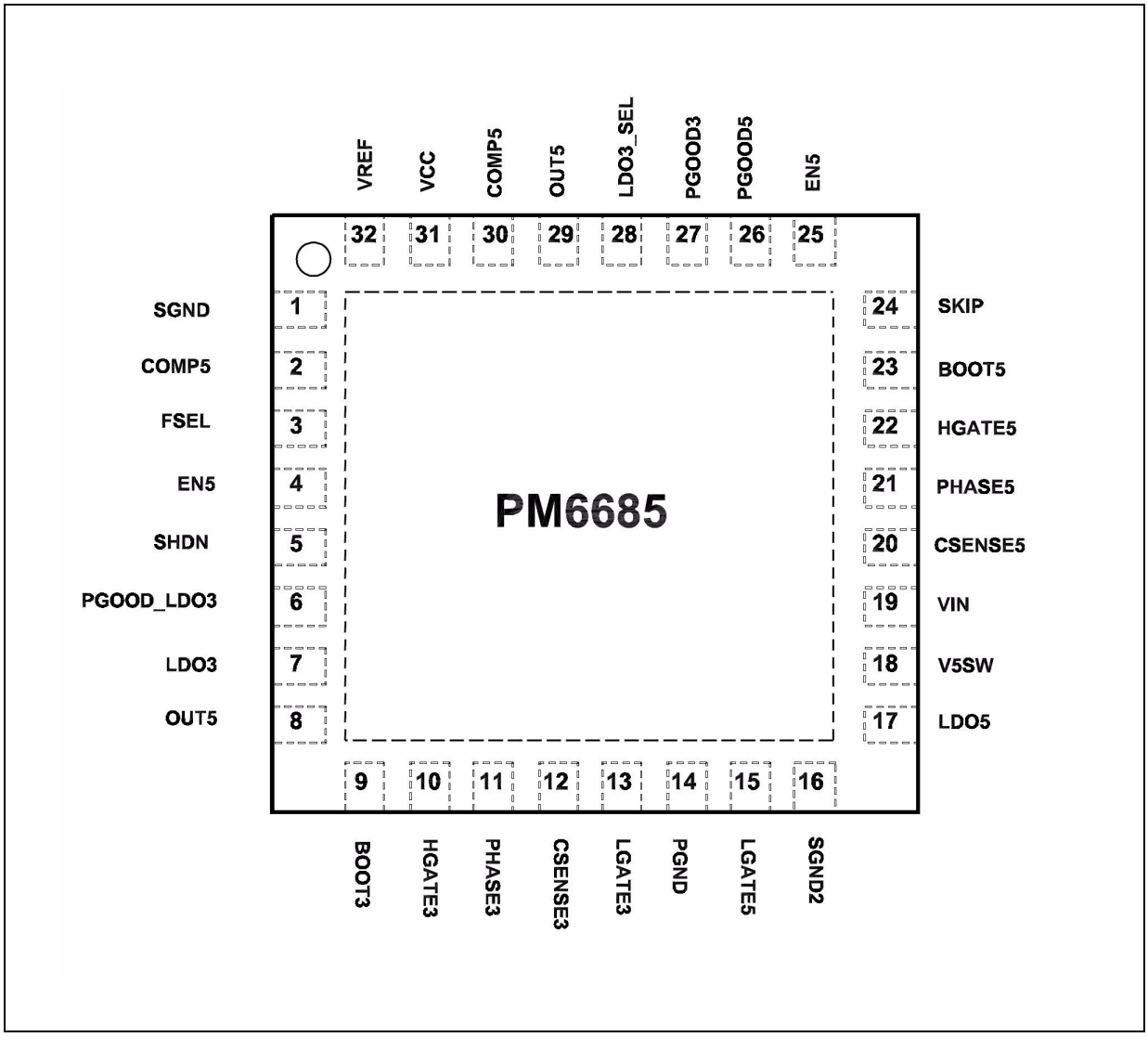


Table 3. Pin description

Pin No	PM6685	Function
1	SGND	Signal ground. Reference for internal logic circuitry.
2	COMP3	DC voltage error compensation pin for the 3.3V switching section.
3	FSEL	Frequency selection pin. It provides a selectable switching frequency, allowing either 200kHz/300kHz, 300kHz/400kHz or 400kHz/500kz operation of the 5V/ 3.3V switching sections.
4	EN3	3.3V SMPS enable input. The 3.3V section is enabled appling a high logic level (>2.4V) to this pin, while is disabled appling a low logic level (<0.8V). When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. If both EN3 and EN5 pins are low and SHDN pin is high the device enters in standby mode.
5	SHDN	Shutdown control input. The device enters its shutdown mode with 9µA of supply current if VSHDN is less than the device off threshold voltage and doesn't restart until VSHDN is greater than the device on threshold voltage. The SHDN pin can be connected to Vbatt through a voltage divider to program an undervoltage lockout. In shutdown mode, the gate drivers of the two switching sections are in high impedance.
6	PGOOD LDO3	Power Good ouput signal for the 3.3V linear regulator. This pin is an open drain output. It is shorted to GND if LDO3_SEL pin is at its low level or if the ouput voltage on LDO3 pin is lower than 2.6V.
7	LDO3	3.3V Linear regulator output. LDO3 can provide 100mA peak current. If LDO3_SEL pin is connected to VREF and OUT3 is greater than the LDO3 bootstrap switch threshold, the LDO3 regulator shuts down and the LDO3 pin will be directly connected to OUT3 through a 3 (max) switch. If LDO3_SEL pin is at its low level the LDO3 is always OFF. If LDO3_SEL pin is at its high level the LDO3 is always ON.
8	OUT3	Output voltage sense for the 3.3V switching section.This pin must be directly connected to the output voltage of the switching section.
9	BOOT3	Bootstrap capacitor connection for the switching 3.3V section. It supplies the high-side gate driver.
10	HGATE3	High-side gate driver ouput for the 3.3V section.
11	PHASE3	Switch node connection and return path for the high side driver for the 3.3V section.
12	CSENSE3	Current sense input for the switching 3.3V section. This pin must be connected through a resistor to the drain of the synchronous rectifier (RDSON sensing) or to the source of the synchronous rectifier (RSENSE sensing) to set the current limit threshold.
13	LGATE3	Low-side gate driver output for the 3.3V section.
14	PGND	Power ground.
15	LGATE5	Low-side gate driver output for the 5V section.
16	SGND2	Signal ground for analog circuitry.
17	V5SW	Internal 5V regulator bypass connection. When the main 5V ouput voltage is greater than the boostrap switch threshold, the LDO5 regulator shuts down and the LDO5 pin will be directly connected to OUT5 through a 3 (max) switch. If not used, it must be tied to ground.

Table 3. Pin description

18	LDO5	5V internal regulator output. LDO5 pin supplies all gate drivers, the internal circuitry and an external load. It can provide up to 100mA peak current.
19	VIN	Device input supply voltage. A bypass filter (4 Ω and 4.7 µF) between the battery and this pin is recommended.
20	CSENSE5	Current sense input for the switching 5V section. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) or to the source of the synchronous rectifier (R_{SENSE} sensing) to set the current limit threshold.
21	PHASE5	Switch node connection and return path for the high side driver for the 5V section.
22	HGATE5	High-side gate driver ouput for the 5V section.
23	BOOT5	Bootstrap capacitor connection for the switching 5V section. It supplies the high-side gate driver.
24	SKIP	Pulse skipping mode control input. It is a three states pin. If the pin is at its high level(e.g. cnnected to LDO5) the PWM mode is enabled. If the pin is at its low level (e.g. connected to GND), the pulse skip mode is enabled. If the pin is at its middle level (e.g. connected to Vref) the pulse skip mode is enabled but limiting the min frequency to 25KHz.
25	EN5	5V SMPS enable input. The 5V section is enabled appling a high logic level (>2.4V) to this pin, while is disabled appling a low logic level (<0.8V). When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. If both EN3 and EN5 pins are low and SHDN pin is high the device enters in standby mode.
26	PGOOD5	Power Good ouput signal for the 5V section. This pin is an open drain ouput. The pin is pulled low if the output is disabled or is out of the specified window (approximately +/- 10% of its nominal value).
27	PGOOD3	Power Good ouput signal for the 3.3V section. This pin is an open drain ouput. The pin is pulled low if the output is disabled or is out of the specified window (approximately +/- 10% of its nominal value).
28	LDP3SEL	Control pin for the 3.3V internal linear regulator. This pin determines three operative modes for the LDO3. If LDO3_SEL pin is at its low level the LDO3 is always OFF. If LDO3_SEL pin is at its high level the LDO3 is always ON If LDO3_SEL pin is connected to VREF and OUT3 is greater than the LDO3 bootstrap switch threshold, the LDO3 regulator shuts down and the LDO3 pin will be directly connected to OUT3 through a 3 (max) switch.
29	OUT5	Output voltage sense for the 5V switching section.This pin must be directly connected to the output voltage of the switching section.
30	COMP5	DC voltage error compensation pin for the 5V switching section.
31	V_{CC}	Device Supply Voltage pin. Connect this pin to LDO5
32	VREF	High accuracy output voltage reference (1.237V). It can deliver 50uA. Bypass to SGND with a 100nF capacitor.

4 Electrical characteristics

(V_{IN} = 12V; T_{amb} = 0°C to 85°C unless otherwise specified)

Table 4. Supply section

Simbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	V_{out}=V_{ref}, LDO5 in regulation	6		28	V
V_{CC}	IC supply voltage		4.5		5.5	V
V_{V5SW}	Turn-on voltage threshold			4.8	4.9	V
	Turn-off voltage threshold		4.6	4.75		V
	Hysteresis			50		mV
V_{V5SW}	Maximum operating range				5.5	V
$R_{DS(on)}$	LDO5 Internal Bootstrap Switch Resistance	V5SW >4.9V		1.8	3	Ω
$R_{DS(on)}$	LDO3 Internal Bootstrap Switch Resistance	VOUT3 = 3.3V		1.8	3	Ω
	OUT_ Discharge-Mode On-resistance			12	25	Ω
	OUT3, OUT5_ Discharge-Mode Synchronuos Rectifier Turn-on level		0.2	0.35	0.5	V
Pin	Operating Power consumption	VOUT5>5.1V,VOUT3>3.34V V5SW to 5V LDO5, LDO3 no load			4	mW
Ish	V_{IN} Shutdown Current	SHDN connected to GND,		14	18	µA
Isb	V_{IN} Standby Current	ENx to GND, V5SW to GND		150	250	µA

Table 5. Shutdown section

Simbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SHDN}	Device ON threshold		0.95	1.35	1.6	V
	Device OFF threshold		0.8	0.85	0.9	V

Table 6. Electrical characteristics (continued)

Simbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
	Soft Start Ramp time			2		6	ms
I_{CSENSE}	Input bias current limit			90	100	110	µA
	Comparator offset	V_{CSENSE} - V_{PGND}		-5		5	mV
	Zero Crossing Comparatot Offset	V_{PGND} - V_{PHASE}		-5		5	mV
	Fixed Negative current limit Threshold	V_{PGND} - V_{PHASE}			-120		mV
T_{ON}	ON-Time duration	FSEL to GND	OUT5=5V		2083		ns
			OUT3=3.3V		917		
		FSEL to VREF	OUT5=5V		1390		
			OUT3=3.3V		688		
		FSEL to LDO5	OUT5=5V		1040		
			OUT3=3.3V		550		
T_{OFFMIN}	Minimum OFF-Time				300	350	ns
V_{REF}	Voltage Accuracy	4.2V < V_{LDO5} < 5.5V		1.224	1.237	1.249	V
	Load regulation	-100µA < I_{REF} < 100µA		-4		4	mV
	Undervoltage Lockout fault threshold	Falling edge of REF				0.95	V
COMP	Over voltage clamp				250		mV
COMP	Under voltage clamp				-150		
	Line regulation	Both SMPS, 6V< V_{IN} <28V				0.004	%/V
V_{LDO5}	LDO5 linear Output Voltage	6V < V_{IN} < 28V, 0 < I_{LDO5} < 50mA		4.9	5.0	5.1	V
	LDO5 line regulation	6V < V_{IN} < 28V, I_{LDO5} = 50mA LDO3_SEL tied to GND				0.004	%/V
I_{LDO5}	LDO5 Current limit	V_{LDO5} > UVLO, I_{LDO3} = 0A V_{OUT5} > 5.1V, V_{OUT3} > 3.34V		300	350	400	mA
UVLO	Under Voltage Lockout of LDO5			3.94	4	4.13	V
V_{LDO3}	LDO3 linear Ouput Voltage	0 < I_{LDO3} < 50mA		3.23	3.3	3.37	V
I_{LDO3}	LDO3 Current limit	V_{LDO5} > UVLO		130		200	mA
	HGATE driver on-resistance	HGATEx high state(pullup)			2.0	3	Ω
		HGATEx low state (pulldown)			1.8	2.7	Ω
	LGATE driver on-resistance	LGATEx high state(pullup)			1.4	2.1	Ω
		LGATEx low state (pulldown)			0.6	0.9	Ω

Table 6. Electrical characteristics (continued)

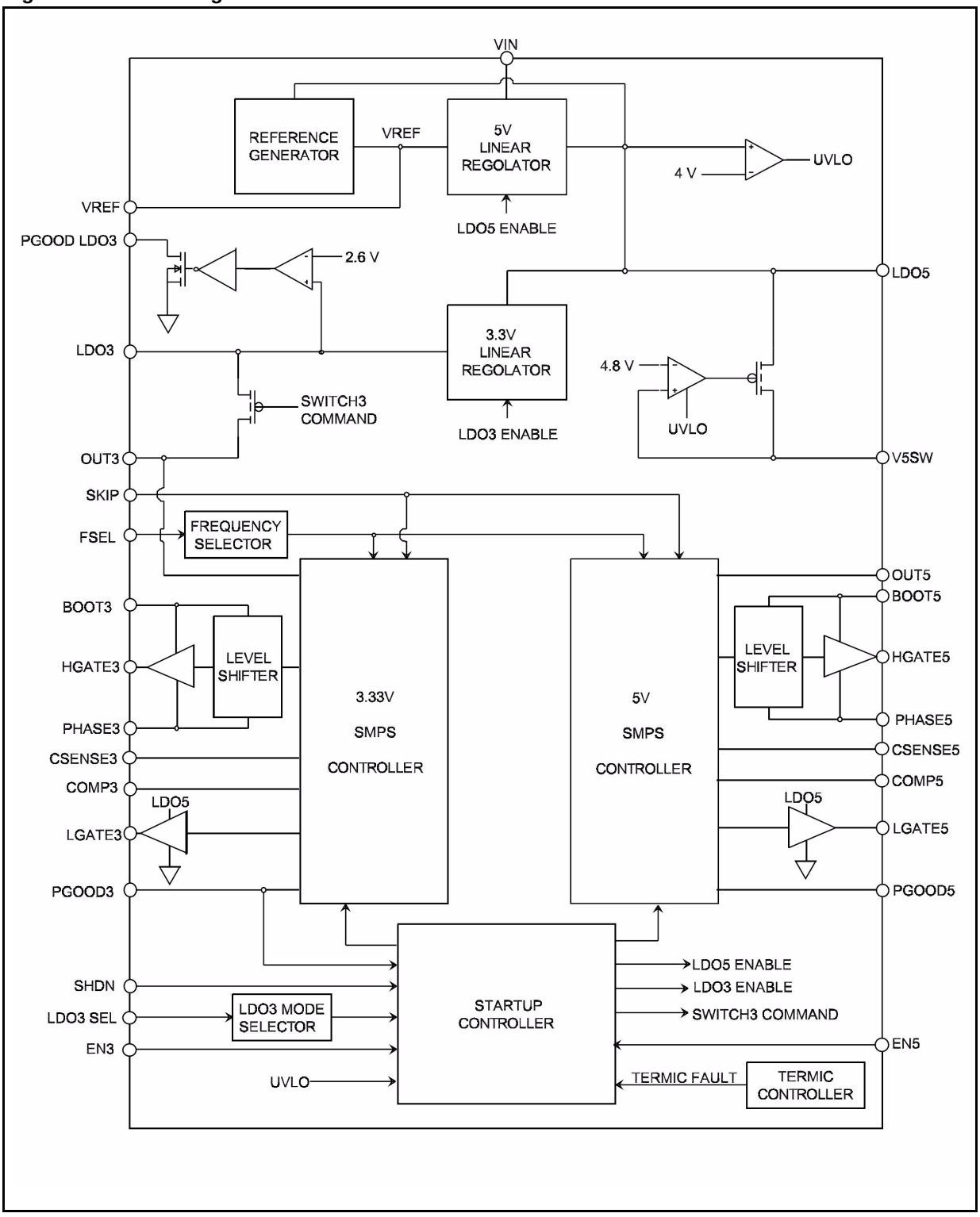
Simbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	High side rise time	HGATEx-PHASE from 1V to 4V CLOAD = 3.3nF			20	ns
	High side fall time				20	
	Low side rise time	LGATEx-PGND from 1V to 4V CLOAD = 8.2nF			40	ns
					40	
OVP	Over voltage threshold	Both SMPS sections with respect to VREF.	113	116	120	%
UVP	Under voltage threshold		66	70	72	%
PGOOD3,5	Upper threshold (VFB-VREF)		107	110	113	%
	Lower threshold (VFB-VREF)		90	92	94	%
$I_{PGOOD3,5}$	PGOOD leakeage current	VPGOOD3,5 forced to 5.5V			1	µA
$V_{PGOOD3,5}$	Ouput Low Voltage	ISink = 4mA		150	250	mV
PGOOD LDO3	Rising voltage threshold			2.58		V
	Falling voltage threshold			2.55		V
	Hytseresis			25		mV
I_{PGOOD_LDO3}	PGOOD leakeage current	$V_{PGOOD\ LDO3}$ forced to 5.5V			1	µA
V_{PGOOD_LDO3}	Ouput Low Voltage	ISink = 4mA		150	250	mV
T_{SDN}	Shutdown Temperature				150	°C
EN3,5	SMPS disabled level				0.8	V
	SMPS enabled level		2.4			
FSEL	Frequency selection range	Low level			0.5	V
		Middle level	1.0		V_{LDO5} -1.5	
		High level	V_{LDO5} -0.8			
LDO3 SEL	3.3V Linear Regulator Selection Pin	Always-off level			0.5	V
		Boostrap level	1.0		V_{LDO5} -1.5	
		Always-on level	V_{LDO5} -0.8			
SKIP	Pulse Skip Mode				0.5	V
	PWM Mode		1.0		V_{LDO5} -1.5	
	Ultrasonic Mode		V_{LDO5} -0.8			

Table 6. Electrical characteristics (continued)

Simbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{LEAK}	Input leakage current	$V_{EN3,4}$ = 0 to 5V			TBV	µA
		V_{SKIP} = 0 to 5V			TBV	
		V_{SHDN} = 0 to 5V			TBV	
		V_{FSEL}= 0 to 5V			TBV	
		V_{LDO3_SEL} = 0 to 5V			TBV	

5 Functional & block diagram

Figure 3. Block diagram



6 Package Mechanical Data

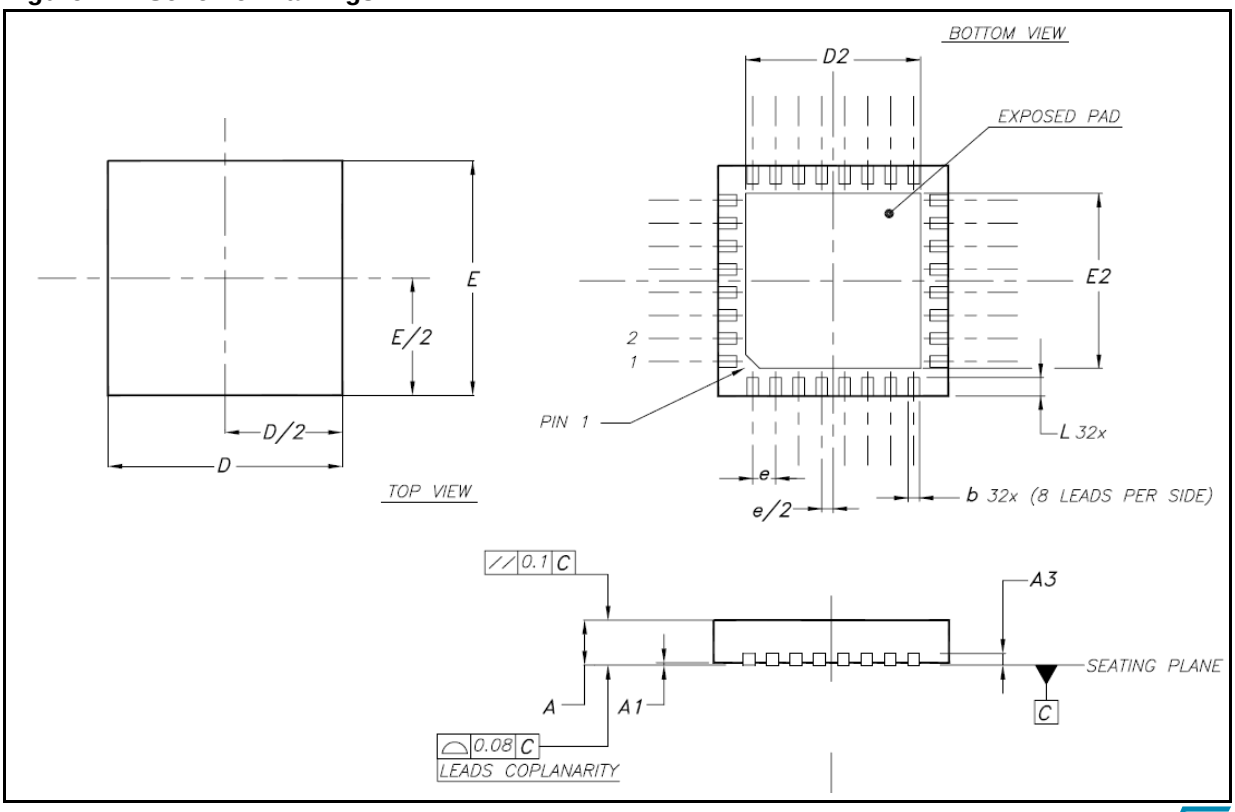
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 7. VFQFPN 5x5x1.0 32L Pitch 0.50

Dim.	Databook (mm.)			Drawing (mm.)		
	Min.	Typ.	Max	Min.	Typ.	Max
A	0.80	0.90	1.00	0.80		1.00
A1	0	0.02	0.05	0		0.05
A3		0.20			0.25	
b	0.18	0.25	0.30	0.225		0.275
D(3)	4.85	5.00	5.15	4.90	5.00	5.10
D2(5)	3.65		3.95	3.65		3.95
E(3)	4.85	5.00	5.15	4.90	5.00	5.10
E2(5)	3.65		3.95	3.65		3.95
e		0.50			0.50	
L	0.30	0.40	0.50	0.35		0.45

1. – VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead.
   Very thin: A = 1.00mm Max.
2. – The leads size have been increased by Pb/Sn thickness in tin plating electrolytic process.
3. – Dimensions D & E do not include mold protusion, not to exceed 0,15mm.
4. – Package outline exclusive of metal burr dimensions.
5. – Dimensions D2 & E2 are not in accordance with JEDEC.

Figure 4. Scheme Drawings



7 Revision history

Date	Revision	Changes
23-Sep-2005	1	Initial release.