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PM7325

S/UNI®-ATLAS-3200

2488 Mbit/s SATURN® User Network Interface ATM Layer Solution

Data Sheet

Proprietary and Confidential

Preliminary

Issue 4: June 2001

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Public Revision History

Issue No.	Issue Date	Details of Change
1 Draft 1 Draft 2 Draft 3 Draft 4 Draft 5	 May 1999 June 1999 Aug 1999 Aug 1999 Sep 1999	 Initial draft. Added detailed functional description, register listing,functional timing. Aligns with newest 2-chip Embedded-DRAM Solution. Corrected and updated information on UL3 and POS interfaces, per-PHY counting, packet bypass, routing of APS cells. Added Operations Section. TAT and PHYTAT increased to 34 bits. Backwards VCRA and PHYID moved to Linkage Row to help make room. Policing Reserved moved to Row 1 and Parity to Row 0, also to make room. Frame counts added to per-PHY policing. Core Logic Voltage changed to 1.8V. I/O voltage clarified to be 3.3V. Parity added on Address of SRAM as well as data. Pin and block diagrams corrected. PHYID added to Secondary Key. Field B expanded from 11 to 12 bits. Unused bits in Search Table and Linkage Row redistributed to easily accommodate future expansion. Drop_VC does not permit the generation any cells on that connection, whether to OCIF or BCIF. Operation of MCR in GFR policing clarified to explicitly state that MCR operations are performed on frame boundaries only. AUTO_RDI becomes a per-VC bit. DRAM bank number changed to the 2 LSBs of the VCRA rather than the 2 MSBs. Per-PHY counts updated to include counts of EFCI and Timed-Out cells. SRAM, DRAM, per-PHY policing, and PM microprocessor accesses adjusted to access entire records at once, and to have per-field write and Clear-On-Read masks. Basic description of DRAM and SRAM bandwidth allocation added. Gen_halfsecclk bit moved to CP. Slow Background Processing Interrupt added. Capability to switch Input BCIF to Slave mode for use with testers added. Placement of interrupts in Utopia/POS and SDQ blocks changed. Burst length set to a maximum of 256 bytes. Buffer Available thresholds set to a max of 511 bytes. Package changed from 432 TBGA to 576 TBGA to add power/ground balls. Documented separate 1.5V supply for the DRAM. Lower bound of temperature range changed to 0 degrees C. Address map adjusted for easier decode. Added APS cell routing back in.

Issue No.	Issue Date	Details of Change
2	Feb 2000	Core logic changed to 1.5V. VC Table parity replaced with CRC-10. "Bwd PM Pending" bit extended for use with Fwd PM Permission cells. VPRMSEL replaced with the more descriptive VP_RM_PTI6. Search key diagrams corrected of typos. Added 1 reserved bit to Source field of Count Rollover FIFO. Fixed TPU_ADDR signal in Figure 6. Fixed PM RAM access ClearOnRd defaults. Removed DMA Request Enable. Moved DMAREQINV to the MCIF. Renamed all references to DMA REQ correctly. Added UPURS_to_OCIF. Added 1 bit to Cell Type field of UPURS and BCIF causation words to add many more cell types. Deleted 1 bit from source ID of the BCIF causation word to make room. Changed all references to AUTOAIS to AUTO_AIS to ensure consistency. Added APStoBCIF and ActDeToBCIF bits. InactivetoUP applies to connections disabled due to CRC errors. Bwd LB cells are not routed to the micro at flow end-points unless the source ID matches the programmed Loopback Location ID, unless the Bwd_LB_to_UP_at_End bit is logic 1. XCLK added to Clock Activity monitor. Device now powers-up in reset, must be held there to allow the DRAM to settle for 200 us. Per-PHY counting bit descriptions of Cnt_Inv_OAM and Cnt_Rsvd_VCI_PTI corrected. Added VPC Counting. Added Policing Rollover FIFO Enable bits. Added FREE[7:0]. Added LBtoOCIF. Added RxPHYTxPHY internal test bit. Made Maximum Frame Length test disabled if MFL = all ones, to match ATLAS. Added feature for allowing CC alarms to not generate COS entries, via the OAM Config status bit. Added a globally enabled feature that permits Bwd PM cells to carry the Fwd PM Cell's time stamp, if the Bwd PM cell is able to be generated immediately. Added Don't-Touch designation for OC-48C cascading. SDQ register map substantially reorganized. Meanings of Buffer Available and Data Available thresholds changed slightly. SDQ per-PHY counts reduced to 4 bits; aggregate cell count increased to 32 bits. Added generic names for UL3/PL3 pins for easier reference. INBANDADDR function added to PL3 blocks to accommodate single-PHY operation. Updated SRAM configuration diagrams and descriptions to reflect xclk/sclk_o/sysclk scheme. Updated SRAM AC and Functional timing to illustrate relationship of SCLK_O, SYSCLK. Reduced VC depth to 64K VCs from 128K VCs. Updated PL3 pin descriptions to match latest POS-PHY release (release 4). Added PL3/UL3 AC timing. Clarified the meaning of "noting" non-compliant cells in policing by saying "just counted". Documented fact that packet counting is based on CLP of EOM. Updated references to other documents (ATLAS, UL3, I.610). Corrected formatting of COS FIFO, and simplified the bit description. Corrected the reset value of Per-PHY Processing Enable Register 2.

Issue No.	Issue Date	Details of Change
3	Oct 2000	Clarified that UPURS_to_OCIF overrides XPREPO, and that PROC_CELL or PROCESS_PHY overrides XPREPO. Absolute Maximum ratings updated (SRAM interface specced relative to VDD25; absolute min voltage changed to –0.3, absolute max to VDDx+0.3, Max current on pins reduced to 10mA). Clarified translation options to BCIF. Added Mkt_NUM register in ID register. Added dropped-cells counter on MCIF. Added note that reserved fields in the Search and Linkage tables must be programmed to logic 0 for proper operation. Adjusted format of Count Rollover FIFO. Added extra notes about the restriction on the 2 LSBs of the VPC Pointer. Changed Inact_on_Par_Err to Inact_on_DRAM_Err. Corrected RxL, TxL Indirect Address register. Increased min prop delay on UL3/PL3 to 1.5 ns. Changed package from 576 to 768 TBGA. Split SCLK_O into SYSCLK_O and SRAMCLK_O. Added Timeout_To_UP bit to Register 0x100. Renamed AIS_VPC to Sending_AIS. Changed COS fifo description to show all bits. Renamed a few of the CP interrupts to have more expressive names. Clarified that Returned LB cells are translated like other generated cells (RDI and Bwd PM). Renamed F4toF5AIS to F4toF5OAM to reflect the fact it controls both AIS and RDI. Clarified the difference between Block_Ptr and FIFO_Number in the SDQ Configuration description. Clarified that Ete Loopback cells are looped back at end-to-end points if their LLID = all 1, or if it matches the LLID of the end point. Modified Sat_PM_BIP16 to Sat_Fast_PM_Counts and made it affect the Lost PM Cell Counts as well. Changed drop_vc to have no effect on the generation of OAM cells to the BCIF. F5 AIS cells due to F4 AIS carry the F4 AIS defect location/type. When F4-to-F5, per-PHY or CC AIS is generated, then if ATLAS is within a segment for that VC, both Segment and ETE AIS are generated. Changed “SCSB” to “SCEB” for consistency. Fixed an inconsistency in fm_interrupt_enable naming. Corrected description of EFCI count. Updated PM documentation to better reflect behavior with SECBs. Added documentation that Count Rollover for lost PM cell counts can be suppressed. Corrected definition of reserved vpi/vci. Clarified allowable settings of Action 1 and Action 2 in GFR policing. Note added that 2.5V I/Os are not 3.3V tolerant. SDQ register map and configuration dramatically simplified: eliminated FIFO numbers, buffer thresholds become fixed, banks eliminated, block size increased, starting point restrictions removed, interrupts reorganized. SDQ per-PHY cell counter measures fill level rather than throughput. Updated the TxLink documentation. Produced much more precise definitions of PTPA and STPA on both input and output. Bwd VCRA moved from Linkage row to VC Table Row 0. Added BCIF AC timing. RDB low to microprocessor data valid propagation delay increased to 30 ns. RDB high to microprocessor data tristate extended to 13 ns. WRB high to Microprocessor Data hold time extended to 3 ns. SRAMCLK_O to SRAM output data and control valid extended from 4.5 to 5.5 ns (SRAM setup is 1.5 ns, allowing 1 ns slack). Added minimum XCLK frequency. Power tolerances set to 0.3V on 3.3V power, 0.2V on 2.5V power, 0.075 on 1.5V power. Added per-VP policing.

Issue No.	Issue Date	Details of Change
4		Revealed COS_CC_DIS bit. Changed ATM_FIELD default to 0x00. Documented the fact that micro accesses can take as long as 40 cycles (for a read) or 90 cycles (for a write) in certain unusual cases. IBCIF and OBCIF default to odd parity, not even parity. PHY and Link blocks should be left in their default state when not being used. Typo to INSRST corrected. Direction of OBCIF, IBCIF clocks in figures 5,6,7,8 corrected. INSRDY documentation corrected to say that INSRDY stays high until a full cell has been written in. Halfsecclk input pin description altered to point correctly to the gen_halfsecclk bit. Documented the proper default state for the one-second CC, AIS, and Failure counts. Updated Boundary Scan description to match BSDL notation. Clarified that SDQ, PHY, and LINK interrupts are only asserted for interrupts that are enabled at the TSB level. Clarified that min freq for icif_clk and ocif_clk is 75 MHz, but that full bandwidth is only guaranteed at 104 MHz. Block size of 1 in Bypass SDQ explicitly not supported. OBCIF dropped-cells counter exposed, with a comment about the total BCIF capacity. VC_to_BCIF documented with the overflow mechanism. RxPhy calendar now states that it should be set to at least 64 entries, and preferably as close to 128 entries as possible, for maximum efficiency. Clarified that LBtoOCIF also overrides discarding due to LB_Route functionality. Clarified DLLRUN Bit functionality. Deleted XferErrToUP function; parity errors and rlp_err/tpp_err indications have no effect on ATM cells (beyond the assertion of an interrupt for a parity error). Recommended that the FLUSH bit be set for all disabled FIFOs, to eliminate spurious interrupts. Clarified that CntUndefOAM has no effect on OAMERRI. Increased maximum secondary search depth to 18. Changed PL3 loading to 30 pf to match the PL3 standard. Changed voltage rail spec. to +/-5%. Clarified that FM_to_UP does not control loopback cells, since LB_ROUTE does this. Added TM0 Details. Added thermal information. Specified max power at 3.0 W. Input High Current respecified to –15 uA/+650 uA on 3.3 V interface.

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1 Definitions

This table defines the acronyms used in this data sheet.

Acronym	Definition
AIS	**Alarm Indication Signal.** AIS cells are OAM Fault Management cells whose Function Type fields identify them as AIS cells as per ITU-T I.610. They are sent once per second by an ATM Network Element which has detected certain error conditions, such as a loss of continuity. AIS alarm refers to the detection that the S/UNI-ATLAS-3200 is receiving AIS cells on a particular VC.
BT	**Burst Tolerance.** The burst tolerance is a policing parameter that indicates the maximum length of a burst (at the peak allowable cell rate) that is permitted before the Sustained Cell Rate test will be violated.
Bwd PM	**Backwards Performance Management Cell.** These PM OAM cells are sent by a PM session on reception of a Fwd PM cell, and carry data about the cell flow as observed by both the start and end point of the PM flow.
Bwd LB	**Backwards, or Returned Loopback Cell.** An OAM Loopback cell whose Loopback Indication bit is zero, indicating it has already been looped back.
CBR	**Constant Bit Rate.** CBR service is one of the standard traffic contracts, in which a constant, unchanging amount of bandwidth is guaranteed to the user, with time-of-delivery guarantees. Voice traffic is a classic use of CBR service
CDV	**Cell Delay Variation.** The CDV Tolerance is one of the parameters that determines the policing parameters, particularly the Limit parameter of the Peak Cell Rate test.
CLP	**Cell Loss Priority.** This is a field in the header of an OAM cell. High-priority cells are those with CLP = 0, and are sometimes referred to as CLP0 cells. Low priority blocks are sometimes referred to as CLP1 cells, and the aggregate flow is referred to as CLP0+1.
CC	**Continuity Check.** CC cells are OAM Fault Management cells whose Function Type fields identfy them as CC cells as per ITU-T I.610. They are sent once per second by a flow start point in the absence of user traffic, to indicate that the connection remains active. CC alarm refers to the detection that a VC on the S/UNI-ATLAS-3200 has received neither user cells nor CC cells for a nominal period of 3 seconds.
F4	The F4 OAM Layer is the OAM Layer associated with the Virtual Path. In S/UNI-ATLAS-3200, a VC may be part of an F4 flow or an F5 flow. In the case of an F4 flow being sourced or terminated, a number of VCs which form part of F5 flows may have an associated F4 OAM VC, which performs the OAM for the F4 flow. This F4 OAM VC is specified by the VPC Pointer in the Linkage Table.
F5	The F5 OAM Layer is the OAM Layer associated with the Virtual Channel.
FM	**Fault Management.** Fault Management OAM cells include AIS cells, RDI cells, CC cells, and LB cells.
Fwd LB	**A Forward, or Parent, Loopback cell.** An OAM Loopback cell whose Loopback Indication bit is 1, indicating it has not yet been looped back.
Fwd PM	**Forward Performance Management cell.** These PM OAM cells are sent by a PM session at an OAM start point every N cells, where N is a programmable number ranging from 128 to 32K. They contain information about the cell flow on a VC as seen by the transmitting point.
GCRA	**Generic Cell Rate Algorithm.** The GCRA is the “Leaky Bucket” policing algorithm described in ITU-T I.371.

Acronym	Definition
GFC	**Generic Flow Control.** At the UNI, a congestion-control flow called GFC is used. The GFC field occupies the most significant 4 bits of each ATM cell. At the Network-Network Interface, these 4 bits are used for VPI instead.
GFR	**Guaranteed Frame Rate.** GFR is one of the standard traffic contracts (like CBR, VBR, and ABR) and is a frame-aware standard supporting AAL5 partial packet discard. S/UNI-ATLAS-3200 supports GFR policing.
LB	**Loopback.** Loopback cells are OAM cells used to test the connectivity of the network, usually during call setup or diagnostics. They are inserted into the network, and looped back at network nodes based on the content of their loopback location ID. When loopback cells are first inserted, they are referred to as Parent Loopback cells. Once looped back (indicated by the Loopback Indication field being zero) they are referred to as Returned Loopback cells.
MCR	**Minimum Cell Rate.** MCR is a parameter of Guaranteed Frame Rate (GFR) traffic contracts. It is analogous to the Sustained Cell Rate (SCR) parameter, but is only enforced at frame boundaries.
NNI	**Network-Network Interface.**
NPC	**Network Parameter Control.** NPC is defined as the set of actions taken by the network to monitor and control traffic at the Network-Network interface. NPC is what the standards call policing at an NNI. The main purpose of UPC and NPC is to protect network resources from malicious as well as unintentional misbehavior, which can affect the QoS of other already established connections, by detecting violations of negotiated parameters and taking appropriate actions. Such actions may include cell discard and cell tagging.
OAM	**Operations And Maintenance.** OAM cells include Fault Management, Performance Management, Loopback, Activate/Deactivate, and System Administration cells, as well as other non-standard cells whose VCI or PTI identify them as OAM cells as per ITU-T I.610.
Parent LB	**A Parent, or Forward, Loopback cell.** An OAM Loopback cell whose Loopback Indication bit is 1, indicating it has not yet been looped back.
PCR	**Peak Cell Rate.** The PCR is a parameter of most traffic contracts, and is enforced by the policing (UPC/NPC) functions of the device.
PHY	A Physical layer device, or a cell queue associated with a physical-layer interface.
PM	**Performance Management.** PM is a process whereby cells are transmitted over a VC, carrying information about the traffic from the point of view of the start point and end point. From the comparison of the two, statistics about the performance of the connection can be maintained.
PTI	**Payload Type Identifier.** The PTI is a 3-bit cell field that immediately follows the VCI, and is used to identify the cell type for VCCs.
RDI	**Remote Defect Indication.** RDI cells are generated once per second by an OAM end point, and looped back to be sent in the reverse direction, to indicate that AIS cells have been received at that end point.
Rtd LB	**A Returned, or Backwards, Loopback cell.** An OAM Loopback cell whose Loopback Indication bit is zero, indicating it has already been looped back.
Rx Link	When configured as an Ingress device, the input of the S/UNI-ATLAS-3200 acts as a Link Layer device as defined in the UTOPIA Level 3 and POS-PHY3 specs, and connects to a PHY. This interface is a Master interface in UL3, and a Slave interface in POS-PHY3.
Rx PHY	When configured as an Ingress device, the output of S/UNI-ATLAS-3200 acts as a PHY layer device as defined in the UL3 and POS-PHY Level 3 specs, and connects to a TM or switch that acts as a Link Layer device. This interface is a Slave interface for UL3, and a Master interface for POS-PHY Level 3.
SCR	**Sustained Cell Rate.** The sustained cell rate is a parameter of some traffic contracts, and indicates the maximum throughput that may be sustained over a long period of time.

Acronym	Definition
	It is typically paired with a Peak Cell Rate (PCR) parameter, and is enforced by the policing (UPC/NPC) functions of the device.
TM	**Traffic Management.** A Traffic Management device may be connected to the switch side of the S/UNI-ATLAS-3200.
Tx Link	When configured as an Egress device, the output of S/UNI-ATLAS-3200 acts as a Link Layer device as defined in the UTOPIA Level 3 and POS-PHY Level 3 specs, and connects to a PHY. This interface is a Master interface for both UL3 and POS-PHY3.
Tx Master	On the Egress PHY side, the UTOPIA and POS-PHY interfaces act as a master, controlling the transfers to the PHY. This interface is also referred to as the Tx Link interface.
Tx PHY	When configured as an Egress device, the input of S/UNI-ATLAS-3200 acts as a PHY layer device.as defined in the UL3 and POS-PHY Level 3 specs, and connects to a TM or switch that acts as a Link Layer device. This interface is a Slave interface for both UL3 and POS-PHY Level 3.
Tx Slave	On the Egress System side, the UTOPIA and POS-PHY interfaces act as a slave; that is, S/UNI-ATLAS-3200 looks like a PHY from the point of view of the upstream device. This interface is also referred to as the Tx PHY interface.
TRCC	**Total Received Cell Count.** Used in Performance monitoring. A rolling 16-bit count of user cells (either CLP0, or CLP0+1) received by the Fwd PM sink point..
TUC	**Total User Cell [Count].** Used in Performance monitoring. A rolling 16-bit count of user cells (either CLP0, or CLP0+1) transmitted by the Fwd PM source.
TUCD	**Total User Cell Difference.** This is the difference between the number of cells transmitted in the block (as indicated in the fwd PM cell) and the number received. For example, TUCD0 = {[TUC0(t) – TUC0(t-1)] Mod 64K} - {[TRCC0(t) – TRCC0(t-1)] Mod 64K}.
UNI	**User-Network Interface.**
UPC	**Usage Parameter Control.** This is what the standards call policing at the User-Network Interface (UNI). The main purpose of UPC and NPC is to protect network resources from malicious as well as unintentional misbehavior, which can affect the QoS of other already established connections, by detecting violations of negotiated parameters and taking appropriate actions. Such actions may include cell discard and cell tagging.
VC	**Virtual Connection.** VCs may be Virtual Path Connections (VPCs) or Virtual Channel Connections (VCCs). Each bidirectional VC serviced by S/UNI-ATLAS-3200 has one VC Record in context memory in each direction.
VCC	**Virtual Channel Connection.**
VCRA	**Virtual Connection Record Address.** This is the address of the VC's context table in memory. While it is listed as 17 bits, the MSB must be logic 0 in the S/UNI-ATLAS-3200.
VPC	**Virtual Path Connection.**

2 Features

The S/UNI®- ATLAS-3200 device is a monolithic, single chip device that handles ATM Layer functions for one direction including VPI/VCI address translation, cell appending, cell rate policing, per-connection counting, and I.610-compliant OAM requirements for 64K VCs (virtual connections). Two or more S/UNI-ATLAS-3200 devices can be cascaded to support additional VCs. The device:

- Can be configured as an Ingress mode device or an Egress mode device.
- Supports a full duplex 16-bit SCI-PHY™ Backwards Cell Interface Port that allows an Ingress mode device and an Egress mode device to communicate and behave as a single bi-directional device. The SCI-PHY port is a UTOPIA Level 2, non-polled, cell handshaking interface that handles 64-byte extended cells with prepended routing information. This can also be described as a 16-bit, 52 MHz UTOPIA Level 1 interface, with prepended routing information.
- With its instantaneous transfer rate of 3200 Mbit/s, it supports a cell transfer rate of 5.68×10^6 cells/s (e.g. one STS-48c or four STS-12c streams).
- When configured as an Ingress mode device:
  - The Input interface supports a 32-bit 104 MHz UTOPIA Level 3 Link Layer (Master) interface using Multi-PHY addressing with user-programmable weighted polling for up to 48 PHY queues on a single physical port. Extended ATM cell lengths of 52 to 64 bytes are supported, with optional HEC/UDF, prepend, and postpend words. Mapping of physical PHYs to logical PHYs is supported, to facilitate Automated Protection Switching.
  - The Output interface supports a 32-bit 104MHz UTOPIA Level 3 PHY Layer (Slave) interface using Multi-PHY handshaking for up to 48 PHY sources. Extended ATM cell lengths of 52 to 64 bytes are supported, with optional HEC/UDF, prepend, and postpend words. A non-polled, direct mode is also supported for this interface.
  - Alternately, the Input Interface supports a 32-bit 104 MHz POS-PHY™ Level 3 Rx Link Layer interface, capable of handling a mix of packets and ATM cells. Each of 48 PHY queues on a single physical port must be set up to carry either packets or cells. Cells are processed by S/UNI-ATLAS-3200, but packets are not processed and are buffered and passed through transparently. In this case, the Output interface supports a 32-bit 104 MHz POS-PHY Rx PHY Layer interface.
- When configured as an Egress mode device:
  - The Input interface supports a 32-bit 104 MHz UTOPIA level 3 PHY Layer (Slave) interface using Multi-PHY handshaking for up to 48 PHY destinations. Extended ATM cell lengths of 52 to 64 bytes are supported, with optional HEC/UDF, prepend, and postpend words.

- The Output interface supports a 32-bit 104 MHz UTOPIA Level 3 Link Layer (Master) interface using Multi-PHY addressing with user-programmable weighted polling for up to 48 PHY queues on a single physical port. Extended ATM cell lengths of 52 to 64 bytes are supported, with optional HEC/UDF, prepend, and postpend words. Mapping of logical PHYs to physical PHYs is supported, to facilitate Automated Protection Switching.
- Alternately, the Input Interface supports a 32-bit 104 MHz POS-PHY Level 3 Tx PHY Layer interface, capable of handling a mix of packets and ATM cells. Each of 48 PHY queues on a single physical port must be set up to carry either packets or cells. Cells are processed by S/UNI-ATLAS-3200, but packets are not processed and are buffered and passed through transparently. In this case, the Output interface supports a 32-bit 104 MHz POS-PHY Tx Link Layer interface.

- Is compatible with a wide range of switching fabrics and traffic management architectures including per-VC or per-PHY queuing.
- Contains a highly-flexible CAM-type cell and connection identification, which can use arbitrary PHYID/VPI/VCI values and/or cell appended bytes for connection identification in both directions. 34-bits of discrimination allows the entire PHYID/VPI/VCI address range to be resolved.
- Includes header translation functions, permitting the translation of the VPI, VCI, and/or cell appended bytes. Information about the cell and connection type can be included in appended bytes in order to aid downstream processing.
- Provides comprehensive cell processing functionality, which includes a highly flexible search engine that covers the entire PHYID/VPI/VCI address range, programmable dual leaky bucket UPC/NPC, per-connection CLP0 and CLP1 cell counts (programmable), OAM-PM termination, generation and monitoring, OAM-FM termination, generation and alarm generation (monitoring), and OAM-LB address matching, termination, and loopback.
- Provides a Count Rollover FIFO greatly, which reduces the need to poll internal counts.
- Provides available AAL5 Frame counting via the policing counts.
- Provides per-PHY output buffering, which resolves head-of-line blocking issues.
- Provides a UPC/NPC function, which is a programmable dual leaky bucket policing device with a programmable action (tag, discard, or count only) for each bucket. A total of 3 programmable 16-bit non-compliant cell counts are provided. The non-compliant cell counts may be programmed to count, for example, dropped CLP0 cells, dropped CLP1 cells, and tagged CLP0 cells. The UPC/NPC function also has a *continuously violating* mode, where a programmable action is taken on all cells regardless of their compliance.
- Provides guaranteed Frame Rate policing, including AAL5 partial packet discard, so that the remainder of an AAL5 packet can be discarded if a single cell in the packet is discarded as a result of violating policing. AAL5 packets may also be completely tagged or discarded as appropriate. GFR policing is selectable on a per-connection basis.

- In addition to the per-connection dual leaky bucket, provides a single leaky bucket UPC/NPC function on a per-PHY basis. A programmable action (tag, discard or count only) may be configured for each PHY policing device. Three programmable non-compliant cell or frame counts are provided for each PHY. The non-compliant cell counts may be programmed to count, for example, tagged CLP0 cells, dropped cells, and dropped CLP0 frames. Frame counts are relevant either for GFR policing or for generic frame counting. The per-PHY policing parameters and non-compliant cell counts are maintained in an on-chip RAM that can be programmed and read via the 32-bit general purpose microprocessor interface.
- Allows groups of F5 connections to be policed in aggregate at the F4 level instead of at the F5 level, through the use of the VP_POLICE bit.
- Provides OAM-Fault Management on a per-connection basis. Simultaneous segment and end-to-end F4 and F5 AIS, RDI and CC cell generation, termination and monitoring is supported. Alarm bits and interrupt masks are provided on a per-connection basis. F4 to F5 AIS alarm splitting and F5 to F4 aggregation are provided. Paced insertion of FM cells is provided.
- Allows OAM-Loopback address identification, termination, and loopback to be per-connection configurable. Loopback cells may also be extracted to the microprocessor.
- Provides a high-speed 32-bit microprocessor bus for configuration, control, and status monitoring.
- Provides a FIFO buffered cell insertion and extraction capability via the microprocessor bus interface.
- Supports DMA access for cell extraction.
- Uses up to 16 Mbit/s of external Pipelined ZBT SRAM (with or without parity) for maintaining the data structure for the search tree. A 64 bit data + 8 bit parity 125 MHz bus interface is used to connect to the external SRAM.
- Uses internal DRAM for maintaining VC context information.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 0.18 micron, 1.5 V CMOS technology with 2.5 V embedded DRAM, 2.5 V external SRAM interface, and 3.3 V other external interfaces.
- 768 Tape BGA package.

2.1 Policing

- Policing is performed for adherence to peak cell rate (PCR), cell delay variation (CDV), sustained cell rate (SCR) and burst tolerance (BT). Violating cells can be dropped, tagged, or just counted.
- Policing is performed using the virtual scheduling Generic Cell Rate Algorithm (GCRA) described in ITU-T I.371.
- GFR policing as described in ATM Forum TM 4.1 is provided, with enforcement of PCR, MCR, CLP Conformance, and Maximum Frame Length.

- Two policing instantiations available per VC. The policed cell streams can be any combination of user cells, OAM cells, Resource Management, high priority cells or low priority cells.
- Per-PHY policing may also be enabled. Each of 48 PHY devices may have a single leaky bucket enabled, in addition to the dual leaky bucket of the connection. Violating cells or frames can be dropped, tagged, or just counted.
- When aggregating or terminating a VPC, policing may be performed on the VPC instead of the individual VCCs.

2.2 Performance Management

- The S/UNI-ATLAS-3200 device provides OAM-Performance Management functions in each of its two modes (Ingress Mode and Egress Mode). When an Ingress mode device is used in conjunction with an Egress mode device, the combination supports bi-directional PM sessions. A maximum of 512 PM sessions may be simultaneously active in one device. When using an Ingress mode + Egress mode device, the combination supports upto 512 bi-directional PM sessions. PM is supported on the F4 and F5 levels. The S/UNI-ATLAS-3200 device provides for the generation of Forward Monitoring and Backward Reporting PM cells (both segment and end-to-end), the termination of Forward Monitoring and Backward Reporting cells, and for non-intrusive monitoring of Forward Monitoring and Backward Reporting cells. The following statistics are collected when terminating or monitoring PM flows:
  - Forward Impaired Block.
  - Forward Lost/Misinserted Impaired Block
  - Forward Severely Errored Cell Block (Lost).
  - Forward Severely Errored Cell Block (Misinserted).
  - Forward Severely Errored Cell Block (BIP-16 violations).
  - Forward Severely Errored Cell Block Combined (non-saturating)
  - Forward Lost CLP0+1 cell count.
  - Forward Lost CLP0 cell count.
  - Forward Tagged CLP0 cell count
  - Forward Misinserted CLP0+1 cell count.
  - Forward Errored cell count.
  - Forward Total Lost CLP0+1 cell count.
  - Forward Total Lost CLP0 cell count.
  - Forward Lost Forward Monitoring cell count.
  - Backward Impaired Block.
  - Backward Lost/Misinserted Impaired Block.
  - Backward Severely Errored Cell Block (Lost).
  - Backward Severely Errored Cell Block (Misinserted).
  - Backward Severely Errored Cell Block (BIP-16 violations).

- Backward Severely Errored Cell Block Combined (non-saturating)
- Backward Severely Errored Cell Block Combined (saturating)
- Backward Lost CLP0+1 cell count.
- Backward Lost CLP0 cell count.
- Backward Tagged CLP0 cell count.
- Backward Misinserted CLP0+1 cell count.
- Backward Errored cell count.
- Backward Total Lost CLP0+1 cell count.
- Backward Total Lost CLP0 cell count.
- Backward Lost Fwd Monitoring PM cell count.
- Backward Lost Backward Reporting PM cell count.
- Total Transmitted CLP0+1 cell count.
- Total Transmitted CLP0 cell count.

- Statistics for PM sessions are held in on-chip RAM that can be read at any time through the 32-bit general purpose microprocessor port.
- Paced insertion of PM cells is provided.
- PM block size generation and termination is per-session programmable ranging from 128 – 32768 cells.
- Each of the 512 PM sessions can be configured to be a source, sink or non-intrusive monitoring point of PM cells.
- PM processes support the aggregation of F5 flows into F4 flows, and the termination of F4 flows into its constituent F5 flows.

2.3 Cell Counting

- Counts maintained on a per-VC basis include total low or high priority user cells, OAM cells, RM cells, and invalid cells, cells violating the traffic contract, and total AAL5 frames. Aggregate counts are also provided when aggregating or terminating VPCs.
- Counts maintained on a per-PHY basis include: number of CLP0 cells received, number of CLP1 cells received, number of OAM cells received, number of RM cells received, number of errored OAM cells, number of errored RM cells, number of cells with unassigned, unprovisioned, or invalid VPI/VCI/PTI, the number of inserted OAM cells timed-out to avoid head-of-line blocking, and the number of cells received with a non-zero GFC and/or with EFCI indicated in their PTI fields.
- The Per-VC Non-Compliant and Per-PHY Non-Compliant counts can be used to count total frames, whether or not policing is enabled.

3 Applications

- Core ATM Switches.
- Wide Area Network ATM Core and Edge Switches.
- ATM Enterprise and Workgroup Switches.
- Broadband Access Multiplexers.
- XDSL Access Multiplexers.

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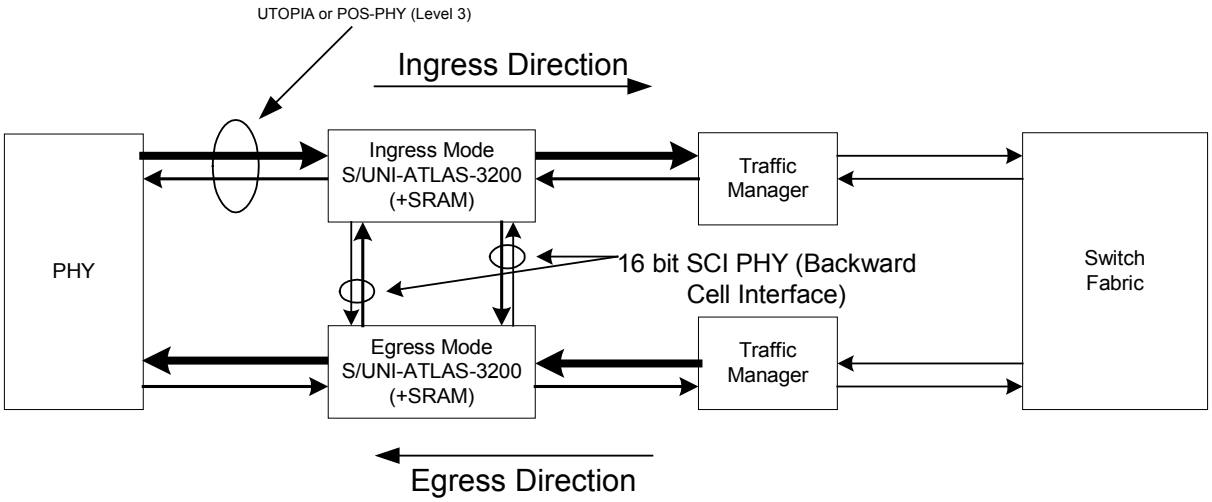
- PMC-1980495 – POS-PHY Level 3: Saturn Compatible Interface for Packet Over SONET Physical Layer and Link Layer Devices, Issue 4, June 7, 2000.

5 Application Examples

The S/UNI®0 ATLAS-3200 device is an integrated circuit that implements the ATM Layer functions that include header translation, cell rate policing, performance management and fault management. The S/UNI-ATLAS-3200 device is a uni-directional part. When used in the ingress direction, it is intended to be situated between the physical layer (PHY) devices and a traffic manager (which schedules traffic into the switch fabric). When used in the egress direction, it is intended to be situated between a traffic manager (which shapes traffic out of the switch fabric) and the PHY devices. This application is shown in the figure below.

Figure 1 S/UNI-ATLAS-3200 Application



5.1 Cascading

Multiple S/UNI-ATLAS-3200 devices can be cascaded when more than 64K VCs are required.

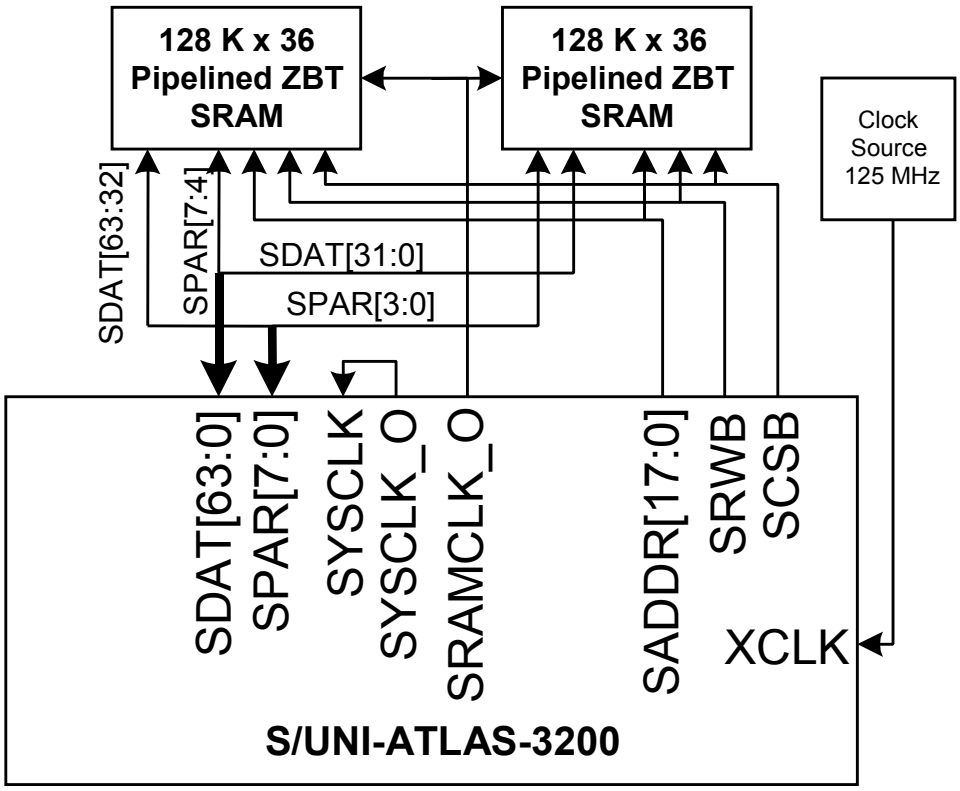
In a configuration with “n” cascaded devices, each device is configured (using the per-PHY Processing register) to only process cells from some of the 48 possible PHYs (the PHYs meant for that device). Cells from the other PHYs (which the device has been told to not process) will be passed through. A passed through cell will have already been processed by an upstream device in the cascade, or will be processed by a downstream device. When cascading, each PHYs cells will be processed in exactly one device and will be passed through all the other devices.

Such cascading allows the total number of VCs supported to be “n” times 64K where “n” is the number of cascaded devices (and the 48 available PHYs are partitioned among the “n” devices). In each device, the 64K VCs that it has available are shared between all the PHYs that it is processing. Cascading does not result in an increase in aggregate throughput.

5.2 RAM Configurations

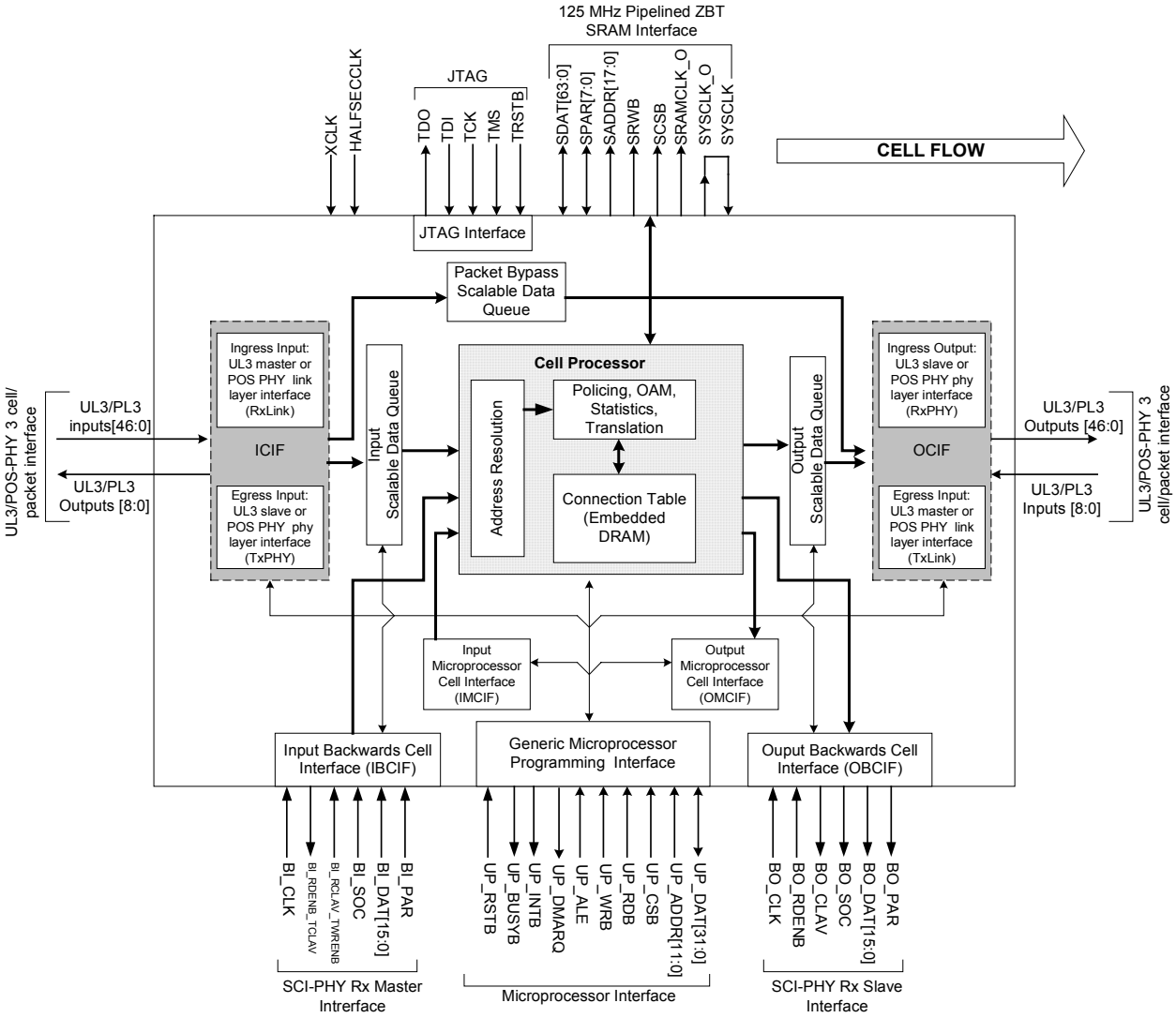
The S/UNI-ATLAS-3200 device uses an external SRAM to store the search tree data structure. This SRAM is required to be Synchronous Pipelined ZBT SRAM with cycle time less than 7 ns, and a bus width of 64 bits + parity. The typical configuration is 8M of SRAM in a pair of 128Kx36 RAMs. This configuration will support 64K VCs. Up to 16M of SRAM may be used if additional search depth is desired, though no more than 64K VCs are supported. Alternatively, the amount of SRAM may be reduced, if less than 64K VCs are to be supported.

Figure 2 Interface between S/UNI-ATLAS-3200 and External RAM



6 Block Diagram

Figure 3 S/UNI-ATLAS-3200 Block Diagram



7 Description

The PM7325 S/UNI®-ATLAS-3200 device is a monolithic integrated circuit that implements the ATM Layer functions that include fault and performance management, header translation and cell rate policing. The S/UNI-ATLAS-3200 device is a uni-directional part that is intended to reside between the physical layer (PHY) devices and a traffic manager in the ingress side, and a traffic shaper and the PHY devices in the egress side. The S/UNI-ATLAS-3200 supports a sustained aggregate throughput of $5.68x10^6$ cells/s in each of the Ingress and Egress modes. The S/UNI-ATLAS-3200 uses external SRAM to store the search tree data structures. The device is capable of supporting up to 64K connections. Apart from the operation of the UL3 or POS-PHY™ Level 3 interfaces, the S/UNI-ATLAS-3200 is fully symmetric, with identical features and configuration options in either direction.

The Input Cell Interface can be connected to a PHY device supporting up to 48 PHY queues via a UTOPIA Level 3 or POS-PHY Level 3 bus, or may emulate up to 48 PHYs via multi-PHY addressing over a UTOPIA Level 3 or POS-PHY Level 3 bus. The 52- or 53-byte ATM cell is encapsulated in a data structure that can contain prepended or postpended routing information, and can fill the HEC field out to 32 bits. Received cells are buffered in a programmable-depth per-PHY FIFO. All idle cells, physical layer and unassigned cells are discarded, and any cells from PHY queues designated as packet PHYs are routed to the output untouched. For the remaining cells, a subset of ATM header and appended bits is used as a search key to find the VC Table record for the virtual connection. If a connection is not provisioned and the search terminates unsuccessfully as a result, the cell is discarded and a count of invalid cells is incremented. If the search is successful, subsequent processing of the cell is dependent on the contents of the cell and configuration fields in the VC Table Record.

The S/UNI-ATLAS-3200 performs header translation, if so configured. The ATM header is replaced by the contents of fields in the VC Table Record for that connection. The VCI contents are passed through transparently for VPC connections; the PTI is passed through transparently for all connections. The CLP bit may only be altered via the policing function. Appended bytes can be replaced, added or removed.

If the S/UNI-ATLAS-3200 is the end point for a F4 or F5 OAM flow, the OAM cells are terminated and processed. If the S/UNI-ATLAS-3200 is not the end point, the OAM cells are passed to the Output Cell Interface with an optional copy passed to the Microprocessor Cell Interface FIFO. The reception of AIS or RDI cells results in the appropriate alarms (segment or end-to-end alarm). Interrupts corresponding to the alarm bits can be masked on a per-connection basis. When configured as a sink of PM cells, upon the arrival of a Forward Monitoring cell, error counts are updated and a Backward Reporting cell is optionally generated and routed to the Backwards Cell Interface that is connected to the opposite-direction S/UNI-ATLAS-3200. When configured as a source of PM cells, the S/UNI-ATLAS-3200 generates a Forward Monitoring cell when the per-session programmable user cell block size is reached. The insertion of PM cells is paced so that bursts of generated cells will not cause a backup.

Cell rate policing is supported through a dual leaky bucket policer that conforms to the ITU-T I.371 Generic Cell Rate Algorithm for each connection. Each cell that violates the traffic contract can be tagged, discarded, or just counted. To allow full flexibility, each GCRA instance can be programmed to police any combination of user cells, OAM cells, Resource Management cells, high priority cells or low priority cells. On a per-connection basis, one of eight policing configurations may be chosen. Three 16-bit non-compliant cell counts are provided on a per-connection basis. These counters are programmable and allow for the counting of, for example, dropped CLP0 cells, dropped CLP1 cells and tagged CLP0 cells.

On a per-VC basis, the dual leaky bucket policer may be configured to perform ATM Forum TM 4.1-compliant GFR policing. In this mode, the non-compliant counts may be configured to count received frames, dropped frames, or tagged frames as well as counting dropped or tagged cells.

The S/UNI-ATLAS-3200 also supports a single leaky bucket policer on a per-PHY basis (up to 48 instances can be programmed). Any or all connections on a particular PHY can be policed by the PHY GCRA. Each PHY GCRA has a programmable action field that allows violating cells to be tagged, discarded, or just counted. Three configurable non-compliant cell counts (on each PHY GCRA) are also provided. Each PHY GCRA can be programmed to police any combination of user cells, OAM cells, Resource Management cells, high priority cells or low priority cells. Any one of four PHY policing configurations may be chosen.

The 32-bit Microprocessor Interface is provided for device configuration, control and monitoring by an external microprocessor. This interface provides access to the external SRAM and internal DRAM to allow creation of the data structure, configuration of individual connections, and monitoring of the connections. The Microprocessor Cell FIFO permits insertion and extraction of cells. Programmed cell types can be routed to the Microprocessor Cell FIFO (and subsequently read through the Microprocessor cell interface). The microprocessor may insert cells into the cell stream which may be processed, translated, counted, routed, and policed by the S/UNI-ATLAS-3200, or not, at the option of the microprocessor.

When the device is in Egress mode, the Output Cell Interface is a 32-bit UTOPIA Level 3 or POS-PHY Level 3 transmit Link Layer interface which can address up to 48 PHY queues on a PHY device using polled addressing. Cells are stored in a per-PHY programmable-depth FIFO and subsequently transferred to a PHY device. A total of 192 cell buffers are provided, which may be divided up among the PHYs as desired. A PHY output buffer requires at least 12 cell buffers if it is to maintain full STS-12 or more on that PHY, 4 cell buffers if it is to maintain STS-3 on that PHY, and 2 cell buffers if it is to maintain STS-1 or less on that PHY. The FIFO depth for each PHY can be configured to hold 2, 4, 12, or 48 cells.

When the device is in Ingress UL3 mode, the Output Cell Interface is a 32-bit UTOPIA Level 3 Rx PHY (Slave) interface which may mimic up to 48 PHYs using polled addressing, or may optionally operate without polling. When configured in Ingress POS-PHY mode, the Output Cell Interface is a POS-PHY Level 3 Rx PHY Layer which mimics up to 48 PHYs. Cells are stored in a per-PHY programmable-depth FIFO and subsequently transferred to a TM or switch device. A total of 192 cell buffers are provided, which may be divided up among the PHYs as desired. A PHY output buffer requires at least 12 cell buffers if it is to maintain full STS-12 or more on that PHY, 4 cell buffers if it is to maintain STS-3 on that PHY, and 2 cell buffers if it is to maintain STS-1 or less on that PHY. The FIFO depth for each PHY can be configured to hold 2, 4, 12, or 48 cells.

The S/UNI-ATLAS-3200 is implemented in low power 0.18 micron 1.5 Volt CMOS technology with 2.5 Volt embedded DRAM. The SRAM interface uses 2.5 Volt signalling; all other I/Os are 3.3 Volts. Note that the 2.5 Volt interfaces are not 3.3 Volt-tolerant. The S/UNI-ATLAS-3200 is packaged in a 768-pin Tape BGA package.

8 Pin Diagram

The S/UNI-ATLAS-3200 is packaged in a 768-pin Tape BGA package with a body size of 40 mm x 40 mm x 1.54 mm and a ball pitch of 1 mm. This pin diagram is available in a spreadsheet format in PMC-2001760.

Figure 4 Pin Diagram

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
38	sdat_61	VSS	sdat_58	sdat_55	sdat_52	VDD25	VSS	sdat_46	sdat_43	VDD15	VSS	sdat_36	VDD15	VDD25	VDD15	sdat_28	VSS	sdat_23	sdat_21
37	VDD25	sdat_62	sdat_59	sdat_56	sdat_53	sdat_50	sdat_49	sdat_47	sdat_44	sdat_41	VSS	sdat_38	sdat_35	sdat_32	VSS	VSS	sdat_26	sdat_24	VDD15
36	zetmdl	VSS	VSS	VDD15	sdat_57	sdat_54	VDD15	sdat_51	sdat_48	sdat_45	sdat_42	sdat_39	sdat_37	sdat_34	sdat_31	sdat_29	sdat_27	VSS	sdat_22
35	VSS	VSS	sramclk_o	sdat_63	VSS	VSS	VSS	VSS	VDD25	VDD25	VSS	VSS	sdat_40	VSS	sdat_33	sdat_30	VSS	sdat_25	VDD25
34	ocif_dat_29	VSS	ocif_dat_31	VDD25	VDD25	sdat_60	VSS	VSS	VDD25	VDD25	VSS	VSS	VDD33	VDD33	VSS	VSS	VDD25	VDD25	VSS
33	ocif_dat_27	ocif_dat_28	ocif_dat_30	VDD15	zetmdr	VSS	VSS	VSS	VDD33	VDD15	VSS	VSS	VDD25	VDD15	VSS	VSS	VDD33	VDD15	VSS
32	ocif_dat_25	VSS	VDD33	VDD25	VDD15	VDD25													
31	ocif_dat_24	VSS	ocif_dat_26	VDD25	VDD15	VDD33													
30	ocif_dat_21	ocif_dat_22	ocif_dat_23	VSS	VSS	VSS													
29	ocif_dat_18	ocif_dat_19	ocif_dat_20	VSS	VSS	VSS													
28	VDD33	ocif_dat_16	ocif_dat_17	VDD33	VDD33	VDD15													
27	VSS	ocif_dat_13	ocif_dat_15	VDD33	VDD33	VDD25													
26	ocif_dat_10	ocif_dat_11	ocif_dat_12	ocif_dat_14	VSS	VSS													
25	VDD15	ocif_dat_9	VSS	VSS	VSS	VSS													
24	VSS	ocif_dat_6	ocif_dat_7	ocif_dat_8	VDD25	VDD15													
23	VSS	ocif_dat_3	ocif_dat_4	ocif_dat_5	VDD25	VDD33													
22	ocif_dat_2	ocif_dat_0	VDD15	ocif_dat_1	VSS	VSS													
21	VSS	ocif_par	VSS	ocif_eop	VSS	VSS													
20	VDD15	ocif_soc_sop	VSS	VDD15	VDD33	VDD15													
19	ocif_sx	ocif_err	VDD15	VSS	VDD33	VDD25													
18	ocif_mod_1	ocif_mod_0	ocif_clav_ptpa	VDD15	VSS	VSS													
17	ocif_enb_stpa	VDD33	ocif_addr_5	ocif_addr_4	VSS	VSS													
16	ocif_addr_3	VSS	ocif_addr_2	ocif_addr_0	VDD25	VDD15													
15	ocif_addr_1	ocif_clk	ocif_ctrl	VSS	VDD25	VDD33													
14	halfsecclk	VDD15	VDDQ15	VDD15	VSS	VSS													
13	VSS	VDDQ15	VSS	VSS	VSS	VSS													
12	VSS	VSS	VSS	VDD33	VDD33	VDD15													
11	VDDQ15	VDDQ15	VDDQ15	VDD33	VDD33	VDD25													
10	VSS	VDDQ15	VSS	VSS	VSS	VSS													
9	VSS	VDDQ15	tck	VSS	VSS	VSS													
8	VSS	dtclk	NC	VDD25	VDD15	VDD33													
7	dtmb	VDDQ15	NC	VDD25	VDD15	VDD25													
6	VSS	trstb	VDDQ25	NC	VSS	VDD25	VSS	VSS	VDD15	VDD33	VSS	VSS	VDD15	VDD25	VSS	VSS	VDD15	VDD33	VSS
5	NC	NC	NC	NC	VSS	bi_dat_11	VSS	VSS	VDD25	VDD25	VSS	VSS	VDD33	VDD33	VSS	VSS	VDD25	VDD25	VSS
4	VDDQ25	VDDQ25	VDD15	tdo	bi_dat_12	bi_dat_7	VSS	VSS	VDD25	VDD25	VSS	VSS	bi_rclav_twrenb	VDDQ15	bo_soc	bo_dat_0	bo_dat_2	VSS	bo_dat_7
3	NC	NC	tdi	bi_dat_13	bi_dat_8	VDDQ25	bi_dat_4	VDDQ25	bi_dat_0	VSS	VDDQ15	VSS	bo_rdenb	bo_clav	VDD33	VSS	bo_dat_3	VDDQ15	VSS
2	VSS	tms	bi_dat_14	bi_dat_9	bi_dat_5	VDDQ15	bi_dat_2	bi_dat_1	bi_par	bi_clk	VSS	VDDQ15	VSS	VDDQ15	VSS	bo_dat_1	VSS	bo_dat_5	bo_dat_6
1	NC	bi_dat_15	bi_dat_10	bi_dat_6	VDDQ15	bi_dat_3	VSS	VDDQ15	VSS	bi_soc	bi_rrdenb_tclav	VSS	VSS	bo_clk	bo_par	VSS	VDDQ15	bo_dat_4	VSS
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

Top View

Top View

Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV	
sdat_19	sdat_16	sdat_14	VSS	sdat_11	sdat_10	VDD25	VSS	sdat_2	spar_7	spar_4	spar_1	VDD25	VSS	VSS	saddr_17	saddr_14	saddr_10	saddr_6	38
VSS	sdat_17	VSS	sdat_13	VSS	sdat_8	VDD25	sdat_4	sdat_1	spar_6	spar_3	spar_0	xclk	sysclk_o	srwb	VDD25	saddr_11	VSS	VDD15	37
VDD15	VSS	VSS	VSS	VDD15	sdat_7	sdat_5	sdat_3	sdat_0	spar_5	spar_2	VSS	sysclk	sceb	saddr_15	saddr_12	saddr_7	VSS	VDD15	36
sdat_20	sdat_18	sdat_15	sdat_12	sdat_9	sdat_6	VSS	VSS	VSS	VDD25	VDD25	VSS	VSS	saddr_16	VSS	saddr_8	saddr_4	saddr_2	saddr_1	35
VSS	VDD25	VDD25	VSS	VSS	VDD33	VDD33	VSS	VSS	VDD25	VDD25	VSS	VSS	saddr_13	saddr_9	VSS	VDD25	icif_enb_stpa	VDD33	34
VSS	VDD25	VDD15	VSS	VSS	VDD33	VDD15	VSS	VSS	VDD25	VDD15	VSS	VSS	VDD25	saddr_5	saddr_3	saddr_0	VSS	icif_addr_0	33
													VDD33	VDD15	VDD25	icif_clav_ptpa	icif_addr_1	icif_addr_3	32
													VDD25	VDD15	VDD25	icif_clk	VDD15	icif_addr_4	31
													VSS	VSS	VSS	icif_addr_2	icif_ctrl	icif_mod_0	30
													VSS	VSS	VSS	icif_addr_5	icif_err	VSS	29
													VDD33	VDD33	VDD33	icif_mod_1	icif_sx	icif_eop	28
													VDD15	VDD33	VDD33	icif_soc_sop	icif_par	VSS	27
													VSS	VSS	VSS	icif_dat_0	icif_dat_2	icif_dat_3	26
													VSS	VSS	icif_dat_1	VDD15	icif_dat_5	VDD33	25
													VDD25	VDD25	icif_dat_4	icif_dat_6	icif_dat_7	VSS	24
													VDD15	VDD25	icif_dat_8	icif_dat_9	VDD15	icif_dat_10	23
													VSS	VSS	icif_dat_11	icif_dat_12	VSS	icif_dat_13	22
													VSS	VSS	VDD15	icif_dat_14	icif_dat_15	icif_dat_16	21
													VDD33	VDD33	VSS	VDD15	icif_dat_17	icif_dat_18	20
													VDD15	VDD33	icif_dat_19	VDD15	icif_dat_20	VSS	19
													VSS	VSS	icif_dat_22	icif_dat_21	icif_dat_23	VDD15	18
													VSS	VSS	icif_dat_26	icif_dat_25	icif_dat_24	VDD33	17
													VDD25	VDD25	icif_dat_29	icif_dat_28	VSS	icif_dat_27	16
													VDD15	VDD25	VDDQ15	VSS	VDD33	icif_dat_30	15
													VSS	VSS	VSS	VDDQ15	VSS	icif_dat_31	14
													VSS	VSS	VDDQ15	VSS	VDD15	VSS	13
													VDD33	VDD33	VDD33	VSS	VSS	up_dat_31	12
													VDD15	VDD33	VDD33	VSS	VDDQ15	up_dat_30	11
													VSS	VSS	VSS	up_dat_29	VSS	VDDQ15	10
													VSS	VSS	VSS	up_dat_26	up_dat_27	up_dat_28	9
													VDD25	VDD15	VDD25	VDDQ25	up_dat_25	VSS	8
													VDD33	VDD15	VDD25	VDDQ15	VSS	VDDQ25	7
VSS	VDD15	VDD25	VSS	VSS	VDD15	VDD33	VSS	VSS	VDD15	VDD25	VSS	VSS	VSS	NC	up_dat_23	VDDQ15	VDDQ15	VSS	6
VSS	VDD25	VDD25	VSS	VSS	VDD33	VDD33	VSS	VSS	VDD25	VDD25	VSS	VSS	up_dat_15	up_dat_19	NC	up_dat_22	VDDQ25	VSS	5
bo_dat_8	VSS	VSS	VDDQ15	up_wrb	VSS	up_addr_2	VSS	VSS	VDD25	VDD25	VSS	VSS	VDDQ25	up_dat_14	up_dat_18	NC	up_dat_21	up_dat_24	4
VSS	VSS	bo_dat_10	bo_dat_12	bo_dat_15	up_rdb	up_dmareq	up_addr_1	up_addr_6	up_addr_9	up_dat_1	up_dat_5	up_dat_6	VDDQ15	VSS	up_dat_13	VSS	NC	up_dat_20	3
VSS	VSS	VDDQ15	bo_dat_11	bo_dat_14	up_rstb	VSS	up_busyb	up_addr_3	up_addr_5	up_addr_8	up_addr_11	up_dat_2	up_dat_4	up_dat_8	up_dat_10	up_dat_12	up_dat_17	NC	2
VDDQ15	VDDQ15	bo_dat_9	VDDQ25	bo_dat_13	up_intb	up_ale	up_csb	up_addr_0	up_addr_4	up_addr_7	up_addr_10	up_dat_0	up_dat_3	up_dat_7	up_dat_9	up_dat_11	VSS	up_dat_16	1
Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV	

Table 1 Signal Ball Assignment (Alphabetical)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
bi_clk	K2	icif_dat_28	AT16	saddr_15	AP36	sdat_9	AD35
bi_dat_0	J3	icif_dat_29	AR16	saddr_16	AN35	spar_0	AL37
bi_dat_1	H2	icif_dat_3	AV26	saddr_17	AR38	spar_1	AL38
bi_dat_10	C1	icif_dat_30	AV15	saddr_2	AU35	spar_2	AK36
bi_dat_11	F5	icif_dat_31	AV14	saddr_3	AR33	spar_3	AK37
bi_dat_12	E4	icif_dat_4	AR24	saddr_4	AT35	spar_4	AK38
bi_dat_13	D3	icif_dat_5	AU25	saddr_5	AP33	spar_5	AJ36
bi_dat_14	C2	icif_dat_6	AT24	saddr_6	AV38	spar_6	AJ37
bi_dat_15	B1	icif_dat_7	AU24	saddr_7	AT36	spar_7	AJ38
bi_dat_2	G2	icif_dat_8	AR23	saddr_8	AR35	sramclk_o	C35
bi_dat_3	F1	icif_dat_9	AT23	saddr_9	AP34	srwb	AP37
bi_dat_4	G3	icif_enb_stpa	AU34	sceb	AN36	sysclk	AM36
bi_dat_5	E2	icif_eop	AV28	sdat_0	AH36	sysclk_o	AN37
bi_dat_6	D1	icif_err	AU29	sdat_1	AH37	tck	C9
bi_dat_7	F4	icif_mod_0	AV30	sdat_10	AE38	tdi	C3
bi_dat_8	E3	icif_mod_1	AT28	sdat_11	AD38	tdo	D4
bi_dat_9	D2	icif_par	AU27	sdat_12	AC35	tms	B2
bi_par	J2	icif_soc_sop	AT27	sdat_13	AC37	trstb	B6
bi_rclav_twrenb	N4	icif_sx	AU28	sdat_14	AB38	up_addr_0	AH1
bi_rrdenb_tclav	L1	ocif_addr_0	D16	sdat_15	AB35	up_addr_1	AG3
bi_soc	K1	ocif_addr_1	A15	sdat_16	AA38	up_addr_10	AL1
bo_clav	P3	ocif_addr_2	C16	sdat_17	AA37	up_addr_11	AL2
bo_clk	P1	ocif_addr_3	A16	sdat_18	AA35	up_addr_2	AF4
bo_dat_0	T4	ocif_addr_4	D17	sdat_19	Y38	up_addr_3	AH2
bo_dat_1	T2	ocif_addr_5	C17	sdat_2	AH38	up_addr_4	AJ1
bo_dat_10	AB3	ocif_clav_ptpa	C18	sdat_20	Y35	up_addr_5	AJ2
bo_dat_11	AC2	ocif_clk	B15	sdat_21	W38	up_addr_6	AH3
bo_dat_12	AC3	ocif_ctrl	C15	sdat_22	W36	up_addr_7	AK1
bo_dat_13	AD1	ocif_dat_0	B22	sdat_23	V38	up_addr_8	AK2
bo_dat_14	AD2	ocif_dat_1	D22	sdat_24	V37	up_addr_9	AJ3
bo_dat_15	AD3	ocif_dat_10	A26	sdat_25	V35	up_ale	AF1
bo_dat_2	U4	ocif_dat_11	B26	sdat_26	U37	up_busyb	AG2
bo_dat_3	U3	ocif_dat_12	C26	sdat_27	U36	up_csb	AG1
bo_dat_4	V1	ocif_dat_13	B27	sdat_28	T38	up_dat_0	AM1
bo_dat_5	V2	ocif_dat_14	D26	sdat_29	T36	up_dat_1	AK3
bo_dat_6	W2	ocif_dat_15	C27	sdat_3	AG36	up_dat_10	AR2
bo_dat_7	W4	ocif_dat_16	B28	sdat_30	T35	up_dat_11	AT1
bo_dat_8	Y4	ocif_dat_17	C28	sdat_31	R36	up_dat_12	AT2
bo_dat_9	AB1	ocif_dat_18	A29	sdat_32	P37	up_dat_13	AR3

Signal	Ball
bo_par	R1
bo_rdenb	N3
bo_soc	R4
dtclk	B8
dtmb	A7
halfsecclk	A14
icif_addr_0	AV33
icif_addr_1	AU32
icif_addr_2	AT30
icif_addr_3	AV32
icif_addr_4	AV31
icif_addr_5	AT29
icif_clav_ptpa	AT32
icif_clk	AT31
icif_ctrl	AU30
icif_dat_0	AT26
icif_dat_1	AR25
icif_dat_10	AV23
icif_dat_11	AR22
icif_dat_12	AT22
icif_dat_13	AV22
icif_dat_14	AT21
icif_dat_15	AU21
icif_dat_16	AV21
icif_dat_17	AU20
icif_dat_18	AV20
icif_dat_19	AR19
icif_dat_2	AU26
icif_dat_20	AU19
icif_dat_21	AT18
icif_dat_22	AR18
icif_dat_23	AU18
icif_dat_24	AU17
icif_dat_25	AT17
icif_dat_26	AR17
icif_dat_27	AV16

Signal	Ball
ocif_dat_19	B29
ocif_dat_2	A22
ocif_dat_20	C29
ocif_dat_21	A30
ocif_dat_22	B30
ocif_dat_23	C30
ocif_dat_24	A31
ocif_dat_25	A32
ocif_dat_26	C31
ocif_dat_27	A33
ocif_dat_28	B33
ocif_dat_29	A34
ocif_dat_3	B23
ocif_dat_30	C33
ocif_dat_31	C34
ocif_dat_4	C23
ocif_dat_5	D23
ocif_dat_6	B24
ocif_dat_7	C24
ocif_dat_8	D24
ocif_dat_9	B25
ocif_enb_stpa	A17
ocif_eop	D21
ocif_err	B19
ocif_mod_0	B18
ocif_mod_1	A18
ocif_par	B21
ocif_soc_sop	B20
ocif_sx	A19
saddr_0	AT33
saddr_1	AV35
saddr_10	AU38
saddr_11	AT37
saddr_12	AR36
saddr_13	AN34
saddr_14	AT38

Signal	Ball
sdat_33	R35
sdat_34	P36
sdat_35	N37
sdat_36	M38
sdat_37	N36
sdat_38	M37
sdat_39	M36
sdat_4	AG37
sdat_40	N35
sdat_41	K37
sdat_42	L36
sdat_43	J38
sdat_44	J37
sdat_45	K36
sdat_46	H38
sdat_47	H37
sdat_48	J36
sdat_49	G37
sdat_5	AF36
sdat_50	F37
sdat_51	H36
sdat_52	E38
sdat_53	E37
sdat_54	F36
sdat_55	D38
sdat_56	D37
sdat_57	E36
sdat_58	C38
sdat_59	C37
sdat_6	AE35
sdat_60	F34
sdat_61	A38
sdat_62	B37
sdat_63	D35
sdat_7	AE36
sdat_8	AE37

Signal	Ball
up_dat_14	AP4
up_dat_15	AN5
up_dat_16	AV1
up_dat_17	AU2
up_dat_18	AR4
up_dat_19	AP5
up_dat_2	AM2
up_dat_20	AV3
up_dat_21	AU4
up_dat_22	AT5
up_dat_23	AR6
up_dat_24	AV4
up_dat_25	AU8
up_dat_26	AT9
up_dat_27	AU9
up_dat_28	AV9
up_dat_29	AT10
up_dat_3	AN1
up_dat_30	AV11
up_dat_31	AV12
up_dat_4	AN2
up_dat_5	AL3
up_dat_6	AM3
up_dat_7	AP1
up_dat_8	AP2
up_dat_9	AR1
up_dmareq	AF3
up_intb	AE1
up_rdb	AE3
up_rstb	AE2
up_wrb	AD4
xclk	AM37
zetmdl	A36
zetmdr	E33

Table 2 Power/Ground Ball Assignment (Alphabetical)

Signal	Ball
VDD15	A20

Signal	Ball
VDD25	K34

Signal	Ball
VSS	A9

Signal	Ball
VSS	B36

Signal	Ball
VDD15	A25
VDD15	AA6
VDD15	AB33
VDD15	AD36
VDD15	AE6
VDD15	AF33
VDD15	AJ6
VDD15	AK33
VDD15	AN11
VDD15	AN15
VDD15	AN19
VDD15	AN23
VDD15	AN27
VDD15	AP31
VDD15	AP32
VDD15	AP7
VDD15	AP8
VDD15	AR21
VDD15	AT19
VDD15	AT20
VDD15	AT25
VDD15	AU13
VDD15	AU23
VDD15	AU31
VDD15	AV18
VDD15	AV36
VDD15	AV37
VDD15	B14
VDD15	C19
VDD15	C22
VDD15	C4
VDD15	D14
VDD15	D18
VDD15	D20
VDD15	D33
VDD15	D36
VDD15	E31
VDD15	E32
VDD15	E7
VDD15	E8

Signal	Ball
VDD25	K35
VDD25	K4
VDD25	K5
VDD25	N33
VDD25	P38
VDD25	P6
VDD25	U34
VDD25	U5
VDD25	V34
VDD25	V5
VDD25	W35
VDD33	A28
VDD33	AE33
VDD33	AE34
VDD33	AE5
VDD33	AF34
VDD33	AF5
VDD33	AF6
VDD33	AN12
VDD33	AN20
VDD33	AN28
VDD33	AN32
VDD33	AN7
VDD33	AP11
VDD33	AP12
VDD33	AP19
VDD33	AP20
VDD33	AP27
VDD33	AP28
VDD33	AR11
VDD33	AR12
VDD33	AR27
VDD33	AR28
VDD33	AU15
VDD33	AV17
VDD33	AV25
VDD33	AV34
VDD33	B17
VDD33	C32
VDD33	D11

Signal	Ball
VSS	AA2
VSS	AA3
VSS	AA36
VSS	AA4
VSS	AB36
VSS	AB37
VSS	AB4
VSS	AC33
VSS	AC34
VSS	AC36
VSS	AC38
VSS	AC5
VSS	AC6
VSS	AD33
VSS	AD34
VSS	AD37
VSS	AD5
VSS	AD6
VSS	AE4
VSS	AF2
VSS	AF35
VSS	AG33
VSS	AG34
VSS	AG35
VSS	AG38
VSS	AG4
VSS	AG5
VSS	AG6
VSS	AH33
VSS	AH34
VSS	AH35
VSS	AH4
VSS	AH5
VSS	AH6
VSS	AL33
VSS	AL34
VSS	AL35
VSS	AL36
VSS	AL4
VSS	AL5

Signal	Ball
VSS	B38
VSS	C10
VSS	C12
VSS	C13
VSS	C20
VSS	C21
VSS	C25
VSS	C36
VSS	D10
VSS	D13
VSS	D15
VSS	D19
VSS	D25
VSS	D29
VSS	D30
VSS	D9
VSS	E10
VSS	E13
VSS	E14
VSS	E17
VSS	E18
VSS	E21
VSS	E22
VSS	E25
VSS	E26
VSS	E29
VSS	E30
VSS	E35
VSS	E5
VSS	E6
VSS	E9
VSS	F10
VSS	F13
VSS	F14
VSS	F17
VSS	F18
VSS	F21
VSS	F22
VSS	F25
VSS	F26

Signal	Ball
VDD15	F12
VDD15	F16
VDD15	F20
VDD15	F24
VDD15	F28
VDD15	G36
VDD15	J6
VDD15	K33
VDD15	K38
VDD15	N38
VDD15	N6
VDD15	P33
VDD15	R38
VDD15	U6
VDD15	V33
VDD15	W37
VDD15	Y36
VDD25	A37
VDD25	AA33
VDD25	AA34
VDD25	AA5
VDD25	AB34
VDD25	AB5
VDD25	AB6
VDD25	AF37
VDD25	AF38
VDD25	AJ33
VDD25	AJ34
VDD25	AJ35
VDD25	AJ4
VDD25	AJ5
VDD25	AK34
VDD25	AK35
VDD25	AK4
VDD25	AK5
VDD25	AK6
VDD25	AM38
VDD25	AN16
VDD25	AN24
VDD25	AN31

Signal	Ball
VDD33	D12
VDD33	D27
VDD33	D28
VDD33	E11
VDD33	E12
VDD33	E19
VDD33	E20
VDD33	E27
VDD33	E28
VDD33	F15
VDD33	F23
VDD33	F31
VDD33	F8
VDD33	J33
VDD33	K6
VDD33	N34
VDD33	N5
VDD33	P34
VDD33	P5
VDD33	R3
VDD33	U33
VDD33	V6
VDDQ15	A11
VDDQ15	AA1
VDDQ15	AB2
VDDQ15	AC4
VDDQ15	AN3
VDDQ15	AR13
VDDQ15	AR15
VDDQ15	AT14
VDDQ15	AT6
VDDQ15	AT7
VDDQ15	AU11
VDDQ15	AU6
VDDQ15	AV10
VDDQ15	B10
VDDQ15	B11
VDDQ15	B13
VDDQ15	B7
VDDQ15	B9

Signal	Ball
VSS	AL6
VSS	AM33
VSS	AM34
VSS	AM35
VSS	AM4
VSS	AM5
VSS	AM6
VSS	AN10
VSS	AN13
VSS	AN14
VSS	AN17
VSS	AN18
VSS	AN21
VSS	AN22
VSS	AN25
VSS	AN26
VSS	AN29
VSS	AN30
VSS	AN38
VSS	AN6
VSS	AN9
VSS	AP10
VSS	AP13
VSS	AP14
VSS	AP17
VSS	AP18
VSS	AP21
VSS	AP22
VSS	AP25
VSS	AP26
VSS	AP29
VSS	AP3
VSS	AP30
VSS	AP35
VSS	AP38
VSS	AP9
VSS	AR10
VSS	AR14
VSS	AR20
VSS	AR26

Signal	Ball
VSS	F29
VSS	F30
VSS	F33
VSS	F35
VSS	F9
VSS	G1
VSS	G33
VSS	G34
VSS	G35
VSS	G38
VSS	G4
VSS	G5
VSS	G6
VSS	H33
VSS	H34
VSS	H35
VSS	H4
VSS	H5
VSS	H6
VSS	J1
VSS	K3
VSS	L2
VSS	L33
VSS	L34
VSS	L35
VSS	L37
VSS	L38
VSS	L4
VSS	L5
VSS	L6
VSS	M1
VSS	M3
VSS	M33
VSS	M34
VSS	M35
VSS	M4
VSS	M5
VSS	M6
VSS	N1
VSS	N2

Signal	Ball
VDD25	AN33
VDD25	AN8
VDD25	AP15
VDD25	AP16
VDD25	AP23
VDD25	AP24
VDD25	AR31
VDD25	AR32
VDD25	AR37
VDD25	AR7
VDD25	AR8
VDD25	AT34
VDD25	D31
VDD25	D32
VDD25	D34
VDD25	D7
VDD25	D8
VDD25	E15
VDD25	E16
VDD25	E23
VDD25	E24
VDD25	E34
VDD25	F11
VDD25	F19
VDD25	F27
VDD25	F32
VDD25	F38
VDD25	F6
VDD25	F7
VDD25	J34
VDD25	J35
VDD25	J4
VDD25	J5
VDD25	K34

Signal	Ball
VDDQ15	C11
VDDQ15	C14
VDDQ15	E1
VDDQ15	F2
VDDQ15	H1
VDDQ15	L3
VDDQ15	M2
VDDQ15	P2
VDDQ15	P4
VDDQ15	U1
VDDQ15	V3
VDDQ15	Y1
VDDQ25	A4
VDDQ25	AC1
VDDQ25	AN4
VDDQ25	AT8
VDDQ25	AU5
VDDQ25	AV7
VDDQ25	B4
VDDQ25	C6
VDDQ25	F3
VDDQ25	H3
VSS	A10
VSS	A12
VSS	A13
VSS	A2
VSS	A21
VSS	A23
VSS	A24
VSS	A27
VSS	A35
VSS	A6
VSS	A8
VSS	A9

Signal	Ball
VSS	AR29
VSS	AR30
VSS	AR34
VSS	AR9
VSS	AT11
VSS	AT12
VSS	AT13
VSS	AT15
VSS	AT3
VSS	AU1
VSS	AU10
VSS	AU12
VSS	AU14
VSS	AU16
VSS	AU22
VSS	AU33
VSS	AU36
VSS	AU37
VSS	AU7
VSS	AV13
VSS	AV19
VSS	AV24
VSS	AV27
VSS	AV29
VSS	AV5
VSS	AV6
VSS	AV8
VSS	B12
VSS	B16
VSS	B31
VSS	B32
VSS	B34
VSS	B35
VSS	B36

Signal	Ball
VSS	P35
VSS	R2
VSS	R33
VSS	R34
VSS	R37
VSS	R5
VSS	R6
VSS	T1
VSS	T3
VSS	T33
VSS	T34
VSS	T37
VSS	T5
VSS	T6
VSS	U2
VSS	U35
VSS	U38
VSS	V36
VSS	V4
VSS	W1
VSS	W3
VSS	W33
VSS	W34
VSS	W5
VSS	W6
VSS	Y2
VSS	Y3
VSS	Y33
VSS	Y34
VSS	Y37
VSS	Y5
VSS	Y6

9 Pin Description

Pin Name	Type	Pin No	Function
SRAM Interface (95 Pins) The SRAM interface is a 2.5V, 125 MHz ZBT SRAM interface.			
XCLK	Input		Crystal clock, nominally 125 MHz.
SRAMCLK_O	Output		SRAM Clock Out. This clock is derived from XCLK, and must drive both the SRAM and the SYSCLK input for proper operation.
SYSCLK_O	Output		SYSCLK Output Feedback Clock. This clock is identical to SRAMCLK_O, but must be connected to the SYSCLK input. It is used to match the delays that SRAMCLK_O experiences, allowing the timing on the SRAM interface to be guaranteed.
SYSCLK	Input		System Clock. This clock must be driven by the SYSCLK_O output.
SDAT[63:0]	I/O		SRAM Data. During a write, this output is updated on SRAMCLK_O. During reads, this input is sampled on the rising edge of SYSCLK. One cycle of high-impedance is inserted between changes of direction on this I/O.
SPAR[7:0]	I/O		SRAM Parity. These bits provide byte parity protection across SDAT[63:0] and SADDR[17:0]. During writes, SPAR[7:0] is generated by XORing together 8 bits of odd parity on SDAT[63:0] with 3 bits, LSB justified, of odd parity on SADDR[17:0]. During writes, this output is updated on the rising edge of SRAMCLK_O. During reads, this input is sampled on the rising edge of SYSCLK. One cycle of high-impedance is inserted between changes of direction on this I/O.
SADDR[17:0]	Output		SRAM Address. 18 bits are provided, to support up to a 256Kx72 external SRAM. If less SRAM is provisioned, the MSB of the RAM address (which selects the Linkage vs Search tables) should still be connected to SADDR[17]; SADDR[16] may be left unconnected if only 8M of external SRAM is needed, SADDR[16:15] if only 4M, and so on. This output is updated on the rising edge of SRAMCLK_O.
SRWB	Output		SRAM Read/Write. Indicates whether a read or a write access is to be executed on the SRAM. Updated on the rising edge of SRAMCLK_O.
SCEB	Output		SRAM Chip Enable. When low, activates the external SRAM for an access. When high, the SRAM is deselected, and must go high-impedance on the third subsequent rising edge of SRAMCLK_O. Updated on the rising edge of SRAMCLK_O.

Pin Name	Type	Pin No	Function
Input Cell/Packet Interface (49 Pins) This interface can work in one of four different modes: Mode A (ingress UL3 master input) : Rx Link Layer UTOPIA L3 interface (prefix: RLU_*) Mode B (egress UL3 slave input) : Tx PHY Layer UTOPIA L3 interface (prefix: TPU_*) Mode C (PosPhy ingress input) : Rx Link Layer PosPhy L3 interface (prefix: RLP_*) Mode D (PosPhy egress input) : Tx PHY Layer PosPhy L3 interface (prefix: TPP_*) One of these four modes may be chosen in software. The choice of mode is static is must not be changed during chip operation. The easiest way to read the table below is to pick a mode of operation (A,B,C, or D) and to read only those lines that pertain to the chosen mode. Each pin also has a generic name, which may be used to reference the pin diagrams.			
ICIF_CLK	Input		
(A) RLU_CLK			(A) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz.
(B) TPU_CLK			(B) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz.
(C) RLP_CLK			(C) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz.
(D) TPP_CLK			(D) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz.
ICIF_DAT[31:0]	Input		
(A) RLU_DAT[31:0]			(A) 32-bit data bus. The data path for data from the PHY to the S/UNI-ATLAS-3200. In the 32-bit data path, RLU_DAT[31] is the MSB, RLU_DAT[0] is the LSB.
(B) TPU_DAT[31:0]			(B) 32-bit data bus. The data path for data from the Traffic Manager/Fabric to the S/UNI-ATLAS-3200. In the 32-bit data path, TPU_DAT[31] is the MSB, TPU_DAT[0] is the LSB.
(C) RLP_DAT[31:0]			(C) 32-bit data bus. The RLP_DAT[31:0] bus carries the packet octets that are read from the receive FIFO and the in-band port address of the selected receive FIFO. RLP_DAT[31:0] is considered as valid packet data when RLP_VAL is asserted. When RLP_EOP is asserted, the RLP_MOD[1:0] bits indicate how many bytes are valid. When RLP_SX is asserted, RLP_DAT[7:0] contains the in-band port address, and RLP_DAT[31:24] optionally carries the Payload Type field identifying the packet as ATM or POS. RLP_DAT[31] is the most significant bit.
(D) TPP_DAT[31:0]			(D) 32-bit data bus. This bus carries the packet octets that are written to the selected transmit FIFO and the in-band port address to select the desired transmit FIFO. The TPP_DAT bus is considered valid packet data when TPP_ENB is asserted. When TPP_SX is asserted, TPP_DAT[7:0] contains the in-band port address, and TPP_DAT[31:24] optionally carries the Payload Type field identifying the packet as ATM or POS. TPP_DAT[31] is the most significant bit.

Pin Name	Type	Pin No	Function
ICIF_PAR	Input		
(A) RLU_PAR			(A) Parity over RLU_DAT (programmable to odd or even)
(B) TPU_PAR			(B) Parity over TPU_DAT (programmable to odd or even)
(C) RLP_PAR			(C) Parity over data bus (programmable to odd or even) The receive parity (RLP_PAR) signal indicates the parity calculated over the RLP_DAT bus, and is required to be valid whenever RLP_VAL or RLP_SX are asserted.
(D) TPP_PAR			(D) Parity over data bus (programmable to odd or even) The transmit parity (TPP_PAR) signal indicates the parity calculated over the TPP_DAT bus. TPP_PAR is considered valid only when TPP_ENB or TPP_SX are asserted.
ICIF_SOC_SOP	Input		
(A) RLU_SOC			(A) Start of cell. Active high signal asserted to indicate the start of cell position. Whenever RLU_SOC is logic 1, the S/UNI-ATLAS-3200 will assume that the start of cell is present, and will synchronize itself accordingly.
(B) TPU_SOC			(B) Start of cell. Active high signal asserted to indicate the start of cell position. Whenever RLU_SOC is logic 1, the S/UNI-ATLAS-3200 will assume that the start of cell is present, and will synchronize itself accordingly.
(C) RLP_SOP			(C) Start of packet. RLP_SOP is used to delineate the packet boundaries on the RLP_DAT bus. When RLP_SOP is high, the start of the packet is present on the RLP_DAT bus. RLP_SOP is required to be present at the start of every packet and is considered valid when RLP_VAL is asserted.
(D) TPP_SOP			(D) Start of packet. TPP_SOP is used to delineate the packet boundaries on the TPP_DAT bus. When TPP_SOP is high, the start of the packet is present on the TPP_DAT bus. TPP_SOP is required to be present at the beginning of every packet and is considered valid only when TPP_ENB is asserted.

Pin Name	Type	Pin No	Function
ICIF_EOP	Input		
(A) not used			
(B) not used			
(C) RLP_EOP			(C) End of packet. RLP_EOP is used to delineate the packet boundaries on the RLP_DAT bus. When RLP_EOP is high, the end of the packet is present on the RLP_DAT bus. RLP_MOD[1:0] indicates the number of valid bytes the last double-word is composed of when RLP_EOP is asserted. RLP_EOP is required to be present at the end of every packet and is considered valid only when RVAL is asserted. S/UNI-ATLAS-3200 will always end a transfer at EOP, and perform a new RLP_SX cycle. As a result, the minimum average packet size for which OC-48 throughput can be guaranteed is 32 bytes.
(D) TPP_EOP			(D) End of packet. TPP_EOP is used to delineate the packet boundaries on the TPP_DAT bus. When TPP_EOP is high, the end of the packet is present on the TPP_DAT bus. TPP_MOD[1:0] indicates the number of valid bytes the last double-word is composed of when TPP_EOP is asserted. TPP_EOP is required to be present at the end of every packet and is considered valid only when TPP_ENB is asserted. S/UNI-ATLAS-3200 will always end a transfer at EOP, and perform a new SX cycle. As a result, the minimum average packet size for which OC-48 throughput can be guaranteed is xx bytes. Each transfer requires a separate positive PTPA response. As a result, the minimum average packet size which can be guaranteed in single-PHY operation is xx bytes.

Pin Name	Type	Pin No	Function
ICIF_MOD[1:0]	Input		
(A) not used			
(B) not used			
(C) RLP_MOD[1:0]			(C) Number of bytes in packet modulo 4 RLP_MOD[1:0] indicates the number of valid bytes of data in RLP_DAT[31:0]. The RLP_MOD bus should always be all zero, except during the last double-word transfer of a packet on RLP_DAT[31:0]. When RLP_EOP is asserted, the number of valid packet data bytes on RLP_DAT[31:0] is specified by RLP_MOD[1:0] RLP_MOD[1:0] = "00" RLP_DAT[31:0] valid RLP_MOD[1:0] = "01" RLP_DAT[31:8] valid RLP_MOD[1:0] = "10" RLP_DAT[31:16] valid RLP_MOD[1:0] = "11" RLP_DAT[31:24] valid RLP_MOD[1:0] is considered valid only when RLP_VAL is asserted.
(D) TPP_MOD[1:0]			(D) Number of bytes in packet modulo 4 TPP_MOD[1:0] indicates the number of valid bytes of data in TPP_DAT[31:0]. The TPP_MOD bus should always be all zero, except during the last double-word transfer of a packet on TPP_DAT[31:0]. When TPP_EOP and TPP_ENB are asserted, the number of valid packet data bytes on TPP_DAT[31:0] is specified by TPP_MOD[1:0]. TPP_MOD[1:0] = "00" TPP_DAT[31:0] valid TPP_MOD[1:0] = "01" TPP_DAT[31:8] valid TPP_MOD[1:0] = "10" TPP_DAT[31:16] valid TPP_MOD[1:0] = "11" TPP_DAT[31:24] valid
ICIF_ERR	Input		
(A) not used			
(B) not used			
(C) RLP_ERR			(C) Error: discard packet. RLP_ERR is used to indicate that the current packet is aborted and should be discarded. RLP_ERR shall only be asserted when RLP_EOP is asserted. Conditions that can cause RLP_ERR to be set may be, but are not limited to, FIFO overflow, abort sequence detection and FCS error. RLP_ERR is not expected to be asserted for ATM cells, and has no effect on their processing. RLP_ERR is considered valid only when RLP_VAL is asserted.
(D)TPP_ERR			(D) Packet in Error. If TPP_ERR is asserted when TPP_EOP and TPP_ENB are also asserted, then the packet is flagged in error. TPP_ERR is not expected to be asserted for ATM cells, and has no effect on their processing.

Pin Name	Type	Pin No	Function
ICIF_ADDR[5:0]	I/O		
(A) RLU_ADDR[5:0]	Output		(A) PHY address. RLU_ADDR indicates the PHYID for which a response is expected on RLU_CLAV, and (on the last cycle during which RLU_RDENB is deasserted) indicates the PHYID on which to transfer then next cell.
(B) TPU_ADDR[5:0]	Input		(B) PHY address. TPU_ADDR indicates the PHYID for which TPU_CLAV is to respond, and (on the last cycle during which TPU_WRENB is deasserted) indicates the PHYID which the subsequent cell belongs to.
(C) not used	Input		(C) Unused
(D) TPP_ADDR[5:0]	Input		(D) PHY address (valid values 0 to 47) . The TPP_ADDR bus is used with the TPP_PTPA signal to poll the transmit FIFOs packet available status. When TPP_ADDR is sampled on the rising edge of TPP_CLK by the PHY, the polled packet available indication TPP_PTPA signal is updated with the status of the port specified by the TPP_ADDR address on the following rising edge of TPP_CLK.
ICIF_CTRL	Input		
(A) RLU_CLAV			(A) Cell available. When sampled high, this pin indicates that the PHY can transfer at least one cell on the polled PHY, in addition to any cell currently being transferred. If RLU_CLAV is asserted at least 8 cycles before the end of the cell, then an additional cell may be transferred on the same PHY without loss of efficiency.
(B) TPU_WRENB			(B) Write enable. Active low signal initiates a cell transfer. Used for address selection in Multi-PHY mode when deasserted.
(C) RLP_VAL			(C) Data valid. RLP_VAL indicates the validity of the receive data signals. RLP_VAL is low between transfers, when RSX is asserted, and when the PHY pauses a transfer due to an empty receive FIFO. When RLP_VAL is high, the RLP_DAT[31:0], RLP_MOD[1:0], RLP_SOP, RLP_EOP and RLP_ERR signals are valid. When RLP_VAL is low, the RLP_DAT[31:0], RLP_MOD[1:0], RLP_SOP, RLP_EOP and RLP_ERR signals are invalid and must be disregarded. When a transfer is paused by holding RLP_ENB low, RVAL will hold its value unchanged, although no new data will be present on RDAT[31:0] until the transfer resumes. The RLP_SX signal is valid when RLP_VAL is low.
(D) TPP_ENB			(D) Write enable. The TPP_ENB signal is used to control the flow of data to the S/UNI-ATLAS-3200. When TPP_ENB is high, the TPP_DAT, TPP_MOD, TPP_SOP, TPP_EOP and TPP_ERR signals are invalid and are ignored. The TPP_SX signal is valid when TPP_ENB is high. When TPP_ENB is low, the TPP_DAT, TPP_MOD, TPP_SOP, TPP_EOP and TPP_ERR signals are valid and are processed. TPP_SX is ignored when TPP_ENB is low.

Pin Name	Type	Pin No	Function
ICIF_ENB_STPA	Output		
(A) RLU_RDENB			(A) Read enable. Active low signal asserted to initiate a cell transfer. Used for address selection during the last cycle before it is asserted.
(B) not used			
(C) RLP_ENB			(C) Read enable. The RLP_ENB signal is used to control the flow of data from the PHY's receive FIFOs. During data transfer, RLP_VAL will be monitored as it will indicate if the RLP_DAT[31:0], RLP_PAR, RLP_MOD[1:0], RLP_SOP, RLP_EOP, RLP_ERR and RLP_SX are valid. RLP_ENB will be deasserted anytime the S/UNI-ATLAS-3200 is unable to accept data from the PHY device. When RLP_ENB is sampled high by the PHY device, a read should not be performed and the RLP_DAT[31:0], RLP_PAR, RLP_MOD[1:0], RLP_SOP, RLP_EOP, RLP_ERR, RLP_SX and RLP_VAL signals must remain unchanged on the following rising edge of RLP_CLK.
(D) TPP_STPA			(D) Selected PHY packet available. TPP_STPA is high whenever there are at least 16 32-bit words available in the transmit FIFO for the currently selected PHY. When TPP_STPA transitions low, it indicates that there are less than 16 32-bit words available in the Transmit FIFO. The latency on this signal is no more than 8 cycles. If STPA is being used, the source must take this latency into account in using STPA to avoid overflow. The use of STPA is optional; the source may safely rely solely on PTPA. The port whose status TPP_STPA reports is updated on the following rising edge of TPP_CLK after the PHY address on TPP_DAT is sampled by the PHY device.

Pin Name	Type	Pin No	Function
ICIF_SX	Input		
(A) not used			
(B) not used			
(C) RLP_SX			(C) Start of transfer. RLP_SX indicates when the in-band port address is present on the RLP_DAT bus. When RLP_SX is high and RLP_VAL is low, the value of RLP_DAT[7:0] is the address of the receive FIFO to be selected by the PHY. Subsequent data transfers on the RDAT bus will be from the FIFO specified by this in-band address. In the case of a single-PHY interface, the RLP_SX bit is optional. It may be tied low, in which case the Inbandaddr bit in the RxL Configuration Register should be set to logic 0, and the PHYID will always be assumed to be 0. RLP_SX must be high only when RLP_VAL is low.
(D) TPP_SX			(D) Start of transfer. TPP_SX indicates when the in-band port address is present on the TPP_DAT bus. When TPP_SX is high and TPP_ENB is high, the value of TPP_DAT[7:0] is the address of the transmit FIFO to be selected. Subsequent data transfers on the TPP_DAT bus will fill the FIFO specified by this in-band address. In the case of a single-PHY interface, the TPP_SX bit is optional. It may be tied low, in which case the Inbandaddr bit in the TxP Configuration Register should be set to logic 0, and the PHYID will always be assumed to be 0. TPP_SX is considered valid only when TPP_ENB is not asserted.
ICIF_CLAV_PTPA	Output		
(A) not used			
(B) TPU_CLAV			(B) Cell available. TPU_CLAV is asserted high in response to TPU_ADDR if at least one cell, in addition to any cell currently being transferred, can be accepted on the PHY specified by TPU_ADDR. TPU_CLAV is updated on the rising edge of TPU_CLK following the cycle in which TPU_ADDR is sampled.
(C) not used			
(D) TPP_PTPA			(D) Polled PHY packet available. TPP_PTPA is asserted high in response to polling on TPP_ADDR whenever the selected PHY can accept another burst of (at most) 16 32-bit words. A PHY may be polled while data is being transferred to it, and it will indicate whether or not it can accept another burst of (at most) 16 32-bit words in addition to the current burst. TPP_PTPA is updated on the rising edge of TPP_CLK following the cycle in which TPP_ADDR is sampled.

Pin Name	Type	Pin No	Function
Output Cell/Packet Interface (49 Pins) This interface can work in one of four different modes: Mode A (ingress UL3 slave output): Rx PHY Layer UTOPIA L3 interface (prefix: RPU_*) Mode B (egress UL3 master output): Tx Link Layer UTOPIA L3 interface (prefix: TLU_*) Mode C (ingress PosPhy 3 output): Rx PHY Layer PosPhy L3 interface (prefix: RPP_*) Mode D (egress PosPhy 3 output): Tx Link Layer PosPhy L3 interface (prefix: TLP_*) One of these four modes may be chosen in software. The choice of mode is static is must not be changed during chip operation. The easiest way to read the table below is to pick a mode of operation (A,B,C, or D) and to read only those lines that pertain to the chosen mode. Each pin also has a generic name, which may be used to reference the pin diagrams.			
OCIF_CLK	Input		
(A) RPU_CLK			(A) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz
(B) TLU_CLK			(B) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz
(C) RPP_CLK			(C) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz
(D) TLP_CLK			(D) Clock. Valid frequency is 75 to 104 MHz. All signals on this interface are sampled at the rising edge of this clock. Full OC-48c bandwidth is guaranteed only for 104 MHz
OCIF_DAT[31:0]	Output		
(A) RPU_DAT[31:0]			(A) 32-bit data bus. Data path for data from the S/UNI-ATLAS-3200 to the Traffic Manager/Fabric. RPU_DAT[31] is the MSB and RPU_DAT[0] is the LSB.
(B) TLU_DAT[31:0]			(B) 32-bit data bus. Data path for data from the S/UNI-ATLAS-3200 to the PHY. TLU_DAT[31] is the MSB and TLU_DAT[0] is the LSB.
(C) RPP_DAT[31:0]			(C) 32-bit data bus. The RPP_DAT[31:0] bus carries the packet octets that are read from the receive FIFO and the in-band port address of the selected receive FIFO. RPP_DAT[31:0] is considered valid only when RPP_VAL is asserted When RPP_SX is asserted, RPP_DAT[7:0] contains the in-band port address, and RPP_DAT[31:24] optionally carries the Payload Type field identifying the packet as ATM or POS. RPP_DAT[31] is the most significant bit.
(D) TLP_DAT[31:0]			(D) 32-bit data bus. This bus carries the packet octets that are written to the selected transmit FIFO and the in-band port address to select the desired transmit FIFO. The TLP_DAT bus is considered valid only when TLP_ENB is simultaneously asserted. When TLP_SX is asserted, TLP_DAT[7:0] contains the in-band port address, and TLP_DAT[31:24] optionally carries the Payload Type field identifying the packet as ATM or POS. TLP_DAT[31] is the most significant bit.

Pin Name	Type	Pin No	Function
OCIF_PAR	Output		
(A) RPU_PAR			(A) Parity over data bus (programmable to odd or even)
(B) TLU_PAR			(B) Parity over data bus (programmable to odd or even)
(C) RPP_PAR			(C) Parity over data bus (programmable to odd or even) The receive parity (RPP_PAR) signal indicates the parity calculated over the RPP_DAT bus. RPP_PAR is valid whenever RPP_VAL or RPP_SX are asserted.
(D) TLP_PAR			(D) Parity over data bus (programmable to odd or even) The transmit parity (TLP_PAR) signal indicates the parity calculated over the TLP_DAT bus. TLP_PAR is considered valid only when TLP_ENB or TLP_SX is asserted.
OCIF_SOC_SOP	Output		
(A) RPU_SOC			(A) Start of cell. Active high signal asserted to indicate the start of cell position. It is expected that, in case of loss of synchronization, that RPU_SOC will serve to resynchronize the interface.
(B) TLU_SOC			(B) Start of cell. Active high signal asserted to indicate the start of cell position. It is expected that, in case of loss of synchronization, that TLU_SOC will serve to resynchronize the interface.
(C) RPP_SOP			(C) Start of packet. RPP_SOP is used to delineate the packet boundaries on the RPP_DAT bus. When RPP_SOP is high, the start of the packet is present on the RPP_DAT bus. RPP_SOP is required to be present at the start of every packet and is considered valid when RPP_VAL is asserted..
(D) TLP_SOP			(D) Start of packet. TLP_SOP is used to delineate the packet boundaries on the TLP_DAT bus. When TLP_SOP is high, the start of the packet is present on the TLP_DAT bus. TLP_SOP is required to be present at the beginning of every packet and is considered valid only when TLP_ENB is asserted.

Pin Name	Type	Pin No	Function
OCIF_EOP	Output		
(A) not used			
(B) not used			
(C) RPP_EOP			(C) End of packet. RPP_EOP is used to delineate the packet boundaries on the RPP_DAT bus. When RPP_EOP is high, the end of the packet is present on the RPP_DAT bus. RMOD[1:0] indicates the number of valid bytes the last double-word is composed of when RPP_EOP is asserted. REOP is required to be present at the end of every packet and is considered valid only when RVAL is asserted.
(D) TLP_EOP			(D) End of packet. TLP_EOP is used to delineate the packet boundaries on the TLP_DAT bus. When TLP_EOP is high, the end of the packet is present on the TLP_DAT bus. TLP_MOD[1:0] indicates the number of valid bytes the last double-word is composed of when TLP_EOP is asserted. TLP_EOP is required to be present at the end of every packet and is considered valid only when TLP_ENB is asserted. The S/UNI-ATLAS-3200 always ends a burst when EOP is asserted. The minimum average packet length for which OC-48 throughput may be guaranteed is 32 bytes.
OCIF_MOD[1:0]	Output		
(A) not used			
(B) not used			
(C) RPP_MOD[1:0]			(C) Number of bytes in packet modulo 4 RPP_MOD[1:0] indicates the number of valid bytes of data in RPP_DAT[31:0]. The RPP_MOD bus should always be all zero, except during the last double-word transfer of a packet on RPP_DAT[31:0]. When RPP_EOP is asserted, the number of valid packet data bytes on RPP_DAT[31:0] is specified by RPP_MOD[1:0] RPP_MOD[1:0] = “00” RPP_DAT[31:0] valid RPP_MOD[1:0] = “01” RPP_DAT[31:8] valid RPP_MOD[1:0] = “10” RPP_DAT[31:16] valid RPP_MOD[1:0] = “11” RPP_DAT[31:24] valid RPP_MOD[1:0] is considered valid only when RPP_VAL is asserted.
(D) TLP_MOD[1:0]			(D) Number of bytes in packet modulo 4 TLP_MOD[1:0] indicates the number of valid bytes of data in TLP_DAT[31:0]. The TLP_MOD bus should always be all zero, except during the last double-word transfer of a packet on TLP_DAT[31:0]. When TLP_EOP and TLP_ENB are asserted, the number of valid packet data bytes on TLP_DAT[31:0] is specified by TLP_MOD[1:0]. TLP_MOD[1:0] = “00” TLP_DAT[31:0] valid TLP_MOD[1:0] = “01” TLP_DAT[31:8] valid TLP_MOD[1:0] = “10” TLP_DAT[31:16] valid TLP_MOD[1:0] = “11” TLP_DAT[31:24] valid

Pin Name	Type	Pin No	Function
OCIF_ERR	Output		
(A) not used			
(B) not used			
(C) RPP_ERR			(C) Error: discard packet. RPP_ERR is used to indicate that the current packet is in error and should be discarded. RPP_ERR is only asserted when RPP_EOP is asserted. RPP_ERR is considered valid only when RPP_VAL is asserted.
(D) TLP_ERR			(D) Error. Packet should be aborted. Will only be asserted when TEOP is simultaneously asserted; only valid when TENB is asserted.
OCIF_ADDR[5:0]	I/O		
(A) RPU_ADDR[5:0]	Input		(A) PHY address (valid values 0 to 47). RPU_ADDR indicates the PHYID for which RPU_CLAV is to respond, and (on the last cycle during which RPU_ENB is deasserted) indicates the PHYID on which to transfer then next cell. The use of these bits is optional. If the UTOPIA Master is not designed to poll this interface, then the Rx PHY UTOPIA interface can be made to look like a single-PHY interface via the SERVEOVRD bit in the RxP Configuration Register. In this case, S/UNI-ATLAS-3200 will perform weighted-round-robin servicing on all the PHY queues internally, and CLAV will indicate whether a cell is available on any PHYID. In this case, these bits should be tied low.
(B) TLU_ADDR[5:0]	Output		(B) PHY address. TLU_ADDR indicates the PHYID for which TLU_CLAV is to respond, and (on the last cycle during which TLU_WRENB is deasserted) indicates the PHYID which the subsequent cell belongs to.
(C) not used	Input		(C) Unused
(D) TLP_ADDR[5:0]	Output		(D) PHY address (valid values 0 to 47). The TLP_ADDR bus is used with the TLP_PTPA signal to poll the transmit FIFOs packet available status. When TLP_ADDR is sampled on the rising edge of TLP_CLK by the PHY, the polled packet available indication TLP_PTPA signal is expected to be updated with the status of the port specified by the TLP_ADDR address on the following rising edge of TLP_CLK.

Pin Name	Type	Pin No	Function
OCIF_CTRL	Output		
(A) RPU_CLAV			(A) Cell available. RPU_CLAV is asserted in response to polling on RPU_ADDR to indicate that at least one complete cell is available on the PHYID specified by RPU_CLAV. If the interface is configured to look like a single-phy interface (via the SERVEOVRD bit in the RxP Configuration Register) then this bit indicates whether any complete cells are ready for transfer.
(B) TLU_WRENB			(B) Write enable. TLU_WRENB is asserted to enable the transfer of cell data. On the last cycle before it is asserted, the TLU_ADDR indicates the PHYID to which the subsequent cell belongs.
(C) RPP_VAL			(C) Data valid. RPP_VAL indicates the validity of the receive data signals. RPP_VAL is low between transfers, when RPP_SX is asserted, and when the S/UNI-ATLAS-3200 pauses a transfer due to an empty FIFO. When a transfer is paused by holding RPP_ENB low, RPP_VAL will hold its value unchanged, although no new data will be present on RDAT[31:0] until the transfer resumes. When RPP_VAL is high, the RPP_DAT[31:0], RPP_MOD[1:0], RPP_SOP, RPP_EOP and RPP_ERR signals are valid. When RPP_VAL is low, the RPP_DAT[31:0], RPP_MOD[1:0], RPP_SOP, RPP_EOP and RPP_ERR signals are invalid and must be disregarded. The RPP_SX signal is valid when RPP_VAL is low.
(D) TLP_ENB			(D) Write enable. The TLP_ENB signal is used to control the flow of data to the transmit FIFOs. When TLP_ENB is high, the TLP_DAT, TLP_MOD, TLP_SOP, TLP_EOP and TLP_ERR signals are invalid and are ignored by the PHY. The TLP_SX signal is valid and is processed by the PHY when TLP_ENB is high. When TLP_ENB is low, the TLP_DAT, TLP_MOD, TLP_SOP, TLP_EOP and TLP_ERR signals are valid and are processed by the PHY. Also, the TLP_SX signal is ignored by the PHY when TLP_ENB is low.

Pin Name	Type	Pin No	Function
OCIF_ENB_STPA	Input		
(A) RPU_RDENB			(A) Active-Low Read enable. When RPU_RDENB is asserted, a read is executed from the S/UNI-ATLAS-3200 on the PHYID which was present on RPU_ADDR during the cycle before RPU_RDENB was asserted.
(B) not used			
(C) RPP_ENB			(C) Active-Low Read enable. The RPP_ENB signal is used to backpressure the flow of data from the receive FIFOs. During data transfer, RPP_VAL must be monitored as it will indicate if the RPP_DAT[31:0], RPP_MOD[1:0], RPP_SOP, RPP_EOP, RPP_ERR and RPP_SX are valid. The system may deassert RPP_ENB at anytime if it is unable to accept data from the S/UNI-ATLAS-3200. When RPP_ENB is sampled low, a read is performed from the receive FIFO and the RPP_DAT[31:0], RPP_PAR, RPP_MOD[1:0], RPP_SOP, RPP_EOP, RPP_ERR, RPP_SX and RPP_VAL signals are updated on the following rising edge of RPP_CLK. When RPP_ENB is sampled low by the PHY device, a read is not performed and the RPP_DAT[31:0], RPP_PAR, RPP_MOD[1:0], RPP_SOP, RPP_EOP, RPP_ERR, RPP_SX and RPP_VAL signals will not updated on the following rising edge of RPP_CLK.
(D) TLP_STPA			(D) Selected PHY packet available. TLP_STPA always provides status indication for the selected port of PHY device in order to avoid FIFO overflows while polling is performed. The use of TLP_STPA is optional. If USE_STPA is logic 0 in the TxLink Configuration Register, then TLP_STPA is ignored. If USE_STPA is logic 1, then the S/UNI-ATLAS-3200 will cease transmission immediately after sampling TLP_STPA high, and may switch to another PHY at that point. The port which TLP_STPA reports is updated on the following rising edge of TLP_CLK after the PHY address on TLP_DAT is sampled by the PHY device.
OCIF_SX	Output		
(A) not used			
(B) not used			
(C) RPP_SX			(C) Start of transfer. RPP_SX indicates when the in-band port address is present on the RPP_DAT bus. When RPP_SX is high and RPP_VAL is low, the value of RPP_DAT[7:0] is the address of the receive FIFO to be selected by the PHY. Subsequent data transfers on the RDAT bus will be from the FIFO specified by this in-band address. RPP_SX will not be asserted at the same time as RPP_VAL.
(D) TLP_SX			(D) Start of transfer. TLP_SX indicates when the in-band port address is present on the TLP_DAT bus. When TLP_SX is high and TLP_ENB is high, the value of TLP_DAT[7:0] is the address of the transmit FIFO to be selected. Subsequent data transfers on the TLP_DAT bus will fill the FIFO specified by this in-band address. TLP_SX will not be asserted at the same time as TLP_ENB

Pin Name	Type	Pin No	Function
OCIF_CLAV_PTPA	Input		
(A) not used			
(B) TLU_CLAV			(B) Cell available. To indicate that space for at least one cell is available in the PHY's transmit cell buffer. For back-to-back transfer to be guaranteed, TLU_CLAV must be asserted at least 5 cycles before the end of the current transfer. The value of TLU_CLAV is not used between the selection of an new PHYID and the second cycle after TLU_SOC is presented on the interface.
(C) not used			
(D) TLP_PTPA			(D) Polled PHY packet available. TLP_PTPA is used together with TLP_ADDR to poll for transmit FIFOs that have room available. S/UNI-ATLAS-3200 expects that if TLP_PTPA is asserted in response to TLP_ADDR, then that FIFO can accept at least one additional burst of 16 32-bit words, in addition to any burst currently being transferred. S/UNI-ATLAS-3200 will terminate a burst at an End Of Packet even if a full 16 words have not been transferred. TLP_PTPA is expected to be valid in the cycle following the cycle in which TLP_ADDR was sampled in the PHY.
Backwards Input Cell Interface (21 pins) SCI-PHY Interface (16-bit UTOPIA Level 1 with routing information prepended to cells). It can act as an Rx Master (its default, intended for attachment to an S/UNI-ATLAS-3200 Backwards Output Cell Interface) or as a Tx Slave (used when connecting to a device that is not an S/UNI-ATLAS-3200).			
BI_CLK	Input		IBCIF Clock. This clock should run between 40 to 52 MHz to ensure sufficient throughput on the Backwards Cell Interface.
BI_RRDENB _TCLAV	Output		Receive Read Enable (in BCIF Rx Master mode)/ Transmit Cell Available (in BCIF Tx Slave mode) In Rx Master mode, this bit is asserted low to read cells from the interface. In Tx Slave mode this indicates to the master that a cell is available in the transmit buffer.
BI_RCLAV _TWRENB	Input		Receive Cell Available (in BCIF Rx Master mode)/ Transmit Write Enable (in BCIF Tx Slave mode) In Rx Master mode the slave indicates that it has a cell in its transmit buffer by asserting this signal. In Tx Slave mode, the master indicates that it is going to transfer data into the slave device by asserting this signal.
BI_SOC	Input		Start of Cell. Must be asserted when the first word of the cell is on the data bus.
BI_DAT[15:0]	Input		16-bit data bus
BI_PAR	Input		Parity over BI_DAT[15:0].
Backwards Output Cell Interface (21 pins) SCI-PHY Interface (16-bit UTOPIA Level 1 with routing information prepended to cells)			
BO_CLK	Input		OBCIF Clock. This clock should run between 40 to 52 MHz to ensure sufficient throughput on the Backwards Cell Interface.

Pin Name	Type	Pin No	Function
BO_RDENB	Input		Read Enable. The S/UNI-ATLAS-3200 will transfer data out onto the data bus when this signal is asserted.
BO_CLAV	Output		Cell Available. Indicates that the S/UNI-ATLAS-3200 has at least one cell to transfer.
BO_SOC	Output		Start of Cell. Asserted when the first word of the cell is on the data bus.
BO_DAT[15:0]	Output		Data
BO_PAR	Output		Parity over BO_PAR[15:0].
Microprocessor Access Port (52 Pins)			
UP_DAT[31:0]	I/O		The bi-directional data bus, UP_DAT[31:0] is used during S/UNI-ATLAS-3200 Microprocessor Interface Port register reads and write accesses. UP_DAT[31] is the MSB.
UP_ADDR[11:0]	Input		The address UP_ADDR[11:0] selects specific Microprocessor Interface Port registers during S/UNI-ATLAS-3200 register accesses. UP_ADDR[11] is the Test Register Select (TRS) address pin. TRS selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
UP_RDB	Input		UP_RDB is low during S/UNI-ATLAS-3200 Microprocessor Interface Port register read accesses. The S/UNI-ATLAS-3200 drives the UP_DAT[31:0] bus with the contents of the addressed register while UP_RDB and UP_CSB are low.
UP_WRB	Input		UP_WRB is low during S/UNI-ATLAS-3200 Microprocessor Interface Port register write accesses. The UP_DAT[31:0] bus contents are clocked into the addressed register on the rising edge of UP_WRB while UP_CSB is low.
UP_CSB	Input		UP_CSB is low during S/UNI-ATLAS-3200 Microprocessor Interface Port register accesses. If UP_CSB is not required (i.e. register accesses controlled using UP_RDB and UP_WRB signals only), UP_CSB should be connected to an inverted version of the UP_RSTB input.
UP_ALE	Input		The Microprocessor Address Strobe, UP_ALE, is active high and latches the address bus, UP_ADDR[11:0], when low. When UP_ALE is high, the internal address latches are transparent. It allows the S/UNI-ATLAS-3200 to interface to a multiplexed address/data bus. UP_ALE has an internal pull up resistor.

Pin Name	Type	Pin No	Function
UP_DMAREQ	Output		The DMA request (UP_DMAREQ) is asserted when the Microprocessor Cell Interface (MCIF) contains a cell to be read. The first read of the MCIF Data register will return the first word of the cell. UP_DMAREQ is deasserted after the last word of the cell has been read or an abort has been signaled. The polarity of UP_DMAREQ is determined by the DMAREQINV bit in the Microprocessor Cell Interface Configuration register. By default, UP_DMAREQ is active high.
UP_BUSYB	Output		The UP_BUSYB output is asserted while a microprocessor initiated access to external SRAM or internal DRAM data is pending (for internal SRAM accesses, a microprocessor must poll the appropriate BUSY register bit). The BUSY bit will be asserted within 20 ns the rising edge of WRB on which the RAM access is initiated. The UP_BUSYB output is deasserted after the access has been completed. A microprocessor access to external SRAM is typically completed within 30 SYSCLK cycles; an access to internal DRAM is typically completed within 220 cycles. If the STANDBY bit in the Master Configuration is set to logic 1, the access time is reduced to typically than 10 SYSCLK cycles for internal accesses and 25 clock cycles for internal DRAM accesses. The polarity of the UP_BUSYB output is programmable and defaults to active low.
UP_INTB	Output		The Interrupt Request (UP_INTB) output goes low when an S/UNI-ATLAS-3200 interrupt source is active and that source is unmasked. UP_INTB returns high when the interrupt is acknowledged via an appropriate register access. UP_INTB is an open drain output.
UP_RSTB	Input		The active low reset (UP_RSTB) signal provides an asynchronous S/UNI-ATLAS-3200 reset. UP_RSTB is a Schmitt trigger input with an integral pull up resistor. When UP_RSTB is forced low, all S/UNI-ATLAS-3200 registers are forced to their default states.
Miscellaneous (1 pin)			
HALFSECCLK	Input		Half-second clock. This signal must pulse once every half second, in order to correctly perform OAM alarm monitoring, OAM cell generation, and policing. If the GEN_HALFSECCLK register bit is set to logic 1 in the Cell Processor Configuration Register, then the half-second clock may be internally generated from the 125 MHz SYSCLK input, and the HALFSECCLK input may be left unused.
IEEE P1149.1 (JTAG) Interface (5 pins)			
TCK	Input		The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input Internal Pull-Up		The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull up resistor.
TDI	Input Internal Pull-Up		The test data input (TDI) signal carries test data into the S/UNI-ATLAS-3200 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.

Pin Name	Type	Pin No	Function
TDO	Tristate		The test data output (TDO) signal carries test data out of the S/UNI-ATLAS-3200 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is tri-stated except when the scanning of data is in progress
TRSTB	Schmitt Trigger Input Internal Pull-Up		The active low test reset (TRSTB) signal provides an asynchronous S/UNI-ATLAS-3200 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. The JTAG TAP controller must be initialized when the S/UNI-ATLAS-3200 is powered up. If the JTAG port is not used, TRSTB must be connected to the RSTB input or VSS.
DRAM Test (2 Pins)			
Reserved	Input Internal Pull-up		This pin must be tied to logic 1 in operation to avoid permanent damage to the device.
Reserved	Input Internal Pull-up		This pin must be tied to logic 1 to ensure correct operation.
ZETMDL	I/O		This pin must be tied to logic 0 for proper operation
ZETMDR	I/O		This pin must be tied to logic 1 for proper operation
Power/Ground			
VDD33	Power		3.3V I/O Power.
VDD25	Power		2.5V I/O Power
VDDQ25	Power		2.5V DRAM Core Power. This supply should be kept quiet to improve DRAM performance.
VDDQ15	Power		1.5V DRAM Core Power. This supply should be kept quiet to improve DRAM performance.
VDD15	Power		1.5V Core Power
VSS	Ground		Common Ground

Notes on Pin Description:

1. All S/UNI-ATLAS-3200 inputs and bi-directionals present minimum capacitive loading and operate at LVTTL logic levels.
2. All inputs and bi-directionals have internal pull-up resistors.
3. The recommended power supply sequencing is as follows:
   - 3.1 During power-up, VDD33 must be brought up before or at the same time as VDD25 and VDDQ25, which must be brought up before or at the same time as VDD15 and VDDQ15.
   - 3.2 The VDD33 and VDD25 power must be applied before input pins are driven or the input current per pin be limited to less than the maximum DC input current specification. (10 mA)
   - 3.3 Power down the device in the reverse sequence.

10 Functional Description

10.1 Input and Output Interfaces

The S/UNI-ATLAS-3200 supports two kinds of signaling: UTOPIA Level 3, which is used for transferring fixed-length ATM cells; and POS-PHY Level 3, which is used for transferring variable-length packets. Applications that require the S/UNI-ATLAS-3200 to transfer mixed cell and packet traffic should use POS-PHY signaling.

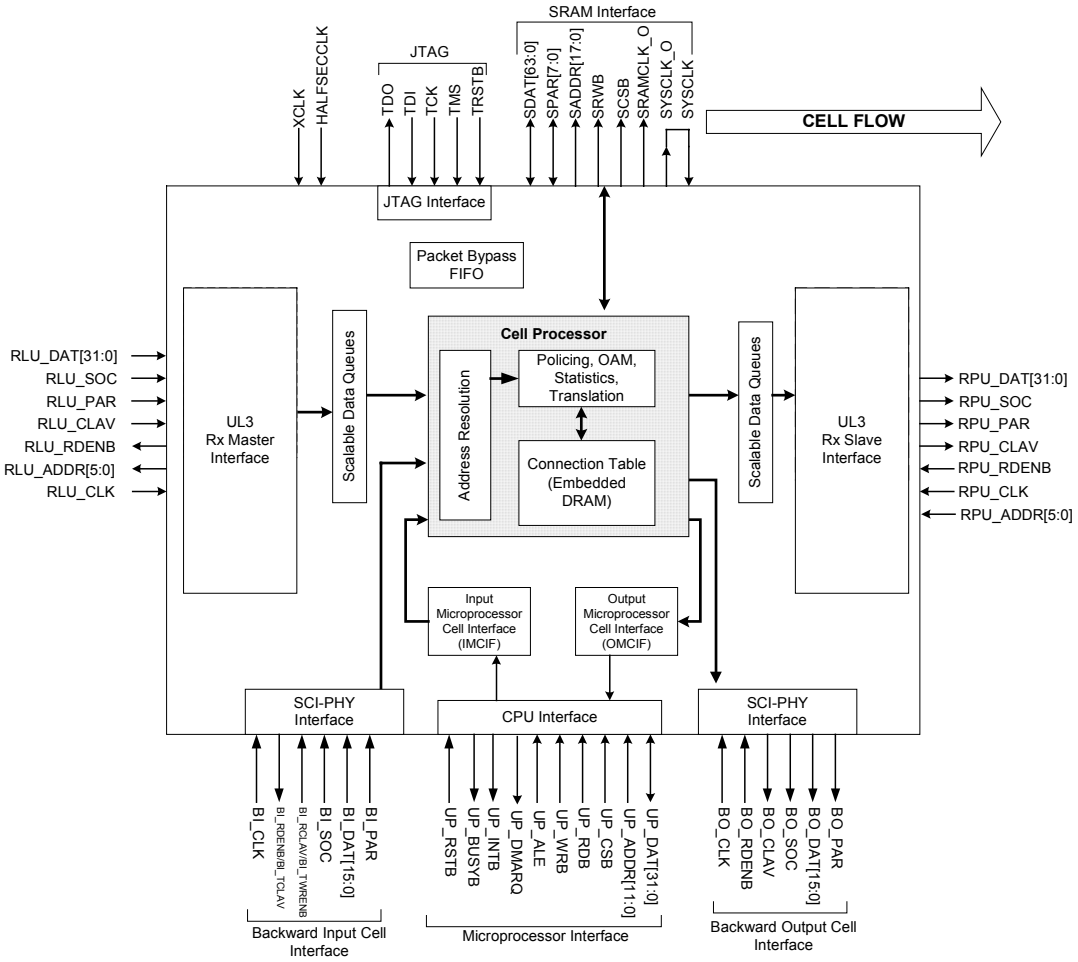
Independent of the UL3 or POS signaling, the S/UNI-ATLAS-3200 may operate in two modes: the Ingress and the Egress mode. The S/UNI-ATLAS-3200 is typically deployed in pairs. One chip of the pair receives cells/packets from PHY devices and sends them towards the traffic manager/switch core. This chip is said to be in Ingress mode. The other chip of the pair receives cells/packets from the switch core and sends them to the PHY devices. This chip is said to be in Egress mode.

Thus, the S/UNI-ATLAS-3200 can be configured in four ways: UTOPIA or POS-PHY signaling, and Ingress or Egress mode. The S/UNI-ATLAS-3200 is in Ingress POS-PHY mode on reset, which is the state in which all UL3/POS pins that can be either inputs or outputs, are inputs. This avoids contention on startup.

10.1.1 Ingress Mode with UTOPIA Level 3 Signaling

In this configuration, the S/UNI-ATLAS-3200 receives traffic from a PHY, and transmits traffic to a traffic manager. This traffic consists of ATM cells, transferred using UTOPIA Level 3 signaling.

Figure 5 UTOPIA Level 3 Ingress Interface



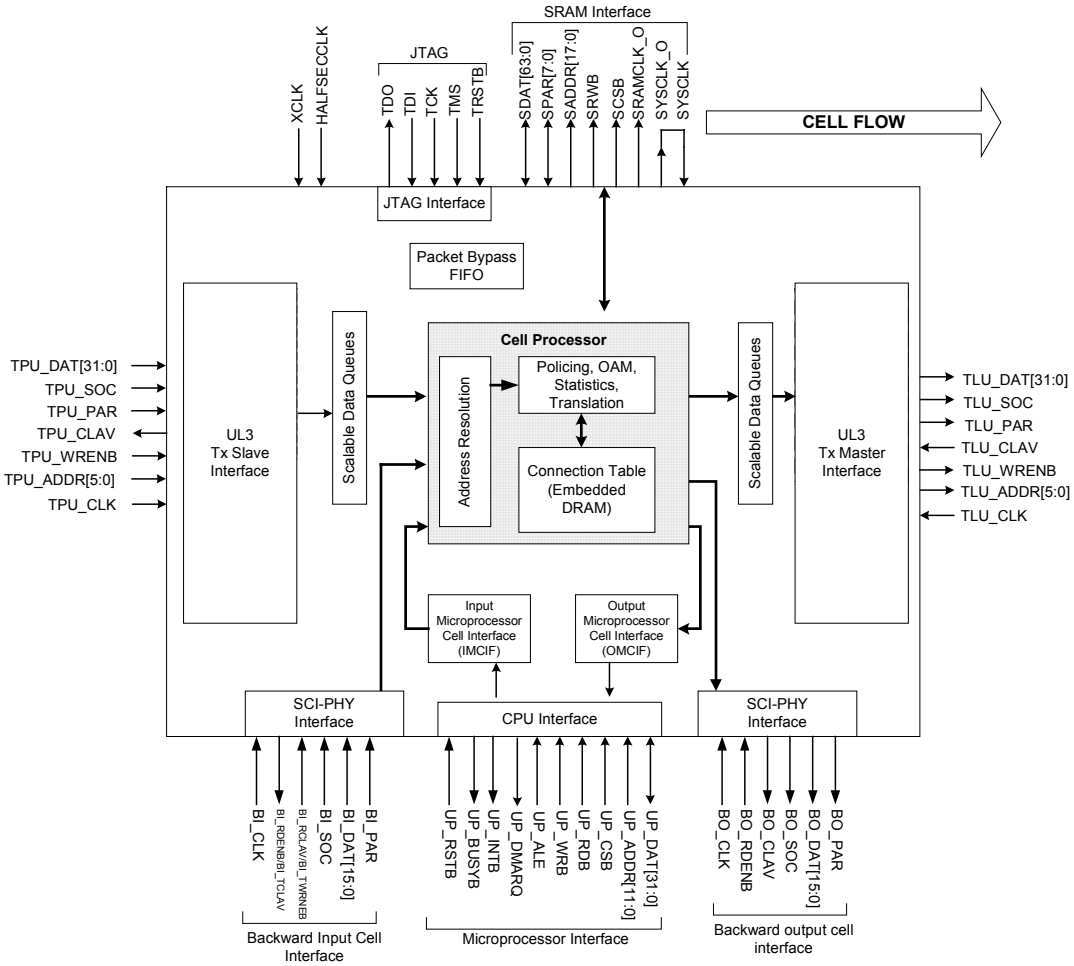
The S/UNI-ATLAS-3200 input interface must behave as an Rx Link Layer device on the UTOPIA bus. As a Link Layer device, it controls the address bus, RLU_ADDR, in order to poll the PHY Layer device to obtain cell available status. Polling is performed in a weighted round-robin fashion controlled by a software-configurable calendar. Once the Cell Available information has been collected through polling, port selection is performed using the same calendar. The calendar is programmed via the RxLink block's Calendar Address and Data Register, and is described in Section 10.1.7. The RxLink block can map external PHY addresses to different internal PHY addresses via a user-programmable port map, as described in Section 10.1.6. The RxLink block, assisted by the SDQ block (see below) performs these functions. The RxLink configuration registers may be found in Section 11.6.

The S/UNI-ATLAS-3200 output interface must behave as an Rx PHY layer device on the UTOPIA bus. As a PHY layer device, it responds with the appropriate cell available status when a channel address is on the bus, RPU_ADDR. When the Link Layer device (a TM or switch) engages a transfer, the S/UNI-ATLAS-3200 must respond by sending the next cell for the channel that has been selected. Optionally, the S/UNI-ATLAS-3200 will behave as a single-PHY device, ignoring RPU_ADDR. It will service the internal per-PHY cell queues in a weighted round-robin fashion controlled by a software-configurable calendar. The calendar is programmed via the RxPhy block's Calendar Address and Data Register, and is described in Section 10.1.7. The RxPhy block, assisted by the SDQ block (see below) performs these functions. The RxPhy configuration registers may be found in section 11.9.

10.1.2 Egress Mode with UTOPIA Level 3 Signaling

In this configuration, the S/UNI-ATLAS-3200 receives traffic from a traffic manager, and transmits traffic to a PHY. This traffic consists of ATM cells, transferred using UTOPIA Level 3 signaling.

Figure 6 UTOPIA Level 3 Egress Interface



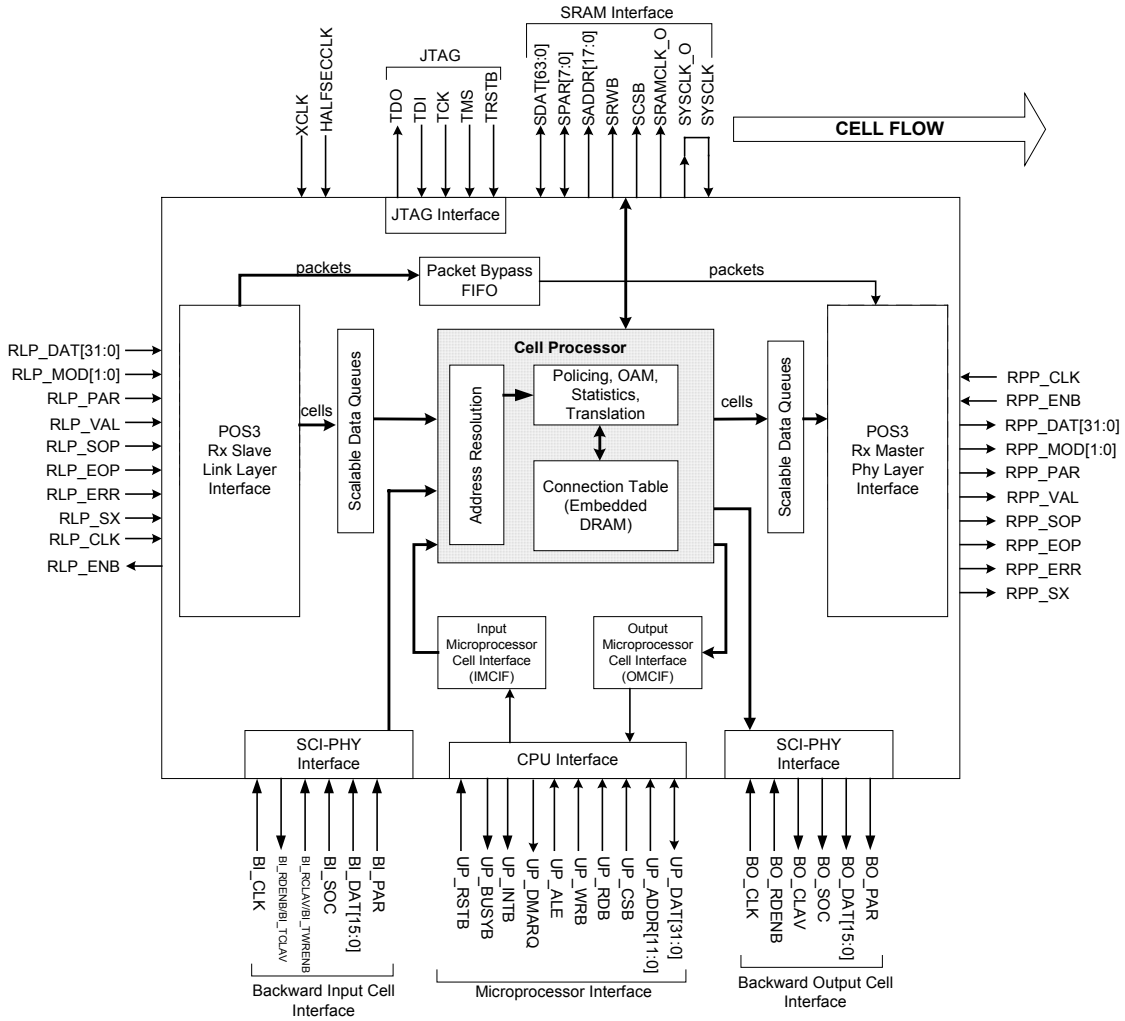
The S/UNI-ATLAS-3200 input interface must behave as a Tx PHY layer device on the UTOPIA bus. As a PHY layer device, it responds with the appropriate cell available (buffer) status when a channel address is on the bus, TPU_ADDR. Additionally, when the ATM layer device engages a transfer, the S/UNI-ATLAS-3200 must respond by accepting cell for the channel that has been selected. The TxPhy block, assisted by the SDQ (see below) performs these functions. The TxPhy configuration registers may be found in Section 11.7.

The S/UNI-ATLAS-3200 output interface must behave as a Tx Link Layer device on the UTOPIA bus. As a Link Layer device, it controls the address bus, TLU_ADDR, in order to poll the PHY to obtain cell available (buffer) status. Polling is performed in a weighted round-robin fashion controlled by a software-configurable calendar. Once the Cell Available information has been collected through polling, port selection is performed using the same calendar. The calendar is programmed via the TxLink block's Calendar Address and Data Register, and is described in Section 10.1.7. The TxLink block can map internal PHY addresses to different external PHY addresses via a user-programmable port map, as described in Section 10.1.6. The TxLink block, assisted by the SDQ (see below) performs these functions. The TxLink configuration registers may be found in Section 11.10.

10.1.3 Ingress Mode with POS-PHY Level 3 Signaling

In this configuration, the S/UNI-ATLAS-3200 receives traffic from a PHY, and transmits traffic to a traffic manager. This traffic consists of variable-length packets, transferred using POS-PHY Level 3 signaling.

Figure 7 POS-PHY Level 3 Ingress Interface



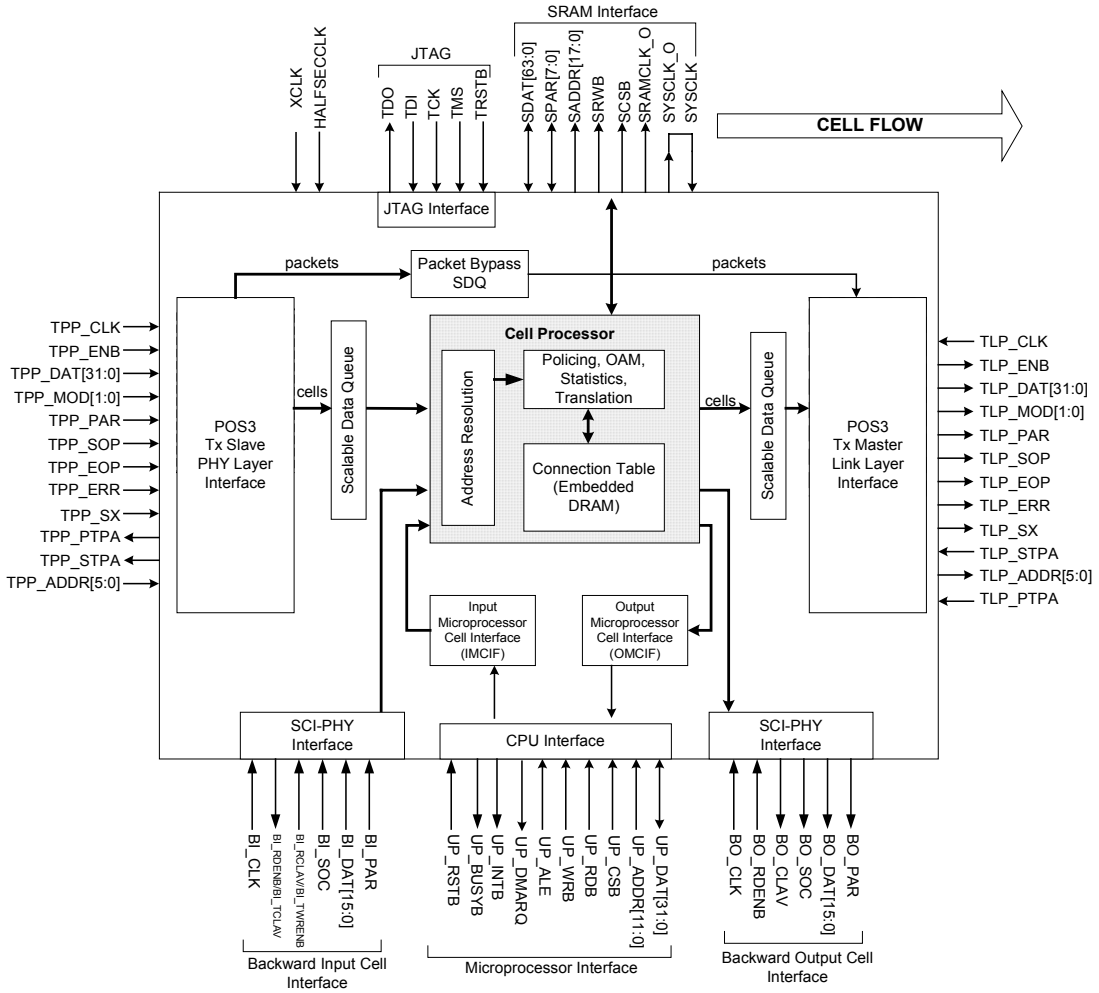
The S/UNI-ATLAS-3200 input interface must behave as the Rx Link-layer on the POS-PHY bus. As the Link-layer, its function is to accept information sent by the PHY-layer, which controls the flow of data and the selection process. The Link-layer provides a back-pressure indication (RLP_ENB) to prevent it from overflowing. The RxLink block can map external PHY addresses to different internal PHY addresses via a user-programmable port map, as described in Section 10.1.6. The RxLink block, assisted by the SDQ block (see below) performs the above functions. The RxLink configuration registers may be found in Section 11.9

The S/UNI-ATLAS-3200 output interface must behave as the Rx PHY-layer on the POS-PHY bus. As the PHY-layer, it controls the flow of information to the Link-layer. It does so by selecting the channel for transfer on the data bus, RPP_DAT. Channel selection is performed in a weighted round-robin fashion controlled by a software-configurable calendar. The calendar is programmed via the RxPhy block's Calendar Address and Data Register, and is described in Section 10.1.7. When a PHY queue is serviced, it is permitted to transfer one ATM cell or POS-PHY packet, or an amount of data equal to the Burst Size for that PHY, whichever is less. The RxPhy block, assisted by the Output SDQ block (see below) performs the above functions. Its configuration registers may be found in Section 11.9.

10.1.4 Egress Mode with POS_PHY Level 3 Signaling

In this configuration, the S/UNI-ATLAS-3200 receives traffic from a traffic manager, and transmits traffic to a PHY. This traffic consists of variable-length packets, transferred using POS-PHY Level 3 signaling.

Figure 8 POS-PHY Level 3 Egress Interface



The S/UNI-ATLAS-3200 input interface must behave as the Tx PHY layer device on the POS-PHY bus. As the PHY-layer, its function is to accept information sent by the Link-layer, to respond to polling on TPP_ADDR with the appropriate packet available (buffer) status on TPP_PTPA, and to provide backpressure on the selected port on TPP_STPA. The TxPhy block, assisted by the SDQ block (see below) performs the above functions. Its configuration registers may be found in Section 11.7.

The S/UNI-ATLAS-3200 must behave as a Tx Link-layer on the POS-PHY bus. As the Link-layer, it controls the flow of information to the PHY Layer device, by polling the PHY Layer device to obtain packet available (buffer) status. Polling is performed in a weighed round-robin fashion controlled by a software-configurable calendar. Once the Cell Available information has been collected through polling, port selection is performed using the same calendar. The calendar is programmed via the TxLink block's Calendar Address and Data Register, and is described in Section 10.1.7. When a PHY is serviced, it is permitted to transfer one ATM cell or POS-PHY packet, or an amount of data equal to the programmed Burst Size for that PHY, whichever is less. The TxLink block can map internal PHY addresses to different external PHY addresses via a user-programmable port map, as described in Section 10.1.6. The TxLink block, assisted by the SDQ block (see below) performs the above functions. Its configuration registers may be found in Section 11.10.

10.1.5 Polling and Servicing Calendar

Polling and servicing of PHY queues is performed in a weighted round-robin fashion. The order of the polling, and the relative weighting of different PHYs is directly configured by writing a calendar to each of the interface blocks that supports polling or servicing. The calendar is a circular list of PHY IDs. When polling, the poller continuously presents the PHY IDs in the order shown in the calendar, and records the resulting Cell/Buffer Available signals. The more often a given PHYID appears in the calendar, the more often it gets polled. The length of the calendar is configurable, and the maximum length of the calendar is 128 entries, to allow considerable flexibility in weighting the 48 possible PHYs. Servicing is done in exactly the same way as polling, using the same calendar. When the time comes to select the next cell or packet to transmit, the interface block scrolls forward from its current position through the PHY IDs in the calendar until it finds one that can transfer a cell. The more often a PHY ID appears in the calendar, the more frequently it will be serviced, assuming it is enabled and offers traffic. Table 3 below illustrates a simple, 16-long calendar for three STS-12 connections (PHYs 0, 1, and 2) and four STS-3 connections (PHYs 3, 4, 5, and 6). Note how the STS-12 connections have four times as many entries as the STS-3 connections. Note also that the entries for any given PHY are distributed evenly throughout the calendar in order to ensure maximum usefulness of the polling and maximum fairness of the servicing.

Table 3 Polling and Servicing Calendar Example

Calendar Address	Calendar Data
0	0
1	1
2	2
3	3

Calendar Address	Calendar Data
4	0
5	1
6	2
7	4
8	0
9	1
10	2
11	5
12	0
13	1
14	2
15	6

There are two pointers used in the calendar algorithm. They are the polling pointer and the servicing pointer. The servicing pointer moves down the calendar, and the first positive cell available assertion the pointer encounters will be the PHY selected for transfer on the next subsequent opportunity. It is recommended that repeated entries in the calendar be spread in a uniform manner in the calendar. This will help maximize the chances of selection in a proportional manner. Information that is gathered during polling is kept and maintained in a persistent fashion. According to UTOPIA Level 3 specification, once a PHY has asserted cell available, it is committed to transmission sometime in the future. The servicing algorithm remembers all assertions for cell available made in the past and advances the servicing pointer through the responses without regard to the age of the response. This algorithm provides flexibility in servicing without starvation so long as the number of entries in the calendar for a PHY is proportional to the bandwidth of that PHY.

Both the polling and servicing algorithms are designed to take into account that Cell Available signals on connections that are selected are not valid until two cycles after TxL_SOC has been presented.

Generally, the calendar should be set up at device initialization and subsequently be left unchanged. When the calendar length, or a calendar entry is updated during cell or packet flow, there may be an impact on polling, which may result in loss of data for a short period of time on any PHY that is transferring data.

For maximum efficiency, it is recommended that the RxPhy calendar length be set to at least 64, and preferably as close to 128 as is practical. A shorter set of calendar entries can simply be repeated several times to pad out to a greater length.

10.1.6 PHY Mapping

In order to support APS and other applications, the RxLink and TxLink blocks have the capability of remapping the PHY IDs used by the PHY devices over the UL3 or POS-PHY bus to another PHY ID to be used internal to the S/UNI-ATLAS-3200 and switch. In both the Ingress and Egress modes, the translation is done on the side of the device facing the PHYs, i.e. in the RxLink or TxLink block. The RxLink and TxLink use the external address in their calendar, and in specifying the mapping table. The remainder of the device, including the data queue blocks, use the translated PHY ID.

To facilitate this function, a table is provided in indirect registers in the RxLink and TxLink blocks which allows the microprocessor to specify, for any given external PHY address, the internal PHYID to which the PHY address is to be mapped.

Table 4 PHY Mapping

PHY Device Address	Indirect Address for Calendar & Mapping	Data in Mapping Table	PHY ID Internal to ATLAS and Switch
0	0	37	37
1	1	12	12
2	2	2	2
…	…		
47	47	7	7

10.1.7 Scalable Data Queue

In all the above configurations, both the input and output interfaces use Scalable Data Queue blocks (SDQs). There is an Input Data Queue and an Output Data Queue which buffer cells for the input and output, and a Bypass Data Queue which is used for packet bypass. Each SDQ offers generic storage and buffering for cells or packets. It has a capacity of 12288 bytes, which may be carved up into 1 to 48 different FIFOs. The depths of the various FIFOs are highly configurable (within the bounds set by the total available storage). For example, if a system has 48 STS-1 ATM PHY devices, then one may configure the input and output SDQs to behave as 48 FIFOs (one per PHY), each having 4 cells worth of storage. If there are higher-rate interfaces, then PHY buffers may be reduced in size or eliminated, to accommodate larger buffers on higher-rate PHYs. The Input and Bypass Data Queues may be configured to suit the system's buffering requirements. However, the Output Data Queue must be set to at least 4 cells for data rates greater than STS-1, and to at least 12 cells for data rates greater than STS-3. The registers to configure the Input SDQ are described in Section 11.8, and the registers to configure the Output SDQ are described in Section 11.11.

Each SDQ maintains a set of per-PHY 11-bit counters of the number of cells or packets currently in each of the FIFOs, a 32-bit aggregate count of the total number of cells accepted by all the PHY queues, and a 16-bit count of the total number of cells dropped by all the FIFOs. These counts are separate from the Cell Processor's per-PHY counters, and are used for diagnostic purposes.

Section 13.1 describes how to set up the SDQs.

10.1.8 Packet-Bypass Mode

The S/UNI-ATLAS-3200 can operate in a mixed packet/cell environment. In this case, the PHY interfaces must be configured as POS-PHY Level 3 interfaces. Each PHY queue can be configured to be in packet mode by writing the Enable bit for that PHY in the Bypass Data Queue to logic 1, and setting the corresponding bit to logic 0 in the Input and Output Data Queues. The PHY queue can be configured to be in cell mode by writing the Enable bit for that PHY in the Input and Output Data Queues to logic 1, and setting the corresponding bit to logic 0 in the Bypass Data Queue; in all cases, PHYs in the Input and Output SDQs must be set to ATM Cell mode (FIFO_TYPE = 0) and those in the Bypass SDQ to Packet mode (FIFO_TYPE = 1).

If a PHY is in packet mode, it is bypassed around the cell processor via the Bypass Data Queue. Effectively, all packet traffic cuts through the S/UNI-ATLAS-3200 unchanged, except for the PHY mapping function in the Link blocks.

Conversely, if a PHY is in cell mode, then its traffic is assumed to be ATM; hence the traffic is subject to the normal cell processing functions including policing, FM and PM, as described in the previous subsections.

POS-PHY Level 3 is capable of transferring both packets and cells. Using POS-PHY Level 3, Cells are transferred as fixed-length packets. The format of the packet is configured in the same way as for UTOPIA level 3, by specifying (in the interface blocks) the presence or lack of prepended, postpended, or HEC/UDF words. Thus the length of the ATM-cell packets can be 52, 56, 60, or 64 bytes. Non-ATM packets, of course, can be of any length. If even one of the PHY devices is configured to be in packet mode, then the S/UNI-ATLAS-3200 must use POS-PHY signaling at both its input and output interfaces. On the other hand, if *all* the PHY devices are configured to be in cell mode, then the S/UNI-ATLAS-3200 may use UTOPIA signaling or POS-PHY signaling.

10.1.9 ATM Cell Format

Whether in POS-PHY or UTOPIA mode, the S/UNI-ATLAS-3200 can accept ATM cells with or without HEC/UDF, and with one or two Prepended/Postpended d-words. The format of the cell must be preprogrammed at each interface, but it may be different at the device output than at the input. Total cell lengths of 52, 56, 60, or 64 bytes are supported, and the total number of prepended + postpended d-words must be less than or equal to 2. The format of the extended ATM cells is illustrated in Figure 9.

Figure 9 ATM Cell Format

Note: optional words encased in [].

Bits 31 -24	Bits 23 -16	Bits 15 - 8	Bits 7- 0
[Pre1	Pre2	Pre3	Pre4]
[Pre5	Pre6	Pre7	Pre8]
Header 1	Header 2	Header 3	Header 4
[UDF1/HEC	UDF 2	UDF 3	UDF 4]
Payload 1	Payload 2	Payload 3	Payload 4
:	:	:	:
Payload 45	Payload 46	Payload 47	Payload 48
[Post1	Post2	Post3	Post4]
[Post5	Post6	Post7	Post8]

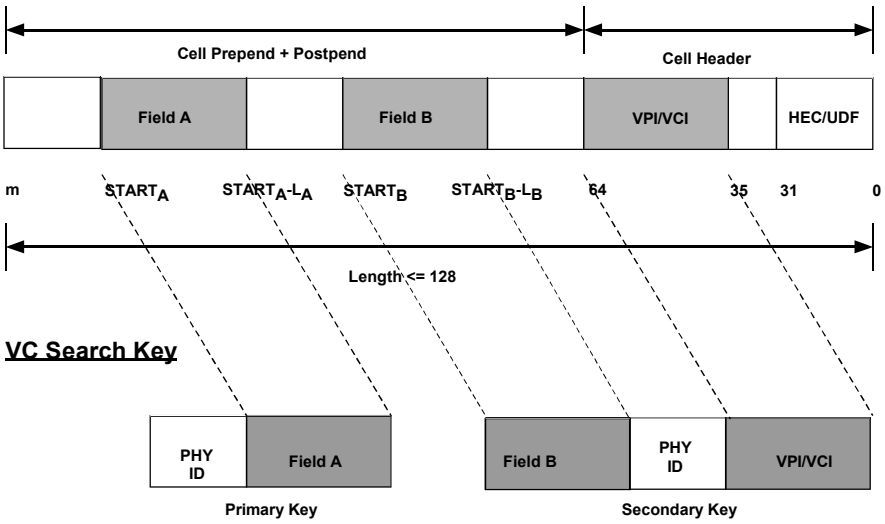
The prepended/postpended bytes and HEC/UDF will be translated, added, or subtracted as needed based on the translation settings, the input cell format, and the output cell format.

10.2 Connection Identification

The ATLAS makes use of a flexible approach to identify incoming cells and to determine the record in the VC Table with which they are associated. The ATLAS identifies the VC record of each connection by traversing a search tree in SRAM using selected portions of the cell header, prepend, postpend and the PHY address. To do this, the ATLAS creates an internal *Routing Word*, which is the concatenation of the cell prepend, cell postpend, and cell header. The ATLAS is programmed to select portions of the Routing Word plus the PHY address to create a *VC Search Key*. The VC Search Key, therefore, consists of portions of the cell's header, prepend, postpend and PHY address.

The figure below illustrates the Routing Word and VC Search Key construction. This figure is not intended to imply any restrictions on the positioning of Field A and Field B. These fields may occur anywhere within the appended octets or the ATM header. The Primary Key and Secondary Key may also intersect.

Figure 10 VC Search Key Extraction

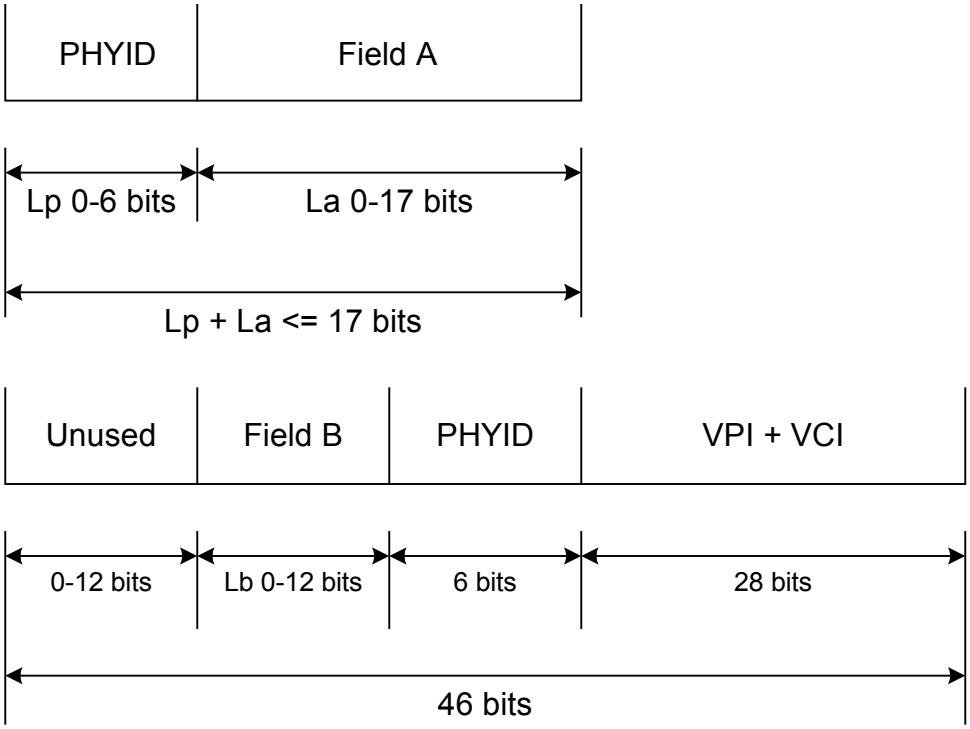


The ATLAS divides the VC Search Key into two search keys – the Primary Key and the Secondary Key. The Primary Key is 17 bits long. It is constructed from two fields – the *PHY ID* field and *Field A*. The PHY ID field and Field A can be programmed to be 0-6 bits and 0-17 bits long, respectively; the Primary Key is LSB justified and padded on the left with zeroes to make it 17 bits long. The PHY ID field is the UTOPIA (or POS) address and must, therefore, include sufficient bits to encode all the PHYs at the PHY Layer interface of the ATLAS. Field A starts at location STARTA of the Routing Word, and has length L_A. The number of bits in Field A plus the number of bits in the PHY ID field must be less than or equal to 17. Field A and the PHYID are always LSB justified within the 17-bit Primary Key (any unused MSBs are set to logic 0).

The Secondary Key is 46 bits long (although only 17 bits can be resolved at-speed in any given search) and consists of three fields. The first field, *Field B*, is 0 to 12 bits long and may start anywhere in the Routing Word. Field B parameters include starting position, STARTB and length, L_B. The second field is the 6-bit PHYID (zeroes are padded into the MSBs of the PHYID if the PHYID is less than 6 bits). The third field is the 28-bit VPI/VCI taken from the cell header.

Field B and the VPI/VCI field are “right justified” within the Secondary Key.

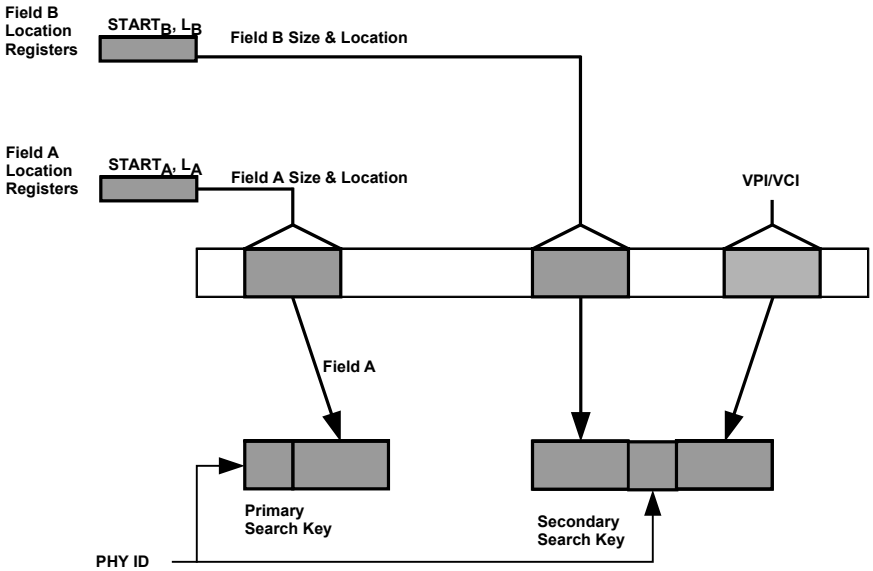
Figure 11 Parameters of the Primary and Secondary Keys



The user can program the ATLAS with the length and position parameters of Fields A and B.

The figure below provides a representation of how the ATLAS creates the Primary and Secondary Search Keys. Field location and length registers are used to select Field A and Field B from the Routing Word. Field A and the PHY ID are concatenated to form the Primary Search Key. Field B, the PHY ID, and the VPI/VCI field are concatenated to form the Secondary Search Key.

Figure 12 VC Search Key Construction



Once the search keys are assembled, the Primary Search Key is first used to address an external direct look-up table (this is the array of Primary Search Pointers in bits(16:0) of the external search SRAM at SADDR(17) = 0). This table occupies 2^n memory locations, where $n = L_{PHY} + L_A$, i.e. the length of the Primary Search Key. The result of this direct lookup is the address of a root node of a search tree. From this root node, the Secondary Search Key is used by a patented search algorithm to find the VC Table record address of the connection. The VC Table Record address is used to access the VC Table Record in internal DRAM and to fetch the F4 Record address if active and up to two PM Record addresses from the external linkage SRAM at SADDR(17) = 1. These addresses are used to access the appropriate records (all of which are stored on chip).

The validity of the record addresses fetched from the SRAM is checked by comparing the secondary search key with the search key (VPI, VCI, and Field B) stored in first row of the VC Table Record. Any unused bits within this stored search key word must be set to zero. The Configuration field of the VC Table Record contains the NNI bit. This bit identifies if the virtual connection belongs to a Network-Network Interface. If the NNI bit is set to zero, the connection is part of a UNI, which means that the four MSBs of the VPI are excluded from the Secondary Key verification. If the VCI field in the VC Table is set to all zeros, this signifies the connection is a VPC, and the VCI field is to be ignored. If the search process does not lead to the successful identification of the cell concerned (i.e. the search key stored in the VC Table does not match the Secondary Search Key used for the search), the cell is declared to be invalid, and will not be output. Optionally, the cell may be routed to the Microprocessor Cell Interface for error logging.

The length of time required to perform the VC Table search is variable. Since the Primary Search Key is used in a direct lookup, only one cycle is required to process the Primary Search Key. The Secondary Search Key processing time is highly dependent on the key's contents, but the maximum number of processing cycles required is equal to the number of bits in the Secondary Search Key which must be examined to make a unique identification. Some VPI and VCI bits may always be zero; therefore, they need not be used in the search. In some instances, the Primary Search Key may overlap the Secondary Search Key; therefore, the intersecting bits are only required for the confirmation of a search. If the number of bits used by the binary search is no greater than 18, a sustained rate of 5.682×10^6 cells/s is guaranteed. The general expression for guaranteed throughput is given below

$$\text{Throughput} = \frac{20}{22} \frac{1}{(2 + \max(\text{max. binary tree depth}, 18))(\text{SYSCLK period})} \text{cells/s}$$

Note, however, if the binary tree depth is less than 18, the throughput remains 5.68×10^6 cells/s.

10.2.1 Search Table Data Structure

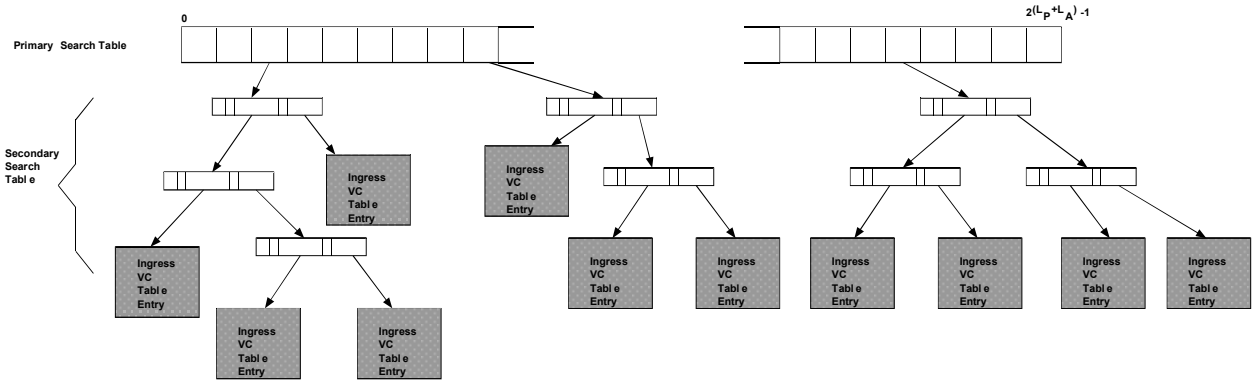
The Primary and Secondary Search Key table fields reside in the lower 8 Mbits of the external SRAM (SADDR[17] = 0). Each SRAM word is 64 bits wide. The Primary Table Record entry is located in bits 17 to 0 of each word and the secondary table record entry is located in bits 63 to 18. There are a total of 128K possible primary and secondary records (all located in the lower 8 Mbits of the external SRAM). The following table shows the format of each 64 bit word in the lower 8Mbits of the external SRAM.

Table 5 Search Table

63									0
2	Selector (6)	Left Leaf (1)	1	Left Branch (17)	Right Leaf (1)	1	Right Branch (17)	1	Primary Search Pointer (17)
Shaded Fields are Reserved, and must be programmed to logic 0 for proper operation.									

The figure below illustrates the relationship between the Primary Search Table Key, Secondary Search Table Key and the VC Table and shows the search tree's that are used in connection identification.

Figure 13 Construction of Primary and Secondary Keys



The following gives the immutable coding rules for the search data structures. The coding supports numerous possible algorithms, but the S/UNI-ATLAS-3200 software driver presents an algorithm that is optimized for most applications.

Primary Search Table

The Primary Search Table contains an array of pointers (the Primary Search Pointers) that point to the roots of binary trees. The table is directly indexed by the contents of the Primary Search Key, as defined above. For any given received cell, the Search Table entry pointed to by the Primary Search Key contains the Primary Search Pointer which points to the root of the Secondary Search binary tree for that cell.

The entire Primary Search Table must be initialized to all zeros. A table value of zero represents a null pointer; therefore, the initial state means no provisioned connections are defined. If a connection is added which results in a new binary search tree (i.e. it is the only connection associated with a particular Primary Search Key), the appropriate Primary Search Pointer must point to the newly created binary search tree root. If the last connection with a particular Primary Search Key is removed, the associated Primary Search Pointer must be set to all zeros.

Secondary Search Table

The Secondary Search Table consists of a set of binary search trees. Each tree's root is pointed to by a Primary Search Pointer. Each node in the tree is represented by a 42-bit data structure. The fields of the Secondary Search Table are described below.

Table 6 Secondary Search Table Fields

Name	Description
Selector	The Selector field is a 6 bit field which is the index of the Secondary Search Key bit upon which the branching decision of the binary search is based. An index of zero represents the LSB. If the selected bit is a logic 1, the Left Leaf and Left Branch fields are subsequently used. Likewise, if the selected bit is a logic 0, the Right Leaf and Right Branch are subsequently used. Typically, the Selector value decreases monotonically with the depth of the tree, but

Name	Description
	other search sequences are supported by the flexibility of this bit.
Left Leaf	This flag indicates if this node is a leaf. If Left Leaf is a logic 1, the left branch is a leaf and the binary search terminates if the decision bit is a logic 1. If Left Leaf is a logic 0, the Left Branch value points to another node in the binary tree.
Left Branch	The pointer to the node accessed if the decision bit is a logic 1. If Left Leaf is a logic 1, Left Branch contains the 16-bit address identifying the VC Linkage Record and VC Table Record for that connection. If Left Leaf is a logic 0, Left Branch contains the (up to) 17-bit address pointing to another Secondary Search Table entry.
Right Leaf	This flag indicates if this node is a leaf. If Right Leaf is a logic 1, the Right Branch is a leaf and the binary search terminates if the decision bit is a logic 0. If Right Leaf is a logic 0, the Right Branch field points to another node in the binary tree.
Right Branch	The pointer to the node accessed if the decision bit is a logic 0. If Right Leaf is a logic 1, Right Branch contains the 16-bit address identifying the VC Linkage Record and VC Table Address for that connection. If Right Leaf is a logic 0, Right Branch contains the 17-bit address pointing to another Secondary Search Table entry.

The above encoding defines the binary search tree recursively.

The following special cases must be respected:

A binary tree with only one connection must have both the Left and Right Branches pointing to the solitary VC Table Record. Both the Left Leaf and Right Leaf flags must be a logic 1.

If the Primary Search Table is not used (i.e. $L_{PHY} = L_A = 0$), then the primary key is considered to be all-zeroes, and the Primary Pointer at SA[16:0] = 0x00000 contains the root of the Secondary Search Tree.

If the Primary Search Table is in use, no root node shall use location SA[16:0]=0x00000, although this location may be used for nodes at least one level down. A value of 0x00000 in the Primary Search Pointer represents a null pointer.

10.3 VC Linkage Table

The VC Linkage table occupies the top half of the external SRAM address space, and contains pointers to other context entries with which a VC is associated.

Table 7 VC Linkage Table

63											0
1	PHYID (6)	2	Reserved (16)	PM 2 Active (1)	1	PM 2 Address (8)	PM 1 Active (1)	1	PM 1 Address (8)	VPC Pointer Active (1)	2	VPC Pointer (16)
Shaded fields are reserved, and must be programmed to logic 0 for proper operation.												

The PM Active and PM Address fields are used to select Performance Management entries to be associated with a particular VC. Their function is fully described in Section 10.14 on PM processing.

The VPC Pointer Active and VPC Pointer fields are used to associate a VCC record entry with a VPC record entry when VCCs are being aggregated to, or split out from a VPC. All connections that are NOT VCCs being aggregated to, or split out from VPCs must have their VPC Pointer Active bit set to logic 0. The function of the VPC pointer is more fully described in Sections 10.10 and 10.11 on F4 to F5 and F5 to F4 OAM processing. **Note that, if active, the 2 least significant bits of the VPC Pointer cannot be equal to the 2 LSBs of the VC Record Address.** Failure to adhere to this restriction will result in the connection being treated as inactive.

The PHYID field indicates the Physical Layer device that this connection is associated with. This field is used to determine the destination of all generated AIS, CC, RDI, LB, and PM cells. This field is also used in determining per-PHY statistics and per-PHY policing. If it is not the same as the PHYID of cells on the connection, proper operation cannot be guaranteed.

10.4 VC Record Table

The VC Record Table is a 7-row data structure which contains context information for one connection. The VC Table is comprised of 64K VC Table records stored in internal DRAM, one record for each of the 64K connections. The VC Table is used for connection configuration and connection processing functions. Unused bits within the table should be set to logic zero for future backward compatibility.

Table 8 VC Record Table

Row	127																0
0 Read-Only Config	Action 2 (2)	Inc 2 (14)	Limit 2 (14)	Action 1 (2)	Inc 1 (14)	Limit 1 (14)	Field B (12)	VPI (12)	VCI (16)	2	Bwds VCRA (16)	VC Table CRC-10 (10)					
1 Status & Config	Status (10)	Configuration (14)	OAM Configuration (23)	Internal Status (21)	Policing Configuration (11)	Reserved (16)	Maximum Frame Length (11)	GFR State (3)	Policing Reserved (3)	ETE Received Defect Type (8)	Segment Received Defect Type (8)						
2 Counting	Alternate Count 2 (32)			Alternate Count 1 (32)			Count 2 (32)			Count 1 (32)							
3 Policing	Unused (1)	Remaining Frame Count (11)		Non-Compliant Count 3 (16)		Non-Compliant Count 2 (16)		Non-Compliant Count 1 (16)		TAT2 (34)		TAT1 (34)					
4 Trans-lation	Unused (4)	Translated VPI (12)		Translated VCI (16)		Translated HEC (8)		Translated UDF (24)		Translated Pre/Po 1 (32)		Translated Pre/Po 2 (32)					
5 Seg DL	Segment Received Defect Location (128)																
6 ETE DL	End-to-End Received Defect Location (128)																

The fields of the VC table are described in the following sections.

10.5 Cell Processing

After a VPI/VCI search has been completed for a cell, the resulting actions are dependent upon the cell contents and the VC Table Record. Particular features such as policing and OAM cell processing can be disabled on a global and per-connection basis.

The VPI/VCI search results in a VCRA[15:0] value which points to a VC Table record. The fields of each VC Table record are described below.

When a new VC is provisioned, the management software must initialize the contents of the VC Table record. Once provisioned, the management software can retrieve the contents of the VC Table record.

Table 9 VC Table Fields used in Cell Processing

Row	127											0
0	Action 2 (2)	Inc 2 (14)	Limit 2 (14)	Action 1 (2)	Inc 1 (14)	Limit 1 (14)	Field B (12)	VPI (12)	VCI (16)	2	Bwds VCRA (16)	VC Table CRC-10 (10)
1	Status (10)	Configuration (14)	OAM Configuration (23)	Internal Status (21)	Policing Configuration (11)	Reserved (16)	Maximum Frame Length (11)	GFR State (3)	Policing Reserved (3)	ETE Received Defect Type (8)	Segment Received Defect Type (8)	
2	Alternate Count 2 (32)			Alternate Count 1 (32)			Count 2 (32)			Count 1 (32)		
3	Unused (1)	Remaining Frame Count (11)		Non-Compliant Count 3 (16)		Non-Compliant Count 2 (16)		Non-Compliant Count 1 (16)		TAT2 (34)		TAT1 (34)
4	Unused (4)	Translated VPI (12)		Translated VCI (16)		Translated HEC (8)		Translated UDF (24)		Translated Pre/Po 1 (32)		Translated Pre/Po 2 (32)
5	Segment Received Defect Location (128)											
6	End-to-End Received Defect Location (128)											

Table 10 Status VC Table Field

Bit	Name	Description
9	FIFO Must Write	This bit should be set to zero when the connection is setup.
8	DRAM_CRC_Err	When this bit is logic 1, this VC table entry has suffered a DRAM CRC-10 error. If the Inact_on_DRAM_Error register bit in the Cell Processor Configuration Register is logic 1, and this bit is a logic 1, then the connection is considered inactive. This bit can only be cleared by a microprocessor write.
7	OAM_Failure	This bit becomes a logic 1 if a segment or end-to-end RDI, AIS or CC condition has persisted for 3.5 ± 0.5 seconds. OAM_Failure is cleared as soon as no RDI, AIS or CC condition remains.
6	AIS_end_to_end alarm	This bit becomes a logic 1 upon receipt of a single end-to-end AIS cell. The alarm status is cleared upon the receipt of a single user cell or end-to-end CC cell, or if no end-to-end AIS cell has been received within the last 2.5 ± 0.5 sec.
5	AIS_segment alarm	This bit becomes a logic 1 upon receipt of a single segment AIS cell. The alarm status is cleared upon the receipt of a single user cell or segment CC cell, or if no segment AIS cell has been received within the last 2.5 ± 0.5 sec.
4	RDI_end_to_end alarm	This bit becomes a logic 1 upon receipt of a single end-to-end RDI cell. This bit is cleared if no end-to-end RDI cell has been received within the last 2.5 ± 0.5 sec.
3	RDI_segment alarm	This bit becomes a logic 1 upon receipt of a single segment RDI cell. This bit is cleared if no segment RDI cell has been received within the latest 2.5 ± 0.5 sec.
2	CC_end_to_end alarm	This bit becomes a logic 1 if no user cell or end-to-end CC cell has been received within the last 3.5 ± 0.5 sec. This bit is cleared upon receipt of a user cell, or end-to-end CC cell. If this connection is an

Bit	Name	Description
		end-to-end source point, this alarm may not indicate a problem, as a source point cannot expect to receive CC cells. In this case, the COS_FIFO_EN bit in the OAM Confiiguration register may be useful for suppressing these warnings.
1	CC_segment alarm	This bit becomes a logic 1 if no user, segment CC cell has been received within the last 3.5 ± 0.5 sec. This bit is cleared upon receipt of a user cell, or segment CC cell. Segment CC alarms are declared only if the VC is part of a segment flow (Segment_Flow = 1) or is a segment end point (Segment_End_Point = 1)
0	Reserved	This bit should be set to logic 0.

Table 11 Configuration VC Table Field

Bit	Name	Description
13	Reserved	This bit must be programmed to logic 0 for backwards compatibility.
12	Reserved	This bit must be programmed to logic 0 for backwards compatibility.
11	Active	Identifies the connection as active. This bit is checked during the S/UNI-ATLAS-3200 background processes to determine if the connection is still active. It is the responsibility of the management software to set and clear this bit during activation and deactivation, respectively, of a connection. It is recommended to set this bit to logic 0 until the search and linkage rows have been correctly configured. Cells received on a connection for which Active is a logic 0 will be dropped, with an optional copy to the Microprocessor Cell Interface if the InactiveToUP register bit is a logic 1. These cells will not be counted by the Cell Processor.
10	NNI	When the NNI bit is logic 0, then the top four bits of the VPI are considered to be part of the GFC field. As such, they will not be used to verify the correctness of the search, and will not be translated unless the XGFC register bit is a logic 1.
9	Count Config Select	This bit is used to address one of two possible combinations of programmable cell counts. If this bit is a logic 0, the Cell Count 1[31:0] and Cell Count 2[31:0] are programmed from the Cfg1 settings in the Cell Counting Configuration register. If this bit is a logic 1, the cell counts are derived from the Cfg2 settings in Cell Counting Configuration.
8	APStoUP	When this bit is a logic 1, all Automated Protection Switching Coordination Protocol cells are copied to the microprocessor. If the APStoBCIF bit is also set to logic 1 in the Routing Configuration Register, then APS cells are passed to BCIF instead of the microprocessor. APS cells are also passed to the OCIF, unless S/UNI-ATLAS-3200 is an OAM flow end-point and the APStoOCIF bit in the Routing Configuration register is logic 0.
7:6	LB_Route[1:0]	The LB_Route bits determine the handling of loopback cells. Regardless of the setting of LB_Route, Loopback cells are always dropped at flow end points unless LBtoOCIF is logic 1 in the Routing Configuration Register. LBtoOCIF = 1 always causes loopback cells to be copied to the OCIF, but does not otherwise affect the functionality of LB_Route. When LB_Route[1:0] = 00 then loopback cells will be dropped at flow end points, but otherwise will be routed to the OCIF. This

Bit	Name	Description
		setting is intended for nodes that do not support LB functionality. When LB_Route[1:0] = 01, then loopback cells will be automatically looped back based on the contents of the Loopback Indication, Source ID, and Loopback Location ID. Cells with Loopback Indication = 0 (“Returned Loopback Cells”) will be dropped and routed to the Microprocessor Cell Interface at connection points whose Loopback Location ID Register matches the Source ID of the loopback cell. At flow end points, all Returned LB cells may be routed to the microprocessor if the Rtd_LB_to_UP_at_End register bit is set to logic 1 in the Routing Configuration field. For cells with Loopback Indication = 1 (“Parent Loopback Cells”) segment Loopback cells will be dropped and looped back if their Loopback Location ID matches the Loopback Location ID register, and looped back but not dropped if their Loopback Location ID is all-zeroes. Both segment and end-to-end cells will be dropped and looped back at flow end points if their Loopback Location ID is all-ones, or if it matches the the Loopback Location ID register at the end point. In any event, Loopback cells are always dropped at flow end points. Cells which are looped back always have their Loopback Indication bit set to 0, and have their Loopback Location ID field replaced with the contents of the Loopback Location ID Registers. When Route_LB[1:0] = 10 then Loopback cells are handled the same as if Route_LB[1:0] = 01, but instead of automatically looping back the cells, cells are routed (without modification to Loopback Location ID or Loopback Indication) to the Microprocessor Cell Interface. When Route_LB[1:0] = 11 then all loopback cells are dropped and routed to the Microprocessor Cell Interface. When using this setting, if the microprocessor later reinserts these cells it should set the PROC_CELL bit to logic 0 to ensure they do not simply get routed to the microprocessor once again.
5	FM_to_UP	If this bit is a logic 1, all Fault Management cells (AIS, RDI, CC) are copied to the Microprocessor Cell Interface. The Segment_End_Point and End_to_end_point bits determines whether or not FM cells are output to the Output Cell Interface. FM_to_UP does not control the routing of loopback cells, which are controlled by the LB_ROUTE bits.
4	VC_to_BCIF	If this bit is logic 1, all cells arriving on this connection are copied to the Backwards Cell Interface, unaltered except for the header translation normally specified for cells being routed to OBCIF (e.g. Xlate_to_OBCIF, OBCIF_Cell_Info, etc). If Drop_VC = 1 and VC_to_BCIF = 1, then it is assumed that a per-VC loopback function is being implemented, and cells from the IBCIF will be permitted to proceed to the OCIF, and will not be sent to OBCIF. All other cells will be sent to OBCIF, and not sent to OCIF. If more cells are sent to the OBCIF than can be accommodated, then cells can be lost due to FIFO overflow. RDI and Bwd PM cells generated by S/UNI-ATLAS-3200 will not be lost, but Loopback cells and cells routed via VC_to_BCIF may be lost. The OBCIF is drained at the lesser of the opposite-direction Backward Cell Interface Pacing rate, and the capacity of the BCIF link (approximately 1.3 million cells per second).

Bit	Name	Description
3	VC_to_UP	If this bit is logic 1, all cells arriving on this connection are copied, unaltered except for the insertion of the Cell Info Field, to the Microprocessor Cell Interface
2	Drop_VC	If this bit is a logic 1, no cells are routed to the OCIF. The setting of this bit supercedes all other routing bits. If the Drop_VC bit is set, the S/UNI-ATLAS-3200 will not output generated OAM cells to the OCIF (AIS, CC, Fwd PM). Drop_VC has no effect on the generation of OAM cells to the BCIF. If Drop_VC = 1 and VC_to_BCIF = 1, then it is assumed that a per-VC loopback function is being implemented, and cells from the IBCIF will be permitted to proceed to the OCIF, and will not be sent to OBCIF. All other cells will be sent to OBCIF, and not sent to OCIF.
1	Rollover_FIFO_enable	Enables the 32-bit billing counts to generate entries in the Count Rollover FIFO whenever their MSB becomes logic 1. If the Count Rollover FIFO is full, the MSB will remain logic 1 until an entry has been successfully generated, at which time the MSB will become logic 0. If this bit is logic 0, then the counts operate as normal saturating counters, and must be polled periodically by the microprocessor.
0	COS_FIFO_enable	Enables changes in the Status field to result in COS FIFO entries.

Table 12 Internal Status VC Table Field

Bit	Name	Description
20	Reserved	This bit must be programmed to logic 0 for backwards compatibility.
19	Reserved	This bit must be programmed to logic 0 for backwards compatibility.
18	Sending_AIS	If this bit is logic 1, this connection transmitted an AIS cell at the last one-second processing interval. This indicates that, if a half-second background process is being executed, the cause of AIS is not new, and no AIS should be sent until the next one-second process. This bit should be set to logic 0 when the connection is set up.
17	Sending_RDI_Seg	This bit enables the S/UNI-ATLAS-3200 to generate the first segment RDI cell within 500msec of detecting a condition which requires the generation of segment RDI cells. This bit is set to logic 1 by the S/UNI-ATLAS-3200 when a segment RDI cell is transmitted, and set to logic 0 when the RDI background process determines there is no reason to continue sending segment RDI. In addition to setting this bit when transmitting a segment RDI cell on reception of an AIS cell, the S/UNI-ATLAS-3200 will use the 0.5 second background process to scan through all connections and determine if a segment RDI cell is to be transmitted (within 0.5 seconds of detecting the appropriate condition). When the first segment RDI cell is transmitted, this bit is asserted and subsequent segment RDI cells are only transmitted by the 1 second background process. If this bit is logic 0, the S/UNI-ATLAS-3200 has not yet begun to transmit segment RDI cells (possibly due the RDI BCIF being full). This bit should be set to logic 0 when the connection is set up.
16	Sending_RDI_Ete	This bit enables the S/UNI-ATLAS-3200 to generate the first end-to-end RDI cell within 500msec of detecting a condition which requires the generation of end-to-end RDI cells.

Bit	Name	Description
		This bit is set to logic 1 by the S/UNI-ATLAS-3200 when a end-to-end RDI cell is transmitted, and set to logic 0 when the RDI background process determines there is no reason to continue sending end-to-end RDI. In addition to setting this bit when transmitting a end-to-end RDI cell on reception of an AIS cell, the S/UNI-ATLAS-3200 will use the 0.5 second background process to scan through all connections and determine if a end-to-end RDI cell is to be transmitted (within 0.5 seconds of detecting the appropriate condition). When the first end-to-end RDI cell is transmitted, this bit is asserted and subsequent end-to-end RDI cells are only transmitted by the 1 second background process. If this bit is logic 0, the S/UNI-ATLAS-3200 has not yet begun to transmit end-to-end RDI cells (possibly due the RDI BCIF being full). This bit should be set to logic 0 when the connection is set up.
15:14	OAM_Failure_Count	This count is set to 3 (to provide a 3.5 ± 0.5 second count) whenever there is no AIS, CC or RDI alarm declared, and is decremented at one-second intervals whenever there is an AIS, CC, or RDI alarm. If it is read back as 0, then the OAM_Failure bit will be set to logic 1, and an interrupt and/or an entry in the COS fifo will be made, as appropriate. This field should be set to 3 when the connection is set up.
13	Send_Seg_CC_Count	The Send_Seg_CC_Count is set to logic 1 (to provide a one second count) at connection setup time and each time the S/UNI-ATLAS-3200 sends a user (or a received segment CC cell) cell on this connection. The count is decremented at one second intervals. If this count reaches zero and is still 0 when it is read in the subsequent second, then a Segment CC cell is generated, if the CC_Activate_Segment bit is set. This bit should be set to logic 1 when the connection is set up.
12	Send_End_CC_Count	The Send_End_CC_Count is set to logic 1 (to provide a one second count) at connection setup time and each time the S/UNI-ATLAS-3200 sends a user cell (or a received end-to-end CC cell) on this connection. The count is decremented at one second intervals. If this count reaches zero and is still 0 when it is read in the subsequent second, then an End-to-End CC cell is generated, if the CC_Activate_End_to_End bit is set. This bit should be set to logic 1 when the connection is set up.
11:10	Seg_CC_Count[1:0]	The Seg_CC_Count is set to a value of 3 (to provide a 3.5 +/- 0.5 sec count) upon receipt of a user or segment CC cell, and decremented at one second intervals. If the Seg_CC_Count reaches 0 and is still 0 when it is read in the subsequent second, the CC_segment Alarm is raised. This field should be set to 3 when the connection is set up.
9:8	End_CC_Count[1:0]	The End_CC_Count is set to a value of 3 (to provide a 3.5 +/- 0.5 sec count) upon receipt of a user or end-to-end CC cell, and decrements at one second intervals. If the End_CC_Count reaches 0 and is still 0 when it is read in the subsequent second, the CC_end_to_end Alarm is raised. This field should be set to 3 when the connection is set up.
7:6	Seg_RDI_Count[1:0]	The Seg_RDI_count is set to a value of 2 (to provide a 2.5 +/- 0.5 sec count) upon receipt of a segment RDI cell, and decrements at one second intervals. If the Seg_RDI_Count reaches 0 and is still 0

Bit	Name	Description
		when it is read in the subsequent second, the RDI_segment Alarm is cleared. This field should be set to 0 when the connection is set up.
5:4	End_RDI_Count[1:0]	The End_RDI_Count is set to a value of 2 (to provide a 2.5 +/- 0.5 sec count) upon receipt of an end-to-end RDI cell, and decrements at one second intervals. If the End_RDI_count reaches 0 and is still 0 when it is read in the subsequent second, the RDI_end_to_end Alarm is cleared. This field should be set to 0 when the connection is set up.
3:2	Seg_AIS_Count[1:0]	The Seg_AIS_Count is set to a value of 2 (to provide a 2.5 +/- 0.5 sec count) upon receipt of a segment AIS cell, and decrements at one second intervals. If the Seg_AIS_Count reaches 0 and is still 0 when it is read in the subsequent second, the AIS_segment Alarm is cleared. This field should be set to 0 when the connection is set up.
1:0	End_AIS_Count[1:0]	The End_AIS_Count is set to a value of 2 (to provide a 2.5 +/- 0.5 sec count) upon receipt of an end-to-end AIS cell, and decrements at one second intervals. If the End_AIS_Count reaches 0 and is still 0 when it is read in the subsequent second, the AIS_end_to_end Alarm is cleared. This field should be set to 0 when the connection is set up.

Table 13 OAM Configuration VC Table Field

Bit	Name	Description
22	Reserved	This bit must be programmed to logic 0 for backwards compatibility.
21	COS_CC_DIS	When this bit is logic 1, then entering or exiting CC Alarm will not generate a COS entry. When this bit is logic 0, COS entries are generated as normal. This feature is intended for use with older equipment that does not correctly support CC, in order to avoid flooding the microprocessor with CC-related COS entries.
20	Send_AIS_segment	If this bit is a logic 1, a segment AIS cell is generated once per second (nominally).
19	Send_AIS_end_to_end	If this bit is a logic 1, an end-to-end AIS cell is generated once per second (nominally).
18	Send_RDI_segment	If this bit is a logic 1, a segment RDI cell is generated once per second (nominally).
17	Send_RDI_end_to_end	If this bit is a logic 1, an end-to-end RDI cell is generated once per second (nominally).
16	CC_Activate_Segment	Enables Continuity Checking on segment flows. If the ForceCC register bit is logic 0, then when no user or CC cells are transmitted over a 1.0 second (nominal) interval, a segment CC OAM cell is generated. The segment CC cell is generated at an interval of one per second (nominally). If the connection is an F4 OAM connection that is being aggregated, then any cells transmitted on any of the constituent F5 connections are considered user cells. If the ForceCC register bit is logic 1, then when the CC_Activate_Segment bit is logic 1, a segment CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells. ITU-T I.610 9.2.1.1.2, 9.2.2.1.2.

Bit	Name	Description
15	CC_Activate_End_to_End	Enables Continuity Checking on end-to-end flows. If the ForceCC register bit is logic 0, then when no user or end-to-end CC cells are transmitted over a 1.0 second (nominal) interval, an end-to-end CC OAM cell is generated. The end-to-end CC cell is generated at an interval of one per second (nominally). If the connection is an F4 OAM connection that is being aggregated, then any cells transmitted on any of the constituent F5 connections are considered user cells. If the ForceCC register bit is logic 1, then when the CC_Activate_End_to_End bit is logic 1, an end-to-end CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells. ITU-T I.610 9.2.1.1.2, 9.2.2.1.2.
14	FM_interrupt_enable	This bit enables the generation of segment and end-to-end AIS, RDI Continuity Check, and OAM Failure alarm interrupts. If this bit is logic 1, the S/UNI-ATLAS-3200 will assert OAM Failure and segment and end-to-end AIS, RDI and Continuity Check interrupts, as required, regardless of whether or not the S/UNI-ATLAS-3200 is a connection end-point (segment or end-to-end) for the connection. This bit would typically be programmed to logic 1 at segment or end-to-end-points only. If this bit is logic 0, no alarm interrupts will be asserted, however, the Status field will reflect the connection state.
13:6	Generated OAM Defect Type [7:0]	The Defect Type bits determine the Defect Type that is inserted into AIS cells generated due to the CC_AIS_RDI process, via per-PHY AIS, and via the Send_AIS_End_to_End or Send_AIS_Segment bits, and into RDI cells generated via the CC_AIS_RDI process, via per-PHY RDI generation, or via the per-VC bits Send_RDI_End_To_End or Send_RDI_Segment.
5	F4toF5OAM	The F4toF5OAM bit indicates whether or not an F5 (VCC) connection will send AIS or RDI cells due to an associated F4 (VPC) connection being in AIS alarm. This bit is only significant if the connection is an F5. When an F4 (VPC) is terminated (i.e. there is an F4 connection end-point which is associated with this F5 connection) at the S/UNI-ATLAS-3200, the F5 connections are switched. If the F4 receives AIS cells, then the F5 connections will send AIS and/or RDI cells once per second, carrying the Defect Location and Defect Type contained in the received F4 AIS cells. If F4toF5OAM is set to logic 0, then this process is disabled, and no F5 AIS or RDI cells will be generated based on the condition of the associated F4.
4	AUTO_RDI	The AUTO_RDI bit enables the generation of segment and end-to-end RDI cells while in an AIS alarm or Continuity alarm state. If AUTO_RDI is logic 1, an RDI cell is transmitted (and looped from the Cell Processor to the reverse cell stream) immediately upon the reception of the first AIS cell at a flow end-point. (if the S/UNI-ATLAS-3200 is an end-to-end point for that connection, an end-to-end RDI cell will be generated, if the S/UNI-ATLAS-3200 is a segment end point, a segment RDI cell will be generated, and if the S/UNI-ATLAS-3200 is both a segment and end-to-end point, both types of RDI cells will be generated) and once per second thereafter until the AIS state is exited. Similarly, if the CC_AIS_RDI bit is logic 1, RDI cells are generated once per second if no user or CC cells have been received in the last 3.5 +/- 0.5 seconds. RDI cells can also be transmitted if the Send_RDI_segment and Send_RDI_end_to_end bits are set, or if the PHYRDI register bits are set.
3	CC_AIS_RDI	If this bit is a logic 1, AIS or RDI cells are generated at one second intervals upon the declaration of a CC_alarm (assuming AIS_alarm is not also declared). If the connection is not a segment or ETE end point, then ETE AIS will be generated once per second on declaration of ETE CC alarm. If

Bit	Name	Description
		Segment_Flow = 1, then Segment AIS will be generated on declaration of Segment CC alarm. If the connection is a segment end point, then ETE AIS and Segment RDI will be generated once per second on declaration of Segment CC alarm. If the connection is an ETE end point, then ETE RDI will be generated once per second on declaration of ETE CC alarm. If the connection is both a segment and an ETE point, then Segment RDI will be generated once per second on declaration of Segment CC alarm, and ETE RDI will be generated once per second on declaration of ETE CC alarm. AIS and RDI cells generated via the CC_AIS_RDI process have the Defect Type programmed in the Generated OAM Defect Type field, and the Defect Location programmed in the global Defect Location register. In any event, AIS/RDI cells will not be generated at a rate of more than one segment and one end-to-end AIS cell per second, nominally. In particular, Segment and ETE AIS cells will not be generated via this process if the connection is already receiving Segment or ETE AIS cells, respectively.
2	Segment Flow	The Segment_Flow bit indicates whether a connection is part of a defined segment. When Segment_Flow is logic 1, then Segment AIS cells may be sent due to CC alarm (controlled by CC_AIS_RDI), due to per-PHY AIS declaration (controlled by the per-PHY AIS Generation Control registers), or due to AIS declaration at the F4 connection associated with an F5 connection (controlled by the F4toF5OAM bit). The SegmentFlow bit should not be set to a logic 1 at segment end-points, or at segment start-points.
1	Segment_End_Point	Defines the S/UNI-ATLAS-3200 as a Segment termination point. For F4 connections (VPCs), all cells with VCI = 3 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 100 are terminated and processed.
0	End_to_End_Point	Defines the S/UNI-ATLAS-3200 as an End-to-End termination point. For F4 connections (VPCs), all cells with VCI = 4 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 101 are terminated and processed. All segment OAM cells are dropped at End-to-End points, but they are not processed unless the Segment_End_Point bit is also logic 1.

Table 14 VC Table Miscellaneous Fields

Name	Description
VCI[15:0]	Specifies the VCI associated with this VC. For VPCs and F4 OAM connections, this field should be coded to all zeroes, and will be unused. For VCCs, this field is compared to the VCI of incoming cells to confirm that the search completed correctly. If the VCI field and the VCI of the incoming cell do not match, the search is considered invalid, and the cell will be dropped, with an optional copy to the microprocessor. This field is also used when generating OAM cells, if header translation is disabled.
VPI[11:0]	Specifies the VPI associated with this VC. This field is compared to the VPI of incoming cells to confirm that the search completed correctly. If the VPI field and the VPI of the incoming cell do not match, the search is considered invalid, and the cell will be dropped, with an optional copy to the microprocessor. If the connection is configured as a UNI (the NNI bit in the Configuration field is set to logic 0) then the first 4 bits of the VPI contain the GFC field and are thus not used in the comparison. This field is also used

Name	Description
	when generating OAM cells, if header translation is disabled. If the connection is a UNI, the first four bits of the VPI field should be set to zero.
Field B [11:0]	This field is compared against the Field B extracted from the cell during the search. If the Field B from the VC table and the Field B from the incoming cell do not match, the search is considered invalid and the cell is dropped, with an optional copy to the microprocessor. Any unused bits in this field should be set to logic 0. If Field B is configured to be less than 12 bits, the data should be LSB justified in this field.
Bwds VCRA [15:0]	The Backwards Direction VCRA indicates the VC Record Address of the corresponding VC in the opposite-direction S/UNI-ATLAS-3200. If the OBCIF_Bwd_VCRA bit is logic 1 in the Cell Processor Routing Configuration register, this field will be inserted, along with the PHY ID and other routing information, in prepended bytes of cells sent to the Backwards Cell Interface, to permit the opposite-direction S/UNI-ATLAS-3200 to identify the cell without performing a search on it. If OBCIF_Bwd_VCRA is logic 1, then it is expected that Search_From_IBCIF will be logic 0 in the opposite-direction S/UNI-ATLAS-3200.
VC Table CRC-10 [9:0]	This field provides a CRC-10 over the VC table in DRAM. If a CRC-10 error occurs, the DRAM_CRC_Err bit is set, an interrupt is raised, and the connection is optionally rendered inactive, depending on the setting of the Inactivate_On_DRAM_Err bit in the Cell Processor Configuration Register.
Cell Count 1 and 2 [31:0] Alternate Cell Count 1 and 2 [31:0]	These fields contain the billing cell counts, configured by the Cell Counting Configuration register bits. The Count Config Select field in the VC Record Table's Configuration field selects between the possible configurations . The Alternate counts are intended for use in time-of-day billing. When the Alternate_Count register bit is set to logic 1, the Cell Count fields in all VC records stop being incremented, and the Alternate Cell Count fields are incremented instead. The handover is done in such a way that no cell counts are missed. These counts represent the number of cells received, including cells from the BCIF, and cells from the MCIF (assuming PROC_CELL = 1). This counting occurs **before** policing is evaluated. The non-compliant cell counts can be subtracted to determine the state of the counts **after** policing. Cells received on connections with the Active bit equal to logic 0 will not be counted.
Received End-to-End Defect Location [127:0]	This field is used to store the Defect Location from a received end-to-end AIS or RDI cell. In the case of received AIS cells, this field is used in RDI cells generated due to End-To-End AIS declaration, via the AUTO_RDI function. If RDI cell generation is forced (using either the send_RDI table bits or the per-phy RDI register bits) or generated by the CC_AIS_RDI process, the contents of the global Generated Defect Location registers will be used. If the connection is an F4 being split out into F5s, then this field is used to determine the Defect Location of F5 AIS and RDI cells sent due to F4 End-to-End AIS declaration. In the case of received RDI cells, the defect location is simply stored for future retrieval. Defect locations from RDI cells will not be stored if End-to-end AIS alarm has been declared, and will be overwritten on the arrival of AIS cells, so this field is only valid for RDI cells if End-to-end RDI alarm is declared and End-to-end AIS alarm is not.
Received End-to-End AIS Defect Type [7:0]	This field is used to store the Defect Type from a received end-to-end AIS or RDI cell. In the case of received AIS cells, this field is used in RDI cells generated due to End-To-End AIS declaration, via the AUTO_RDI function. If RDI cell

Name	Description
	generation is forced (using either the send_RDI table bits or the per-phy RDI register bits) or generated by the CC_AIS_RDI process, the contents of the Generated OAM Defect Type field will be used. If the connection is an F4 being split out into F5s, then this field is used to determine the Defect Type of F5 AIS and RDI cells sent due to F4 End-to-End AIS declaration. In the case of received RDI cells, the defect type is simply stored for future retrieval. Defect types from RDI cells will not be stored if End-to-end AIS alarm has been declared, and will be overwritten on the arrival of AIS cells, so this field is only valid for RDI cells if End-to-end RDI alarm is declared and End-to-end AIS alarm is not.
Received Segment Defect Location [127:0]	This field is used to store the Defect Location from a segment AIS or RDI cell. In the case of received AIS cells, this field is used in RDI cells generated due to Segment AIS declaration via the AUTO_RDI function. If RDI cell generation is forced (using either the send_RDI table bits or the per-phy RDI register bits) or generated by the CC_AIS_RDI process, the contents of the global Defect Location registers will be used. If the connection is an F4 being split out into F5s, then this field is used to determine the Defect Location of F5 AIS and RDI cells sent due to F4 Segment AIS declaration. In the case of received RDI cells, the defect location is simply stored for future retrieval. Defect locations from RDI cells will not be stored if Segment AIS alarm has been declared, and will be overwritten on the arrival of AIS cells, so this field is only valid for RDI cells if Segment RDI alarm is declared and Segment AIS alarm is not.
Received Segment AIS Defect Type [7:0]	This field is used to store the Defect Type from a received segment AIS or RDI cell. In the case of received AIS cells, this field is used in segment RDI cells generated due to Segment AIS declaration via the AUTO_RDI function. If RDI cell generation is forced (using either the send_RDI table bits or the per-phy RDI register bits) or generated by the CC_AIS_RDI process, the contents of the Generated OAM Defect Type field will be used. If the connection is an F4 being split out into F5s, then this field is used to determine the Defect Location of F5 AIS and RDI cells sent due to F4 Segment AIS declaration. In the case of received RDI cells, the defect type is simply stored for future retrieval. Defect types from RDI cells will not be stored if Segment AIS alarm has been declared, and will be overwritten on the arrival of AIS cells, so this field is only valid for RDI cells if Segment RDI alarm is declared and Segment AIS alarm is not.

10.6 Header Translation

Once the appended octets, header, HEC, and UDF have been used in connection identification, they may be replaced with the contents of fields in Row 4 of the VC table.

Table 15 VC Table Fields For Header Translation

Row	127						0
4	Unused (4)	Translated VPI (12)	Translated VCI (16)	Translated HEC (8)	Translated UDF (24)	Translated Pre/Po 1 (32)	Translated Pre/Po 2 (32)

The S/UNI-ATLAS-3200 accepts cells ranging from 52 bytes (1 d-word of header and 12 of payload) to 64 bytes (2 prepends or postpends, 1 d-word of header, 1 d-word of HEC and UDF, and 12 of payload). The HEC/UDF fields are optional, and there may be no prepended/postpended d-words, one or two prepended d-words, one or two postpended d-words, or one prepend and one postpend. The S/UNI-ATLAS-3200 can also send words with any of those combinations. Prepended, Postpended and HEC/UDF d-words are added, translated, or deleted as necessary to adjust from the input cell interface configuration to the output cell interface configuration, and to match the global header translation instructions.

Prepended or Postpended words are replaced with or generated from the contents of the Translated Pre/Po1 and Translated Pre/Po2 fields if the XPREPO bit is logic 1 in the Cell processor Configuration register. If XPREPO is logic 0, but the output cells have prepends or postpends associated, then generated cells will contain 6A6A6A6A hex in those fields. As an additional option, the prepended/postpended words may be replaced with a descriptive word identifying the cell's VC Record, cell type, and some information about the connection. This Cell Info Field is identical to the Microprocessor Cell Info Field described in Section 10.17.5; its insertion is controlled by the Cell_Info_to_OCIF bit in the Cell Processor Configuration Register.

The header contents of each cell can be altered, and replaced with the contents of the Translated VPI and Translated VCI fields. Substitution of the VPI/VCI contents can be enabled by setting the XVPIVCI register bit. The PTI and CLP fields are not modified by the header translation process. If the connection is a Virtual Path (i.e. the VCI value in the VC Table is coded as all zeros), the VCI field is passed through transparently. As a globally configured option, the GFC field in UNI cells can be left unmodified; otherwise, it is replaced by the four most significant bits of the Translated VPI field. The HEC and UDF fields can be passed through transparently, or replaced by the Translated HEC and Translated UDF fields of the VC Table, as configured by the XHEC and XUDF bits.

10.7 Cell Rate Policing

10.7.1 Per-VC Policing

The S/UNI-ATLAS-3200 supports two instances of the Generic Cell Rate Algorithm (GCRA) for each connection. The policing operation is performed according to the Virtual Scheduling Algorithm outlined in ITU-T I.371. The per-VC policing fields are held in the VC table in Rows 0,1, and 3.

Table 16 VC Table Policing Fields

Row	127										0
0	Action 2 (2)	Inc 2 (14)	Limit 2 (14)	Action 1 (2)	Inc 1 (14)	Limit 1 (14)	Field B (12)	VPI (12)	VCI (16)	2	Bwds VCRA (16)	VC Table CRC-10 (10)
1	Status (10)	Configuration (14)	OAM Configuration (23)	Internal Status (21)	Policing Configuration (11)	Reserved (16)	Maximum Frame Length (11)	GFR State (3)	Policing Reserved (3)	ETE Received Defect Type (8)	Segment Received Defect Type (8)	
3	Unused (1)	Remaining Frame Count (11)	Non-Compliant Count 3 (16)	Non-Compliant Count 2 (16)	Non-Compliant Count 1 (16)	TAT2 (34)	TAT1 (34)					

Table 17 Policing Configuration VC Table Field

Bit	Name	Description
10	GFR_MCR_PPD	If this bit is logic 1, GFR policing is enabled and the MCR test is enabled to discard (i.e. Action 2 = Discard) then the policer will perform partial packet discard when a connection begins to fail MCR. If this bit is logic 0, then the MCR is only permitted to perform actions on frame boundaries, as per the GFR standard.
9	VP_Police	If this bit is a logic 1, then policing will be done using the parameters and configuration for the associated F4 rather than for this connection. All cells received on F5s will be considered user cells for the purposes of F4 policing. Note that only received cells are ever policed – generated cells of any sort are immune to policing, and do not affect TATs. This bit must be set to logic 0 if the F4 Pointer Active bit in the Linkage Row is logic 0. GFR policing is not possible at the F4 level.
8	COCUP	The Conditional Conformance Update (COCUP) bit is used to introduce a coupling between the two GCRAs. If COCUP=0, then GCRA1 and GCRA2 are completely independent of each other and the updating of the TAT1 and TAT2 fields are independent. If the cell is conforming to a GCRA, the TAT field for that GCRA will be updated. If COCUP is a logic 1, then the updating of the TAT fields is conditional on both GCRAs. The operation is more fully explained below.
7	Policing Rollover FIFO Enable	Enables the Non-Compliant counts to generate entries in the Count Rollover FIFO whenever their MSB becomes logic 1. If the Count Rollover FIFO is full, the MSB will remain logic 1 until an entry has been successfully generated, at which time the MSB will become logic 0. If this bit is logic 0, then the counts operate as normal saturating counters, and must be polled periodically by the microprocessor.
6	CLPCC_CLP1_Discard	If the CLP Conformance Check CLP1 Discard bit is set to logic 1, then during GFR policing, if a cell arrives with CLP = 1 in a frame whose first cell had CLP = 0, then the frame will undergo Partial Packet Discard. If the CLP=1 cell is the end of packet, then every cell until the next CLP = 0 end of packet will be discarded. If this bit is logic 0, then CLP = 1 cells in CLP = 0 frames will not be treated as non-compliant.
5	PHY Police	If the PHY Policing bit is logic 1, then PHY policing is enabled on this connection. If this bit is logic 0, then this connection is not affected by per-PHY policing, and does not affect per-PHY policing parameters.
4	GFR	If the Guaranteed Frame Rate bit is a logic 1, then the frame-aware GFR policing algorithm is enabled. GFR policing is discussed in section 10.7.3. When GFR policing is enabled, GCRA 1 must be configured to police the PCR, with the action set to discard, and GCRA2 must be configured to police the MCR, with the action set to either tag or discard. Actions due to violation of MCR will only be performed on frame boundaries, unless the GFR_MCR_PPD bit is logic 1. If the GFR bit is logic 0, then normal, non-frame-aware policing is performed.
3	Violate	**When the VIOLATE bit is logic 1, the policer acts as if GCRA2 always fails. Actions taken on the cell, and updating of PHY TAT, GCRA1 TAT, and non-compliant count values is exactly as if GCRA 2 had failed. VIOLATE is not compatible with GFR policing.**
2:0	Policing Config Select	The Policing Config Select bits select one of 8 Policing Configurations stored in registers. Policing Config Select = 000 selects Connection Policing Configuration # 1, and Policing Config Select = 111 selects Connection Policing Configuration # 8. These configurations dictate which of CLP0, CLP1, User, OAM, RM, and Other cells are policed by each GCRA.

To allow full flexibility, the S/UNI-ATLAS-3200 supports 8 possible configurations, selected by the Policing Config Select bits, which allow each GCRA to police any combination of user cells, OAM cells, RM Cells, high priority cells or low priority cells.

The Theoretical Arrival Time fields (TAT1 and TAT2), Increment fields (I1 and I2), and Limit fields (L1 and L2) must be initialized before policing is enabled. When the connection is setup, the TAT fields must be set to all zeros, and they should not be modified by the management software after the connection has been initialized. The Increment and Limit fields must be programmed to the desired traffic rate. These fields relate to the traffic contract parameters as follows:

$$I = \frac{1}{PCR(\Delta t)}$$

$I = \text{Increment Field}$

$PCR = \text{Peak Cell Rate (cells/s)}$

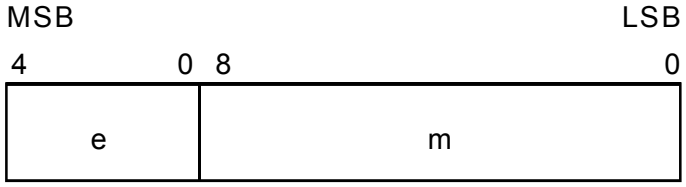
$\Delta t = \text{clock period (s)}$

In order to obtain the granularity required in ITU-T I.371, the Increment fields are encoded as floating-point fields as follows:

$$I = 2^e\left(1 + \frac{m}{512}\right) \quad \text{where} \quad 0 \le e \le 31$$

$$0 \le m \le 511$$

The exponent, *e*, is a 5-bit field and the mantissa, *m*, is a 9-bit field. The Increment field is formatted as follows:



The floating-point encoding format of the Increment field ensures the granularity of the S/UNI-ATLAS-3200 is 0.19% in accordance with ITU-T I.371 5.4.1.2.

The Limit field is defined as:

$$L = \frac{\tau}{\Delta t}$$

where $\tau = \text{Cell Delay Variation (s)}$

For a Sustained Cell Rate (SCR) conformance definition, the parameters relate as follows:

$$I = \frac{1}{SCR(\Delta t)}$$

$$L = \frac{BT}{\Delta t} = \frac{(MBS - 1)\left(\frac{1}{SCR} - \frac{1}{PCR}\right)}{\Delta t}$$

where

$SCR = \text{Sustaned Cell Rate (cells/s)}$

$MBS = \text{Maximum Burst Size at the Peak Cell Rate (cells)}$

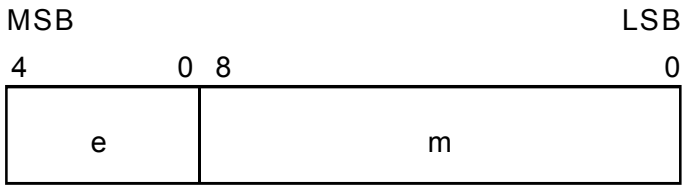
$BT = \text{Burst Tolerance (s)}$

In order to compensate for the potentially large CDV and Burst Tolerance limits anticipated in ATM networks, the Limit fields, L1 and L2 are encoded as floating-point values, in the same manner as the Increment fields:

$$L = 2^e\left(1 + \frac{m}{512}\right) \quad \text{where} \quad 0 \le e \le 31$$

$$0 \le m \le 511$$

where *e* is the 5-bit exponent and *m* is the 9-bit mantissa. The Limit fields are formatted as follows:



The Theoretical Arrival Time (TAT1 and TAT2) are encoded as fixed-point values with an integer and fraction portion. The integer portion of the TAT field is a 31-bit value, and the fractional portion is a 3-bit value. The TAT fields are formatted as follows:

33 3	2 0
Integer Portion	Fractional Portion

The fractional portion of the TAT field is measured in fractions of the clock period, Δt. For a 8 ns clock period, the accuracy of the policing algorithm can be measured as follows:

$PCR\max = 5651328 \text{ cells/s}$ (this is the maximum cell rate at 2488 Mbps)

$$T\min = \frac{1}{PCR\max} = 176.949 \text{ ns}$$

$$\text{Accuracy} = \frac{TAT\min}{T\min} = \frac{(0.125)(8\text{ns})}{176.949 \text{ ns}} = 0.00565 = 0.57\%$$

Thus, the accuracy of the S/UNI-ATLAS-3200 policing algorithm satisfies the ITU-T I.371 recommendation of 1%.

It is important to note that since the Limit field is a floating-point number, its maximum value exceeds the maximum TAT (2147483647) value; therefore, L should not exceed this value. If the encoded value of L is greater than TAT_{max}, then L shall be taken to be TAT_{max}. Thus,

$$L \le TAT_{\max}$$

The value of Δt and the range of I and L determine the lowest PCR that can be policed, the PCR granularity supported at the highest expected PCR and the largest CDV expected.

$$PCR_{\min} = \frac{1}{I_{\max}(\Delta t)}$$

granularity as a fraction of PCR $= PCR(\Delta t)$

$$\tau_{\max} = L_{\max}(\Delta t)$$

The maximum value for increment field supported in the S/UNI-ATLAS-3200 is $2^{28} - 1 = 268435455$, therefore, the smallest peak (or sustainable) cell rate supported is PCR_{min} = 0.465 cells/s

As described previously, the Limit field, L is a 14-bit floating point field, with $L_{max} = TAT_{max} =$ 2147483647. Therefore, with an 8ns cycle time, CDV_{max} = 17.18 s.

Note, the PCR (or SCR) and CDV (or BT) can be changed while the connection is provisioned without disrupting the policing algorithm. That is, the Increment and Limit fields may be changed at any point, and the policing algorithm will immediately begin policing to the new settings.

The action taken on a non-conforming cell is programmed on a per-connection basis by the Action1[1:0] and Action2[1:0] fields in Row 0 of the VC Table (Action1 controls the action taken when a cell is non-conforming with GCRA1, and Action2 controls the action taken when a cell is non-conforming with GCRA2).

Table 18 Policing Actions

Action1[1:0] and Action2[1:0]	Definition
00	Set the Police status bit, but take no other action than to increment the appropriate non-compliant cell counts.
01	Reduce the priority of high priority cells (i.e. tag CLP=0 cells. Increment the appropriate non-compliant cell counts.
10	Reduce the priority of high priority cells and discard the low priority cells. Increment the appropriate non-compliant cell counts.
11	Discard all non-conforming cells. Increment the appropriate non-compliant cell counts.

Policing can be effectively disabled for a connection if the increment fields (I1 and I2) are set to all zeros.

The Conditional Conformance Update (COCUP) bit is used to introduce a coupling between the two GCRAs.

If COCUP=0, then GCRA1 and GCRA2 are completely independent of each other and the updating of the TAT1 and TAT2 fields are independent. If the cell is conforming to a GCRA, the TAT field for that GCRA will be updated. The table below describes the behavior of the ATLAS:

Table 19 Actions on Policing with COCUP=0

GCRA1		GCRA2			
		Pass	Fail		
			No Action	Tag	Discard
Pass		Update TAT1 Update TAT2	Update TAT1	Update TAT1	Update TAT1
Fail	No Action	Update TAT2	No Update	No Update	No Update
	Tag	Update TAT2	No Update	No Update	No Update
	Discard	Update TAT2	No Update	No Update	No Update

If COCUP=1, then GCRA1 and GCRA2 are coupled and the updating of the TAT1 and TAT2 fields are conditional. The S/UNI-ATLAS-3200 reacts as described in the table below.

Table 20 Actions on Policing with COCUP=1

GCRA1		GCRA2			
		Pass	Fail		
			No Action	Tag	Discard
Pass		Update TAT1 Update TAT2	Update TAT1	Update TAT1	No Update
Fail	No Action	Update TAT2	No Update	No Update	No Update
	Tag	Update TAT2	No Update	No Update	No Update
	Discard	No Update	No Update	No Update	No Update

In both cases (COCUP=1 and COCUP=0), if a cell fails both GCRA1 and GCRA2, the most severe action is taken on the cell.

The three 16-bit non-compliant counts are programmed in either the NCOUNTx[3:0] or the GFR_NCOUNTx[3:0] fields of the Per-VC Non-Compliant Cell Counting Configuration, depending on whether the GFR bit is set to logic 1 in the policing configuration field of the VC table. Each non-compliant count has the following programming options:

Table 21 Non-Compliant Cell Count Configurations

NCOUNTx[3:0]	Definition
0000	Non-compliant CLP=0 cells.
0001	Non-compliant CLP=0+1 cells.
0010	Discarded CLP=0 cells.
0011	Discarded CLP=0+1 cells.
0100	Tagged CLP=0 cells which are not discarded
0101	Non-compliant CLP=0 frames (GFR only)
0110	Non-compliant CLP=0+1 frames (GFR only)
0111	Partially or Completely Discarded CLP=0 frames (GFR Only)
1000	Partially or Completely Discarded CLP=0+1 frames (GFR Only)
1001	Tagged CLP=0 Frames which are not discarded (GFR Only)
1010	Total CLP=0 AAL5 Frames Received
1011	Total CLP=0+1 AAL5 Frames Received
1100	Total cells non-compliant to GCRA1
1101	Total cells non-compliant to GCRA2
1110	Total cells non-compliant to the PHY GCRA
1111	Reserved

The Total AAL5 Frames Received counts are available in non-GFR connections, but the other frame-aware counts should not be selected except in the GFR case. Counting of CLP0 vs. CLP 1 frames is based on the CLP of the received EOP.

These non-compliant cell counts may, for instance, be programmed to satisfy the following requirements:

- Non-Compliant Cell Count1[15:0]: the number of CLP0+1 cells discarded by the UPC/NPC function. GR-1248-CORE R9-6.
- Non-Compliant Cell Count2[15:0]: the number of CLP0 cells discarded by the UPC/NPC function. GR-1248-CORE R9-7.
- Non-Compliant Cell Count3[15:0]: the number of CLP0 cells tagged as CLP1 cells by the UPC/NPC function. GR-1248-CORE CO9-8.

If the Policing Rollover FIFO Enable bit in the Policing Configuration field of the VC Table is logic 1, then whenever the MSB of any of the non-compliant counts is logic 1, an attempt is made to make an entry to the Count Rollover FIFO. If the entry is made successfully, then the MSB is set back to logic 0. Otherwise, it remains 1 until an entry is sucessfully made. Thus each Count rollover entry represents 2^{15} non-compliant count events. If the Policing Rollover FIFO Enable bit is logic 0, then the non-compliant counts will saturate at all 1's.

10.7.2 Per-PHY Policing

The Cell Processor also maintains a single GCRA instance per-PHY (48 in total) in an internal RAM which may be programmed via the PHY Policing Address and Access Control Register. The per-PHY policing may be selectively enabled for any number of connections for a PHY. The PHY Police bit in the Policing Configuration field of the VC table determines whether or not PHY policing is active on that connection. The PHYID[5:0] field in the VC Linkage Table determines which of the 48 internal policing instances is addressed if per-PHY policing is active.

The per-PHY policing is evaluated alongside the per-connection policing. If a cell is discarded as a result of per-PHY policing, the per-connection policing parameters are not updated. Similarly, if a cell is discarded as a result of per-connection policing, the per-PHY policing parameters are not updated.

The table below describes the S/UNI-ATLAS-3200 actions when per-PHY policing is enabled.

Table 22 Actions with per-PHY Policing

Per-VC GCRA (Note, the per-VC GCRAs are evaluated as described in Table 18, Table 19, and Table 20)		Per-PHY GCRA			
		Pass	Fail		
			No Action	Tag	Discard
Pass		Update VC TAT Update PHY TAT	Update VC TAT	Update VC TAT	No Update
Fail	No Action	Update PHY TAT	No Update	No Update	No Update
	Tag	Update PHY TAT	No Update	No Update	No Update
	Discard	No Update	No Update	No Update	No Update

The per-PHY policing has a programmable action field and configurable register bits to police any combination of user cells, OAM cells, RM cells, high priority cells and low priority cells.

Non-compliant cell counts are also maintained on a per-PHY basis.

It is the responsibility of the management entity to ensure the per-PHY policing parameters are programmed correctly. All RAM addresses can be written to and read by an external microprocessor.

The internal per-PHY policing RAM is shown below

Table 23 Internal Per-PHY Policing RAM

Address [1:0]	31 0					
00	PhyTAT LSB (32)					
01	Reserved (2)	PHY I (14)		PHY L (14)		PhyTAT MSB (2)
10	PHY Non-Compliant2 (16)			PHY Non-Compliant1 (16)		
11	Unused (10)	PHY Policing Rollver FIFO EN (1)	PHY VC Count (1)	PHY Police Config. (2)	PHY Action (2)	PHY Non-Compliant3 (16)

The PHY Policing Configuration[1:0] field (of the Internal PHY Policing RAM at Addr[1:0] = 11) selects 1 of 4 settings (in the PHY Policing Configuration Register) in the Cell Processor which allows any combination of CLP=0 or CLP=1 user cells, segment OAM cells, or RM cells to be policed by the PHY GCRA. When the PHY Policing Rollover FIFO EN bit is logic 1, then when the MSB of any of the non-compliant counts is set, an entry is generated into the Count Rollover FIFO, and the MSB is cleared. When the PHY Policing Rollover FIFO EN bit is logic 0, no entries will be made due to per-PHY non-compliant counts, and the counts will saturate at all-ones.

The PHY I (Increment) and L (Limit) fields are analogous to the per-VC Increment and Limit fields and are programmed in the same way. The PHY Action[1:0] field controls the programmable action to be taken on cells which are non-conforming to the PHY GCRA. Note that tagging on a per-PHY basis is incompatible with performing GFR policing on any of the connections on the PHY. If GFR is to be supported, then either PHY policing should be disabled for those VCs, or the per-PHY policing action should be set to “00” or “11”.The PHY Action field is programmed as follows:

Table 24 Per-PHY Policing Actions

PHY Action[1:0]	Description
00	Set the Police status bit, but take no other action than to increment the appropriate non-compliant cell counts.
01	Reduce the priority of high priority cells (i.e. tag CLP=0 cells. Increment the appropriate non-compliant cell counts. This option is incompatible with GFR policing on any VCs on the PHY.
10	Reduce the priority of high priority cells and discard the low

PHY Action[1:0]	Description
	priority cells. Increment the appropriate non-compliant cell counts. This option is incompatible with GFR policing on any VCs on the PHY.
11	Discard all non-conforming cells. Increment the appropriate non-compliant cell counts.

The PHY non-compliant cell counts are programmed in the PHYNCOUNTx[3:0] fields of the Non-Compliant Cell Counting register. Each non-compliant cell count has the following programming options:

Table 25 Per-PHY Policing Non-Compliant Count Options

PHYNCOUNTx[3:0]	Definition
0000	Non-compliant CLP=0 cells.
0001	Non-compliant CLP=0+1 cells.
0010	Discarded CLP=0 cells.
0011	Discarded CLP=0+1 cells.
0100	Tagged CLP=0 cells which are not discarded
0101 .. 1001	Reserved
1010	Total CLP=0 AAL5 Frames Received
1011	Total CLP=0+1 AAL5 Frames Received
1100	Total cells non-compliant to GCRA1
1101	Total cells non-compliant to GCRA2
1110	Total cells non-compliant to the PHY GCRA
1111	Reserved

The PHYVCCount bit determines whether cells which are non-compliant with the per-VC policer are counted in the per-PHY non-compliant cell counts and vice versa (i.e. cells which are non-compliant with the per-PHY policer are counted in the per-VC non-compliant cell counts). The table below describes the programming options.

Table 26 Per-PHY/Per-VC Non-Compliant Cell Counting PHYVCCount=0

PHYVCCount=0		Per-VC Policing	
		Compliant	Non-Compliant
Per-PHY Policing	Compliant	No update.	Update per-VC non-compliant counts Don't update per-PHY non-compliant counts.
	Non-Compliant	Don't update per-VC non-compliant counts. Update per-PHY non-compliant counts	Update per-VC non-compliant counts. Update per-PHY non-compliant counts.

Table 27 Per-PHY and per-VC Non-Compliant Cell Counting PHYVCCount=1

PHYVCCount=1		Per-VC Policing	
		Compliant	Non-Compliant
Per-PHY Policing	Compliant	No update.	Update per-VC non-compliant counts Update per-PHY non-compliant counts.
	Non-Compliant	Update per-VC non-compliant counts. Update per-PHY non-compliant counts	Update per-VC non-compliant counts. Update per-PHY non-compliant counts.

10.7.3 Guaranteed Frame Rate Policing

The S/UNI-ATLAS-3200 supports Guaranteed Frame Rate (GFR) policing in accordance with the ATM Forum Traffic Management Specification 4.1. A total of four policing actions are observed for GFR policing. They are: Maximum Frame Length (MFL) conformance test, Peak Cell Rate (PCR) test, Minimum Cell Rate (MCR) conformance test, and the CLP Conformance test. When GFR policing is enabled, the GFR policing algorithm is enabled. The conformance tests are evaluated sequentially, in the following order:

1. MFL conformance test. When an End Of Message cell in a packet is received, the Remaining Frame Count field of the VC Table is loaded, after testing for MFL conformance with the current value, with the value programmed in the Maximum Frame Length field in the VC Table. The Remaining Frame Count is then decremented with each cell received in the new frame. If this value reaches zero before an End Of Message cell is received, the remainder of the frame is discarded (the EOM cell is identified by having an SDUTYP equal to logic 1). The MFL conformance test can be disabled by setting the MFL field in the VC table to all ones.

2. PCR conformance test. This test is performed using GCRA1 in much the same manner as normal cell policing. However, for compliance to the GFR specification, Action 1 must be set to 11 (discard). If the PCR conformance test is deemed to be non-compliant, the remainder of the cells in the current frame will be discarded. If the non-compliant cell is the start of packet, then a complete packet discard is executed; if it is in the middle of a packet, a partial packet discard is executed; if it is the end of a packet, it is discarded along with every subsequent cell until a EOP is received which is not discarded.

3. MCR conformance test. This test is performed using GCRA2, however, it differs slightly from the normal cell policing. The MCR conformance test is only performed at the start of a frame. If the first cell of a frame is a conforming cell, then all remaining cells in that frame will be processed as if they are conforming to the MCR conformance test. If the first cell is non-conforming, then the action specified by Action2[1:0] will be performed on the entire frame. Normally, the MCR conformance test will be programmed to tag non-conforming CLP=0 frames (Action = 01, CLP0 cells policed). If the first cell of a frame is a non-conforming CLP=0 cell, then that cell and all other cells in that frame (including the EOM) will be tagged. However, the MCR may be programmed to discard (Action = 11), in which case a complete packet discard will be performed on frames whose first cell is non-compliant to MCR.

   In order to support AAL5 frame-aware policing on connections that do not support full GFR, the GFR_MCR_PPD bit in the Policing Configuration register is provided. If this bit is a logic 1, then the MCR is permitted to perform PPD, if configured to discard; tagging will still be performed only on frame boundaries.

4. CLP conformance test: This test is performed on every cell in a frame, including the EOM. The CLP conformance test can be enabled on a per-connection basis; this is controlled by the CLPCC_CLP1_Discard bit of the Policing Configuration field in the VC Table. If the Start of Frame is a CLP = 1 cell, then any subsequent CLP=0 cell will be tagged. If the first cell of the frame is a CLP=0 cell, then if the CLPCC_CLP1_Discard bit is logic 1, any subsequent CLP=1 cell received in the frame will result in a partial packet discard being executed.

The relevant GFR fields in the VC are described below:

Name	Description
GFR	If this bit is a logic 1, the S/UNI-ATLAS-3200 will utilize GFR policing on the connection as described above. If this bit is logic 0, the connection will not use the GFR policing, rather it will use the normal cell-based policing described previously.
GFR_MCR_PPD	If this bit is logic 1, GFR policing is enabled and the MCR test is enabled to discard (i.e. Action 2 = Discard) then the policer will perform partial packet discard when a connection begins to fail MCR. If this bit is logic 0, then the MCR is only permitted to perform actions on frame boundaries, as per the GFR standard.
CLPCC_CLP1_Discard	If the CLP Conformance Check CLP1 Discard bit is set to logic 1, then during GFR policing, if a cell arrives with CLP = 1 in a frame whose first cell had CLP = 0, then the frame will undergo Partial Packet Discard. If the CLP=1 cell is the end of packet, then every cell until the next CLP = 0 end of packet will be discarded. If this bit is logic 0, then CLP = 1 cells in CLP = 0 frames will not be treated as non-compliant.
Maximum Frame Length	This field indicates the maximum permissible length of a frame for GFR connections. Frames exceeding this length will undergo PPD. A maximum frame length of zero is invalid, and is treated as an MFL of 1.
Remaining Frame Count	When an End Of Message cell in a packet is received, the Remaining Frame Count field of the VC Table is loaded, after testing for MFL conformance with the current value, with the value programmed in the Maximum Frame Length field in the VC Table. The Remaining Frame Count is then decremented with each cell received in the new frame. If this value reaches zero before an End Of Message cell is received, the remainder of the frame is discarded (the EOM cell is identified by having

Name	Description
	an SDUTYP equal to logic 1). The MFL conformance test can be disabled by setting the MFL field in the VC table to all ones. This field should be initialized to MFL – 1.
GFR State[2:0]	The GFR State is an internally maintained state variable which must be programmed to 0 at connection startup and not changed thereafter.

10.8 Cell Counting

The S/UNI-ATLAS-3200 maintains counts on a per-connection basis, per-PHY basis and over the aggregate cell stream.

The following parameters are stored on a per-connection basis in the VC Tables:

- Two 32-bit "billing" cell counts that may be programmed to count any combination of the following:
  A. CLP0 user cells.
  B. CLP1 user cells.
  C. CLP0 OAM cells.
  D. CLP1 OAM cells.
  E. CLP0 RM cells.
  F. CLP1 RM cells.
  G. CLP0 cells with Invalid VCI/PTI
  H. CLP1 cells with Invalid VCI/PTI.
- Three Non-compliant cell counts, which may count (Non-Compliant CLP0 or CLP0+1 cells, Discarded CLP0 or CLP0+1 Cells, Tagged Cells, Total CLP 0 or CLP0+1 frames, Non-Compliant CLP0 or CLP1 Frames, etc.) These counts are described in Section 10.7, which covers policing.
- Per-PHY counts of CLP0, CLP1, valid OAM, valid RM, Invalid OAM/RM, Congested (EFCI or GFC), timed-out, and Bad VPI/VCI/PTI cells.

The two programmable 32-bit cell counts represent the state of the cells before policing. The non-compliant cell counts can be used to derive the cell counts after policing.

The programmability of the two 32-bit cell counts allows the ability to provision scheduled measurements and special studies on each connection.

When aggregating or terminating a VPC, the VPC OAM Connection's 32-bit billing counts are updated based on the total traffic arriving on the VPC. That is, all cells arriving on associated VCCs are counted as user cells in the VPC OAM Connection. This permits aggregate counts to be generated with little microprocessor effort.

If Performance Management is activated, a range of forward monitoring and backward reporting statistics are stored. These statistics are described in Section 10.14 which covers Performance Management.

The S/UNI-ATLAS-3200 can be configured to have some of its counters roll over or saturate at all ones. All per-PHY counts, the per-connection cell counts, non-compliant cell counts, and the PM counts are configurable in this manner.

The Rollover_FIFO_EN bit in the Configuration field of the VC table controls whether the 32-bit per-VC Cell counts saturate, or whether they generate Count Rollover FIFO entries when their MSB is logic 1, and then reset their MSBs to 0. The Policing Rollover FIFO EN bit in the Policing Configuration field performs this function for the non-compliant counts; The PHY Policing Rollover_FIFO_EN bit in the PHY Policing RAM performs the same function for the per-PHY non-compliant counts, as does the PHY Rollover_FIFO_EN bit in the Per-PHY Counter Configuration register for the other per-PHY counts. The PM_Rollover_FIFO_EN bit in the PM Configuration Field of the Internal PM table controls whether the Performance Management counts generate Count Rollover FIFO entries. The Count Rollover FIFO is described in Section 10.16.

All per-PHY and per-VC counts have a Clear On Read option. If this bit is logic 1, then when the microprocessor reads the counter value, the value is immediately set to zero. If the per-PHY or per-VC Clear On Read register bit is logic 0, the counter value is not cleared when it is read, and the value must be cleared by explicitly writing all zeros to that counter location.

In order to allow for a time-of-day billing mechanism, the S/UNI-ATLAS-3200 provides Alternate Count fields for the general 32-bit counts. When the Alternate_Count bit in the Cell Processor Configuration register is set to logic 1, the 32-bit cell counts in all VCs stop incrementing, and the Alternate Counts are incremented instead. The cell counts may then be read at leisure by the microprocessor. When the Alternate_Count bit is set to logic 0 again, the counting reverts to the regular 32-bit counts, and the Alternate Counts may be read (and presumably cleared) at leisure by the microprocessor.

One of the objectives of counting is to count, somewhere, every cell that arrives. Almost all cells can be counted in the per-VC cell counts. However, cells that do not belong to any particular connection (i.e. they do not search to a valid, active connection) cannot be counted per-VC. These cells have their own per-PHY count, the Invalid VPI/VCI/PTI cell count. The only overlap between this count and the per-VC counts is for cells with a reserved VCI or PTI. The Cnt_Rsvd_VCI_PTI bit in the per-PHY count configuration register controls whether cells with reserved VCI or PTI are counted in the Invalid VPI/VCI/PTI cell count.

10.9 Operations, Administration and Maintenance (OAM) Cell Servicing

The S/UNI-ATLAS-3200 is capable of terminating and monitoring F4 and F5 segment and end-to-end OAM flows. Complete processing of Fault Management cells is provided on all connections. Performance Management is provided on a limited number of connections (512 simultaneous sessions in each direction are supported). Activate/Deactivate and Undefined OAM cells are passed to the Microprocessor Cell Interface or to the Output Cell Interface for external processing. Loopback cells are examined, and routed based on their Loopback Indication, Loopback Location ID, and Source ID.

The programming of the Configuration and OAM Configuration field in the VC Table determines how the S/UNI-ATLAS-3200 will behave with respect to a particular connection.

Upon receipt of an OAM cell, the CRC-10 is checked. If the check sum is incorrect, the OAM cell is not processed (i.e. alarms and counts are not updated) and the per-PHY errored OAM cell count is incremented. If CRC10toUP is set in the Cell Processor Routing Configuration register, bad-CRC OAM cells will be routed to the Microprocessor Cell interface. Otherwise, further processing is dependent upon the contents of the OAM Type field and the programming of the S/UNI-ATLAS-3200 for that connection.

If a connection is not provisioned as an end point (segment end-point or end-to-end point), all incoming OAM cells (other than certain Loopback cells) are passed to the Output Cell Interface (subject to policing, if so configured), regardless of whether or not the OAM Type or Function Type fields have defined values. As an option, OAM cells may be discarded at non-flow end points if the CRC-10 is incorrect. At flow end points, all OAM cells are terminated, except Activate/Deactivate and Undefined OAM cells which may, optionally, be routed to the OCIF for external processing.

10.9.1 Fault Management Cells

Fault Management cells are identified with an OAM Cell Type field of 0001. The S/UNI-ATLAS-3200 supports segment and end-to-end AIS, RDI, Continuity Check (CC) and Loopback cells.

Segment and End-to-End AIS alarm status bits in the Status field are set upon receipt of a single AIS (function type = 0000) cell (segment or end-to-end). If the connection FM_Interrupt_Enable bit is set, a globally maskable interrupt will be asserted at the change of state of the (segment or end-to-end) AIS alarm. The alarm status is cleared upon receipt of a single user or CC cell, or if no AIS cell has been received within the last 2.5 +/- 0.5 sec. If the AUTO_RDI VC table bit is set, an RDI cell (segment or end-to-end) is generated immediately upon receipt of the first AIS cell at a flow end point and once a second thereafter until the AIS state is exited. The S/UNI-ATLAS-3200 generates RDI cells for insertion in the reverse flow and sends them to the companion chip through the Backward Cell Interface. In addition, the S/UNI-ATLAS-3200 will insert any RDI cells it receives over the backward cell interface into the cell stream it sources.

When the S/UNI-ATLAS-3200 receives a segment or end-to-end AIS cell, the Defect Location and Defect Type fields of the AIS cell are copied into the VC Table. These fields are used when RDI cells are generated at segment or end-to-end points as a result of the AUTO_RDI process.

Segment and End-to-End RDI alarm status bits are set upon receipt of a single RDI (function type = 0001) cell (segment or end-to-end). The defect location and type fields will be copied into the VC table for subsequent retrieval, so long as AIS alarm is not declared. While it is not reasonable to expect the reception of both AIS and RDI of the same type (i.e. both segment or both end-to-end), if this occurs the AIS defect location will be given priority for storage, so that it can be used in the generation of RDI cells. If the connection FM_Interrupt_Enable bit is set, a globally maskable interrupt will be asserted at the change of state of the (segment or end-to-end) RDI alarm. The alarm status is cleared if no RDI cell has been received within the last 2.5 +/- 0.5 sec.

If the CC_Activate_Segment bit is a logic 1, and no user cells have been transmitted within a 1.0 second (nominal) window, a segment CC cell is generated and sent to the Output Cell Interface. The forced generation of CC cells (independent of the flow of user cells) at one second (nominal) intervals is enabled when the CC_Activate_Segment bit is logic 1 and the ForceCC register bit is logic 1. If the ForceCC register bit is logic 0, then the generation of CC cells is dependent on the flow of user cells. Regardless of the state of the CC_Activate_Segment bit, if no user cells or segment CC cells have been received within a 3.5 +/- 0.5 sec window, the CC_Alarm_Segment status bit is set. If the connection FM_Interrupt_Enable bit is set, a globally maskable interrupt will be asserted at the change of state of the segment CC alarm. The Segment CC alarm is cleared upon the reception of the first user or Segment CC cell.

If the S/UNI-ATLAS-3200 is configured as a segment end-point, and the AUTO_RDI and CC_AIS_RDI bits of the OAM Configuration field is set, a segment RDI cell is generated once per second into the reverse direction while the segment CC alarm is declared. In addition, if the AUTO_AIS bit is logic 1, then an ETE AIS cell is generated once per second while segment CC alarm is declared.

If the S/UNI-ATLAS-3200 is not configured as a segment end point, then if the Segment_Flow bit is logic 1, the AUTO_AIS register bit is set, and the CC_AIS_RDI bit is set in the OAM Configuration field of the VC table, a segment AIS cell is generated once per second while Segment CC alarm is declared and Segment AIS alarm is not declared.

When AIS cells are generated by the S/UNI-ATLAS-3200 due to the AUTO_AIS function, the per-PHY AIS generation bits, or the per-VC Send_AIS bits, the Generated_Defect_Type[7:0] field in the VC table is used for the defect type, and the Defect Location register fields are used for the defect location.

When F5 AIS cells are generated due to F4 AIS, the defect location and type of the F4 AIS cell that caused the alarm are sent. Similarly, when F4 Ete AIS cells are sent as a result of reception of Segment AIS cells (via the APSx function) the Defect Location and Type of the received Segment AIS cell is used.

For each segment OAM capability described above, the same capability exists for the End-to-End.

The S/UNI-ATLAS-3200 also supports the generation of F5 AIS and RDI cells when associated F4 connections, which are terminated, enter the AIS alarm state. This is described in detail in section 10.10.

The S/UNI-ATLAS-3200 may be configured on a per-PHY basis to output AIS or RDI cells (or both) on all connections whose PHYID matches those set in a programmable register. The Per-PHY RDI Cell Generation Control and Per-PHY AIS Cell Generation Control registers control the generation of RDI and AIS cells on entire PHYs at once. When the PHY AIS bits are set, end-to-end cells (and, if Segment_Flow is logic 1, segment AIS cells) are sent once per second, except at flow end points. When the PHY RDI bits are set, RDI cells will be sent once per second in the reverse flow direction on all connections which are segment or end-to-end points. In the case of a segment end point, one segment RDI and one end-to-end AIS cell will be sent per second, if both the PHY AIS and PHY RDI bits are set.

10.9.2 Loopback Cells

The S/UNI-ATLAS-3200 provides support for generating Returned Loopback cells via the BCIFs. Generation of parent loopback cells is left up to the microprocessor.

If enabled, loopback cells will have their Loopback Indication and Loopback Location ID examined. Cells with Loopback Indication = 0 will be dropped and routed to the Microprocessor Cell Interface at flow end-points, and at intermediate points whose Loopback Location ID Register matches the Source ID Field of the loopback cell. For cells with Loopback Indication = 1, segment Loopback cells will be dropped and looped back if their Loopback Location ID matches the Loopback Location ID register, and looped back but not dropped if their Loopback Location ID is all-zeroes. Both segment and end-to-end cells will be dropped and looped back at flow end points if their Loopback Location ID is all-ones. In any event, Loopback cells are always dropped at flow end points. Cells which are looped back always have their Loopback Indication bit set to 0, and their Loopback Location ID replaced with the contents of the Loopback Location ID Register.

Alternately, loopback cells may also be routed to the microprocessor for external processing.

10.9.3 Activation/Deactivation Cells

Activation/Deactivation cells are identified with an OAM Cell Type of 1000. They are used by the management entity to implement the handshaking required to initiate or cease the Performance Management or Continuity Check processes.

The S/UNI-ATLAS-3200 does not process these cells. If this S/UNI-ATLAS-3200 is not an end-point for an OAM flow, all Activate/Deactivate cells are passed to the Output Cell Interface. If the S/UNI-ATLAS-3200 is an OAM flow end-point, the Activate/Deactivate cells are optionally passed to the Microprocessor Cell Interface or to the Output Cell Interface. The flow of Activate/Deactivate cells is controlled by the ACTDEtoUP, ACTDEtoBCIF and ACTDEtoOCIF register bits.

10.9.4 System Management Cells

System Management cells are identified with an OAM Cell Type of 1111. Their use is largely for security puposes, and is under consideration by the ITU. The S/UNI-ATLAS-3200 does not process these cells. If the S/UNI-ATLAS-3200 is not a flow end-point for an OAM flow, all System Management cells are passed to the Output Cell Interface. If the S/UNI-ATLAS-3200 is an OAM flow end-point, the System Management cells are optionally passed to the Microprocessor Cell Interface.

10.9.5 Automated Protection Switching Cells

APS Coordination Protocol cells are identified with an OAM Cell Type of 0101. They are handled like other OAM cells, and can be copied to the MCIF via the APStoUP bit in the Configuration field of the VC Table, or to the BCIF via the combination of the per-VC APStoUP bit and the APStoBCIF bit in the Routing Configuration Register. They are identified by a code in the Cell Type field of the Microprocessor Cell Info field and the BCIF Cell Info Field. APS CP cells may be passed on to the OCIF at OAM end-points by setting the APStoOCIF bit to logic 1 in the Routing Configuration Register.

10.9.6 Resource Management Cells

Resource Management (RM) cells are identified by a PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. As a programmable option, VP-RM cells can be further qualified by PTI=110.

The S/UNI-ATLAS-3200 does not process the RM cell payload, but simply passes these cells to the Output Cell Interface with an optionally translated header. As a programmable option, the S/UNI-ATLAS-3200 can copy RM cells to the Microprocessor Cell Interface.

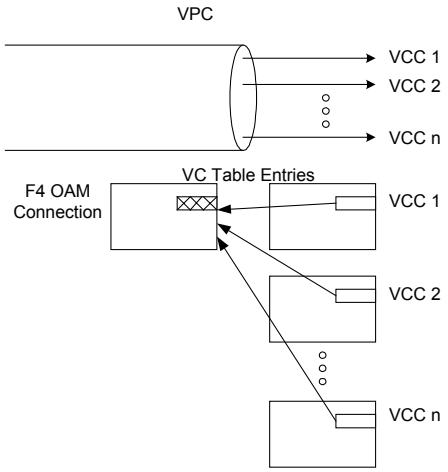
10.10 F4 to F5 OAM Processing

The S/UNI-ATLAS-3200 supports the termination of F4 (VPCs) to F5 (VCCs) while maintaining the F4 to F5 transmission of OAM cells. Each VCC of a VPC must be setup as a separate connection in the VC Table. An additional connection must be set up for the F4 OAM flow. The search table must be set up so that both Segment OAM cells (VCI=3) and End-to-End OAM cells (VCI=4) of the VPC resolve to this F4 OAM connection, but the VCI field in its VC Table must be set to all-zeroes to indicate that it is to be handled like an F4 connection. The F4 OAM connection may be set up as both a segment and end-to-end point, or as an end-to-end-point only. The VCC connections have a VPC Pointer [16:0] and a VPC Pointer Active bit in the Linkage Table. The pointer must be configured to point to the F4 OAM connection. Note that the two least significant bits of the VPC Pointer (i.e. the VCRA of the F4 OAM connection) must be different from the two LSBs of any of its associated VCC connections. Failure to adhere to this rule will result in all the VCC connections being treated as inactive until the problem is resolved. If the VPC pointer of a connection is not used, then the VPC Pointer Active bit must be set to logic 0. If a segment or end-to-end AIS alarm condition is indicated on the VPC connection, a background process ensures that VCC AIS cells will be transmitted on all VCCs associated with that VPC, while the VPC is in AIS alarm condition.

The Continuity Check process is also active at the F4 and F5 levels. When a user cell or CC cell is received on a VCC, the VPC connection is updated to ensure it does not enter the CC Alarm state.

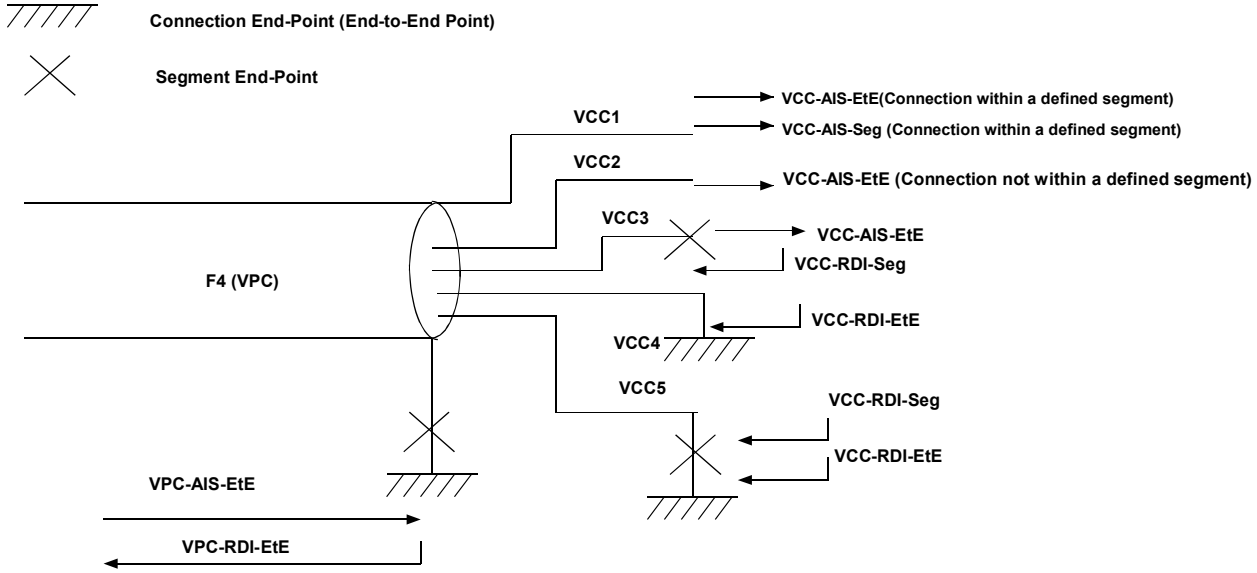
The figure below illustrates how the S/UNI-ATLAS-3200 supports OAM flows when terminating VPC connections. Note that each VCC connection has its VPC pointer pointing to the F4 OAM connection. The F4 OAM connection's VPC pointer active bit must be set to logic 0, and its VPC pointer field is not used.

Figure 14 F4 to F5 OAM Flows



The following F4 to F5 Fault Management scenarios are supported by the S/UNI-ATLAS-3200.

Figure 15 Termination of F4 Segment and End-to-End-Point Connection



In Figure 15 above, a VPC flow is being terminated. The VPC flow is both a segment end-point, and a connection (end-to-end) point. In the search table both the segment and end-to-end connections would resolve to a single F4 OAM connection. Five VCCs are being switched out from the VPC connection (all five VCCs would be setup as separate connections). In the event that an end-to-end VPC-AIS cell is received on end-to-end VPC connection, an end-to-end VPC-RDI cell would be generated (if the AUTO_RDI bit is logic 1 in the VC Table). The end-to-end VPC-RDI cell would carry the end-to-end AIS Defect Location and Defect Type fields. The response of the switched VCCs is as follows:

VCC1 belongs to a segment flow, therefore, both End-to-End and segment VCC-AIS cells are generated within 0.5 seconds of noticing that the end-to-end VPC connection is in AIS alarm. VCC1 will continue to generate ETE and segment VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e the AIS_end_to_end alarm bit is asserted for the end-to-end VPC connection).

VCC2 does not belong to a segment flow, therefore, an end-to-end VCC-AIS cell is generated within 0.5 seconds of noticing that the VPC connection is in end-to-end AIS alarm. VCC2 will continue to generate end-to-end VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e. the AIS_end_to_end alarm bit is asserted for the VPC connection).

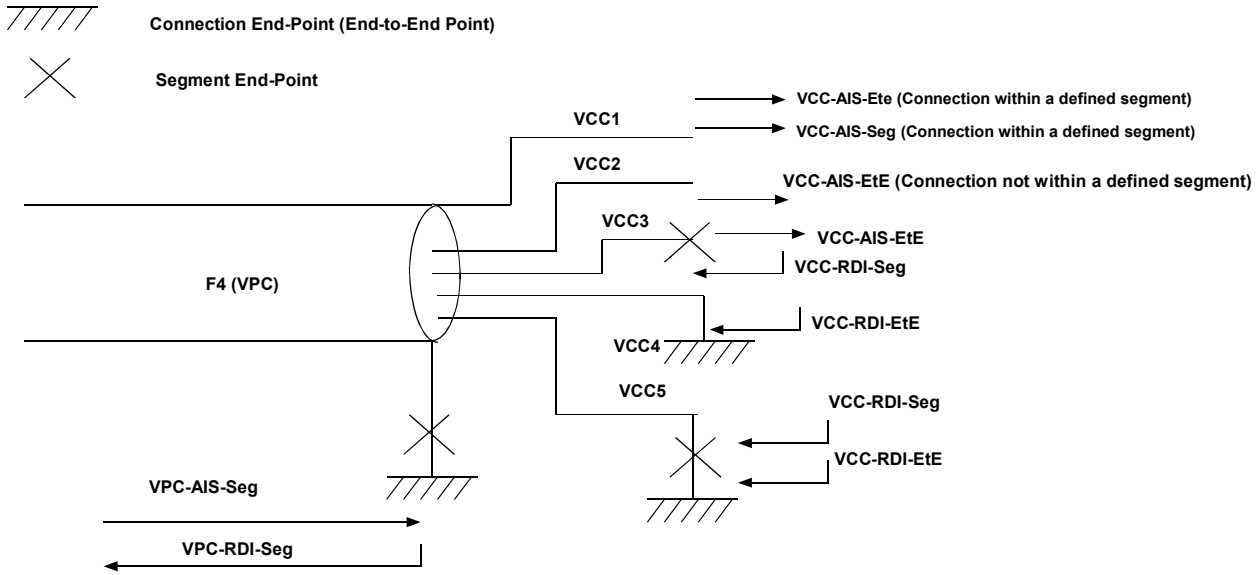
VCC3 is a segment end-point, therefore a segment VCC-RDI cell (assuming the AUTO_RDI bit is logic 1 in the VC Table) and an end-to-end VCC-AIS cell are generated for this connection within 0.5 seconds of noticing that the VPC connection is in end-to-end AIS alarm. VCC3 will continue to generate segment VCC-RDI and end-to-end VCC AIS cells at a rate of one per second (nominally) while the VPC connection is in end-to-end AIS alarm (i.e. the AIS_end_to_end alarm bit is asserted for the VPC connection).

VCC4 is a connection end-point, therefore an end-to-end VCC-RDI cell is generated (assuming the AUTO_RDI bit is logic 1 in the VC Table) within 0.5 seconds of noticing that the VPC connection is in end-to-end AIS alarm. VCC4 will continue to generate end-to-end VCC-RDI cells at a rate of one per second (nominally) while the VPC connection is in end-to-end AIS alarm (i.e the AIS_end_to_end alarm bit is asserted for the VPC connection).

VCC5 is a segment end-point and a connection end-point, therefore a segment VCC-RDI cell and an end-to-end VCC-RDI cell are generated (assuming the AUTO_RDI bit is logic 1 in the VC Table) within 0.5 seconds of noticing that the VPC connection is in end-to-end AIS alarm. VCC5 will continue to generate segment VCC-RDI and end-to-end VCC-RDI cells at a rate of one per second (nominally) while the VPC connection is in end-to-end AIS alarm (i.e. the AIS_end_to_end alarm bit is set).

The next scenario has the same connection configurations, however, a VPC-Segment AIS cell is received.

Figure 16 Termination of F4 Segment and End-to-End Point Connection



In Figure 16 above, a VPC flow is being terminated. The VPC flow is both a segment end-point, and a connection (end-to-end) point. In the S/UNI-ATLAS-3200 search table, both the segment and end-to-end connections would resolve to a single F4 OAM connection. Five VCCs are being switched out from the VPC connection (all five VCCs would be setup as separate connections). In this scenario, a segment VPC-AIS cell is received on the VPC connection. A segment VPC-RDI cell would be generated (if the AUTO_RDI bit is logic 1 in the VC Table) and sent to the Backwards Cell Interface. The segment VPC-RDI cell would carry the segment Defect Location and segment Defect Type information. The response of the switched VCCs is as follows:

VCC1 belongs to a segment flow, therefore, a both a segment and an end-to-end VCC-AIS cell are generated within 0.5 seconds of noticing that the VPC connection is in segment AIS alarm. VCC1 will continue to generate segment and ETE VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e the AIS_segment alarm bit is asserted for the VPC connection).

VCC2 does not belong to a segment flow, therefore, an end-to-end VCC-AIS cell is generated within 0.5 seconds of noticing that the VPC connection is in segment AIS alarm. VCC2 will continue to generate end-to-end VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e. the AIS_segment alarm bit is asserted for the VPC connection).

VCC3 is a segment end-point, therefore a segment VCC-RDI assuming the AUTO_RDI bit is logic 1 in the VC Table) and an end-to-end VCC-AIS cell are generated for this connection within 0.5 seconds of noticing that the VPC connection is in segment AIS alarm. VCC3 will continue to generate segment VCC-RDI and end-to-end VCC AIS cells at a rate of one per second (nominally) while the VPC connection is in segment AIS alarm (i.e. the AIS_segment_alarm bit is asserted for the VPC connection).

VCC4 is a connection end-point, therefore an end-to-end VCC-RDI cell is generated (assuming the AUTO_RDI bit is logic 1 in the VC Table) within 0.5 seconds of noticing that the VPC connection is in segment AIS alarm. VCC4 will continue to generate end-to-end VCC-RDI cells at a rate of one per second (nominally) while the VPC connection is in segment AIS alarm (i.e the AIS_segment alarm bit is asserted for the VPC connection).

VCC5 is a segment end-point and a connection end-point, therefore a segment VCC-RDI cell and an end-to-end VCC-RDI cell are generated (assuming the AUTO_RDI bit is logic 1 in the VC Table) within 0.5 seconds of noticing that the VPC connection is in segment AIS alarm. VCC5 will continue to generate segment VCC-RDI and end-to-end VCC-RDI cells at a rate of one per second (nominally) while the VPC connection is in segment AIS alarm (i.e. the AIS_segment_alarm bit is set).

Figure 17 Termination of F4 Segment End-Point Connection

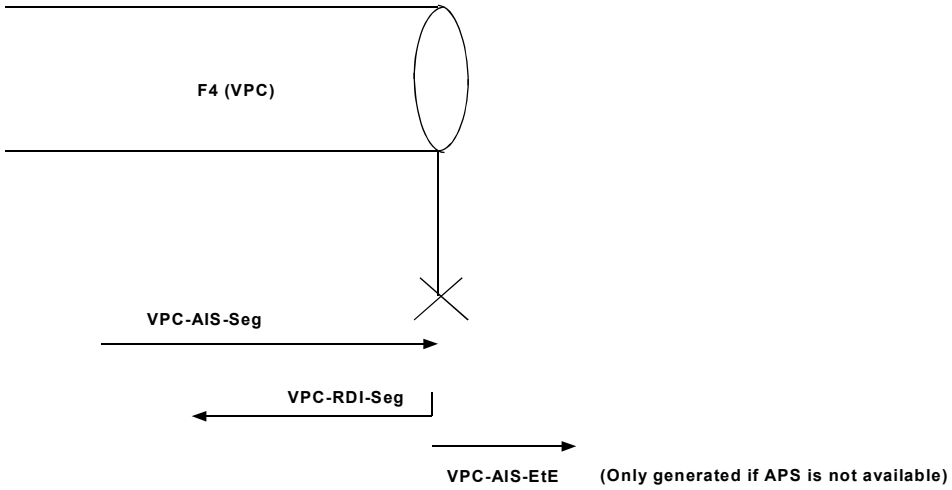


Figure 17 above illustrates the scenario where a VPC segment is being terminated at the S/UNI-ATLAS-3200. In this case, because only a segment end-point is defined, it is assumed that the VCCs are not switched out of the VPC (because the VPC end-to-end point is not provisioned). To enable this scenario, the VPC Pointer Active bit would be set to logic 0 in the Linkage Table entry, and the connection would be configured as a segment end-point. A segment VPC-AIS cell is received and terminated. Within 0.5 seconds of receiving the segment VPC-AIS cell, a segment VPC-RDI cell is generated (assuming the AUTO_RDI bit is logic 1 in the VC Table). As a programmable option, an end-to-end VPC-AIS can be generated if end-to-end AIS is not already being received. This per-PHY configurable option would normally only be enabled if APS is not available. The APSx register bit (where x is 0-47) determines whether or not PHYx has protection switching available. If the APSx register bit is logic 0, an end-to-end VPC-AIS cell will be generated within 0.5 seconds of entering the VPC Segment AIS alarm condition and once per second (nominally) thereafter until the VPC Segment AIS alarm condition is exited.

Figure 18 Termination of F4 End-to-End Point Connection

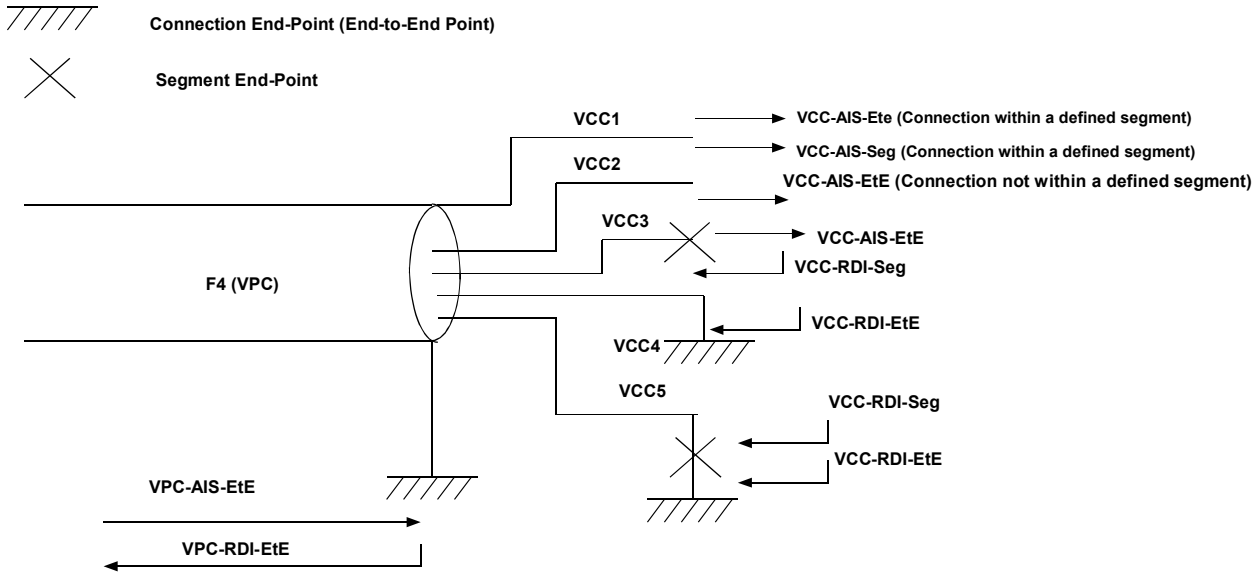


Figure 18 above illustrates the scenario where a VPC is being terminated at an end-to-end point at the S/UNI-ATLAS-3200. In this scenario, the VPC connection is configured as an end-to-end point and has its VPC Pointer Active bit set to logic 0. If an end-to-end VPC-AIS cell is received, it is terminated and an end-to-end VPC RDI cell is generated within 0.5 seconds (assuming the AUTO_RDI bit is logic 1 in the VC Table). The response of the switched VCCs is as follows:

VCC1 is belongs to a segment flow, therefore both segment and ETE VCC-AIS cells are generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm, and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC2 belongs to an end-to-end flow, therefore an end-to-end VCC-AIS cell is generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm, and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC3 is a segment end-point, therefore a segment VCC-RDI cell and an end-to-end VCC-AIS cell are generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm (assuming the AUTO_RDI bit is logic 1 in the VC Table), and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC4 is an end-to-end point, therefore an end-to-end VCC-RDI cell is generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm (assuming the AUTO_RDI bit is logic 1 in the VC Table), and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC5 is a segment end-point and an end-to-end point, therefore, a segment VCC-RDI and an end-to-end VCC-RDI cell are generated within 0.5 seconds of noticing that the VPC connection is in AIS (assuming the AUTO_RDI bit is logic 1 in the VC Table), and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

Note, in the unlikely event that a segment VPC-AIS cell is received on the end-to-end VPC connection, no action would be taken at the F5 level. This is because the VPC connection is only configured as an end-to-end point and no segment OAM cells should be received. The end-to-end VPC connection would only terminate the segment VPC-AIS cell and no further action would be taken at the F4 level.

The table below summarizes the behavior of the S/UNI-ATLAS-3200 for F4 to F5 Fault Management:

Table 28 F4 to F5 Fault Management Processing

Actions taken by S/UNI-ATLAS-3200 upon receipt of F4 AIS cells		VC Connection End-Point	VC Segment End-Point	VC Connection End-Point and Segment End-Point	VC Non End-Point	
VP Termination Type	Received Cell at F4 level				Within a VC Segment	Not within a VC Segment
VP Connection End-Point and Segment End-Point	VP End-to-End AIS	Generate VC End-to-End RDI **(4)**	Generate VC Segment RDI **(1), (4)** Generate VC End-to-End AIS **(2), (4)**	Generate VC End-to-End RDI **(4)** Generate VC Segment RDI (1), (4)	Generate VC Segment AIS **(3), (4)** Generate VC End-to-End AIS (4)	Generate VC End-to-End AIS **(4)**
		Generate VP End-to-End RDI cell on the End-to-End F4 connection.				
	VP Segment AIS	Generate VC End-to-End RDI **(5), (4)**	Generate VC Segment RDI **(4)** Generate VC End-to-End AIS (4), (6)	Generate VC End-to-End RDI **(4) (5)** Generate VC Segment RDI **(4)**	Generate VC Segment AIS **(3), (4)** Generate VC End-to-End AIS (4), (6)	Generate VC End-to-End AIS **(4), (6)**
		Generate VP Segment RDI cell on the Segment F4 connection.				
VP Connection End-Point Only	VP End-to-End AIS	Generate VC End-to-End RDI **(4)**	Generate VC Segment RDI **(1), (4)** Generate VC End-to-End AIS (2), (4)	Generate VC End-to-End RDI **(4)** Generate VC Segment RDI (1), (4)	Generate VC Segment AIS **(3), (4)** Generate VC End-to-End AIS (4)	Generate VC End-to-End AIS **(4)**
		Generate VP End-to-End RDI cell on the End-to-End F4 connection.				
	VP Segment AIS	No action is taken.	No action is taken.	No action is taken.	No action is taken.	No action is taken.
		No action is taken. This represents an unusual case where an F4 segment AIS cell is received on a F4 connection end-point. The segment AIS cell will be terminated at the VP connection end-point, but no other action is taken.				

VP Segment End-Point only	VP End-to-End AIS	No cells are generated. The VP End-to-End AIS cell is passed through. We are assuming that VCs are not switched if the F4 is a Segment End-Point only.
	VP Segment AIS	Generate VPC Segment RDI. Generate VPC End-to-End AIS cell if APS is not available (and end-to-end VP-AIS cells are not being received).
VP non-end point	VP End-to-End AIS	No cells are generated. The received cells are passed through transparently. We are asssuming that, if a VP connection is a non-end point, then any VCCs pointing to that connection are being aggregated into it rather than switched out.
	VP Segment AIS	

This feature is controlled by the F4EAISF5SRDI register bit. When this bit is logic 1, a segment VC-RDI cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point, and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, a segment VC-RDI cell will not be generated in this circumstance.

This feature is controlled by the F4EAISF5EAIS register bit. When this bit is logic 1, an end-to-end VC-AIS cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point, and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, an end-to-end VC-AIS cell will not be generated in this circumstance.

This feature is controlled by the SegmentFlow bit in the Table OAM Configuration field of the VC Table. If this bit is logic 1, the VCC is considered to be part of a segment flow, and a segment VC-AIS cell will be generated when an end-to-end VP-AIS cell is terminated at a VPC end-to-end point.

This feature is controlled by the F4toF5OAM bit in the OAM Configuration field of the VC Table. If this bit is logic 1, the F4 to F5 Fault Management scenarios are enabled. If this bit is logic 0, no F5 Fault Management cells will be generated as a result of the reception of F4 Fault Management cells. However, the Continuity Check process will still be active on the F4 and F5 levels if the VPC Pointer fields are correctly setup.

This feature is controlled by the F4SAISF5ERDI register bit. When this bit is 1, an end-to-end VC-RDI cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point, and the VCC is also an end-to-end point. If this bit is logic 0, an end-to-end VC-RDI cell will not be generated in this circumstance.

This feature is controlled by the F4SAISF5EAIS register bit. When this bit is logic 1, an end-to-end VC-AIS cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point. Note, the VCC connection is not part of a segment flow (SegmentFlow=0). If this bit is logic 0, an end-to-end VC-AIS cell will not be generated in this circumstance.

This feature is controlled on a per-PHY basis by the APSx register bit (where x is from 0-47). When the APSx register bit is logic 0, it indicates there is no automatic protection switching on PHY x . When a VPC connection is configured as a segment end-point only and a segment VPC-AIS cell is received, an end-to-end VPC-AIS cell is generated immediately, and once per second (nominally) thereafter. When the APSx register bit is logic 1, an end-to-end VPC-AIS cell is not generated in this circumstance. No end-to-end AIS will be generated if the connection is already receiving end-to-end AIS.

When an AIS or RDI cell is generated due to CC_AIS_RDI, per-PHY RDI, Send_RDI/AIS_End_to_end, or Send_RDI/AIS_Segment, the AIS/RDI will contain the defect type programmed into the OAM Configuration field of the VC table, and the local defect location programmed in the Defect Location register.

When an AIS or RDI is generated due to reception of an AIS cell, the generated cell will contain the AIS Defect Location and AIS Defect Type fields which are stored in the VC Table of the connection which received the AIS. For instance, an F5 Ete RDI generated as the result of receiving an F4 Segment AIS would use the segment defect location and type stored for the F4 connection.

If an F4 connection enters the AIS alarm condition (segment or end-to-end), the associated F5 connections will not declare AIS themselves (i.e. the AIS_end_to_end alarm and/or the AIS_segment alarm bit will not be asserted on the F5 connection). The F5 connections will, however, most likely be in the CC_alarm condition (both segment and end-to-end), because any cell that would clear the CC alarm in the F5 connections would also clear AIS alarm in the F4.

10.11 F5 to F4 OAM Processing

The S/UNI-ATLAS-3200 also supports the aggregation of F5 connections into F4 connections. The VCs must be set up in much the same way, with one VC for each VCC, and another VC for the F4 OAM connection. However, the OAM connection will not be an end point, and the only OAM functions performed by the F4 are the sourcing of end-to-end and segment CC cells. The F4 OAM connection must still have a valid search onto which cells with VCI = 3 or VCI=4 terminate, as Loopback, RDI, and Bwd PM cells from the BCIF must search correctly onto the connection (if Search_From_BCIF is logic 1).

The F4 Continuity Check process in the aggregated F4 is aware of OAM and other cells generated on the component F5 flows, and correctly counts them as user cells.

F4 Forward PM flows may be generated by associating many F5 connections with a single F4 Forward PM session. This PM connection will treat all F5 cells (other than, optionally, RM cells) as F4 user cells and will include them in the generated PM counts.

10.12 Constraints on F5 and F4 VC Table Record Addresses

The VC Table Record address is a 16 bit number identifying an F5 or F4 flow. This number corresponds to a data structure in the internal DRAM.

Each VC Table record is stored in one of the 4 banks in the internal DRAM. The bank in which a record is stored is identified by the least significant two bits of the VC record. Thus each record is stored in either bank 0 (VCRA[15:0] = xxxxxxxxxxxxxx00), bank 1 (VCRA = xxxxxxxxxxxxxx01), bank 2 (VCRA[15:0] = xxxxxxxxxxxxxx10) or bank 3 (VCRA = xxxxxxxxxxxxxx11).

It is required that the records of an F5 flow and its enclosing F4 flow be in different banks. The constituent F5s need not be in the same bank, so long as they are not in the same bank as the F4 connection. If this rule is violated, then all the constituent F5s will be treated as inactive connections. If the InactiveToUP bit is logic 1 in the Cell Processor Routing Configuration Register, then cells will be routed to the microprocessor, permitting this condition to be detected and corrected.

10.13 Background Processes

The S/UNI-ATLAS-3200 performs numerous background processes to perform correct and compliant OAM-Fault Management cell generation, and alarm monitoring as well as maintaining the per-connection and per-PHY TAT policing parameters. The background processes are triggered either by the internally generated 0.5 second clock event, or by the external 0.5 second clock input pin.

Each Cell Processor maintains 4 background processes. They are:

- RDI cell generation.
- AIS/CC cell generation.
- TAT updating.
- CC, RDI and AIS Change of State and alarm monitoring.

The VC Table Maximum Index register controls the maximum 17-bit VC Table address which must be monitored by the various background processes.

The RDI cell generation process is controlled by the status of the Backward Cell Interface to which the process must send generated RDI cells. If this FIFO is filled, no RDI cells will be generated, and the RDI background process will pause until room becomes available. This ensures that no RDI cells will be lost due to overflow of the Backward Cell Interface.

The AIS/CC cell generation process is controlled by the status of the Output Cell Interface, and by a programmable threshold that determines the maximum rate at which AIS/CC cells can be generated. If an AIS or CC cell is generated, the process will be suspended until the expiry of a user programmable counter threshold. However, AIS cells will only be generated on PHYs that have room in the Output Cell Interface to take them. Connections which, after a timeout period, still cannot insert an AIS cell due to a full Output Cell Interface queue will be skipped, to ensure that other connections are not denied the ability to send AIS cells. If a PHY has cells destined for it, but its Output Cell Interface FIFO is full, and the PHY does not accept any cells whatsoever for a programmable number of cell periods (the Inoperative PHY Declaration Period register, which defaults to 256 cell periods) then the PHY will be declared inoperative, an optional interrupt will be asserted, and any subsequent generated cells destined for that PHY (CC, AIS, RDI, Loopback, Bwd PM and Fwd PM) will be immediately discarded to prevent them from slowing the generation of cells to the remaining PHYs. The PHY queue will be declared operative again as soon as it accepts a single cell from S/UNI-ATLAS-3200.

The TAT updating process ensures the policing theoretical-arrival-times track the free running time-of-arrival counter of the ATLAS.-3200 This ensures that connections which have a long gap between inter-cell arrivals are never mistakenly policed due to a roll over of the free running time-of-arrival counter.

The CC, RDI and AIS change of state and alarm monitoring process is controlled by the fill status of the Change of State FIFO. If the change of state FIFO is not used, then this process is not throttled by the FIFO fill status. If the FIFO is used, then notification of changes of state in CC, RDI and AIS alarms will be suspended until the FIFO is not full. This ensures the management software never misses any change of connection status. The Excessive Policing Status bit is also part of the Change of State FIFO. **It is the responsibility of the management software to ensure the FIFO is read often enough so that the alarm declarations remain compliant with Bellcore GR-1248-CORE and ITU-T I.610.**

Background processes have scheduled processing time available for execution regardless of the cell data rate.

10.14 Performance Management

10.14.1 Performance Management Flows

The S/UNI-ATLAS-3200 supports a highly configurable internal PM statistics RAM. The VC Linkage Table is used to index two internal PM RAM locations. Each pointer can access up to 256 unique PM RAM locations. These two pointers can be used to perform simultaneous sinking and sourcing of a PM flow, simultaneous F4 and F5 PM flows, etc. The PM pointers are located in the VC Linkage Table in external SRAM, and the fields are as follows:

Table 29 Linkage Table Fields Used in PM

63												0
1	PHYID (6)	2	Reserved (16)	PM 2 Active (1)	1	PM 2 Address (8)	PM 1 Active (1)	1	PM 1 Address (8)	VPC Pointer Active (1)	2	VPC Pointer (16)

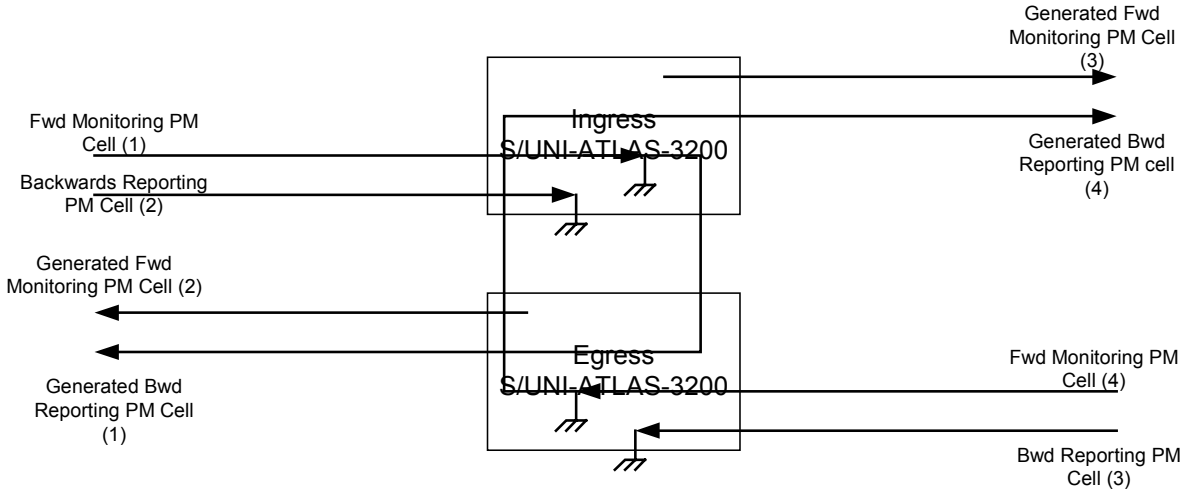
Table 30 PM Activation Fields

Name	Description
PM Active2	Indicates the PM session pointed to by PM Addr2[7:0] is active.
PM Active1	Indicates the PM session pointed to by PM Addr1[7:0] is active.
PM Addr2[7:0]	Indicates which internal PM RAM Address in Bank 2 is to be used for a PM session. Bank 1 and Bank 2 are completely separate. Many connections may point to the same PM session; for instance, if an VPC was being split out to its component VCCs, each VCC table entry, as well as the F4 OAM table entry, might point to a single F4 PM Sink session. The same strategy would work for the aggregation of VCCs into a VPC.
PM Addr1[7:0]	Indicates which internal PM RAM Address in Bank 1 is to be used for a PM session. Bank 1 and Bank 2 are completely separate. Many connections may point to the same PM session; for instance, if an VPC was being split out to its component VCCs, each VCC table entry, as well as the F4 OAM table entry, might point to a single F4 PM Sink session. The same strategy would work for the aggregation of VCCs into a VPC.

These PM connections may be configured to be sinks, sources or monitoring points of F4 or F5 segment or end-to-end PM flows.

The figure below illustrates the PM flow capability of the S/UNI-ATLAS-3200.

Figure 19 PM Flows



The figure above illustrates two unique bi-directional PM flows. In the first PM flow, indicated by (1), the Ingress S/UNI-ATLAS-3200 is terminating a Forward Monitoring PM cell and it generates a Backward Reporting PM cell through the Backward Cell Interface and the Egress S/UNI-ATLAS-3200 . This is one half of the bi-directional PM flow. The second half of the bi-directional flow is indicated by (2). Here, the Egress S/UNI-ATLAS-3200 is generating a Forward Monitoring PM cell . Another downstream entity (e.g. another ATLAS device) would terminate that Forward Monitoring cell and transmit a Backward Reporting PM cell. This Backward Reporting PM cell is received at the Ingress S/UNI-ATLAS-3200 and terminated. To enable this PM session, the termination of the Forward Monitoring PM cell (1) and the statistics collected from the termination of the Backwards Reporting PM cell (2) would be maintained by the Ingress S/UNI-ATLAS-3200 Processor in one RAM location. The generation of the Forward Monitoring PM cell (2) would be maintained by the Egress S/UNI-ATLAS-3200 in one RAM location.

The tags (3) and (4) indicate the second bi-directional PM flow. At the Ingress S/UNI-ATLAS-3200, the Cell Processor generates a Forward Monitoring Cell that is transmitted to the Output Cell Interface (and into the Switch Fabric). A downstream device (e.g. another ATLAS device) would terminate the Forward Monitoring PM cell and generate a Backward Reporting PM cell. This Backward Reporting PM cell is received at the Egress S/UNI-ATLAS-3200 and terminated in its Cell Processor. This is the first half of the bi-directional flow, indicated by (3). The second half of the bi-directional flow is indicated by (4). Here, the Egress S/UNI-ATLAS-3200 terminates a Forward Monitoring PM cell. The Egress S/UNI-ATLAS-3200 then generates a corresponding Backward Reporting PM cell which is transmitted to the Ingress S/UNI-ATLAS-3200 through the Backward Cell Interface and back into the switch core. The generation of the Forward Monitoring PM cell (4) would be maintained by the Ingress S/UNI-ATLAS-3200 in one RAM location. The termination of the Forward Monitoring PM cell (4) and the statistics collected from the termination of the Backwards Reporting PM cell (3) would be maintained by the Egress S/UNI-ATLAS-3200 in one RAM location.

The above discussion is just one example of the PM Flow capability of the S/UNI-ATLAS-3200. Each of the PM flows can be configured as a monitoring point in which PM cells are neither generated nor terminated (note, however, PM cells will be terminated at OAM flow end points), but merely monitored and their statistics maintained. The S/UNI-ATLAS-3200 can also be configured to monitor/sink/source an F4 PM flow. Each F5 connection that is a member of an F4 VPC flow must have one common PM Address for the F4 flow. All user cells (at the F4 level) will be considered to be part of the F4 PM flow, and thus counted as such.

A pair of S/UNI-ATLAS-3200s can also be configured to perform bi-directional PM on a segment connection and an end-to-end connection (simultaneously) for up to 256 bidirectional connections simultaneously. For each connection in each S/UNI-ATLAS-3200, one PM address in the VC Linkage Table would be used to point to the PM RAM location for the end-to-end PM flow, and the other address would be used to point to the PM RAM location for the segment PM flow. The Backwards Cell Interfaces of the two devices permit Backwards PM cells to be inserted into the opposite direction.

The insertion of Forward Monitoring PM Cells is controlled by the Paced Forward PM Cell Generation registers. These registers provide a counter to set the number of cell intervals (defined as 22 SYSCLK clock cycles) between successive Forward Monitoring PM cells. This prevents the S/UNI-ATLAS-3200 from generating Forward Monitoring PM cells back-to-back. Each time a Forward Monitoring PM cell is generated, a counter is loaded with the value set in the Paced Fwd PM Cell Generation register, and that register is decremented at intervals of 32 clock cycles. Another Forward Monitoring cell will not be generated until the counter reaches 0.

The position of the UPC/NPC policing needs to be clearly defined. If the S/UNI-ATLAS-3200 is a sink of Forward Monitoring PM cells, or a monitoring point, the counts maintained in the PM RAM represent the state of the device **before** the UPC/NPC function. If the S/UNI-ATLAS-3200 is a source of Forward Monitoring PM cells, the counts maintained in the PM RAM represent the state of the device **after** the UPC/NPC function.

10.14.2 Performance Management Record Table

The OAM-PM statistics are collected in an on-chip RAM accessible through the microprocessor port.

Table 31 Performance Management Record Table

PM Addr [2:0]	79											0
000	PM Configuration & Status (16)		BIP-16 (16)		Current Count CLP0 (16)		Current Count CLP0+1 (16)		BLER stored (8)	Fwd BMCSN (8)		
001	Fwd TRCC0 (16)		Fwd TRCC0+1 (16)		Fwd TUC0 (16)		Fwd TUC0+1 (16)		Fwd FMCSN (8)	Unused (8)		
010	Bwd TRCC0 (16)		Bwd TRCC0+1 (16)		Bwd TUC0 (16)		Bwd TUC0+1 (16)		Bwd FMCSN (8)	Bwd BMCSN (8)		
011	Fwd Errors (8)	Fwd Impaired (8)	Fwd Lost/Mis Impaired (8)	Fwd SECB Errored (8)	Fwd SECB Lost (8)	Fwd SECB Misins (8)	Fwd SECBC (8)	Fwd Lost Fwd PM Cells (8)	Fwd Tagged CLP0 (16)			
100	Fwd Misinserted (16)		Fwd Lost CLP0 (16)		Fwd Lost CLP0+1 (16)		Fwd Total Lost CLP0 (16)		Fwd Total Lost CLP0+1 (16)			
101	Bwd Errors (8)	Bwd Impaired (8)	Bwd Lost/Mis Impaired (8)	Bwd SECB Errored (8)	Bwd SECB Lost (8)	Bwd SECB Misins (8)	Bwd SECBC (8)	Bwd SECBC Accum. (8)	Bwd Tagged CLP0 (16)			
110	Bwd Misinserted (16)		Bwd Lost CLP0 (16)		Bwd Lost CLP0+1 (16)		Bwd Total Lost CLP0 (16)		Bwd Total Lost CLP0+1 (16)			
111	Transmitted CLP0 Count (32)				Transmitted CLP0+1 Count (32)				Bwd Lost Fwd PM Cells (8)	Bwd Lost Bwd PM Cells (8)		

The Configuration Field of the internal PM Table is shown below:

Table 32 PM Table Configuration Field

Bit	Name	Description
15	Source_FwdPM	If this bit is a logic 1, the PM session is configured to source a PM flow, and a Forward Monitoring cell is output from the S/UNI-ATLAS-3200 once per block of user cells (nominally). Received Forward Monitoring and Backwards Reporting cells will not be processed by this PM session. If the session is an F4 session, then any generated F5 Fwd PM cells, AIS cells, or CC cells will be included in the user cell flow. If the Source_FwdPM bit is a logic 0, then the PM session is configured to process received Forward Monitoring and Backwards Reporting cells. Termination of PM cells depends only on whether the S/UNI-ATLAS-3200 is configured as an end-to-end or segment end point.
14	Generate_BwdPM	If this bit is a logic 1 and the Source_FwdPM bit is a logic 0, a Backward Reporting PM cell is generated when an appropriate Forward Monitoring PM cell is received. The F4_F5B and ETE_SegB bits determine the type of Forward Monitoring cells that are processed, and thus the type of Backward Reporting cell that is generated. If the Fwd_PM0 bit is a logic 1, then a Backward Reporting cell will not be generated (the Fwd_PM0 bit is cleared upon receipt of the first Forward Monitoring PM cell).
13	F4_F5B	If this bit is a logic 1, this PM address is for a F4 (VPC) PM flow. F5 cells, including OAM cells, are user cells as far as this flow is concerned. If this bit is a logic 0, the PM address is for a F5 (VCC) PM flow. F4 OAM cells are ignored.
12	ETE_SegB	If this bit is a logic 1, this PM address is for an end-to-end PM flow. Segment PM cells are ignored. If this bit is a logic 0, this PM address is for a segment PM flow. End-to-end PM cells are ignored. Despite the setting of this bit, F5 OAM cells are treated as user cells if the F4_F5B bit is logic 1.
11	Force_FwdPM	This bit controls the forced insertion of a Forward Monitoring PM cell when the S/UNI-ATLAS-3200 is configured to insert Forward Monitoring PM cells. When the Force_FwdPM bit is logic 1, the S/UNI-ATLAS-3200 will force the insertion of a Forward Monitoring PM cell when the current cell count of CLP0+1 cells reaches N+N/2, where N is the programmed block size, regardless of the state of the Forward PM Pacing register. If this bit is logic 0, then the S/UNI-ATLAS-3200 will not insert a Forward Monitoring PM cell unless the Forward PM Pacing register allows for a PM cell to be inserted. This bit has no effect when Source_FwdPM is logic 0.
[10:9]	Threshold_Select[1:0]	These bits are used to index one of four possible threshold selection register pairs (PM Threshold A1/A2 through PM Threshold D1/D2) which hold the threshold values for Errored, Misinserted and Lost Severely Errored Cell Blocks.

Bit	Name	Description
[8:5]	Blocksize[3:0]	The block size of PM cells selects the nominal block of user cells as follows: 0000 128 cells 0001 256 cells 0010 512 cells 0011 1024 cells 0100 2048 cells 0101 4096 cells 0110 8192 cells 0111 16384 cells 1000 32768 cells 1001-1111 Reserved.
4	CLP0_SECBs_Only	When this bit is a logic 1, then SECBs will not be declared due to lost cells whose CLP = 1. This setting may be used to accommodate connections on which there is no service guaranteee for CLP = 1 cells.
3	PM_Rollover_FIFO_EN	If this bit is logic 0, none of the PM counts will generate entries into the Count Rollover FIFO. If this bit is logic 1 then the Performance Monitoring counts will generate entries into the Count Rollover FIFO. Counts that are designed to roll over in normal operation (the contents of rows 0,1, and 2, plus the SECBC counts) do not generate Count Rollover FIFO entries. A bit in the Cell Processor Configuration Register (Sat_Fast_PM_Counts) controls whether the four counts that can increment very quickly (BIP16 errors, and the counts of Lost PM cells) are excluded from generating Count Rollover FIFO entries. When a counter is enabled for making entries into the CRO FIFO it will do so whenever its MSB becomes logic 1, and it will then reset the MSB to logic 0. If the Count Rollover FIFO is full, the MSB will remain set until such time as it can make an entry in the FIFO. The counts continue counting until they saturate.
2	Reserved	This bit is used for internal purposes, and must be programmed to logic 0 at startup, and must not be altered by the microprocessor thereafter, for proper operation.
1	Fwd_PM0	If Source_FwdPM is a logic 0, the Fwd_PM0 bit must be set to a logic 1 initially. This bit is cleared upon receiving the first Forward Monitoring cell, along with the current cell count, BIP-16, and the entire contents of rows 3 and 4. The Fwd_PM0 bit is used to denote the arrival of the first Forward Monitoring cell. The Fwd_PM0 bit suppresses accumulation of the Forward error counts. If this bit is not set, error counts will be accumulated. If Source_FwdPM is a logic 1, then if this bit is set to a logic 1 initially, rows 1 and 7 will be cleared at the end of the first block of user cells. Initializing Row 0 is the responsibility of the management software during setup.
0	Bwd_PM0	The Bwd_PM0 bit must be set to a logic 1 initially. This bit is cleared upon receiving the first Backward Reporting cell. At that time, the contents of rows 5, 6, and 7 are cleared (except for the Bwd SECBC count which is copied from the Backward Reporting cell) and Row 2 is initialized with values copied from the Backward Reporting cell.

The QOS parameters of the internal PM table are described below. N.B. TUCD0 and TUCD0+1 (which are referred to in this table) are internally computed values in accordance with Bellcore GR-1248-CORE, ITU-T I.610 and ITU-T I.356. TUCD is the difference between the number of cells transmitted in the block (as indicated in the fwd PM cell) and the number received. For example, TUCD0 =
{[TUC0(t) – TUC0(t-1)] Mod 64K} - {[TRCC0(t) – TRCC0(t-1)] Mod 64K}.

Table 33 QOS Parameters for Performance Management

Name	Description
BIP16 (16)	When this PM instance is the source of forward monitoring cells, the Bit-Interleaved Parity 16 is the even parity error detection code computed over the information field of the block of user data cells (CLP0+1) transmitted after the last Forward Monitoring PM cell. When this PM instance terminates or monitors Forward Monitoring cells, BIP-16 is the even parity error detection code computed over the information field of user data cells received after the last Forward Monitoring PM cell.
Current Cell Count CLP0 (16)	When this PM process is the source of Forward Monitoring cells, this count is incremented each time a CLP0 user cell is transmitted. It is used along with the Fwd TUC_0 field to determine the TUC_0 field of newly generated Forward PM cells. When this PM process terminates/monitors Forward Monitoring cells, this count is incremented each time a CLP0 user cell is received. It is used along with Fwd TRCC_0 to determine the new TRCC_0 upon reception of a Forward PM cell, and thus to calculate the Total User Cell Difference CLP0.
Current Cell Count CLP0+1 (16)	When this PM process is the source of Forward Monitoring cells, this count is incremented each time a user cell is transmitted. Whenever this count equals or exceeds the programmed PM block size, a request to generate a Forward PM cell will be made, subject to cell slot availability and pacing. It is also used along with the Fwd TUC_0+1 field to determine the TUC_0+1 field of newly generated Forward PM cells. When this PM process terminates/monitors Forward Monitoring cells, this count is incremented each time a user cell is received. It is used along with Fwd TRCC_0+1 to determine the new TRCC_0+1 upon reception of a Forward PM cell, and thus to calculate the Total User Cell Difference CLP0+1.
BLER Stored (8)	The Stored Block Error Result is the Block Error Result calculated on reception of the previous Forward PM cell. It is stored in this field until it can be used by the generated Backwards Reporting cell.
Fwd TRCC_0 (16)	Total Received Cell Count CLP0. This field is used when terminating/ monitoring Forward PM cells, and stores a running count modulo 65536 of the total number of received CLP0 user cells previous to the most recent Forward Monitoring cell. Fwd TRCC_0 is inserted in the TRCC_0 field of the generated Backwards Reporting cell. It is also used along with the Current Cell Count CLP0 to determine the new TRCC_0 upon reception of a Forward PM cell.
Fwd TRCC_0+1 (16)	Total Received Cell Count CLP0+1. This field is used when terminating/ monitoring Forward PM cells, and stores a running count modulo 65536 of the total number of received user cells previous to the most recent Forward Monitoring cell. Fwd TRCC_0+1 is inserted in the TRCC_0+1 field of the generated Backwards Reporting cell. It is also used along with the Current Cell Count CLP0+1 to determine the new TRCC_0+1 upon reception of a Forward PM cell.

Name	Description
Fwd TUC_0 (16)	Total CLP0 User Cells for Forward Monitoring PM Cells. TUC_0 indicates the number modulo 65536 of CLP 0 user cells transmitted just before the transmission of a Forward PM cell. If this PM process is the source of Forward PM cells then this field stores the value of TUC_0 inserted into the most recent generated Forward PM Cell, and is used together with the Current Cell Count CLP0 to determine TUC_0 of the subsequent generated PM cell. This is a running count and does not need to be initialized. If this PM process terminates/monitors Forward PM cells, then this field stores the value of TUC_0 received from the most recent Forward PM cell, and is used with the received PM cell's TUC_0 to determine the number of CLP0 user cells transmitted between successive Forward PM cells. This count will be initialized automatically on reception of the first Forward Monitoring cell. When not a monitor point, Fwd TUC_0 will be inserted in the TUC_0 field of generated Backwards Reporting cells.
Fwd TUC_0+1 (16)	Total CLP0+1 User Cells. TUC_0+1 indicates the total number modulo 65536 of CLP0 and CLP1 user cells transmitted just before the transmission of a Forward PM cell. If this PM process is the source of Forward PM cells then this field stores the value of TUC_0+1 inserted into the most recent generated Forward PM Cell, and is used together with the Current Cell Count CLP0+1 to determine TUC_0+1 of the subsequent generated PM cell. This is a running count and does not need to be initialized. If this PM process terminates/monitors Forward PM cells, then this field stores the value of TUC_0+1 received from the most recent Forward PM cell, and is used with the received PM cell's TUC_0+1 to determine the number of user cells transmitted between successive Forward PM cells. This count will be initialized automatically on reception of the first Forward Monitoring cell. When not a monitor point, Fwd TUC_0+1 will be inserted in the TUC_0+1 field of generated Backwards Reporting cells.
Fwd FMCSN	The Forward PM Cell Sequence Number. This field contains the sequence number modulo 256 of the most recent Forward Monitoring cell generated/received. The MCSN is incremented for each PM cell generated/received during the PM session. When Forward PM cells are terminated or monitored, the Fwd MCSN is used to identify lost Forward PM cells. If the Fwd FMCSN is out of sequence, then BIP-16 calculations are not done, the Bit Error Code is sent as all-ones in the Backwards Reporting cell, and the Fwd Lost Fwd PM Cells counter is incremented by the number of lost Fwd PM cells. The calculation and reporting of lost, misinserted, and tagged cells, impaired blocks, and SECBs proceeds as normal. Any inference of SECBs due to lost Fwd PM cells is left up to the management software.
Fwd BMCSN	The Forward Bwd PM Monitoring Cell Sequence Number is used to determine the MCSN for generated Backwards Reporting cells. The Fwd BMCSN value is incremented each time a Backwards Routing cell is generated. There is no need to initialize this running count.
Bwd TRCC_0 (16)	Total Received Cell Count CLP0 for Backwards Reporting cells. This field stores the TRCC_0 value received from the most recent Backwards Reporting cell, and is used along with the TRCC_0 field of newly received Backwards reporting cells to determine the number of CLP0 user cells received by the far end point between successive Forwards Monitoring cells. This count will be initialized automatically on reception of the first Bwd PM cell.

Name	Description
Bwd TRCC_0+1 (16)	Total Received CLP0+1 User Cell Count for Backwards Reporting cells. This field stores the TRCC_0+1 value received from the most recent Backwards Reporting cell, and is used along with the TRCC_0+1 field of newly received Backwards reporting cells to determine the number of user cells received by the far end point between successive Forwards Monitoring cells. This count will be initialized automatically on reception of the first Bwd PM cell.
Bwd TUC_0 (16)	Total CLP0 User Cell Count for Backwards Reporting PM Cells. This field stores the value of TUC_0 received from the most recent Backwards Reporting cell, and is used with a newly received Bwd PM cell's TUC_0 to determine the number of cells transmitted by the Forward Monitoring source point between successive Forward PM cells. This count will be initialized automatically on reception of the first Bwd PM cell.
Bwd TUC_0+1 (16)	Total CLP0+1 User Cell Count for Backwards Reporting PM Cells. This field stores the value of TUC_0+1 received from the most recent Backwards Reporting cell, and is used with a newly received Bwd PM cell's TUC_0+1 to determine the number of cells transmitted by the Forward Monitoring source point between successive Forward PM cells. This count will be initialized automatically on reception of the first Bwd PM cell.
Bwd FMCSN (8)	This field contains the Fwd MCSN copied from the most recently received Backwards Reporting cell. It is used to infer the loss of Forward Monitoring cells at the far end point. If the Bwd FMCSN is out of sequence, then the Bwd Lost Fwd PM Cells count is incremented by the number of lost Fwd PM cells, which is presumed to be equal to the change in FMCSN less the change in BMCSN. Any inference of SECBs due to lost Fwd PM cells is left up to the management software.
Bwd BMCSN (8)	This field contains the MCSN copied from the most recently received Backwards Reporting cell. It is used to infer the loss of Backwards Reporting cells. If the received Backwards Reporting MCSN is out of sequence, then the Bwd Lost Bwd PM Cells Count will be incremented by the number of missed MCSNs. All other processing will proceed as normal.
Fwd Errored Cell Count (8) Bwd Errored Cell Count (8)	The Errored Cell Count represents the number of BIP-16 violations (BIPV) during a PM session (on CLP0+1 cells). The Errored Cell counter is incremented whenever the number of BIPV is greater than 0 and less than MERROR in the selected threshold register, so long as there are no lost or misinserted cells, and the MCSNs are in sequence.
Fwd Impaired Blocks (8) Bwd Impaired Blocks (8)	The Impaired Block count represents the sum of PM cell blocks containing at least one BIP error, lost cell or misinserted cell (CLP0+1
Fwd Lost/ Misinserted Impaired Blocks (8) Bwd Lost/ Misinserted Impaired Blocks (8)	The Lost/Misinserted Impaired Block count represents the sum of the PM cell blocks for which there was at least one lost or misinserted cell (CLP0+1). The Lost/Misinserted Block Impaired Block count is incremented whenever there is a non-zero TUCD_0+1.
Fwd SECB Errored (8) Bwd SECB Errored (8)	Severely Errored Cell Block Errored Cells (CLP0+1). The SECB Errored is incremented whenever the number of BIPV errors exceeds MERROR in the selected threshold register, and there are no lost/misinserted cells, and the MCSNs are in sequence. The accumulation of SECB Errored inhibits the accumulation of the count of BIP Errors.

Name	Description
Fwd SECB Lost (8) Bwd SECB Lost (8)	Severely Errored Cell Block Lost Cells. When CLP0_SECBs_Only is a logic 0, the SECB Lost is incremented whenever the number of Lost CLP0+1 cells exceeds MLOST in the selected threshold register. When CLP0_SECBs_Only is a logic 1, SECB Lost is incremented whenever the number of Lost plus Tagged CLP0 cells exceeds MLOST. The accumulation of SECB Lost inhibits the accumulation of the count of Lost CLP0 and Lost CLP0+1 cells.
Fwd SECB Misinserted (8) Bwd SECB Misinserted(8)	Severely Errored Cell Block Misinserted Cells (CLP0+1). The SECB Misinserted is incremented whenever the number of Misinserted cells exceeds MMISINS in the selected threshold register. The accumulation of SECB Misinserted inhibits the accumulation of the count of Misinserted Cells.
Fwd SECBC (8)	Forward Severely Errored Cell Blocks Combined. This running counter increments each time a SECB is declared. This value is inserted into the SECBC field of generated Backwards Reporting cells.
Bwd SECBC (8)	Backward Severely Errored Cell Blocks Combined. This value is copied from the SECBC field of received Backwards Reporting cells, and represents a rolling modulo-256 count of all Severely Errored Cell Blocks. There is no need to initialize this running counter.
Bwd SECBC Accum. (8)	Backward Accumulating SECBC Count. Whenever a received Bwd PM cell has a SECBC field different from the stored Bwd SECBC, this field is incremented by the modulo-256 difference. This is a saturating counter that initializes itself when the first Bwd PM cell is received.
Fwd Lost Fwd PM Cells (8)	The Fwd Lost Fwd PM Cells count uses the MCSN of received Forward Monitoring cells to determine the number of lost Fwd PM cells. Whenever the MCSN of a received Fwd PM cell is out of sequence, this count is incremented by the difference between the expected and received MCSN, and BIP-16 calculations are suppressed.
Fwd Tagged CLP0 Cells (16) Bwd Tagged CLP0 Cells (16)	Whenever there are less CLP0 cells received than were transmitted (TUCD is negative) then those cells have either been lost or tagged. The inference is made that if CLP0 cells were lost, then they should be lost from the CLP0+1 stream as well. Thus when TUCD0 < 0, the Lost CLP0 cells count is incremented by the lesser of –TUCD0 and -TUCD0+1, and the Tagged CLP0 Cell Count is incremented by (-TUCD0) – (-TUCD0+1), so long as the result is positive. This count is not incremented if the SECB Lost or SECB Misins count is incremented.
Fwd Lost CLP0 (16) Bwd Lost CLP0 (16)	The Lost CLP0 Cell Count represents the total number of Lost CLP0 user cells during a PM session. The Lost CLP0 cell count is incremented by the lesser of -TUCD_0 and –TUCD_0+1, whenever that number is greater than zero. This count is not incremented if the SECB Lost count is incremented.
Fwd Lost CLP0+1 (16) Bwd Lost CLP0+1 (16)	The Lost CLP0+1 Cell Count represents the total number of Lost CLP0+1 user cells during a PM session. The Lost CLP0+1 cell count is incremented by the number of Lost CLP0+1 cells, whenever TUCD_0+1 < 0 . This counter will not increment is the SECB Lost counter increments (it is therefore sensitive to CLP0_SECBs_only).
Fwd Misinserted Cells (16) Bwd Misinserted Cells (16)	The Misinserted Cell Count represents the total number of Misinserted CLP0+1 user cells during a PM session. The Misinserted Cell Count is incremented by the number of misinserted CLP0+1 cells, whenever MMISINS≥TUCD_0+1 > 0. (i.e. this count is not incremented if the SECB Misinserted Count is incremented).
Fwd Total Lost CLP0+1 (16) Bwd Total Lost CLP0+1 (16)	The Total Lost CLP0+1 cell count represents the total number of lost CLP0+1 user data cells during a PM session. This count is not dependent on a threshold. That is, the Total Lost CLP0+1 cell count is always incremented by the number of lost CLP0+1 user cells.

Name	Description
Fwd Total Lost CLP0 (16) Bwd Total Lost CLP0 (16)	The Total Lost CLP0 cell count represents the total number of lost CLP0 user data cells during a PM session. This count is not dependent on a threshold. That is, the Total Lost CLP0 cell count is always incremented by the number of lost CLP0 user cells.
Transmitted CLP0+1 User Cells (32)	The Transmitted CLP0+1 User Cell count represents the number of user cells that are originated on a monitored connection by the transmitting end point. If the PM session is configured to source Fwd PM cells, then this count is derived from the number of user cells transmitted. If the PM session is configured to monitor or terminate PM flows, then this count is derived from the difference of the TUC 0+1 fields of successive Backward Reporting cells.
Transmitted CLP0 User Cells (32)	The Transmitted CLP0+1 User Cell count represents the number of CLP0 user cells that are originated on a monitored connection by the transmitting end point. If the PM session is configured to source Fwd PM cells, then this count is derived from the number of CLP0 user cells transmitted. If the PM session is configured to monitor or terminate PM flows, then this count is derived from the difference of the TUC0 fields of successive Backward Reporting cells.
Bwd Lost Bwd PM Cells (8)	If the MCSN of a received BwdPM cell is out of sequence, then this count will be incremented by the difference between the expected MCSN and the received MCSN.
Bwd Lost Fwd PM Cells (8)	The Bwd Lost Fwd PM Cells count represents the number of forward monitoring cells lost in transit to the far end point. This calculation is performed based on the Fwd MCSN field of arriving Backwards Reporting cells. Whenever the FMCSN field of the Bwd PM cell is out of sequence, this count is incremented by the difference between the received and expected MCSN. However, if the Bwd PM cell's own MCSN is also out of sequence, this count will increment by the number of apparently lost Fwd PM cells minus the number of lost Bwd PM cells.

PM Cell Format as defined by ITU-T I.610

Header Fields 5x8	OAM Cell Type (= 0010) 4	OAM Function Type 4	Performance Management Function Specific Fields 45x8	Reserved 6	EDC (CRC-10) 10

The Performance Management Function Specific Fields are listed below:

Fwd = Forward Monitoring PM cell field
Bwd = Backward Reporting PM cell field

Fwd + Bwd	Fwd + Bwd	Fwd	Fwd + Bwd	Fwd		Bwd	Bwd	Bwd	Bwd	Bwd
MCSN (8)	TUC_0+1 (16)	BEDC_0+1 (16)	TUC_0 (16)	Time Stamp (32)	Unused 6AH (27 octets)	Fwd MCSN (8)	SECBC (8)	TRCC_0 (16)	Block Error Result (8)	TRCC_0+1 (16)

The S/UNI-ATLAS-3200 provides only minimal support for the Time Stamp field option in PM cells. The default value of all ones is inserted in the Time Stamp field for all generated Fwd PM cells. Bwd PM cells may contain the time stamp in the received Fwd PM cell if the BCIF is not full when the Fwd PM cell arrives, and the Copy_FwPM_Timestamp bit is logic 1 in the Cell Processor Configuration Register.

10.15 Change of Connection State FIFO

As a configurable option, the S/UNI-ATLAS-3200 maintains a FIFO that monitors all connections for changes of state (i.e. Continuity Check Alarm, AIS Alarm, RDI Alarm, OAM Failure, and DRAM CRC Error). If a connection has a change of state at some time (e.g. due to the receipt of an AIS cell, or due to loss of continuity), a copy of the Status field and the 17-bit connection address will be written into the FIFO.

A maskable interrupt for the FIFO is provided to notify when valid data is in the FIFO, when it is at least half full, and when it is full.

If the FIFO becomes full, a background process which checks for changes of state will be suspended. The process will remain suspended until such time as data have been read out of the FIFO**. It is the responsibility of the management software to ensure the FIFO is polled often enough to ensure the monitoring of changes of state remain compliant to the GR-1248-CORE Bellcore and ITU-T I.610 standards.**

Table 34 Change of State FIFO

Each FIFO is 256 entries deep, and the contents of the FIFO are shown below:

Bit	Name	Description
31:29	Reserved	
28	Segment End Point	If this bit is logic 1, the connection is a segment end-point.
27	End-to-End Point	If this bit is logic 1, the connection is an end-to-end point.
26	Segment Flow	If this bit is logic 1, the connection is part of a defined segment flow.
25	DRAM CRC Err	If this bit is logic 1, then this VC Table entry suffered an error in the DRAM, and may need to be reinitialized.
24	OAM Failure	This bit becomes a logic 1 if a segment or end-to-end RDI, AIS or CC condition has persisted for 3.5 ± 0.5 seconds. OAM_Failure is cleared as soon as no RDI, AIS or CC condition remains.
23	AIS End To End Alarm	This bit becomes a logic 1 upon receipt of a single end-to-end AIS cell. The alarm status is cleared upon the receipt of a single user cell or end-to-end CC cell, or if no end-to-end AIS cell has been received within the last 2.5 ± 0.5 sec.
22	AIS Segment Alarm	This bit becomes a logic 1 upon receipt of a single segment AIS cell. The alarm status is cleared upon the receipt of a single user cell or segment CC cell, or if no segment AIS cell has been received within the last 2.5 ± 0.5 sec. This bit will only be asserted by connections which have the Segment End Point or Segment Flow bits set to logic 1.

Bit	Name	Description
21	RDI End To End Alarm	This bit becomes a logic 1 upon receipt of a single end-to-end RDI cell. This bit is cleared if no end-to-end RDI cell has been received within the last 2.5 ± 0.5 sec.
20	RDI Segment Alarm	This bit becomes a logic 1 upon receipt of a single segment RDI cell. This bit is cleared if no segment RDI cell has been received within the latest 2.5 ± 0.5 sec.
19	CC End to End Alarm	This bit becomes a logic 1 if no user cell or end-to-end CC cell has been received within the last 3.5 ± 0.5 sec. This bit is cleared upon receipt of a user cell, or end-to-end CC cell.
18	CC Segment Alarm	This bit becomes a logic 1 if no user or segment CC cell has been received within the last 3.5 ± 0.5 sec. This bit is cleared upon receipt of a user cell or segment CC cell. Segment CC alarms are declared only if the VC is part of a segment flow (Segment_Flow = 1) or is a segment end point (Segment_End_Point = 1)
17	Reserved	This bit is reserved and should be masked off.
16	Reserved	This bit is reserved and should be masked off.
[15:0]	Connection Address	This field contains the 16-bit connection address with which the change of state is associated.

The FIFO contents may be read through the microprocessor port. The microprocessor may read the COS FIFO, and when the COSVALID bit is asserted, the contents of the COS FIFO are valid. The FIFO read-pointer is incremented when the Change of Connection State Data register is read (assuming the FIFO is not empty). When the Change of Connection State Data Register is read, the COS FIFO BUSY bit is asserted. At this time, the state of the COSVALID bit is undefined. The BUSY bit will be deasserted 3-5 SYSCLK cycles after the Change of Connection State Data register is read. At this time, the COSVALID bit will be defined and will indicate whether subsequent reads are appropriate.

10.16 Count Rollover FIFO

In order to eliminate the need for the microprocessor to periodically poll counts to prevent them from rolling over or saturating, the S/UNI-ATLAS-3200 provides a 256-entry Count Rollover FIFO accessible via the microprocessor port. When the Count Rollover FIFO Enable bit is set in the Cell Processor Configuration register, then the various per-VC, per-PHY, and Performance Management counts may be configured to generate Count Rollover entries. An entry is made to the Count Rollover FIFO every time at least one of these counts has its MSB set. Once an entry has been made to the FIFO, the MSB for that count is cleared. Thus every entry indicates that 2^{15} (for a 16-bit count) or 2^{31} (for a 32-bit count) events have occurred. If the Count Rollover FIFO becomes full, the MSB remains set until there is room in the Count Rollover FIFO again. The counter continues to operate normally until it reaches an all-ones state, at which time it saturates. So long as the Count Rollover FIFO is cleared out before another 2^{15} (or 2^{31}) events can occur, no events will be lost.

One exception is provided for PM counts. Because the 8-bit counts of BIP-16 errors and Lost Fwd and Bwd PM Cells may roll over frequently, they may be disabled from generating FIFO entries by setting the Sat_Fast_PM Counts bit to logic 1 in the Cell Processor Configuration register.

The intention is that the microprocessor use these rollover entries to maintain the most-significant bits of the counters in its own memory. The least-significant bits can be accessed by the microprocessor in the normal way whenever precise counts are needed. Maskable interrupts are provided when the Rollover FIFO is not empty, when it is half full, and when it is nearly full.

There are four possible sources of Rollover FIFO entries: Per-VC counts, Per-PHY counts, PM session 2, or PM session 1. The source of the entry determines its format, and is determined by the setting of bits 30:29 of the entry. The most significant bit of the Source field is reserved for future use. Each source has an associated Rollover FIFO Enable bit to control whether entries are permitted from that source.

Per-VC counts include the 32-bit general cell counts and the 16-bit Policing Non-Compliant counts. The format of a Per-VC rollover FIFO entry is as follows:

Table 35 Count Rollover FIFO Format For Per-VC Count Entries

Bit	Field	Description
31	Reserved	
30:29	Source	“00” for a per-VC count entry
28	Reserved	
27:12	Address	The 16-bit VC Record address that generated this entry
11:7	Unused	
6	Non-Compliant 3	When ‘1’, Policing Non-Compliant Count 3 had its MSB set.
5	Non-Compliant 2	When ‘1’, Policing Non-Compliant Count 2 had its MSB set.
4	Non-Compliant 1	When ‘1’, Policing Non-Compliant Count 1 had its MSB set.
3	Alternate Count2	When ‘1’, per-VC Alternate Count 2 had its MSB set
2	Alternate Count1	When ‘1’, per-VC Alternate Count 1 had its MSB set
1	Count2	When ‘1’, per-VC Count 2 had its MSB set
0	Count1	When ‘1’, per-VC Count 1 had its MSB set

Per-PHY counts include Per-PHY policing counts and the per-PHY counts of received CLP0 cells, CLP1 cells, etc. The format of a per-PHY rollover FIFO entry is as follows:

Table 36 Count Rollover FIFO Format For Per-PHY Count Entries

Bit	Field	Description
31	Reserved	
30:29	Source	“01” for a per-PHY count entry
28:23	PHY Address	The 6-bit PHY address that generated this entry
22:11	Unused	
10	TIMEOUT	When ‘1’, the MSB of the Timed-Out Cell Count was set.
9	EFCI_NZGFC	When ‘1’, the MSB of the EFCI/Non-Zero GFC Cell Count was set.
8	Invalid VPI_VCI_PTI	When ‘1’, the PHY Invalid VPI/VCI/PTI (Search Error, Unprovisioned or Inactive connection, or Reserved VCI/PTI) count had its MSB set.
7	Bad OAM_RM	When ‘1’, the PHY Errored RM/OAM cells count had its MSB set.

Bit	Field	Description
6	RM	When ‘1’, the PHY Valid RM cells count had its MSB set.
5	OAM	When ‘1’, the PHY Valid OAM cells count had its MSB set.
4	CLP1	When ‘1’, the PHY CLP1 cells count had its MSB set.
3	CLP0	When ‘1’, the PHY CLP0 cells count had its MSB set.
2	PHY Non-Compliant 3	When ‘1’, PHY Policing Non-Compliant Count 3 had its MSB set.
1	PHY Non-Compliant 2	When ‘1’, PHY Policing Non-Compliant Count 2 had its MSB set.
0	PHY Non-Compliant 1	When ‘1’, PHY Policing Non-Compliant Count 1 had its MSB set.

PM counts include Forward Lost CLP0 Cells, Backward Lost CLP0+1 Cells, etc.

Table 37 Count Rollover FIFO Format For PM Entries

Bit	Field	Description
31	Reserved	
30:29	Source	“010” for a PM count entry from PM Bank 0, “011” for a PM count entry from PM Bank 1
28:21	PM Address	The 8-bit PM Session address that generated this entry
20	PM Direction	When PM Direction is ‘1’, the counts indicated refer to Forward counts accumulated by the transmission or reception of Fwd PM cells. When PM Direction is ‘0’, the counts indicated refer to Backward counts accumulated by the reception of Bwd PM cells.
19	PM Source	When PM Source is logic 1, then the PM session is a PM flow source point, and only the Transmitted CLP0 and Transmitted CLP0+1 count indications are valid.
18:17	Reserved	
16	Fwd/Bwd Errors	When ‘1’, the Fwd or Bwd Errored Cell Count had its MSB set, depending on the setting of the PM Direction bit. Because this count may roll over quite frequently, there is a register bit, Sat_Fast_PM_Counts, which forces this error count to saturate, and not generate Count Rollover FIFO entries.
15	Fwd/Bwd Impaired	When ‘1’, the Fwd or Bwd Impaired Block count had its MSB set, depending on the setting of the PM Direction bit.
14	Fwd/Bwd Lost/Misins Impaired	When ‘1’, the Fwd or Bwd Impaired Blocks due to Lost or Misinserted Cells count had its MSB set, depending on the setting of the PM Direction bit.
13	Fwd/Bwd SECB Errored	When ‘1’, the Fwd or Bwd Severely Errored Cell Block due to BIP-16 Errors count had its MSB set, depending on the setting of the PM Direction bit.
12	Fwd/Bwd SECB Lost	When ‘1’, the Fwd or Bwd Severely Errored Cell Block due to Lost Cells count had its MSB set, depending on the setting of the PM Direction bit.
11	Fwd/Bwd SECB Misinserted	When ‘1’, the Fwd or Bwd Severely Errored Cell Block due to Misinserted Cells count had its MSB set, depending on the setting of the PM Direction bit.

Bit	Field	Description
10	Bwd SECBC (Accumulated)	When ‘1’, the accumulating Bwd Severly Errored Cell Block Combined count had its MSB set. This indicator is not used if PM Direction is ‘1’.
9	Fwd/Bwd Lost Fwd PM Cells	When ‘1’, the Fwd or Bwd Lost Fwd PM Cells count had its MSB set, depending on the setting of the PM Direction bit. Because this count may roll over quite frequently, there is a register bit, Sat_Fast_PM_Counts, which forces this error count to saturate, and not generate Count Rollover FIFO entries.
8	Bwd Lost Bwd PM cells	When ‘1’, the Bwd Lost Backward PM Cells count had its MSB set. This indicator is not used if PM Direction is ‘1’. Because this count may roll over quite frequently, there is a register bit, Sat_Fast_PM_Counts, which forces this error count to saturate, and not generate Count Rollover FIFO entries.
7	Fwd/Bwd Tagged Cells	When ‘1’, the Fwd or Bwd Tagged Cells count had its MSB set, depending on the setting of the PM Direction bit.
6	Fwd/Bwd Misinserted Cells	When ‘1’, the Fwd or Bwd Misinserted Cells count had its MSB set, depending on the setting of the PM Direction bit.
5	Fwd/Bwd Lost CLP0 Cells	When ‘1’, the Fwd or Bwd Lost High-Priority Cells count had its MSB set, depending on the setting of the PM Direction bit.
4	Fwd/Bwd Lost CLP0+1 Cells	When ‘1’, the Fwd or Bwd Lost Cells count had its MSB set, depending on the setting of the PM Direction bit.
3	Fwd/Bwd Total Lost CLP0 Cells	When ‘1’, the Fwd or Bwd Total Lost Cell count (including those lost in SECBs) had its MSB set, depending on the setting of the PM Direction bit.
2	Fwd/Bwd Total Lost CLP0+1 Cells	When ‘1’, the Fwd or Bwd Lost Cell count (including those lost in SECBs) had its MSB set, depending on the setting of the PM Direction bit.
1	Transmitted CLP0 Count	When ‘1’, the 32-bit Total Transmitted CLP0 Cells count had its MSB set.
0	Transmitted CL0+1 Count	When ‘1’, the 32-bit Total Transmitted Cells count had its MSB set.

10.17 Cell Routing

Generated reverse flow cells (Backward Reporting PM cells, Loopback cells, and RDI cells) are routed to the Output Backward OAM Cell Interfaces of the S/UNI-ATLAS-3200. The output BCIF has a 16 cell FIFO for buffering these cells before they are sent out. Cells generated in the backward direction may be header translated as if they were being transmitted to the OCIF depending on the setting of Xlate_To_OBCIF.

Cells received by the S/UNI-ATLAS-3200 on the Input Backward Cell Interface are buffered in a 16 cell FIFO , paced, and inserted into the cell flow stream.

The destination of each OAM cell depends on the type of OAM cell and whether or not the S/UNI-ATLAS-3200 is the end-point for that particular OAM flow. If the S/UNI-ATLAS-3200 is not an end-point, the OAM cells are routed to the same destination as user cells, with the exception of Loopback cells. If the S/UNI-ATLAS-3200 is an end point, the default configuration terminates and processes all OAM cells except APS, System Management, Activate/Deactivate and Undefined OAM cells, which may optionally be routed to either the Output Cell Interface, or the Backward Cell Interface, or the Microprocessor Cell Interface. End-to-end points are treated as also being segment end-points as well for the purposes of routing these cells, to aid in localization of problems. The cell information fields prepended to cells sent to the MCIF or BCIF is intended as an aid to processing these cells.

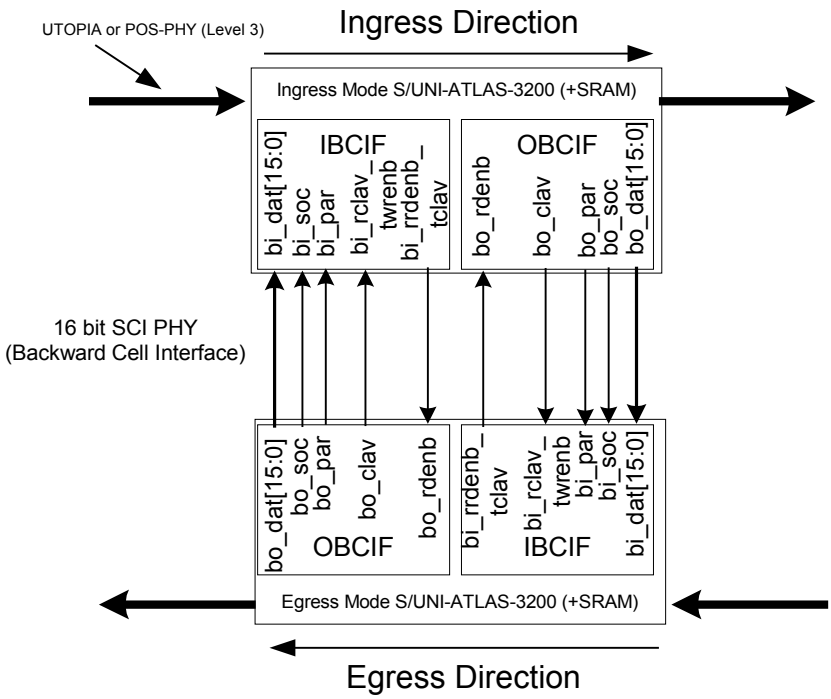
Parent Loopback OAM cells will have their Loopback Location ID examined. Depending on the setting of the Loopback Routing bits in the Configuration field of the VC table, loopback cells may be routed to the Backwards Cell Interface, with their Loopback Indication bit cleared and the local Loopback Location Identifier encoded in their Loopback Location ID field. The Source ID is not changed.

Returned Loopback OAM cells will have their Source ID examined. Depending on the setting of the Loopback Routing bits in the Configuration field of the VC Table, Returned Loopback cells may be dropped and routed to the microprocessor if the Source ID of the cell matches the local Loopback ID programmed into the CP Loopback ID registers. Depending on the setting of the Rtd_LB_to_UP_at_End bit in the CP Routing Configuration register, Returned Loopback cells may be routed to the microprocessor at flow end points irrespective of the Source ID.

10.17.1 Output Backward OAM Cell Interface

The Output Backwards Cell Interface is an extended cell length 16-bit, 52 MHz UTOPIA Level 1 Rx Slave “SCI-PHY” interface. Generated RDI and Backwards Reporting cells, along with Loopback cells, use this interface to access the opposite direction BCIF. A 16-cell FIFO is provided on the Output BCIF, and another 16 cell in the Input BCIF, to facilitate these transfers. The default configuration is shown in Figure 20

Figure 20 Connection of S/UNI-ATLAS-3200 BCIFs



In addition to RDI, Bwd PM, and LB cells, there are bits to route entire VCs, System Management cells, or undefined OAM cells to the BCIF. These options permit the BCIF interface to be connected to a tester for debug purposes, or to an ASIC for external processing of certain cells (so long as the RDI, BwdPM, and LB cells are passed on to the opposite direction ATLAS). In order to allow cells to be inserted in the reverse direction, the S/UNI-ATLAS-3200 prepends routing information stored in the VC table onto the cell. This information consists of the PHYID and Backwards Direction VCRA fields from the VC table. The cell format, which is always a 64-byte cell, is shown in Table 38.

Table 38 Backwards Cell Interface Cell Format

Bit 15 Bit 0			
User Prepend/Postpend Bytes 1 and 2			
User Prepend/Postpend Bytes 3 and 4			
Cell Information Field (9 bits)	PHYID (6 bits)	Reserved(1)	
VC Record Address (16 bits)			
16 LSBs of UL3 UDF field			
VPI (12 bits)		4 MSBs of VCI	
12 LSBs of VCI		PTI (3)	CLP (1)
HEC field	8 MSBs of UDF		
Payload 1			
…			
Payload 24			

The User prepend/postpend bytes, along with the HEC and UDF fields, are the same as the respective bytes on the UL3 interfaces. In the case of cells that are looped back, they contain whatever data was already in these fields; in the case of generated cells (RDI, Bwd PM, and Rtd LB) the contents are undefined. It is expected that the cell will be header translated (Xlate_From_IBCIF = 1) bit in the reverse direction if the contents of the prepend or HEC/UDF fields are to be used. If the optional Xlate_To_OBCIF bit is logic 1, then the VPI, VCI, prepend/postpend, HEC, and UDF fields may contain data from the VC table as configured by the Cell_Info_to_OCIF, XVPIVCI, XGFC, XPREPO, XHEC, and XUDF bits.

The insertion of the PHYID, Backwards VCRA, and Cell Information fields are controlled by the OBCIF_PHYID, OBCIF_Bwd_VCRA, and OBCIF_Cell_Info register bits. However, if the PHYID is not inserted, cells from the BCIF cannot be correctly reinserted in the reverse flow. If the Backwards VCRA is not inserted, then the cell contents (as modified by the Xlate_To_OBCIF in conjunction with the XVPIVCI etc. bits) must be able to be searched correctly, and the Search_From_IBCIF bit must be set to logic 1.

The Cell Info field is purely for the convenience of an ASIC or tester, to assist in identifying the cell and the connection from which it came. The BCIF Cell Info field is very similar to part of the Microprocessor Cell Info Field, and is defined as follows:

Table 39 BCIF Cell Information Field

Cell_Info[8:0]	Definition
Bit 8	Source
Bit 7	NNI
Bit 6	VPC
Bit 5	OAM_Type
Bit 4	TYP[4]
Bit 3	TYP[3]
Bit 2	TYP[2]
Bit 1	TYP[1]
Bit 0	TYP[0]

Source: The source of the cell, encoded as follows:
0 : Input Cell Interface, Microprocessor Cell Interface, or Backwards Cell Interface
1 : Generated RDI or Bwd PM Cell, or Looped-back OAM-LB cell. It is intended that all of these cells be passed to the opposite direction S/UNI-ATLAS-3200.

NNI: Indicates the connection is associated with a Network-Network Interface (NNI). A logic 0 means the connection belongs to a User-Network Interface (UNI).

VPC: Indicates the connection is provisioned as a Virtual Path Connection (VPC). A logic 0 means the connection is provisioned as a Virtual Channel Connection (VCC).

OAM_Type: A logic 1 identifies a segment OAM cell. A logic 0 identifies an end-to-end OAM cell. This bit is only valid when the cell type indicates one of the OAM types.

TYP[4:0]: Cell type. This field is encoded as follows:

TYP[4:0]	Cell Type
00000	User
00001	OAM AIS
00010	OAM RDI
00011	OAM Continuity Check
00100	OAM Parent Loopback
00101	OAM Returned Loopback
00110	OAM Forward Monitoring PM
00111	OAM Backward Reporting PM
01000	OAM Automated Protection Switching
01001	OAM Activate/Deactivate
01010	OAM Undefined
01011	OAM System Management
01100	Forward RM
01101	Backward RM
01110	Invalid PTI/VCI

TYP[4:0]	Cell Type
01111	Unprovisioned Connection
10000	Inactive Connection, or mis-configuration of the VPC Pointer.
10001	Search Error
10010	Cell Transfer Error (bad POS-3 or UL3 parity, or invalid PHYID)
10011	OAM cell with errored CRC-10
10100	RM cell with errored CRC-10
10101	Generated AIS
10110	Generated CC
10111	Generated Forward Monitoring PM
11000..11111	Reserved

10.17.2 Input Backward OAM Cell Interface

The Input Backwards Cell Interface is an extended cell length, 16-bit, 52 MHz UTOPIA Level 1 “SCI-PHY” interface. Normally this interface acts as an Rx Master interface, though it can be configured as a Tx Slave interface for the purposes of attaching a tester or ASIC to it. Generated RDI and Backwards Reporting cells, along with Loopback cells, use this interface to enter the S/UNI-ATLAS-3200 from the opposite-direction S/UNI-ATLAS-3200. Cells received on this interface must carry the PHYID as shown in Table 38, be 64 bytes in length, and either be able to be searched correctly (if Search_From_IBCIF = 1) or carry the VC Record Address as shown in Table 38. Note that if a device other than S/UNI-ATLAS-3200 is placed between two S/UNI-ATLAS-3200s, the Source bit is provided for the purpose of differentiating cells that must be reinserted in the opposite direction (Source = 1) and cells which are routed to the BCIF for further processing (Source = 0). However, any cells produced by such a device must contain the embedded PHYID for proper operation.

The Input Backward OAM Cell Interface (Input BCIF) stores all received cells in a 16-cell FIFO until such time as they are transmitted by the Cell Processor. The S/UNI-ATLAS-3200 will insert cells from the Input Backward OAM Cell Interfaces at the insertion rate programmed into the Backward Cell Interface Pacing register bits. The BCIF insertion rate is the minimum rate at which cells will be inserted from the Input BCIF; cells will be inserted at a higher rate when there is excess capacity in the Cell Processor and Output Cell Interface, and there are no cells from the Input Cell Interface waiting to be processed.

In the event the PHY queue for which the cell at the head of the FIFO is destined becomes inoperative (i.e. no cells are accepted for that PHY), that cell must be dealt with so that it does not prevent other PHY devices from having cells inserted in the cell stream. The Cell Processor can be programmed with a Head-of-Line Time Out function to deal with this problem. If a PHY queue does not make room available within a specified time, the S/UNI-ATLAS-3200 can take a programmable action on that cell. The time out counter is defined in terms of cell periods at the SYSCLK rate, where one cell period is equal to 22 clock cycles. The Head-of-Line Time Out can be programmed to take into account the worst case time for cell transmission (e.g. 48 cell periods, plus 2-3 cell periods for robustness, at an STS-1 rate). The S/UNI-ATLAS-3200 may be programmed to discard the cell, or to route the cell to the Microprocessor Interface, where it may be stored and re-inserted at a later time when the PHY problem has been resolved. This function is provided solely to retain a quality of service for other PHY devices in case a catastrophic event occurs on a particular PHY queue. In normal operating mode, this situation will never be encountered. The Head-of-Line Time Out can optionally be disabled.

Cells from the IBCIF are, by default, header-translated much like cells from the Input Cell Interface. For routing and processing, they are treated as cells that were not received, but (potentially) are transmitted. Thus, they are never included in terminated or monitored PM flows, OAM cells are not dropped at flow end points, and AIS, CC, and RDI alarms are not affected. Cells from the IBCIF are, however, subject to counting and/or policing if their cell type (usually OAM cells) are configured to be counted and/or policed. Cells from the BCIF may optionally not be translated (if the Xlate_From_IBCIF register bit is logic 0) or may have the Prepend/Postpend 2 word from the VC Record Table inserted onto the Prepend/Postpend 1 or HEC/UDF words (via the IBCIF_P2_To_P1 and IBCIF_P2_To_HECUDF bits). These bits are useful when using the BCIFs in a non-standard way, and reside in the Cell Processor Routing Configuration register.

10.17.3 Internal DRAM Access

Microprocessor access to the internal DRAM is provided to allow access to the VC Table records. The access registers allow the microprocessor to read or write an entire VC Table record in one operation. The Cell Counts, Alternate Cell Counts, and Non-Compliant Counts each have a Clear On Read register bit that allows the corresponding count to be cleared whenever a read is performed. Each field in the VC table is individually maskable during writes, to permit settings to be changed without affecting the operation of the device.

The VC Table records are protected by a CRC-10 calculated over the entire entry. This CRC is automatically generated by S/UNI-ATLAS-3200 during microprocessor write operations and normal processing, and is automatically checked during reads, including microprocessor reads, of the DRAM.

Internal DRAM access bandwidth is shared between the internal processing cell processing operations and microprocessor accesses. The microprocessor is guaranteed enough bandwidth to perform at least 140,000 DRAM accesses per second. This is enough to support over 8000 connection setups/teardowns and allow a read or write the VC table record for all 64K VCs. Additional microprocessor access to the DRAM may consume bandwidth required to send OAM-FM and OAM-PM cells and to do background processes, if the aggregate (user cells + generated OAM cells) is in excess of OC-48.

10.17.4 Writing Cells

The S/UNI-ATLAS-3200 contains a one cell buffer for the assembly of a cell by the microprocessor for presentation on the Output Cell Interface. Optional header translation and CRC-10 protection provides full support of diagnostic and OAM requirements.

Cells inserted via the Microprocessor Cell Interface are inserted into the cell stream by the ATM Layer Cell Processor. The ATM Layer Cell Processor gives an equal priority between cells received from the Input Cell Interface and cells received from the Microprocessor Cell Interface. Therefore, it is the responsibility of the management software to ensure that cells are not inserted via the Microprocessor Cell Interface too frequently (i.e. the management software must ensure these inserted cells are paced).

Writes are performed through the Microprocessor Cell Interface Control and Status and Microprocessor Cell Interface Data registers. The steps below outline how to insert a cell through this interface:

1. Poll the INSRDY register bit of the Microprocessor Cell Interface Control and Status register until it is a logic 1. Alternatively, service the interrupts that result from setting the INSRDYE bit in the Master Interrupt Enable register. The INSRDYI bit in the Master Interrupt Status register is set whenever the INSRDY bit goes high.

2. Write the WRSOC bit in the Microprocessor Cell Interface Control and Status register. At the same time, ensure that the CRC10, PROC_CELL and PHY[5:0] register bits are set to their correct values, depending on what operation is required.

   If the PROC_CELL register bit is a logic 1, then the cell will be processed in the Cell Processor as if it came from the Input Cell Interface. If the PROC_CELL register bit is logic 0, then the cell will be passed through without being searched, processed, or counted in any way, as if it were inserted into the cell stream after the Cell Processor.

   PHY[5:0] represents the PHY address that the cell is associated with and will be included in the search key used for VC identification and used to determine the destination PHY queue.

3. Write the cell contents to the Microprocessor Cell Interface Data register. Each subsequent write enters the next word in the cell. The words shall be written in the following order, and all 64 bytes must be written even if some are not used:

Word #	Contents
1	1st prepended/postpended d-word
2	2nd prepended/postpended d-word
3	ATM Header: GFC, VPI, VCI, PTI, CLP
4	HEC and UDF fields
5	1st ATM payload d-word
6	2nd ATM payload d-word
…	…
16	12th ATM payload d-word

The S/UNI-ATLAS-3200 automatically handles cell length mismatches, and will place prepends/postpends in the appropriate locations when transmitting cells. Note that if there is only one prepended word used in cells leaving S/UNI-ATLAS-3200, that the 1st prepended/postpended d-word field (Word 1) would be filled with data for that prepend/postpend, and Word 2 would be a don't-care.

10.17.5 Reading Cells

Cells received on the Input Cell Interface or the Backward Cell Interface can be routed to the 16-cell Microprocessor Cell Interface FIFO based on the type of cell.

Maskable interrupt statuses are generated upon the receipt of a cell and upon buffer overflow. If a buffer overflow occurs, entire cells are lost.

Cells are written into the MCIF FIFO without header translation, as a 64-byte cell. As an option, the prepended information can be overwritten with the PHYID, VC Record Address, and information about the cell and connection. This information, together, is the Microprocessor Cell Info Field and is used to interpret why the cell was routed to the microprocessor, and to provide cell status information. The Cell_Info_to_UP bit in the Cell Processor Configuration Register controls this function.

The Microprocessor Cell Info word has the following format:

Table 40 Microprocessor Cell Information Field

Prepend 1 [31:0]	Definition
Bits 31:13	Unused
Bit 12	Source[1]
Bit 11	Source[0]
Bit 10	End_to_End_Point
Bit 9	Segment_End_Point
Bit 8	TimeOut
Bit 7	NNI
Bit 6	VPC
Bit 5	OAM_Type
Bit 4	TYP[4]
Bit 3	TYP[3]
Bit 2	TYP[2]
Bit 1	TYP[1]
Bit 0	TYP[0]
Prepend 2 [31:0]	
Bits 31:23	Unused
Bits 22:17	PHYID[5:0]
Bit 16	Reserved
Bits 15:0	VC Record Address[15:0]

Source[1:0]: The source of the cell, encoded as follows:
00 : Input Cell Interface
01 : Backwards Cell Interface
10 : Generated Forward PM, AIS, or CC cell
11 : Reserved.

End_to_End_Point: Indicates the connection is provisioned as an OAM flow end point. If the cell type indicates an unprovisioned connection, search error, or cell transfer error, this bit is not valid.

Segment_End_Point: Indicates the connection is provisioned as an OAM flow segment end point. If the cell type indicates an unprovisioned connection, search error, or cell transfer error, this bit is not valid.

TimeOut: Indicates the cell was removed from a Backward Cell Interface or Microprocessor Cell Interface because the head-of-line blocking timer has expired, or the associated PHY has been declared inoperative. When this bit is set, only the SOURCE, PHYID and TYP fields are valid.

NNI: Indicates the connection is associated with a Network-Network Interface (NNI). A logic 0 means the connection belongs to a User-Network Interface (UNI).

VPC: Indicates the connection is provisioned as a Virtual Path Connection (VPC). A logic 0 means the connection is provisioned as a Virtual Channel Connection (VCC).

OAM_Type: A logic 1 identifies a segment OAM cell. A logic 0 identifies an end-to-end OAM cell. This bit is only valid when the cell type indicates one of the OAM types.

TYP[4:0]: Cell type. This field is encoded as follows:

TYP[4:0]	Cell Type
00000	User
00001	OAM AIS
00010	OAM RDI
00011	OAM Continuity Check
00100	OAM Parent Loopback
00101	OAM Returned Loopback
00110	OAM Forward Monitoring PM
00111	OAM Backward Reporting PM
01000	OAM Automated Protection Switching
01001	OAM Activate/Deactivate
01010	OAM Undefined
01011	OAM System Management
01100	Forward RM
01101	Backward RM
01110	Invalid PTI/VCI
01111	Unprovisioned Connection

TYP[4:0]	Cell Type
10000	Inactive Connection, or mis-configuration of the VPC Pointer.
10001	Search Error
10010	Cell Transfer Error (bad POS-3 or UL3 parity, or invalid PHYID)
10011	OAM cell with errored CRC-10
10100	RM cell with errored CRC-10
10101	Generated AIS
10110	Generated CC
10111	Generated Forward Monitoring PM
11000..11111	Reserved

PHYID[5:0]: The index of the PHY device associated with the cell.

VCRA[15:0]: The VC Record associated with the cell

The UP_DMAREQ output and the EXTCA bits of the MCIF Extract Buffer Control and Status registers are asserted if one or more complete cells are available in the buffer. The first read of the MCIF after either the EXTCA bit or the UP_DMAREQ is asserted returns the first word of the cell. Subsequent reads return the remainder of the cell. The sequence of words is the same as for buffer writes (see above). At any time, the read pointer can be returned to the beginning of the cell by setting the RESTART bit. The current cell is discarded upon setting the ABORT bit. The UP_DMAREQ output is deasserted during the read of the last word of the cell.

10.18 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST are supported. The S/UNI-ATLAS-3200 identification code is 073250CD hexadecimal.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI-ATLAS-3200. Normal mode registers (as opposed to test mode registers) are selected when TRS (UP_ADDR[11]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-ATLAS-3200 to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-ATLAS-3200 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-ATLAS-3200 operates as intended, reserved register bits must be written with their default value as indicated by the register bit description.

11.1 List of Registers

Register 0x000: S/UNI-ATLAS-3200 Master Configuration And Reset 151
Register 0x001: S/UNI-ATLAS-3200 Identity / Load Counts 154
Register 0x002: Master Interrupt Status #1 156
Register 0x003: Master Interrupt Status #2 162
Register 0x004: Master Interrupt Enable #1 164
Register 0x005: Master Interrupt Enable #2 166
Register 0x006: Master Clock Monitor 167
Register 0x020: Microprocessor Cell Interface Control and Status 169
Register 0x021: Microprocessor Cell Data 173
Register 0x022: MCIF Dropped Cells Counter 175
Register 0x030: Input Backwards Cell Interface Configuration 176
Register 0x031: IBCIF Dropped Cells Counter 178
Register 0x032: IBCIF Read Cells Counter 179

Register 0x038: Output Backwards Cell Interface Configuration 180
Register 0x039: OBCIF Dropped Cells Counter 181
Register 0x03A: OBCIF Read Cells Counter 182
Register 0x040: SYSCLK Delay Locked Loop Register 1 183
Register 0x041: SYSCLK DLL Register 2 185
Register 0x042: SYSCLK DLL Register 3 186
Register 0x043: SYSCLK DLL Register 4 187
Register 0x100: Cell Processor Configuration 190
Register 0x101: Cell Processor Routing Configuration 197
Register 0x102: Cell Counting Configuration 203
Register 0x104: Backward Cell Interface Pacing and Head of Line Blocking 205
Register 0x105: Per-PHY Processing Enable 1 207
Register 0x106: Per-PHY Processing Enable 2 209
Register 0x107: AIS/CC Pacing and Head of Line Blocking 211
Register 0x108: Fwd PM Pacing and Head of Line Blocking 213
Register 0x109: Inoperative PHY Declaration Period and Indications 215
Register 0x10A: Inoperative PHY Indications 217
Register 0x10B: Search Engine Configuration 219
Register 0x10C: SRAM Access Control 221
Register 0x10D: SRAM Data LSW (SRAM Data[31:0]) 223
Register 0x10E: SRAM Data MSW (SRAM Data [63:32]) 224
Register 0x110: VC Table Maximum Index 225
Register 0x111: VC Table Access Control 226
Register 0x112: VC Table Write Enable 1 229
Register 0x113: VC Table Write Enable 2 231
Register 0x114: VC Table Data Row 0, Word 0 (LSW) (RAM Data [31:0]) 232
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Register 0x1AE: Per-PHY EFCI/Non-Zero GFC Cell Count Holding Register 303
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11.2 Core Registers

Register 0x000: S/UNI-ATLAS-3200 Master Configuration And Reset

Bit	Type	Function	Default
31:18		Unused	X
17	R/W	Reserved	0
16	R/W	Reserved	0
15	R/W	FREE[7]	0
14	R/W	FREE[6]	0
13	R/W	FREE[5]	0
12	R/W	FREE[4]	0
11	R/W	FREE[3]	0
10	R/W	FREE[2]	0
9	R/W	FREE[1]	0
8	R/W	FREE[0]	0
7	R/W	POS_UL3B	1
6	R/W	Egress_IngressB	0
5	R/W	DRAM_BUSY_EN	0
4	R/W	SRAM_BUSY_EN	0
3	R/W	BUSYPOL	0
2	R/W	Reserved	0
1	R/W	STANDBY	1
0	R/W	RESET	1

RESET

The RESET bit allows the S/UNI-ATLAS-3200 to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-ATLAS-3200 is held in reset. On a hardware RESET, this bit is set to logic 1, and must be written to logic 0 to bring the device out of reset. Holding the S/UNI-ATLAS-3200 in a reset state places it into a low power, stand-by mode. In order to initialize the embedded DRAM, **this bit must remain logic 1, with the SYSCLK DLL locked (DLLRUN = 1 in the Master Clock Monitor Register) for at least 200 us following a hardware reset.** Once the 200 us have elapsed, this bit may be written to logic 0, and configuration of the device may proceed.

Note, unlike the hardware reset input, RSTB, the software reset bit does not force the S/UNI-ATLAS-3200 digital output pins tristate.

STANDBY

The STANDBY bit disables Cell Processing to avoid passing corrupted cells while initializing the S/UNI-ATLAS-3200. When STANDBY is a logic 1, the S/UNI-ATLAS-3200 makes all bus cycles available for external SRAM and internal DRAM access (i.e. micro access to the search tree or context is given highest priority, and no other processing will interrupt the SRAM and DRAM busses).

If the STANDBY bit is set while cell processing is in progress, the processing of cells currently in the pipeline is completed, but no more cells are accepted.

Reserved

This bit should be programmed to logic 0 for proper operation.

BUSYPOL

The BUSYPOL bit sets the polarity of the BUSYB primary output. If BUSYPOL is a logic 0, the BUSYB primary output is active low. If BUSYPOL is a logic 1, the BUSYB output is active high.

SRAM_BUSY_EN

When this bit is logic 1, the BUSY signal from the S/UNI-ATLAS-3200 will be asserted whenever the external SRAM is busy. When 0, the BUSY signal will not react to SRAM activity.

DRAM_BUSY_EN

When this bit is logic 1 the BUSY signal from the S/UNI-ATLAS-3200 will be asserted whenever the internal DRAM is busy. When 0 the BUSY signal will not react to DRAM activity.

POS_UL3B

When POS_UL3B is logic 1, then the device uses POS-PHY Level 3 signaling. When POS_UL3B is logic 0, the device uses UTOPIA Level 3 signaling. This bit defaults to logic 1 to ensure that all pins that can be inputs or outputs, power up as inputs.

Egress_IngressB

When Egress_IngressB is logic 1, the device is in Egress mode, and the TxPHY and TxLink blocks are used. When Egress_IngressB is logic 0, the device is in Ingress mode and the RxLink and RxPHY blocks are used. When in egress mode, the RxLink and RxPhy blocks should be left in soft reset. When in ingress mode, the TxLink and TxPhy blocks should be left in soft reset.

FREE[7:0]

These bits have no function. They can be used by software to store configuration information, software version codes, or other user information.

Reserved

This bit must be programmed to logic 0 for correct operation..

Reserved

This bit must be programmed to logic 0 for correct operation.

Register 0x001: S/UNI-ATLAS-3200 Identity / Load Counts

Bit	Type	Function	Default
31:24		Unused	X
23	R	MKT_NUM[15]	0
22	R	MKT_NUM[14]	1
21	R	MKT_NUM[13]	1
20	R	MKT_NUM[12]	1
19	R	MKT_NUM[11]	0
18	R	MKT_NUM[10]	0
17	R	MKT_NUM[9]	1
16	R	MKT_NUM[8]	1
15	R	MKT_NUM[7]	0
14	R	MKT_NUM[6]	0
13	R	MKT_NUM[5]	1
12	R	MKT_NUM[4]	0
11	R	MKT_NUM[3]	0
10	R	MKT_NUM[2]	1
9	R	MKT_NUM[1]	0
8	R	MKT_NUM[0]	1
7	R	TIP	X
6	R	TYPE[2]	0
5	R	TYPE[1]	1
4	R	TYPE[0]	0
3	R	ID[3]	0
2	R	ID[2]	0
1	R	ID[1]	0
0	R	ID[0]	0

Writing to this register simultaneously loads all the aggregate and per-PHY counts in the Input, Output, and Bypass SDQ FIFOs, and the counts in the BCIFs. While this load is in progress, the TIP bit will be logic 1 in this register. When the load is complete, the TIP bit becomes 0.

ID[3:0]

The ID bits can be read to provide a binary number indicating the S/UNI-ATLAS-3200 feature version.

TYPE[2:0]

The TYPE bits can be read to distinguish the S/UNI-ATLAS-3200 from the other members of the S/UNI-ATLAS-3200 family of devices. “001” in this field indicates the S/UNI-ATLAS, while “010” indicates the S/UNI-S/UNI-ATLAS-3200.

TIP

The Transfer In Progress bit is logic 1 while the Input BCIF, Output BCIF, Input SDQ, Output SDQ, or SDQ FIFO counts are being updated. Once the update is complete, TIP becomes logic 0 to indicate that the counts are valid; however, another transfer should not be requested for at least 100ns after TIP returns to 0.

MKT_NUM[15:0]

The Marketing Number register returns 0x7325, the marketing number of the S/UNI-S/UNI-ATLAS-3200.

Register 0x002: Master Interrupt Status #1

Bit	Type	Function	Default
31	R	REG3I	X
30	R	OBCIFFULLI	X
29	R	OBOVFLI	X
28	R	IBCIFFULLI	X
27	R	IBPRTYI	X
26	R	IBOVFLI	X
25	R	IBSOCI	X
24	R	UPCAI	X
23	R	UPOVRI	X
22	R	INSRDYI	X
21	R	Reserved	X
20	R	SlowBGI	X
19	R	DeadPHYI	X
18	R	CROI	X
17	R	XCROI	X
16	R	CROFULLI	X
15	R	COSI	X
14	R	XCOSI	X
13	R	COSFULLI	X
12	R	PHYPOLI	X
11	R	POLI	X
10	R	OAM_FAILI	X
9	R	END_RDII	X
8	R	SEG_RDII	X
7	R	END_AISI	X
6	R	SEG_AISI	X
5	R	END_CCI	X
4	R	SEG_CCI	X
3	R	SRCH_ERRI	X
2	R	OAM_ERRI	X
1	R	INVAL_PTI_VCII	X
0	R	UNPROV_I	X

UNPROVI

The UNPROVI bit indicates that a cell with an unprovisioned VPI/VCI combination or invalid routing bits has been received. When logic 1, the UNPROVI bit indicates that one or more VC Table searches have not resulted in a match. This bit is cleared when this register is read.

INVAL_PTIVCII

The INVAL_PTIVCII bit indicates a cell with an invalid PTI or VCI field has been received. When logic 1, the INVAL_PTIVCII bit indicates one or more F5 cells have the PTI field with PTI='111', F4 cells with an invalid VCI field (VCI 7 through 15) or at least one VP Resource Management cell has been received with PTI not equal to '110'. This bit is cleared when this register is read.

OAM_ERRI

The OAMERRI bit indicates one or more OAM cell with an incorrect OAM Type, Function Type or Error Detection Code field (CRC-10) has been received. When logic 1, the OAMERRI bit indicates one or more errored OAM cells have been received. This bit may also indicate one or more Resource Management cell with an incorrect CRC-10 has been received. This bit is cleared when this register is read.

SRCH_ERRI

The search error bit (SRCHERRI) indicates that a VPI/VCI search in the VC Table has failed due to an improperly constructed secondary search table (i.e. the secondary search takes more than 45 branches) or a parity bit error on the external SRAM (correlate with SPRTY[7:0]). This bit is cleared when this register is read.

SEG_CCI

The Seg_CCI bit indicates that a Segment Continuity Check alarm bit in the VC Table has changed state. When logic 1, the SEG_CCI bit indicates the Segment_CC_Alarm bit in the VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

END_CCI

The END_CCI bit indicates that an End-to-End Continuity Check alarm (in the VC Table) has changed state. When logic 1, the END_CCI bit indicates the End_to_End_CC_Alarm bit in the VC Table has changed state for one or more virtual connection. This bit is cleared when this register is read.

SEG_AISI

The SEG_AISI bit indicates that a Segment AIS alarm (in the VC Table) has changed state. When logic 1, the SEG_AISI bit indicates the Segment AIS Alarm bit in the VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

END_AISI

The END_AISI bit indicates that an End-to-End AIS alarm (in the VC Table) has changed state. When logic 1, the END_AISI bit indicates the End-to-End AIS Alarm bit in the VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

SEG_RDII

The SEG_RDII bit indicates that a Segment RDI alarm (in the VC Table) has changed state. When logic 1, the SEG_RDII bit indicates the Segment RDI Alarm bit in the VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

END_RDII

The END_RDII bit indicates that an End-to-End RDI alarm (in the VC Table) has changed state. When logic 1, the END_RDII bit indicates the End-to-End RDI Alarm bit in the VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

OAM_FAILI

The OAM_FAILI bit indicates that the OAM_Failure bit in the VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

POLI

The POLI bit indicates a non-compliant cell has been received. When logic 1, the POLI bit indicates one or more cells have violated the traffic contract since the last read of this register. This bit is cleared when this register is read.

PHYPOLI

The PHY Policing Interrupt bit (PHYPOLI) indicates that one or more cells have violated one or more per-PHY policing contracts. When logic 1, the PHYPOLI bit indicates one or more cells have violated one or more of the 48 PHY policing instances. This bit is cleared when this register is read.

COSFULLI

The Change of State FIFO Full Interrupt bit (COSFULLI) indicates that the Change of State FIFO is full. When logic 1, the COSFULLI indicates that the Change of State FIFO is full, and no more change of state notifications can be written into the FIFO. This suspends a background process until FIFO space becomes free. It is the responsibility of the management software to ensure this FIFO is read often enough to ensure the notification of changes of state are compliant with Bellcore and ITU standards. This bit is cleared when this register is read.

XCOSI

The Excessive Change of State FIFO Interrupt bit (XCOSI) indicates that the Change of State FIFO is half-full. When logic 1, the XCOSI indicates that the Change of State FIFO is half-full with changes of connection state information. This indicates that the Change of State FIFO should be read quickly to avoid the Change of State FIFO from becoming full. It is the responsibility of the management software to ensure the Change of State FIFO is read often enough to ensure the notification of changes of state are compliant with Bellcore and ITU standards. This bit is cleared when this register is read.

COSI

The Change of State Interrupt bit (COSI) indicates that the Change of State FIFO has become non-empty.

CROFULLI

The Count Rollover FIFO Full Interrupt bit (CROFULLI) indicates that the Count Rollover FIFO is full. When logic 1, the CROFULLI indicates that the Count Rollover FIFO is full, and no more rollover notifications can be written into the FIFO. This causes the counts to retain their MSBs high until room is made in the Count Rollover FIFO.

XCROI

The Excessive Count Rollover FIFO Interrupt bit (XCROI) indicates that the Count Rollover FIFO is half-full. This indicates that the Count Rollover FIFO should be read quickly to avoid it becoming full.

CROI

The Count Rollover FIFO Interrupt bit (CROI) indicates that the Count Rollover FIFO has become non-empty.

DEADPHYI

The Inoperative PHY Interrupt bit (DEADPHYI) indicates that a PHY has had cells ready to be transmitted, and has not accepted any cells whatsoever, for a programmable period of time. The inoperative PHY may be identified by reading the Inoperative PHY Indication registers.

SlowBGI

The Slow Background Process Interrupt (SlowBGI) indicates that, for three consecutive seconds, the TAT update background process was unable to complete a full set of background processing. This may indicate that the S/UNI-ATLAS-3200 is overloaded with both cells and microprocessor accesses to DRAM or SRAM.

UPCAI

The UPCAI bit indicates that a cell has been written into the Microprocessor Cell extract FIFO, and is ready for extraction by an external processor. When logic 1, the UPCAI bit indicates that the EXTCA bit in the Microprocessor Cell Interface Control and Status register has been asserted. The UPCAI bit is cleared when this register is read.

UPOVRI

The UPOVRI bit indicates that a cell was written to the Output Microprocessor Interface, but the FIFO was full, and so the cell was discarded.

INSRDYI

The INSRDYI bit indicates the Microprocessor Cell Interface insert FIFO is ready for another cell. This bit is cleared when this register is read.

IBSOCI

The Input BCIF SOC interrupt indicates that either the IBCIF received a SOC when it was not expecting it, or did not receive a SOC when it was expecting one. This bit is cleared when this register is read.

IBOVFLI

The IBOVFLI bit is set to logic 1 when a cell has been written into the Input BCIF when the IBCIF was already full This bit is cleared when this register is read.

IBPRTYI

When logic 1, the IBPRTYI bit indicates a parity error over the IBDAT[15:0] data bus. This bit is cleared when this register is read.

IBCIFFULLI

When logic 1, the IBCIFFULLI bit indicates that the Input Backward Cell Interface FIFO is full, and cannot accept any more cells generated by the opposite direction S/UNI-ATLAS-3200. This results in the opposite direction's Output BCIF being backed up. If the IBCIFFULLI interrupt persists, the rate at which cells are allowed from the BCIF may have to be increased, so that RDI and Backward Reporting PM cells can be generated at the appropriate intervals. This bit is cleared when this register is read.

OBOVFLI

When logic 1, the OBOVFLI bit indicates that a cell was written to the Output BCIF when it was already full. This indicates that one or more cells destined to be routed to the OBCIF (such as Loopback cells) has been dropped. RDI and Backward PM cells will not be dropped in this fashion, since the information needed to generate them later is stored in the VC and PM tables.

OBCIFFULLI

When logic 1, the OBCIFFULLI bit indicates that the Output Backward Cell Interface FIFO is full, and cannot accept any more cells generated by the Cell Processor. This affects how often RDI and Backward Reporting PM cells can be generated and sent to the backwards direction S/UNI-ATLAS-3200. If the OBCIFFULLI interrupt persists, the rate at which cells are allowed into the cell stream from the BCIF in the backwards direction S/UNI-ATLAS-3200 may have to be increased, so that RDI and Backward Reporting PM cells can be generated at the appropriate intervals. This bit is cleared when this register is read.

REG3I

The REG3I bit indicates that at least one bit in Register 0x003, S/UNI-ATLAS-3200 Master Interrupt Status #2 is currently asserted.

Register 0x003: Master Interrupt Status #2

Bit	Type	Function	Default
31:23	R	Reserved	X
22	R	Bypass_SDQ_I	
21	R	Output_SDQ_I	X
20	R	Tx_Link_I	X
19	R	Rx_PHY_I	X
18	R	Input_SDQ_I	X
17	R	Tx_PHY_I	X
16	R	Rx_Link_I	X
15	R	Reserved	X
14	R	OCLKDLLERRI	X
13	R	ICLKDLLERRI	X
12	R	SYSCLKDLLERRI	X
11	R	Reserved	X
10	R	Reserved	X
9	R	Reserved	X
8	R	DRAM_ERRI	X
7	R	SPRTYI[7]	X
6	R	SPRTYI[6]	X
5	R	SPRTYI[5]	X
4	R	SPRTYI[4]	X
3	R	SPRTYI[3]	X
2	R	SPRTYI[2]	X
1	R	SPRTYI[1]	X
0	R	SPRTYI[0]	X

SPRTYI[7:0]

The SPRTYI[7:0] bits indicate a parity error has been detected on the external SRAM interface SDAT[63:0], data bus. When logic 1, the SPRTYI[7:0] bits indicate the following:
SPRTYI[7]: Parity error over inputs SDAT[63:56]
SPRTYI[6]: Parity error over inputs SDAT[55:48]
SPRTYI[5]: Parity error over inputs SDAT[47:40]
SPRTYI[4]: Parity error over inputs SDAT[39:32]
SPRTYI[3]: Parity error over inputs SDAT[31:24]
SPRTYI[2]: Parity error over inputs SDAT[23:16]
SPRTYI[1]: Parity error over inputs SDAT[15:8]
SPRTYI[0]: Parity error over inputs SDAT[7:0]

All bits are cleared when this register is read.

DRAM_ERRI

The DRAM_ERRI bit indicates that a DRAM read detected a CRC-10 violation. This bit is cleared when this register is read.

SYSCLKDLLERRI

The SYSCLK DLL Error Interrupt indicates that the DLL on SYSCLK found that it was outside of its capture range. This bit is cleared when this register is read.

ICLKDLLERRI:

The Input Clock DLL Error Interrupt indicates that the DLL on ICLK found that it was outside of its capture range. This bit is cleared when this register is read.

OCLKDLLERRI

The Output Clock DLL Error Interrupt indicates that the DLL on OCLK found that it was outside of its capture range. This bit is cleared when this register is read.

Rx_Link_I

The Rx Link Interrupt bit indicates that the Rx Link block has declared an interrupt, which may be read (and cleared) in the RxL Interrupt Register. Only interrupts whose enable bits are logic 1 in the RxL Interrupt Enable register in Section 11.6 will cause this bit to become logic 1.

Tx_PHY_I

The Tx PHY Interrupt bit indicates that the Tx PHY block has declared an interrupt, which may be read (and cleared) in the TxP Interrupt Register. Only interrupts whose enable bits are logic 1 in the TxP Interrupt Enable register in Section 11.7 will cause this bit to become logic 1.

Input_SDQ_I

The Input SDQ Interrupt bit indicates that the Input SDQ block has declared an interrupt, which may be read (and cleared) in the Input SDQ Interrupt Register. Only interrupts whose enable bits are logic 1 in the Input SDQ Interrupts register in section 11.8 will cause this bit to become logic 1.

Rx_PHY_I

The Rx PHY Interrupt bit indicates that the Rx PHY block has declared an interrupt, which may be read (and cleared) in the RxP Interrupt Register. Only interrupts whose enable bits are logic 1 in the RxP Interrupt Enable register in section 11.9 will cause this bit to become logic 1.

Tx_Link_I

The Tx Link Interrupt bit indicates that the Tx Link block has declared an interrupt, which may be read (and cleared) in the TxL Interrupt Register. . Only interrupts whose enable bits are logic 1 in the TxL Interrupt Enable register in Section 11.10 will cause this bit to become logic 1.

Output_SDQ_I

The Output SDQ Interrupt bit indicates that the Output SDQ block has declared an interrupt, which may be read (and cleared) in the Output SDQ Interrupt Register. Only interrupts whose enable bits are logic 1 in the Output SDQ Interrupts register in Section 11.11 will cause this bit to become logic 1.

Bypass_SDQ_I

The Bypass SDQ Interrupt bit indicates that the Bypass SDQ block has declared an interrupt, which may be read (and cleared) in the Bypass SDQ Interrupt Register. Only interrupts whose enable bits are logic 1 in the Bypass SDQ Interrupts register in Section 11.12 will cause this bit to become logic 1.

Register 0x004: Master Interrupt Enable #1

Bit	Type	Function	Default
31	R/W	Reserved	0
30	R/W	OBCIFFULLE	0
29	R/W	OBOVFLE	0
28	R/W	IBCIFFULLE	0
27	R/W	IBPRTYE	0
26	R/W	IBOVFLE	0
25	R/W	IBSOCE	0
24	R/W	UPCAE	0
23	R/W	UPOVRE	0
22	R/W	INSRDYE	0
21	R/W	Reserved	0
20	R/W	SlowBGE	0
19	R/W	DeadPHYE	0
18	R/W	CROE	0
17	R/W	XCROE	0
16	R/W	CROFULLE	0
15	R/W	COSE	0
14	R/W	XCOSE	0
13	R/W	COSFULLE	0
12	R/W	PHYPOLE	0
11	R/W	POLE	0
10	R/W	OAM_FAILE	0
9	R/W	END_RDIE	0
8	R/W	SEG_RDIE	0
7	R/W	END_AISE	0
6	R/W	SEG_AISE	0
5	R/W	END_CCE	0
4	R/W	SEG_CCE	0
3	R/W	SRCH_ERRE	0
2	R/W	OAM_ERRE	0
1	R/W	INVAL_PTI_VCI_E	0
0	R/W	UNPROV_E	0

The above enable bits control the corresponding interrupt status bits in the S/UNI-ATLAS-3200 Master Interrupt Status #1 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

Register 0x005: Master Interrupt Enable #2

Bit	Type	Function	Default
31:23	R/W	Reserved	X
22	R/W	Bypass_SDQ_E	0
21	R/W	Output_SDQ_E	0
20	R/W	Tx_Link_E	0
19	R/W	Rx_PHY_E	0
18	R/W	Input_SDQ_E	0
17	R/W	Tx_PHY_E	0
16	R/W	Rx_Link_E	0
15	R/W	Reserved	0
14	R/W	OCLKDLLERRE	0
13	R/W	ICLKDLLERRE	0
12	R/W	SYSCLKDLLERRE	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	DRAM_ERRE	0
7	R/W	SPRTYE[7]	0
6	R/W	SPRTYE[6]	0
5	R/W	SPRTYE[5]	0
4	R/W	SPRTYE[4]	0
3	R/W	SPRTYE[3]	0
2	R/W	SPRTYE[2]	0
1	R/W	SPRTYE[1]	0
0	R/W	SPRTYE[0]	0

The above enable bits control the corresponding interrupt status bits in the S/UNI-ATLAS-3200 Master Interrupt Status #2 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

Register 0x006: Master Clock Monitor

Bit	Type	Function	Default
31:9		Unused	X
8	R/W	RSTDLL	0
7	R	DLLRUN	X
6	R	HALFSECCLKA	X
5	R	OBCIFCLKA	X
4	R	IBCIFCLKA	X
3	R	OCLKA	X
2	R	ICLKA	X
1	R	XCLKA	X
0	R	SYSCLKA	X

This register provides activity monitoring on S/UNI-ATLAS-3200 clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the clock activity bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock or DLL failures.

SYSCLKA

The System Clock active (SYSCKLA) bit monitors for low to high transitions on the SYSCLK input. SYSCLKA is set high on a rising edge of SYSCLK, and is set low when this register is read.

XCLKA

The Crystal Clock active (XCKLA) bit monitors for low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read.

ICLKA

The Input Clock active (ICLKA) bit monitors for low to high transitions on the RLU_CLK/TPU_CLK/RlP_CLK/TPP_CLK input. ICLKA is set high on a rising edge of this clock, and is set low when this register is read.

OCLKA

The Output Clock active (OCLKA) bit monitors for low to high transitions on the RPU_CLK/TLU_CLK/RPP_CLK/TLP_CLK input. OCLKA is set high on a rising edge of this clock, and is set low when this register is read.

IBCIFCLKA

The Input BCIF Clock Active (IBCIFCLKA) bit monitors for low to high transitions on the BI_CLK input. IBCIFCLKA is set high on a rising edge of this clock, and is set low when this register is read.

OBCIFCLKA

The Output BCIF Clock Active (OBCIFCLKA) bit monitors for low to high transitions on the BO_CLK input. OBCIFCLKA is set high on a rising edge of this clock, and is set low when this register is read.

HALFSECCLKA

The Half Second Clock Active (HALFSECCLKA) bit monitors for low to high transitions on the HALFSECCLK input. HALFSECCLKA is set high on a rising edge of this clock, and is set low when this register is read.

RSTDLL:

The Reset Delay Locked Loop register bit (RSTDLL) controls the resetting of the S/UNI-ATLAS-3200 DLL components. If this bit is logic 1, the SYSCLK, OCLK, and ICLK DLL components will be reset.

DLLRUN

The Delay Locked Loop run register bit (DLLRUN). When logic 1, this bit indicates that all DLL components have locked to their input clocks. This bit is only valid when SYSCLK, ICIF_CLK, and OCIF_CLK are running.

11.3 Microprocessor Cell Interface

Register 0x020: Microprocessor Cell Interface Control and Status

Bit	Type	Function	Default
31:27		Unused	x
26	R	INSRDY	X
25	W	WRSOC	0
24	R/W	PHY[5]	0
23	R/W	PHY[4]	0
22	R/W	PHY[3]	0
21	R/W	PHY[2]	0
20	R/W	PHY[1]	0
19	R/W	PHY[0]	0
18	R/W	PROC_CELL	0
17	R/W	CRC10	0
16	R/W	INSRST	0
15:6		Unused	X
5	R	RSOC	0
4	R	EXTCA	X
3	W	ABORT	0
2	W	RESTART	0
1	R/W	DMAREQINV	0
0	R/W	EXTRST	0

Bits [15 0] Cell Extraction

EXTRST

The EXTRST is used to reset the Microprocessor Extract Cell Interface. When EXTRST is set to logic 0, the Extract FIFO operates normally. When EXTRST is logic 1, the extract FIFO is immediately emptied and ignores writes. The extract FIFO remains empty and continues to ignore writes until a logic 0 is written to EXTRST. While asserted, EXTRST overrides all other bits affecting the Microprocessor Extract Cell Interface.

DMAREQINV

The DMAREQINV bit inverts the polarity of the UP_DMAREQ output. If DMAREQINV is a logic 0, the UP_DMAREQ output is active high. If DMAREQINV is a logic 1, the UP_DMAREQ output is active low.

RESTART

The restart cell read (RESTART) bit resets the microprocessor cell read pointer. If RESTART is set to logic 1 during a cell read, the next word read from the Microprocessor Cell Data register will be the first word of the current cell. Subsequent reads from the Microprocessor Cell Data register return the remaining words of the cell.

RESTART is not readable, and is cleared upon a read of the Microprocessor Cell Data register. RESTART and ABORT should not be simultaneously asserted.

ABORT

The read abort (ABORT) bit allows the microprocessor to discard a cell without reading the contents. If ABORT is logic 1, the current cell being read is purged from the extract FIFO and the DMAREQ output will be deasserted.

ABORT is not readable, and is cleared upon a read of the Microprocessor Cell Data register. ABORT and RESTART should not be simultaneously asserted.

EXTCA

The microprocessor cell available (EXTCA) status bit indicates that at least one cell is present in the cell extract buffer. EXTCA is set to logic 1 when the last word of a cell is received. EXTCA is cleared to logic 0 when the last word in the buffer is read by the microprocessor. If multiple cells exist in the buffer, then EXTCA will remain at logic 1 until the last word of the last cell is read.

Assertion of the EXTCA status bit also results in a maskable interrupt.

RSOC

The RSOC bit is logic 1 when the data in MCD[31:0] contains the first d-word (of 16) in a cell. This word will be part of the Microprocessor Cell Info field if the Cell_Info_to_UP bit is set in the CP Configuration Register.

Bits [31 16] Cell Insertion

INSRST

The INSRST bit is used to reset the Microprocessor Insert Cell Interface. When INSRST is set to logic 0, the insert FIFO operates normally. When INSRST is set to logic 1, the insert FIFO is immediately emptied and ignores writes. The insert FIFO remains empty and continues to ignore writes until a logic 0 is written into INSRST.

Any transfer from the insert FIFO currently in progress will be aborted. While asserted, INSRST overrides all other bits affecting the Microprocessor Insert Cell Interface.

CRC10

The CRC10 bit forces the generation of the Error Detection Code (EDC) for cells written into the insert FIFO. If CRC10 is set to logic 1 prior to assembling the cell in the buffer, the last 10-bits of the cell are overwritten with the CRC-10 value calculated over the information field (payload) of the cell. When CRC10 is logic 1, the last 16 bits of the cell are typically written to zero, and the CRC-10 replaces the 10 least significant bits.

PROC_CELL

The Cell Process Enable (PROC_CELL) bit controls the processing of the current cell written into the insert FIFO. If PROC_CELL was set to logic 1 prior to writing the cell in the buffer, the current is subject to all cell processing functions, just as if the cell had been inserted through the Input Cell Interface. Therefore, the header information and PHYID must correspond to a provisioned VC, or the cell will be discarded.

If PROC_CELL is logic 0, the current cell is passed to the output cell interface without modification, with the exception that appended bytes may be added or stripped off to ensure a correct cell length for the selected interface. The cell need not belong to a provisioned connection. The cell is not processed.

PHYID[5:0]

The PHY identification bits determine the PHY association of the current cell being written by the microprocessor. The state of the PHY[5:0] when the WRSOC is set selects the PHY device for that cell:

PHY[5:0] = 000000, PHY #1/Single PHY.
PHY[5:0] = 000001, PHY #2
PHY[5:0] = 000010, PHY #3
…
PHY[5:0] = 101111, PHY #48.

WRSOC

The write start of cell (WRSOC) bit must identify the first word of the current cell that the microprocessor is writing. If WRSOC is logic 1, the next word written into the Microprocessor Cell Data register becomes the first word of the cell. Subsequent writes to the Microprocessor Cell Data register fill the remainder of the cell sequentially, to a total of 16 writes. If WRSOC is set again before a complete cell is written, the existing contents will be overwritten without transmission.

WRSOC is not readable.

INSRDY

The insert buffer ready status (INSRDY) bit indicates that the insert FIFO is ready to accept another cell. INSRDY is cleared once a full cell of 64 bytes has been written into the MCIF. Reassertion of the INSRDY bit results in the assertion of a maskable interrupt.

Register 0x021: Microprocessor Cell Data

Bit	Type	Function	Default
31	R/W	MCD[31]	X
30	R/W	MCD[30]	X
29	R/W	MCD[29]	X
28	R/W	MCD[28]	X
27	R/W	MCD[27]	X
26	R/W	MCD[26]	X
25	R/W	MCD[25]	X
24	R/W	MCD[24]	X
23	R/W	MCD[23]	X
22	R/W	MCD[22]	X
21	R/W	MCD[21]	X
20	R/W	MCD[20]	X
19	R/W	MCD[19]	X
18	R/W	MCD[18]	X
17	R/W	MCD[17]	X
16	R/W	MCD[16]	X
15	R/W	MCD[15]	X
14	R/W	MCD[14]	X
13	R/W	MCD[13]	X
12	R/W	MCD[12]	X
11	R/W	MCD[11]	X
10	R/W	MCD[10]	X
9	R/W	MCD[9]	X
8	R/W	MCD[8]	X
7	R/W	MCD[7]	X
6	R/W	MCD[6]	X
5	R/W	MCD[5]	X
4	R/W	MCD[4]	X
3	R/W	MCD[3]	X
2	R/W	MCD[2]	X
1	R/W	MCD[1]	X
0	R/W	MCD[0]	X

MCD[31:0]

The MCD[31:0] contains the cell data destined to, or read from, the Microprocessor Cell Interface.

For the cell extract FIFO, the EXTCA bit and associated maskable interrupt indicate that a cell is available to be read. Alternatively, the assertion of the DMAREQ output signals the presence of the cell. Reads of this register return the words of the cell starting with the first. If necessary, the read pointer can be reset to the start of the current cell by setting the RESTART bit. Alternatively, the read pointer can be reset to the start of the next cell by setting the ABORT bit.

In a polled mode, the INSRDY register bit indicates that the microprocessor may write another cell. For interrupt driven systems, the INSRDYI interrupt status bit and associated maskable interrupt indicate that a cell may be written.

Register 0x022: MCIF Dropped Cells Counter

Bit	Type	Function	Default
31:8		Unused	X
7:0	R	DCOUNT[7:0]	X

This register provides a count of cells dropped due to parity errors or FIFO overflow.

DCOUNT[7:0]

A write to this register or the S/UNI-ATLAS-3200 Identity/Load Counts register loads this register with the number of cells dropped by the OMCIF due FIFO overflow since the last such write, and resets the internal counter to zero. The update is done in such a fashion that no events are missed if a counter reset and a dropped cell occur simultaneously. During this transfer, the TIP bit in the S/UNI-ATLAS-3200 Identity/Load Counts register will be logic 1. The contents of this register are valid when the TIP bit returns to logic 0. If this register is not polled regularly, the count value will saturate at 0xFF.

11.4 Backward Cell Interface

Register 0x030: Input Backwards Cell Interface Configuration

Bit	Type	Function	Default
31:5		Unused	X
4	R/W	CALEVEL0	0
3	R/W	IBCIF_DROP_PRTY	0
2	R/W	IBCIF_EVEN_PRTY	0
1	R/W	IBCIF_TxSlave	0
0	R/W	IBCIFRST	1

CALEVEL0

If CALEVEL0 is logic 1, BI_CLAV is deasserted after the last word of the cell is transferred into the FIFO. (i.e. the FIFO is full). If CALEVEL0 is logic 0, then BO_CLAV is deasserted 4 words before the end of the last cell that can be accepted, to indicate that the Input BCIF cannot accept another cell.

IBCIFRST

The IBCIFRST bit is used to reset the 16-cell Input Backwards Cell Interface FIFO. When IBCIFRST is set to logic zero, the FIFO operates normally. When IBCIFRST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to IBCIFRST.

N.B. This FIFO must be reset at startup.

IBCIF_TxSlave

When this bit is a logic 0, then the Input Backwards Cell Interface is an Rx Master interface, and is configured to interact with another S/UNI-ATLAS-3200 Output Backwards Cell Interface. When this bit is logic 1, the Input Backwards Cell Interface is a Tx Slave interface, and is configured to interact with a tester or ASIC.

IBCIF_EVEN_PRTY

When this bit is logic 1, the BI_PAR pin is expected to complete even parity for the BI_DAT[15:0] bus. When it is logic 0, the BI_PAR pin is expected to complete odd parity for the BI_DAT[15:0] bus.

IBCIF_DROP_PRTY

When this bit is logic 1, all cells written into the Input BCIF which have bad parity are discarded. When this bit is logic 0, cells written into the Input BCIF are not discarded due to parity errors. In any event, parity errors may be configured to cause interrupts by setting the IBPRTYE bit to logic 1 in the Master Interrupt Enable #1 Register.

Register 0x031: IBCIF Dropped Cells Counter

Bit	Type	Function	Default
31:8		Unused	X
7:0	R	DCOUNT[7:0]	X

This register provides a count of cells dropped due to parity errors or FIFO overflow.

DCOUNT[7:0]

A write to this register, to the IBCIF Read Cells Counter, or the S/UNI-ATLAS-3200 Identity/Load Counts register loads this register with the number of cells dropped by the IBCIF due to parity errors or FIFO overflow since the last such write, and resets the internal counter to zero. The update is done in such a fashion that no events are missed if a counter reset and a dropped cell occur simultaneously. During this transfer, the TIP bit in the S/UNI-ATLAS-3200 Identity/Load Counts register will be logic 1. The contents of this register are valid when the TIP bit returns to logic 0; however, another transfer should not be requested for at least 100ns after TIP returns to 0. If this register is not polled regularly, the count value will saturate at 0xFF.

Register 0x032: IBCIF Read Cells Counter

Bit	Type	Function	Default
31:24		Unused	X
23:0	R	CCOUNT[23:0]	X

This register provides a count of all cells read out of the IBCIF FIFO.

CCOUNT[23:0]

A write to this register, to the IBCIF Dropped Cells Counter, or the S/UNI-ATLAS-3200 Identity/Load Counts register loads this register with the number of cells read out of the IBCIF since the last such write, and resets the internal counter to zero. The update is done in such a fashion that no events are missed if a counter reset and a dropped cell occur simultaneously. During this transfer, the TIP bit in the S/UNI-ATLAS-3200 Identity/Load Counts register will be logic 1. The contents of this register are valid when the TIP bit returns to logic 0; however, another transfer should not be requested for at least 100ns after TIP returns to 0. If this register is not polled regularly, the count value will saturate at 0xFFFFFF.

Register 0x038: Output Backwards Cell Interface Configuration

Bit	Type	Function	Default
31:5		Unused	X
4	R/W	CALEVEL0	0
3	R/W	Reserved	0
2	R/W	OBCIF_EVEN_PRTY	0
1	R/W	Reserved	0
0	R/W	OBCIFRST	1

CALEVEL0

If CALEVEL0 is logic 1, BO_CLAV is deasserted after the last word of the FIFO is transferrred (i.e. the FIFO is empty). If CALEVEL0 is logic 0, then BO_CLAV is deasserted 4 words before the end of the last cell to indicate that the Output BCIF cannot transfer another cell.

OBCIFRST

The OBCIFRST bit is used to reset the 16-cell Output Backwards Cell Interface FIFO. When OBCIFRST is set to logic zero, the FIFO operates normally. When OBCIFRST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to OBCIFRST.

N.B. This FIFO must be reset at startup.

OBCIF_EVEN_PRTY

When this bit is logic 1, the BO_PAR pin completes even parity for the BO_DAT[15:0] bus. When it is logic 0, the BO_PAR pin completes odd parity for the BO_DAT[15:0] bus.

Reserved

The reserved bits must be programmed to logic 0 for correct operation.

Register 0x039: OBCIF Dropped Cells Counter

Bit	Type	Function	Default
31:8		Unused	X
7:0	R	DCOUNT[7:0]	X

This register provides a count of cells dropped by the OBCIF due toFIFO overflow. Overflow of the OBCIF can only occur for Loopback cells, and cells routed to the BCIF via the VC_to_BCIF function. RDI cells and Bwd PM cells will be delayed and sent later if the OBCIF is full, and thus cannot be lost due to FIFO overflow. The OBCIF is drained at the lesser of the opposite-direction Backward Cell Interface Pacing rate, and the capacity of the BCIF link (approximately 1.3 million cells per second).

DCOUNT[7:0]

A write to this register or the S/UNI-ATLAS-3200 Identity/Load Counts register loads this register with the number of cells dropped by the OBCIF due to FIFO overflow since the last such write, and resets the internal counter to zero. The update is done in such a fashion that no events are missed if a counter reset and a dropped cell occur simultaneously. During this transfer, the TIP bit in the S/UNI-ATLAS-3200 Identity/Load Counts register will be logic 1. The contents of this register are valid when the TIP bit returns to logic 0; however, another transfer should not be requested for at least 100ns after TIP returns to 0. If this register is not polled regularly, the count value will saturate at 0xFF.

Register 0x03A: OBCIF Read Cells Counter

Bit	Type	Function	Default
31:24		Unused	X
23:0	R	CCOUNT[23:0]	X

This register provides a count of all cells read out of the OBCIF FIFO.

CCOUNT[23:0]

A write to this register or the S/UNI-ATLAS-3200 Identity/Load Counts register loads this register with the number of cells read out of by the OBCIF since the last such write, and resets the internal counter to zero. The update is done in such a fashion that no events are missed if a counter reset and a dropped cell occur simultaneously. During this transfer, the TIP bit in the S/UNI-ATLAS-3200 Identity/Load Counts register will be logic 1. The contents of this register are valid when the TIP bit returns to logic 0; however, another transfer should not be requested for at least 100ns after TIP returns to 0. If this register is not polled regularly, the count value will saturate at 0xFFFFFF

Register 0x040: SYSCLK Delay Locked Loop Register 1

Bit	Type	Function	Default
31: 8		Unused	X
7		Unused	X
6		Unused	X
5	R/W	FUNC	0
4	R/W	OVERRIDE	0
3		Unused	X
2		Unused	X
1	R/W	VERN_EN	0
0	R/W	LOCK	0

The DLL Configuration Register controls the basic operation of the DLL.

CAUTION: The following register bits should not be changed after reset. Modifying any of the default values can result in unpredictable or no operation at all. It is highly recommend that these register bits remain unchanged.

LOCK

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after the lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the RFCLK and the reference clock inputs. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between the RFCLK and the reference clock inputs for the first time.

VERN_EN

The vernier enable register (VERN_EN) forces the DLL to ignore the phase detector and use the tap number specified by the VERNIER[7:0] register bits. When VERN_EN is set to logic zero, the DLL operates normally adjusting the phase offset based on the phase detector. When VERN_EN is set to logic one, the delay line uses the tap specified by the VERNIER[7:0] register bits.

OVERRIDE

The override control (OVERRIDE) disables the DLL operation. When OVERRIDE is set low, the DLL generates the DLLCLK by delaying the RFCLK until the rising edge of the reference clock occurs at the same time as the rising edge of RFCLK. When OVERRIDE is set high, the DLLCLK output is a buffered version of the RFCLK input. This feature provides a back-up strategy in case the DLL does not operate correctly.

FUNC

The functional control (FUNC) is a multipurpose configuration signal for top-level uses. The TSB FUNC output is high when FUNC is set high. The TSB FUNC output is low when FUNC is set low.

Register 0x041: SYSCLK DLL Register 2

Bit	Type	Function	Default
31:8		Unused	X
7	R/W	VERNIER[7]	0
6	R/W	VERNIER[6]	0
5	R/W	VERNIER[5]	0
4	R/W	VERNIER[4]	0
3	R/W	VERNIER[3]	0
2	R/W	VERNIER[2]	0
1	R/W	VERNIER[1]	0
0	R/W	VERNIER[0]	0

The Vernier Control Register provides the delay line tap control when using the vernier option.

VERNIER[7:0]

The vernier tap register bits VERNIER[7:0] specifies the phase delay through the DLL when using the vernier feature. When VERN_EN is set high, the VERNIER[7:0] registers specify the delay tap used. When VERN_EN is set low, the VERNIER[7:0] register is ignored. A VERNIER[7:0] value of all zeros specifies the delay tap with the minimum delay through the delay line. A VERNIER[7:0] value of all ones specifies the delay tap with the maximum delay through the delay line.

Register 0x042: SYSCLK DLL Register 3

Bit	Type	Function	Default
31:8		Unused	X
7	R	TAP[7]	X
6	R	TAP[6]	X
5	R	TAP[5]	X
4	R	TAP[4]	X
3	R	TAP[3]	X
2	R	TAP[2]	X
1	R	TAP[1]	X
0	R	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock. Writing to this register performs a software reset of the DLL.

TAP[7:0]

The tap status register bits TAP[7:0] specifies the delay line tap the DLL is using to generate the outgoing clock DLLCLK. When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is all logic one, the DLL is using the delay line tap with maximum phase delay. TAP[7:0] is invalid when vernier enable VERN_EN is set to one.

Register 0x043: SYSCLK DLL Register 4

Bit	Type	Function	Default
31:8		Unused	X
7	R	SYSCLKI	X
6	R	REFCLKI	X
5	R	ERRORI	X
4	R	CHANGEI	X
3		Unused	X
2	R	ERROR	X
1	R	CHANGE	0
0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit RUN indicates the DLL has found a delay line tap in which the phase difference between the rising edge of REFCLK and the rising edge of SYSLCK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1. The RUN register bit is cleared only by a system reset or a software reset (writing to register 0x042).

CHANGE

The delay line tap change register bit CHANGE indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight SYSCLK cycles when the DLL moves to a new delay line tap.

CHANGEI

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one. The CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

REFCLKI

The reference clock event register bit REFCLKI provides a method to monitor activity on the reference clock. When the REFCLK primary input changes from a logic zero to a logic one, the REFCLKI register bit is set to logic one. The REFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

SYSCLKI

The system clock event register bit SYSLCKI provides a method to monitor activity on the system clock. When the SYSCLK primary input changes from a logic zero to a logic one, the SYSCLKI register bit is set to logic one. The SYSCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x048: ICLK Delay Locked Loop Register 1

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x040 for a complete description.

Register 0x049: ICLK DLL Register 2

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x041 for a complete description.

Register 0x04A: ICLK DLL Register 3

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x042 for a complete description.

Register 0x04B: ICLK DLL Register 4

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x043 for a complete description.

Register 0x050: OCLK Delay Locked Loop Register 1

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x040 for a complete description.

Register 0x051: OCLK DLL Register 2

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x041 for a complete description.

Register 0x052: OCLK DLL Register 3

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x042 for a complete description.

Register 0x053: OCLK DLL Register 4

The Operation of this register is identical to the SYSCLK Delay Locked Loop. Refer to register 0x043 for a complete description.

11.5 Cell Processor

11.5.1 General Configuration and Status

Register 0x100: Cell Processor Configuration

Bit	Type	Function	Default
31:29		Unused	X
28	R/W	Copy_FwPM_Timestamp	0
27	R/W	GEN_HALFSECCLK	0
26	R/W	F4SAISF5EAIS	0
25	R/W	F4SAISF5ERDI	0
24	R/W	F4EAISF5EAIS	0
23	R/W	F4EAISF5SRDI	0
22	R/W	ForceCC	0
21	R/W	AUTO_AIS	0
20	R/W	COS_DRAM_ERR_EN	0
19	R/W	Reserved	0
18	R/W	COS_Fail_EN	0
17	R/W	COS_FAIL_ONLY	0
16	R/W	COS_EN	0
15	R/W	Sat_Fast_PM_Counts	0
14	R/W	CRO_FIFO_EN	0
13	R/W	Alternate_Count	0
12	R/W	VP_RM_PTI6	0
11	R/W	Search_Verify_En	1
10	R/W	Inact_on_DRAM_Err	0
9	R/W	SRAM_Even_Parity	0
8	R/W	Cell_Info_to_OCIF	0
7	R/W	Timeout_to_UP	0
6	R/W	Reserved	0
5	R/W	Cell_Info_to_UP	0
4	R/W	XGFC	0
3	R/W	XUDF	0
2	R/W	XHEC	0
1	R/W	XPREPO	0
0	R/W	XVPIVCI	0

XVPIVCI

If the XVPIVCI bit is logic 1, VPI/VCI translation is globally enabled. The ATM cell VPI/VCI bytes can be replaced by the contents of the Translated VPI and Translated VCI words of the VC Table. If the GVPIVCI bit is logic 0, the incoming VPI/VCI combination is passed transparently.

Note that if the connection is F4 (ie. VPC, where the VCI field in the search key is coded as all zeros), then the VCI is passed through transparently, and if the connection is at a UNI, the translation of the GFC field is controlled by XGFC.

XPREPO

If the XPREPO bit is logic 1, substitution of prepend and postpend bytes is globally enabled. Any prepend or postpend bytes of an ATM cell are replaced by the contents of the Translated Pre/Po1 and Translated Pre/Po 2 words of the VC Table. If XPREPO is logic 0, prepend and postpend bytes pass through transparently.

XHEC

If the XHEC bit is logic 1, the HEC field of an ATM cell is replaced by the contents of the Translated HEC word of the VC Table. If GHEC is logic 0, the HEC field of an ATM cell is passed transparently.

XUDF

If the XUDF bit is logic 1, the UDF field of an ATM cell is replaced by the contents of the Translated UDF field in the VC Table. If GUDF is logic 0, the UDF field of an ATM cell is passed transparently.

XGFC

If the XGFC bit is logic 1 and the connection belongs to a UNI, then the GFC field is replaced by the top 4 bits of the Translated VPI field in the VC table. If XGFC is logic 0 and the connection belongs to a UNI, the GFC field is passed through transparently. If the connection belongs to an NNI, then this bit has no effect.

Cell_Info_to_UP

The Cell Info to UP bit allows the Microprocessor Cell Info Field to replace the two Prepend/Postpends of a cell extracted to the Microprocessor Interface. This allows an external microprocessor to immediately determine the reason a cell was routed to the Microprocessor Cell Interface, the PHY it was on, and the VC Record that processed it.

Timeout_To_UP

When the Timeout_To_UP bit is logic 1, then cells from the BCIF which are discarded, either because they timed out (See the Backward Cell Interface Pacing and Head of Line Blocking Register) or because their PHY was declared to be inoperative (See the Inoperative PHY Declaration Period and Indications Register) will be routed to the microprocessor so they can be reinserted later. When Timeout_To_UP is logic 0, these cells will simply be dropped.

Cell_Info_to_OCIF

If this bit is logic 1, then the Microprocessor Cell Info Field described in Section 10.17.5 replaces the two Prepend/Postpends of cells sent to the Output Cell Interface. This Cell Info word permits a device interpreting the cell to determine the cell's source, PHYID, its VC Record Address, what type of cell it is, and certain information about its connection. Cell_Info_to_OCIF supercedes prepend/postpend translation (XPREPO). Note that cells inserted at the microprocessor with PROC_CELL set low, or cells received on PHYs with PROCESS_PHY set to logic 0 will not be processed, and thus Cell_Info_to_OCIF will not affect them.

SRAM_Even_Parity

If this bit is logic 1, the S/UNI-ATLAS-3200 generates and checks even parity for the SRAM. If 0 the S/UNI-ATLAS-3200 generates and checks odd parity.

Inact_On_DRAM_Err

When this bit is logic 1, then if a DRAM CRC-10 violations is detected on any VC connection, that connection will be treated as inactive until its DRAM_CRC_Err bit is written back to logic 0. This ensures that an errored connection cannot route cells spuriously. All cells which experience DRAM CRC errors will, in any case, be discarded.

Search_Verify_En:

The Search Verify Enable bit controls whether or not the secondary search key is used as part of the cell confirmation step.

If this bit is set to logic 1 then, after the VC search is complete, the Secondary search key extracted from the cell is compared to the VPI, VCI, and FieldB fields of the VC Table. Cells that fail this comparison will be dropped, and optionally routed to the microprocessor. Cells which terminate on an F4 connection will not have the VCI compared, and cells that terminate on UNI connections will not have the 4 MSBs of the VPI compared (they form the GFC field in a UNI).

If this bit is set to logic 0 then all cells with a valid Primary Key will be considered part of a valid connection. This bit will typically be set low if the cell is identified completely using only the Primary Key.

VP_RM_PTI6

The VP_RM_PTI6 bit controls the identification of the VPC Resource Management (VP-RM) cells. If VP_RM_PTI6 is a logic 0, VP-RM cells are identified by a VCI=6, the PTI field is ignored. If VP_RM_PTI6 is a logic 1, VP-RM cells are identified by a VCI=6 and a PTI=110. If the PTI field is not equal to 110, the cell is flagged as invalid and optionally can be routed to the Microprocessor Cell Interface by the Cell Processor.

Alternate_Count

The Alternate_Count bit determines whether cell counting is done using the regular Cell Counts, or whether the Alternate Counts are used. This feature is intended for use in time-of-day billing. When Alternate_Count is set to logic 1, the regular cell counts cease incrementing, and the alternate counts increment instead. The regular cell counts may then be read and cleared at leisure. When Alternate_Count is set to logic 0, the alternate counts cease incrementing, and the regular counts increment instead, and the alternate counts may then be read and cleared at leisure. It is the responsibility of the management software to ensure the count locations are cleared before the S/UNI-ATLAS-3200 begins incrementing at these locations.

CRO_FIFO_EN

When the CRO_FIFO_EN bit is logic 1, the Count Rollover FIFO is enabled. Generic, per-PHY, Policing, and PM counts in the Cell Processor which have their MSBs set will generate entries into the Count Rollover FIFO. This eliminates the need to periodically poll counts to prevent saturation.

The Count Rollover FIFO is separately enableable per-VC for billing counts, policing, per-PM session for PM, per-PHY for PHY policing counts, and globally for the per-PHY cell counts. Both the CRO_FIFO_EN bit and the individual enable bits must be logic 1 for the CRO FIFO to be enabled for that group of counts.

Sat_Fast_PM_Counts

The BIP-16 Errors count, and the counts of lost Fwd and Bwd PM Cells in the PM table are 8-bit counts that can quickly accumulate value. As a result, it may be desirable to prevent them from generating count rollover entries, and simply to let them saturate. Setting this bit to logic 1 causes these counts to never generate Count Rollover FIFO entries.

COS_EN

The Change of State FIFO enable (COS_EN) bit enables the monitoring of changes in connection state. If COS_EN is logic 1, all connections which undergo changes in state (i.e. AIS, RDI or CC alarm states) can be logged in a Change of State FIFO. This FIFO is 256 entries deep and holds a copy of the per-connection Status field of the VC Table. Using this feature eliminates the need to periodically poll each connection to determine if any changes in state have occurred. If the COS FIFO becomes full, background processes which monitor for changes in connection state will be suspended until such time as the FIFO becomes able to accept notifications of changes in state. Therefore, it is the responsibility of the management software to ensure the COS FIFO is read often enough so that changes in state remain compliant with the Bellcore and ITU standards.

If COS_EN is logic 0, the COS FIFO is disabled, and the background processes will not be suspended. If COS_EN is logic 0, it is the responsibility of the management software to poll each connection to determine changes in connection state (as reflected in the Status field of the VC Table) and notify higher layers of any changes in state.

The updating of the COS FIFO can be enabled/disabled on a per-connection basis with the COS_FIFO_enable bit of the Configuration field of the VC Table.

COS_Fail_Only

If the microprocessor has no need to know about changes of connection state unless they rise to the level of a service failure (i.e. an OAM fault that persists for at least 4.5 +/- 0.5 seconds) then, by setting this bit to logic 1, it may permit changes of state to be written to the COS FIFO only when the OAM_Fail bit changes state. When this bit is set to logic 0, entries will be made to the COS FIFO, on connections for which it is enabled, if any of the OAM alarms, changes state. In any event, the COS_DRAM_ERR_EN controls whether DRAM CRC errors cause COS entries.

COS_Fail_EN

When this bit is logic 1, changes on the OAM_Fail bit in the Status Field of a VC Table entry will result in entries to the COS FIFO, so long as the COS FIFO is enabled both globally and for that VC. When this bit is logic 0, changes in the OAM_Fail bit will not result in COS FIFO entries.

Reserved

This bit should be programmed to logic 0.

COS_DRAM_ERR_EN

When this bit is logic 1, a CRC-10 error on the DRAM causes a Change of State entry to be generated.

AUTO_AIS

The AUTO_AIS bit enables the generation of segment or end-to-end AIS cells while in a Continuity alarm state. If AUTO_AIS is logic 1, an Ete AIS cell is transmitted once per second if no user or CC cells have been received in the last 3.5 +/- 0.5 seconds. Segment AIS cells will also be generated if the SegmentFlow bit for the connection is logic 1. Automatic AIS generation is enableable on a per-VC basis via the CC_AIS_RDI bit. AIS cells can also be transmitted if the Send_AIS_segment and Send_AIS_end_to_end bits in the VC Table are set.

ForceCC

The ForceCC bit controls whether or not the insertion of CC cells is dependent on the user cell traffic. If ForceCC is logic 0, CC cells are only generated if the CC_Activate_Segment or CC_Activate_End_to_End per-connection bits are logic 1 and if no user cells have been transmitted within one second (nominal). If ForceCC is logic 1, CC cells are generated at a rate of once per second (nominal) if the CC_Activate_Segment or CC_Activate_End_to_End bits are logic 1.

F4EAISF5SRDI

The F4EAISF5SRDI register bit controls the generation of F5 Segment RDI cells upon the reception of an F4 End-to-End AIS cell. When this bit is logic 1, a segment VC-RDI cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, a segment VC-RDI cell will not be generated in this circumstance.

F4EAISF5EAIS

The F4EAISF5EAIS register bit controls the generation of F5 End-to-End AIS cells upon the reception of an F4 End-to-End AIS cell. When this bit is logic 1, an end-to-end VC-AIS cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point, and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, an end-to-end VC-AIS cell will not be generated in this circumstance.

F4SAISF5ERDI

The F4SAISF5ERDI register bit controls the generation of F5 end-to-end RDI cells upon the reception of an F4 segment AIS cell. If this bit is logic 1, an end-to-end VC-RDI cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point, and the VCC is also an end-to-end point. If this bit is logic 0, an end-to-end VC-RDI cell will not be generated in this circumstance.

F4SAISF5EAIS

The F4SAISF5EAIS register bit controls the generation of F5 end-to-end AIS cells upon the reception of an F4 segment AIS cell. If this bit is logic 1, an end-to-end VC-AIS cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point. If this bit is logic 0, an end-to-end AIS cell will not be generated in this circumstance.

GEN_HALFSECCLK

The GEN_HALFSECCLK bit determines the trigger for processing that relies on background processing, such as AIS, RDI and CC cell generation. If the GEN_HALFSECCLK is a logic 1, the 0.5 second clock is derived from SYSCLK, which is assumed to be 125 MHz. If GEN_HALFSECCLK is a logic 0, processing is initiated on the rising edge of the HALFSECCLK input.

Copy_FwPM_Timestamp

When the Copy_FwPM_Timestamp bit is logic 1, then when a Bwd PM cell is generated to the BCIF immediately upon reception of a Fwd PM cell (i.e. the BCIF is not full when the Fwd PM cell arrives) then the timestamp of the generated Bwd PM cell is set equal to the timestamp of the Fwd PM cell. If the BCIF is full when the Fwd PM cell arrives, or if this bit is logic 0, then the timestamp of the Bwd PM cell is set to the default all-ones.

Register 0x101: Cell Processor Routing Configuration

Bit	Type	Function	Default
31	R/W	LBtoOCIF	0
30	R/W	APStoBCIF	0
29	R/W	APStoOCIF	0
28	R/W	Reserved	0
27	R/W	Rtd_LB_to_UP_at_End	0
26	R/W	Xlate_From_IBCIF	1
25	R/W	IBCIF_P2_To_P1	0
24	R/W	IBCIF_P2_To_HECUDF	0
23	R/W	Xlate_To_OBCIF	0
22	R/W	OBCIF_Cell_Info	1
21	R/W	OBCIF_Bwd_VCRA	1
20	R/W	OBCIF_PHYID	1
19	R/W	SYSMANtoBCIF	0
18	R/W	SYSMANtoUP	0
17	R/W	SYSMANtoOCIF	0
16	R/W	UndefToBCIF	0
15	R/W	UndefToUP	0
14	R/W	UndefToOcif	0
13	R/W	ACTDEtoBCIF	0
12	R/W	ACTDEtoUP	0
11	R/W	ACTDEtoOCIF	0
10	R/W	CRC10toUP	0
9	R/W	DROPCRCEOAM	0
8	R/W	InactiveToUP	0
7	R/W	INVPTIVCItoUP	0
6	R/W	DROPINVPTIVCI	0
5	R/W	BADVCtoUP	0
4	R/W	DROPCRCERM	0
3	R/W	DropRM	0
2	R/W	RMtoBCIF	0
1	R/W	RMtoUP	0
0	R/W	PMtoUP	0

PMtoUP

If this bit is logic 1, all Performance management OAM cells are copied to the Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all PM OAM cells are output to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end-point for that connection.

RMtoUP

If the RMtoUP bit is logic 1, all RM cells are copied to the Microprocessor Cell Interface. RM cells are identified PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. If the VP_RM_PTI6 register bit is logic 1, VP-RM cells are further qualified by PTI=110.

RMtoBCIF

If the RMtoBCIF bit is logic 1, all RM cells are copied to the Backwards Cell Interface. RM cells are identified PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. If the VP_RM_PTI6 register is logic 1, VP-RM cells are further qualified by PTI=110.

DropRM

If the DropRM bit is logic 1, all RM cells are dropped (i.e. not passed to the OCIF) though they may be passed to the MCIF or BCIF based on the RMtoBCIF and RMtoUP register bits. RM cells are identified PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. If the VP_RM_PTI6 register bit of the Search Engine Configuration configuration register is logic 1, VP-RM cells are further qualified by PTI=110.

DROPCRCERM

If this bit is logic 1, all Forward and Backward RM cells with an incorrect CRC-10 are discarded. If this bit is logic 0, then all Forward and Backward RM cells are output to the Output Cell Interface regardless of whether their CRC-10 is correct or not.

BADVCtoUP

If the BADVCtoUP bit is logic 1, all cells with an unprovisioned VPI/VCI are dropped and routed to the Microprocessor Cell Interface. If this bit is logic 0, those cells are discarded by the S/UNI-ATLAS-3200 without being routed to the Microprocessor Cell Interface.

DROPINVPTIVCI

If this bit is logic 1, all F5 (VCC) cells with PTI=111 and all F4 (VPC) cells with a VCI of 7 through 15 are not routed to the Output Cell Interface. If DROPINVPTIVCI is logic 0, these cells are passed transparently.

INVPTIVCItoUP

If the INVPTIVCItoUP bit is logic 1, all F5 (VCC) cells with an invalid PTI field (PTI=111) and all F4 (VPC) cells with an invalid VCI field (VCI 7 through 15) are copied to the Microprocessor Cell Interface. The DROPINVPTIVCI register bit determines whether cells with invalid PTI or VCI fields are passed to the Output Cell Interface.

InactiveToUP

When InactiveToUP is logic 1, all cells received on connections whose Active bit is logic 0 in the VC Table (as well as cells received on connections that have their DRAM_CRC_Err bit logic 1 if the Inact_on_DRAM_Err register bit is logic 1, and all cells whose connections have misconfigured VPC pointers) are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, all cells received on inactive connections are dropped by the CP (i.e. not sent to the Output Cell Interface).

DROPCRCEOAM

If the DROPCRCEOAM bit is logic 1, all OAM cells with an errored CRC-10 are dropped (i.e. not routed to the Output Cell Interface). Regardless of the state of this bit, if the S/UNI-ATLAS-3200 is a flow end-point, all OAM cells with an errored CRC-10 are dropped.

CRC10toUP

If the CRC10toUP bit is logic 1, all OAM cells or RM cells with an errored CRC-10 are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, the DROPCRCEOAM and DROPCRCERM bits determine whether or not the S/UNI-ATLAS-3200 will route errored OAM and RM cells, respectively, to the Output Cell Interface.

ACTDEtoOCIF

If the ACTDEtoOCIF bit is logic 1, all Activate/Deactivate cells are routed to the Output Cell Interface. If ACTDEtoOCIF is logic 0, then at flow end points, all Activate/Deactivate cells are dropped. Regardless of the state of this bit, all Activate/Deactivate cells are routed to the Output Cell Interface if the S/UNI-ATLAS-3200 is not a flow end point for that connection.

ACTDEtoUP

If the ACTDEtoUP bit is logic 1, all activate/deactivate OAM cells are copied to the Microprocessor Cell Interface at flow end-points. If the S/UNI-ATLAS-3200 is not a flow end-point for the connection, the Activate/Deactivate cells are not copied to the Microprocessor Cell Interface. Regardless of the state of this bit, all activate/deactivate cells are passed to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end point for that connection.

ACTDEtoBCIF

If the ACTDEtoBCIF bit is logic 1, all activate/deactivate OAM cells are copied to the Backwards Cell Interface at flow end-points. If the S/UNI-ATLAS-3200 is not a flow end-point for the connection, the Activate/Deactivate cells are not copied to the Backwards Cell Interface. Regardless of the state of this bit, all activate/deactivate cells are passed to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end point for that connection.

UndefToOCIF

If the UNDEFtoOCIF bit is logic 1, all OAM cells with an undefined OAM Type or Function Type value are copied to the Output Cell Interface at flow end-points. Regardless of the state of this bit, all OAM cells with an undefined OAM Type or Function Type value are output to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end point for that connection.

UNDEFtoUP

If the UNDEFtoUP bit is logic 1, all OAM cells with an undefined OAM Type or Function Type value are copied to the Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all OAM cells with an undefined OAM Type or Function Type value are output to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end point for that connection.

UNDEFtoBCIF

If the UNDEFtoBCIF bit is logic 1, all OAM cells with an undefined OAM Type or Function Type value are copied to the Backwards Cell Interface at flow end-points. Regardless of the state of this bit, all OAM cells with an undefined OAM Type or Function Type value are output to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end point for that connection.

SYSMANtoOCIF

If the SYSMANtoOCIF bit is logic 1, all System Management cells are routed to the Output Cell Interface. If the SYSMANtoOCIF is logic 0, then at flow end-points, all System Management cells are dropped. Regardless of the state of this bit, all System Management cells are routed to the Output Cell Interface if the S/UNI-ATLAS-3200 is not a flow end-point for that connection.

SYSMANtoUP

If this bit is logic 1, all System Management OAM cells are copied to the Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all System Management OAM cells are output to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end-point for that connection.

SYSMANtoBCIF

If this bit is logic 1, all System Management OAM cells are copied to the Backwards Cell Interface at flow end-points. Regardless of the state of this bit, all System Management OAM cells are output to the Output Cell Interface if the S/UNI-ATLAS-3200 is not an end-point for that connection.

OBCIF_PHYID

If this bit is logic 1, then the PHYID field of the VC Linkage Table overwrites a portion of the prepended bytes of cells routed to the Output Backwards Cell Interface, as shown in Table 38. If this bit is logic 0, then these bits will not be overwritten, but cells sent to the OBCIF will not be able to be correctly reinserted by an S/UNI-ATLAS-3200 Input BCIF.

OBCIF_Bwd_VCRA

If this bit is logic 1, then the Backwards Direction VCRA field of the VC Table overwrites a portion of the prepended bytes of cells routed to the Output Backwards Cell Interface, as shown in Table 38. If this bit is logic 0, then these bits will not be overwritten, but cells sent to the OBCIF must be able to be searched correctly by the receiving S/UNI-ATLAS-3200.

OBCIF_Cell_Info

If this bit is logic 1, then 9 bits of information about the cell and its associated connection overwrite a portion of the prepended bytes of cells routed to the Output Backwards Cell Interface, as shown in Table 38 and Table 39. If this bit is logic 0, then these bits will not be overwritten.

Xlate_To_OBCIF

If this bit is logic 1, then cells routed to the Output Backwards Cell Interface will be header-translated as if they were destined to the Output Cell Interface, i.e. as controlled by the XVPIVCI, XPREPO, XHEC, XUDF, and Cell_Info_to_OCIF bits. The OBCIF_Cell_Info, OBCIF_PHYID, and OBCIF_Bwd_VCRA bits will still cause overwriting of portions of the cell. This bit is normally logic 1 when the Search_From_IBCIF bit is logic 1. When this bit is logic 0, cells routed to the Output BCIF are not translated, and cells generated to the Output BCIF carry the VPI and VCI programmed into the VPI and VCI fields of the VC Table.

IBCIF_P2_To_HECUDF

When this bit is logic 1, then all cells from the Input Backwards Cell Interface will have the Prepend/Postpend 2 word of the VC Table inserted into their HEC and UDF. This feature is used if the HEC and UDF are used as a routing word or identification tag, and cells from the IBCIF require different treatment from cells from the Input Cell Interface. This bit will overwrite changes made via the Xlate_From_IBCIF bit.

IBCIF_P2_To_P1

When this bit is logic 1, then all cells from the Input Backwards Cell Interface will have the Prepend/Postpend 2 word of the VC Table inserted into their Prepend/Postpend 1. This feature is used if the first Prepend/Postpend word is used as a routing word or identification tag, and cells from the IBCIF require different treatment from cells from the Input Cell Interface. This bit will overwrite changes made via the Xlate_From_IBCIF bit.

Xlate_From_IBCIF

When this bit is logic 1, then all cells from the Input Backwards Cell Interface are translated as if they came from the Input Cell Interface, i.e. as controlled by the XVPIVCI, XPREPO, XHEC, and XUDF, and Cell_Info_to_OCIF bits. This is the default choice. When this bit is logic 0, no header translation is performed on cells from IBCIF except as specified by IBCIF_P2_To_HECUDF and IBCIF_P2_To_P1.

Reserved

This function is not supported.

Rtd_LB_to_UP_at_End

When this bit is logic 1, then on connections with LB_Route = “01” or “10”, Returned Loopback cells are routed to the microprocessor at flow end points whether or not the Source ID of the Rtd LB cell matches the value programmed in the Loopback ID Registers. When this bit is logic 0, Returned Loopback cells are routed to the micro only if the source ID in the cell matches the value programmed in the Loopback ID Registers.

APStoOCIF

When APStoOCIF is logic 1, APS Coordination Protocol cells are not dropped at OAM flow end-points. When APStoOCIF is logic 0, APS cells are dropped at flow end-points like other OAM cells. APS cells may be copied to the Microprocessor Cell Interface or BCIF on a per-VC basis via the APStoUP bit in the VC Configuration field of the VC table, and the APStoBCIF bit in this register.

APStoBCIF

If the APStoBCIF bit is logic 1, then for those connections which the APStoUP bit is set to logic 1 in the VC Table Configuration field, the APS cells will be routed to the BCIF instead of to the microprocessor.

LBtoOCIF

When LBtoOCIF is logic 1, Loopback cells are not dropped at flow end-points or due to LB_Route functionalitybut will be passed to the OCIF. When LBtoOCIF is logic 0, all Loopback cells are dropped at flow end-points. Regardless of the setting of this bit, the routing of Loopback cells to MCIF and BCIF is controlled by the LB_Route[1:0] bits in the VC Table OAM Configuration field. This bit is intended to be used when an external device is handling the OAM-LB function.

Register 0x102: Cell Counting Configuration

Bit	Type	Function	Default
31	R/W	Cfg2_COUNT2[7]	0
30	R/W	Cfg2_COUNT2[6]	0
29	R/W	Cfg2_COUNT2[5]	0
28	R/W	Cfg2_COUNT2[4]	0
27	R/W	Cfg2_COUNT2[3]	0
26	R/W	Cfg2_COUNT2[2]	0
25	R/W	Cfg2_COUNT2[1]	0
24	R/W	Cfg2_COUNT2[0]	0
23	R/W	Cfg2_COUNT1[7]	0
22	R/W	Cfg2_COUNT1[6]	0
21	R/W	Cfg2_COUNT1[5]	0
20	R/W	Cfg2_COUNT1[4]	0
19	R/W	Cfg2_COUNT1[3]	0
18	R/W	Cfg2_COUNT1[2]	0
17	R/W	Cfg2_COUNT1[1]	0
16	R/W	Cfg2_COUNT1[0]	0
15	R/W	Cfg1_COUNT2[7]	0
14	R/W	Cfg1_COUNT2[6]	0
13	R/W	Cfg1_COUNT2[5]	0
12	R/W	Cfg1_COUNT2[4]	0
11	R/W	Cfg1_COUNT2[3]	0
10	R/W	Cfg1_COUNT2[2]	0
9	R/W	Cfg1_COUNT2[1]	0
8	R/W	Cfg1_COUNT2[0]	0
7	R/W	Cfg1_COUNT1[7]	0
6	R/W	Cfg1_COUNT1[6]	0
5	R/W	Cfg1_COUNT1[5]	0
4	R/W	Cfg1_COUNT1[4]	0
3	R/W	Cfg1_COUNT1[3]	0
2	R/W	Cfg1_COUNT1[2]	0
1	R/W	Cfg1_COUNT1[1]	0
0	R/W	Cfg1_COUNT1[0]	0

The Cfg1 bits are used when the Count Config Select bit in the VC Table is set to logic 0. The Cfg2 bits are used when the Count Config Select bit in the VC Table is set to logic 1. These bits apply to both the Cell Counts and the Alternate Cell Counts.

COUNT1[7:0]

The COUNT1[7:0] controls which cells the Cell Processor includes in its first per-connection 32-bit cell count. The COUNT1[7:0] field is programmed as follows:

Cell Type	User Cells		OAM Cells		RM Cells		Invalid PTI/VCI	
CLP Bit	1	0	1	0	1	0	1	0
Register Bit	COUNT1 [7]	COUNT1 [6]	COUNT1 [5]	COUNT1 [4]	COUNT1 [3]	COUNT1 [2]	COUNT1 [1]	COUNT1 [0]

A logic 1 written to any of the COUNT1[7:0] bits enables counting on that particular stream. For example, to enable counting of CLP=0+1 User and OAM cells only, the register configuration would be COUNT1[7:0] = 0xF0. If COUNT1[7:0] = 0x00, the first generic cell count for all connections is disabled. OAM and RM cells include those with invalid CRC-10s. Invalid PTI/VCI cells include F5 cells with PTI = "111", F4 cells with VCI = 0, F4 cells with VCI = 7 through 15, and (if vp_rm_pti6 is set to logic 1 in the Routing Configuration Register) F4 RM cells which have PTI not equal to "110". Note that cells which cannot reliably be identified with a particular connection (those that suffer UTOPIA parity errors and failed searches) and cells that are generated by S/UNI-ATLAS-3200 are not counted at all.

COUNT2[7:0]

The COUNT2[7:0] register bits controls which cells the Cell Processor includes in its second per-connection 32-bit cell count. The COUNT2[7:0] field is programmed exactly the same as the COUNT1[7:0] field.

Register 0x104: Backward Cell Interface Pacing and Head of Line Blocking

Bit	Type	Function	Default
31	R/W	BHBTO[15]	0
30	R/W	BHBTO[14]	0
29	R/W	BHBTO[13]	0
28	R/W	BHBTO[12]	0
27	R/W	BHBTO[11]	0
26	R/W	BHBTO[10]	0
25	R/W	BHBTO[9]	0
24	R/W	BHBTO[8]	0
23	R/W	BHBTO[7]	0
22	R/W	BHBTO[6]	0
21	R/W	BHBTO[5]	0
20	R/W	BHBTO[4]	0
19	R/W	BHBTO[3]	0
18	R/W	BHBTO[2]	0
17	R/W	BHBTO[1]	0
16	R/W	BHBTO[0]	0
15	R/W	BCP[15]	0
14	R/W	BCP[14]	0
13	R/W	BCP[13]	0
12	R/W	BCP[12]	0
11	R/W	BCP[11]	0
10	R/W	BCP[10]	0
9	R/W	BCP[9]	0
8	R/W	BCP[8]	0
7	R/W	BCP[7]	0
6	R/W	BCP[6]	0
5	R/W	BCP[5]	1
4	R/W	BCP[4]	0
3	R/W	BCP[3]	0
2	R/W	BCP[2]	0
1	R/W	BCP[1]	0
0	R/W	BCP[0]	0

BCP[15:0]

BCP[15:0] sets the number of cell interval between transfers of cells from the Input Backward Cell Interface (IBCIF). The minimum rate of transfer is 1 in 65535 cell intervals. When BCP[15:0] = 0x0000 back-to-back transfer from the Backward Cell Interface is possible, if there are no transfer requested from the Input Cell Interface or the Microprocessor Cell Interface. The default is set to 1 in 32 cell intervals. A cell interval is 22 SYSCLK cycles.

BHBTO[15:0]

BHBTO[15:0] sets the timeout limit, in cell intervals, before a cell at the head of the Backward Cell Interface FIFO is discarded. This is to prevent a malfunctioning PHY holding a Backward Reporting PM cell or RDI cell at the head of the FIFO, thus blocking all others cells that follow. Default is set to all zeros, which disables this timeout feature. A cell interval is 22 SYSCLK cycles.

Register 0x105: Per-PHY Processing Enable 1

Bit	Type	Function	Default
31	R/W	ProcessPHY[31]	1
30	R/W	ProcessPHY[30]	1
29	R/W	ProcessPHY[29]	1
28	R/W	ProcessPHY[28]	1
27	R/W	ProcessPHY[27]	1
26	R/W	ProcessPHY[26]	1
25	R/W	ProcessPHY[25]	1
24	R/W	ProcessPHY[24]	1
23	R/W	ProcessPHY[23]	1
22	R/W	ProcessPHY[22]	1
21	R/W	ProcessPHY[21]	1
20	R/W	ProcessPHY[20]	1
19	R/W	ProcessPHY[19]	1
18	R/W	ProcessPHY[18]	1
17	R/W	ProcessPHY[17]	1
16	R/W	ProcessPHY[16]	1
15	R/W	ProcessPHY[15]	1
14	R/W	ProcessPHY[14]	1
13	R/W	ProcessPHY[13]	1
12	R/W	ProcessPHY[12]	1
11	R/W	ProcessPHY[11]	1
10	R/W	ProcessPHY[10]	1
9	R/W	ProcessPHY[9]	1
8	R/W	ProcessPHY[8]	1
7	R/W	ProcessPHY[7]	1
6	R/W	ProcessPHY[6]	1
5	R/W	ProcessPHY[5]	1
4	R/W	ProcessPHY[4]	1
3	R/W	ProcessPHY[3]	1
2	R/W	ProcessPHY[2]	1
1	R/W	ProcessPHY[1]	1
0	R/W	ProcessPHY[0]	1

ProcessPHY[31:0]

If the ProcessPHY bit for a particular PHY is logic 0, then cells from that PHY will not be searched or processed, and will be passed through the S/UNI-ATLAS-3200 unrecorded and untouched, except for the PHY mapping functions, and adjustments to the length of the cells (i.e. deleting prepends, postpends, and the HEC/UDF, or adding indeterminate data in these positions). If the ProcessPHY bit is logic 1, then cells from that PHY are processed normally.

This feature is typically used when cells from a certain PHY are to be processed in another device, such as another S/UNI-ATLAS-3200. This allows multiple S/UNI-ATLAS-3200s to be cascaded, each handling cells from some of the PHYs. This can be used to support more than 64K VCs in total.

Register 0x106: Per-PHY Processing Enable 2

Bit	Type	Function	Default
31		Unused	
30		Unused	
29		Unused	
28		Unused	
27		Unused	
26		Unused	
25		Unused	
24		Unused	
23		Unused	
22		Unused	
21		Unused	
20		Unused	
19		Unused	
18		Unused	
17		Unused	
16		Unused	
15	R/W	ProcessPHY[47]	1
14	R/W	ProcessPHY[46]	1
13	R/W	ProcessPHY[45]	1
12	R/W	ProcessPHY[44]	1
11	R/W	ProcessPHY[43]	1
10	R/W	ProcessPHY[42]	1
9	R/W	ProcessPHY[41]	1
8	R/W	ProcessPHY[40]	1
7	R/W	ProcessPHY[39]	1
6	R/W	ProcessPHY[38]	1
5	R/W	ProcessPHY[37]	1
4	R/W	ProcessPHY[36]	1
3	R/W	ProcessPHY[35]	1
2	R/W	ProcessPHY[34]	1
1	R/W	ProcessPHY[33]	1
0	R/W	ProcessPHY[32]	1

ProcessPHY[32:47]

If the ProcessPHY bit for a particular PHY is logic 0, then cells from that PHY will not be searched or processed, and will be passed through the S/UNI-ATLAS-3200 unrecorded and untouched, except for the PHY mapping functions, and adjustments to the length of the cells (i.e. deleting prepends, postpends, and the HEC/UDF, or adding indeterminate data in these positions). If the ProcessPHY bit is logic 1, then cells from that PHY are processed normally.

This feature is typically used when cells from a certain PHY are to be processed in another device, such as another S/UNI-ATLAS-3200. This allows multiple S/UNI-ATLAS-3200s to be cascaded, each handling cells from some of the PHYs. This can be used to support more than 64K VCs in total.

Register 0x107: AIS/CC Pacing and Head of Line Blocking

Bit	Type	Function	Default
31	R/W	AISCCTO[15]	0
30	R/W	AISCCTO[14]	0
29	R/W	AISCCTO[13]	0
28	R/W	AISCCTO[12]	0
27	R/W	AISCCTO[11]	0
26	R/W	AISCCTO[10]	0
25	R/W	AISCCTO[9]	0
24	R/W	AISCCTO[8]	0
23	R/W	AISCCTO[7]	0
22	R/W	AISCCTO[6]	0
21	R/W	AISCCTO[5]	0
20	R/W	AISCCTO[4]	0
19	R/W	AISCCTO[3]	0
18	R/W	AISCCTO[2]	0
17	R/W	AISCCTO[1]	0
16	R/W	AISCCTO[0]	0
15	R/W	AISCCP[15]	0
14	R/W	AISCCP[14]	0
13	R/W	AISCCP[13]	0
12	R/W	AISCCP[12]	0
11	R/W	AISCCP[11]	0
10	R/W	AISCCP[10]	0
9	R/W	AISCCP[9]	0
8	R/W	AISCCP[8]	0
7	R/W	AISCCP[7]	0
6	R/W	AISCCP[6]	0
5	R/W	AISCCP[5]	1
4	R/W	AISCCP[4]	0
3	R/W	AISCCP[3]	0
2	R/W	AISCCP[2]	0
1	R/W	AISCCP[1]	0
0	R/W	AISCCP[0]	0

AISCCP[15:0]

AISCCP[15:0] sets the number of cell intervals between the insertion of consecutive AIS or CC cells into the cell stream. The minimum rate of transfer is 1 in 65535 cell intervals. When AISCCP[15:0] = 0x0000 back-to-back AIS or CC cells are possible, if there are no cells from the Input Cell Interface or the Microprocessor Cell Interface. The default is set to 1 in 32 cell intervals.

AISCCTO[15:0]

AISCCTO[15:0] sets the timeout limit, in cell periods, before an AIS or CC cell being inserted by a background process is discarded. This is to prevent a malfunctioning PHY from causing the background process to wait indefinitely to insert an AIS or CC, thus blocking all other connections from inserting AIS or CC cells. Default is set to all zeros, which disables this timeout feature.

Register 0x108: Fwd PM Pacing and Head of Line Blocking

Bit	Type	Function	Default
31	R/W	FPMTO[15]	0
30	R/W	FPMTO[14]	0
29	R/W	FPMTO[13]	0
28	R/W	FPMTO[12]	0
27	R/W	FPMTO[11]	0
26	R/W	FPMTO[10]	0
25	R/W	FPMTO[9]	0
24	R/W	FPMTO[8]	0
23	R/W	FPMTO[7]	0
22	R/W	FPMTO[6]	0
21	R/W	FPMTO[5]	0
20	R/W	FPMTO[4]	0
19	R/W	FPMTO[3]	0
18	R/W	FPMTO[2]	0
17	R/W	FPMTO[1]	0
16	R/W	FPMTO[0]	0
15	R/W	FPMP[15]	0
14	R/W	FPMP[14]	0
13	R/W	FPMP[13]	0
12	R/W	FPMP[12]	0
11	R/W	FPMP[11]	0
10	R/W	FPMP[10]	0
9	R/W	FPMP[9]	0
8	R/W	FPMP[8]	0
7	R/W	FPMP[7]	0
6	R/W	FPMP[6]	0
5	R/W	FPMP[5]	1
4	R/W	FPMP[4]	0
3	R/W	FPMP[3]	0
2	R/W	FPMP[2]	0
1	R/W	FPMP[1]	0
0	R/W	FPMP[0]	0

FPMP[15:0]

FPMP[15:0] sets the number of cell intervals between the insertion of consecutive Forward PM cells into the cell stream. The minimum rate of transfer is 1 in 65535 cell intervals. When FPMP[15:0] = 0x0000 back-to-back Fwd PM cells are possible, though unlikely. The default is set to 1 in 32 cell intervals.

FPMTO[15:0]

FPMTO[15:0] sets the timeout limit, in cell periods, before a Forward PM cell being inserted into the cell flow is discarded. This is to prevent a malfunctioning PHY from blocking all other connections from inserting Fwd PM cells. Default is set to all zeros, which disables this timeout feature.

Register 0x109: Inoperative PHY Declaration Period and Indications

Bit	Type	Function	Default
31	R	DEADPHY[15]	0
30	R	DEADPHY[14]	0
29	R	DEADPHY[13]	0
28	R	DEADPHY[12]	0
27	R	DEADPHY[11]	0
26	R	DEADPHY[10]	0
25	R	DEADPHY[9]	0
24	R	DEADPHY[8]	0
23	R	DEADPHY[7]	0
22	R	DEADPHY[6]	0
21	R	DEADPHY[5]	0
20	R	DEADPHY[4]	0
19	R	DEADPHY[3]	0
18	R	DEADPHY[2]	0
17	R	DEADPHY[1]	0
16	R	DEADPHY[0]	0
15	R/W	DEADPHYTO[15]	0
14	R/W	DEADPHYTO[14]	0
13	R/W	DEADPHYTO[13]	0
12	R/W	DEADPHYTO[12]	0
11	R/W	DEADPHYTO[11]	0
10	R/W	DEADPHYTO[10]	0
9	R/W	DEADPHYTO[9]	0
8	R/W	DEADPHYTO[8]	0
7	R/W	DEADPHYTO[7]	0
6	R/W	DEADPHYTO[6]	0
5	R/W	DEADPHYTO[5]	0
4	R/W	DEADPHYTO[4]	0
3	R/W	DEADPHYTO[3]	0
2	R/W	DEADPHYTO[2]	0
1	R/W	DEADPHYTO[1]	0
0	R/W	DEADPHYTO[0]	0

DEADPHYTO[15:0]

DEADPHYTO sets the number of cell periods before a PHY which has cells available for it, but which does not accept any cells whatsoever, is declared inoperative. Inoperative PHYs automatically have any AIS, CC, Fwd PM, or cells from the BCIF or MCIF discarded, to avoid head-of-line blocking problems resulting from repeatedly waiting for these cells to time out. Once the PHY accepts even a single cell, the Inoperative declaration is removed. The Dead PHY Timeout field defaults to 0, which disables this feature.

DEADPHY[15:0]

When a PHY is declared inoperative as per the setting of DEADPHYTO, the corresponding DEADPHY bit is set to logic 1. An optional interrupt (DEADPHYI) is declared. PHYs which are not configured in the OSDQ will be declared dead shortly after startup. The resulting interrupt should be cleared, allowing subsequent declarations on configured PHYs to generate an interrupt.

Register 0x10A: Inoperative PHY Indications

Bit	Type	Function	Default
31	R	DEADPHY[47]	0
30	R	DEADPHY[46]	0
29	R	DEADPHY[45]	0
28	R	DEADPHY[44]	0
27	R	DEADPHY[43]	0
26	R	DEADPHY[42]	0
25	R	DEADPHY[41]	0
24	R	DEADPHY[40]	0
23	R	DEADPHY[39]	0
22	R	DEADPHY[38]	0
21	R	DEADPHY[37]	0
20	R	DEADPHY[36]	0
19	R	DEADPHY[35]	0
18	R	DEADPHY[34]	0
17	R	DEADPHY[33]	0
16	R	DEADPHY[32]	0
15	R	DEADPHY[31]	0
14	R	DEADPHY[30]	0
13	R	DEADPHY[29]	0
12	R	DEADPHY[28]	0
11	R	DEADPHY[27]	0
10	R	DEADPHY[26]	0
9	R	DEADPHY[25]	0
8	R	DEADPHY[24]	0
7	R	DEADPHY[23]	0
6	R	DEADPHY[22]	0
5	R	DEADPHY[21]	0
4	R	DEADPHY[20]	0
3	R	DEADPHY[19]	0
2	R	DEADPHY[18]	0
1	R	DEADPHY[17]	0
0	R	DEADPHY[16]	0

DEADPHY[47:16]

When a PHY is declared inoperative as per the setting of DEADPHYTO, the corresponding DEADPHY bit is set to logic 1. An optional interrupt (DEADPHYI) is declared. PHYs which are not configured in the OSDQ will be declared dead shortly after startup. The resulting interrupt should be cleared, allowing subsequent declarations on configured PHYs to generate an interrupt.

11.5.2 Search

Register 0x10B: Search Engine Configuration

Bit	Type	Function	Default
31 : 27		Unused	X
26	R/W	Search_From_IBCIF	0
25	R/W	LPHY[2]	0
24	R/W	LPHY[1]	0
23	R/W	LPHY[0]	0
22	R/W	LA[4]	0
21	R/W	LA[3]	0
20	R/W	LA[2]	0
19	R/W	LA[1]	0
18	R/W	LA[0]	0
17	R/W	STARTA[6]	0
16	R/W	STARTA[5]	0
15	R/W	STARTA[4]	0
14	R/W	STARTA[3]	0
13	R/W	STARTA[2]	0
12	R/W	STARTA[1]	0
11	R/W	STARTA[0]	0
10	R/W	LB[3]	0
9	R/W	LB[2]	0
8	R/W	LB[1]	0
7	R/W	LB[0]	0
6	R/W	STARTB[6]	0
5	R/W	STARTB[5]	0
4	R/W	STARTB[4]	0
3	R/W	STARTB[3]	0
2	R/W	STARTB[2]	0
1	R/W	STARTB[1]	0
0	R/W	STARTB[0]	0

Search_From_IBCIF

When this bit is a logic 1, cells from the Input Backwards Cell Interface are searched by the search engine as if they were from the Input Cell Interface. When this bit is logic 0, the cells are assumed to carry the 16-bit VC Record Address to which they belong in prepended bytes, as shown in Table 38. In any event, the cells MUST carry the PHYID as shown in Table 38.

LPHY[2:0]

The contents of LPHY[2:0] determine the number of PHY ID bits in the Primary Search Key. If less than all six PHY address lines should be considered during the key search (as in the case where only a single PHY interface is used) then LPHY[2:0] must be programmed with the values below.

LPHY[2]	LPHY[1]	LPHY[0]	Number of PHY ID bits in Primary Key
1	1	1	Reserved
1	1	0	6
1	0	1	5 (LSB's)
1	0	0	4 (LSB's)
0	1	1	3 (LSB's)
0	1	0	2 (LSB's)
0	0	1	1 (LSB)
0	0	0	0 (single PHY interface)

STARTA[6:0]

STARTA[6:0] forms the binary address of the MSB of the Field A within the Routing Word. STARTA[6] is the MSB of the address.

LA[4:0]

LA[4:0] gives the length of the Field A in bits. The length is stored in LA[4:0] as binary value with LA[4] as MSB. If no Field A is to be used then LA[4:0] should be set to '00000'. Valid values for this field range from '00000' to '10001.' As a programming example: If a 10 bit Field A should be extracted starting at the 120th bit of the Routing Word, we would set LA ='01010' (length = 10) and STARTA='1110111' (starting address = 119), i.e. write 0x0A77 to this register.

STARTB[6:0]

STARTB[6:0] forms the binary address of the MSB of the Field B within the Routing Word. STARTB[6] is the MSB of the address.

LB[3:0]

LB[3:0] gives the length of the Field B in bits. The length is stored in LB[3:0] as binary value with LB[3] as MSB. If no Field B is to be used then LB[3:0] should be set to '0000'. Valid values for this field range from '0000' to '1100.' As a programming example: If a 10 bit Field B should be extracted starting at the 120th bit of the Routing Word, we would set LB ='1010' (length = 10) and STARTB = '1110111' (starting address = 119), i.e. write 0x0A77 to this register.

Register 0x10C: SRAM Access Control

Bit	Type	Function	Default
31	R/W	RWB	1
30	R	BUSY	X
29		Unused	X
28		Unused	X
27		Unused	X
26		Unused	X
25		Unused	X
24		Unused	X
23		Unused	X
22		Unused	X
21		Unused	X
20		Unused	X
19		Unused	X
18		Unused	X
17	R/W	Search/Linkage	0
16	R/W	SA[16]	0
15	R/W	SA[15]	0
14	R/W	SA[14]	0
13	R/W	SA[13]	0
12	R/W	SA[12]	0
11	R/W	SA[11]	0
10	R/W	SA[10]	0
9	R/W	SA[9]	0
8	R/W	SA[8]	0
7	R/W	SA[7]	0
6	R/W	SA[6]	0
5	R/W	SA[5]	0
4	R/W	SA[4]	0
3	R/W	SA[3]	0
2	R/W	SA[2]	0
1	R/W	SA[1]	0
0	R/W	SA[0]	0

This register allows the microprocessor to access the SRAM address indicated by SA[16:0], and perform the operation specified by the RWB bit on either the Search Table or the Linkage Table. Writing to this register initiates a microprocessor access request cycle.

SA[16:0]

This register holds the SRAM Address to be used for the Microprocessor initiated accesses. SA[16:0] map directly to device pins SADDR[16:0].

Search/Linkage

This bit indicates whether the operation is to address a Searching row or a Linkage row. The access is to a Search row if this bit is logic 0, and to a Linkage row if this bit is logic 1. This bit maps directly to device pin SADDR[17].

BUSY

The BUSY bit is high while a Microprocessor initiated access request to the SRAM is pending. This register should be polled until the BUSY bit goes low before another microprocessor access request is initiated. A microprocessor access request is typically completed within 22 SYSCLK cycles. The maximum possible latency for a read is 40 cycles, and for a write is 90 cycles. If the STANDBY bit in the S/UNI-ATLAS-3200 Master Configuration register is a logic 1, the typical access time is reduced to less than 7 SYSCLK cycles.

RWB

The RWB bit selects the operation to be performed on the addressed VC Table: when RWB is set to a logic 1, a read from the SRAM is requested; when RWB is set to a logic 0, a write to the SRAM is requested.

Register 0x10D: SRAM Data LSW (SRAM Data[31:0])

Bit	Type	Function	Default
31	R/W	SRAM_Data [31]	0
30	R/W	SRAM_Data [30]	0
29	R/W	SRAM_Data [29]	0
28	R/W	SRAM_Data [28]	0
27	R/W	SRAM_Data [27]	0
26	R/W	SRAM_Data [26]	0
25	R/W	SRAM_Data [25]	0
24	R/W	SRAM_Data [24]	0
23	R/W	SRAM_Data [23]	0
22	R/W	SRAM_Data [22]	0
21	R/W	SRAM_Data [21]	0
20	R/W	SRAM_Data [20]	0
19	R/W	SRAM_Data [19]	0
18	R/W	SRAM_Data [18]	0
17	R/W	SRAM_Data [17]	0
16	R/W	SRAM_Data [16]	0
15	R/W	SRAM_Data[15]	0
14	R/W	SRAM_Data[14]	0
13	R/W	SRAM_Data [13]	0
12	R/W	SRAM_Data [12]	0
11	R/W	SRAM_Data [11]	0
10	R/W	SRAM_Data [10]	0
9	R/W	SRAM_Data [9]	0
8	R/W	SRAM_Data [8]	0
7	R/W	SRAM_Data [7]	0
6	R/W	SRAM_Data [6]	0
5	R/W	SRAM_Data [5]	0
4	R/W	SRAM_Data [4]	0
3	R/W	SRAM_Data [3]	0
2	R/W	SRAM_Data [2]	0
1	R/W	SRAM_Data [1]	0
0	R/W	SRAM_Data [0]	0

For writes, this register contains data to be written to the lower 32 bits of the specified SRAM entry. For reads this register contains the data that was read from the 32 LSBs of the specified SRAM entry.

Register 0x10E: SRAM Data MSW (SRAM Data [63:32])

Bit	Type	Function	Default
31	R/W	SRAM_Data[63]	0
30	R/W	SRAM_Data[62]	0
29	R/W	SRAM_Data[61]	0
28	R/W	SRAM_Data[60]	0
27	R/W	SRAM_Data[59]	0
26	R/W	SRAM_Data[58]	0
25	R/W	SRAM_Data[57]	0
24	R/W	SRAM_Data[56]	0
23	R/W	SRAM_Data[55]	0
22	R/W	SRAM_Data[54]	0
21	R/W	SRAM_Data[53]	0
20	R/W	SRAM_Data[52]	0
19	R/W	SRAM_Data[51]	0
18	R/W	SRAM_Data[50]	0
17	R/W	SRAM_Data[49]	0
16	R/W	SRAM_Data[48]	0
15	R/W	SRAM_Data[47]	0
14	R/W	SRAM_Data[46]	0
13	R/W	SRAM_Data[45]	0
12	R/W	SRAM_Data[44]	0
11	R/W	SRAM_Data[43]	0
10	R/W	SRAM_Data[42]	0
9	R/W	SRAM_Data[41]	0
8	R/W	SRAM_Data[40]	0
7	R/W	SRAM_Data[39]	0
6	R/W	SRAM_Data[38]	0
5	R/W	SRAM_Data[37]	0
4	R/W	SRAM_Data[36]	0
3	R/W	SRAM_Data[35]	0
2	R/W	SRAM_Data[34]	0
1	R/W	SRAM_Data[33]	0
0	R/W	SRAM_Data[32]	0

For writes, this register contains data to be written to the most significant 32 bits of the specified SRAM entry. For reads this register contains the data that was read from the 32 MSBs of the specified SRAM entry.

11.5.3 VC Table

Register 0x110: VC Table Maximum Index

Bit	Type	Function	Default
31:17		Unused	X
16	R/W	Reserved	0
15	R/W	MAXVC[15]	0
14	R/W	MAXVC[14]	0
13	R/W	MAXVC[13]	0
12	R/W	MAXVC[12]	0
11	R/W	MAXVC[11]	0
10	R/W	MAXVC[10]	0
9	R/W	MAXVC[9]	0
8	R/W	MAXVC[8]	0
7	R/W	MAXVC[7]	0
6	R/W	MAXVC[6]	0
5	R/W	MAXVC[5]	0
4	R/W	MAXVC[4]	0
3	R/W	MAXVC[3]	0
2	R/W	MAXVC[2]	0
1	R/W	MAXVC[1]	0
0	R/W	MAXVC[0]	0

MAXVC[15:0]

The MAXVC[15:0] bits represent the current maximum VC Table index (VCRA[15:0]). It is used by the background processes of the VC Table as the first connection upon which the background processes act. The index is decremented with each subsequent connection serviced. An accurate value in this location maximizes the efficiency of the S/UNI-ATLAS-3200. Fixing this register to all ones guarantees that all 64K connections will be serviced by the background processes. Because the background processes require access to the Linkage table in external SRAM, **do not set MAXVC[15:0] to a value greater than supported by the depth of external SRAM provisioned.**

Setting MAXVC[15:0] to all zeros effectively halts the background tasks for all locations except VCRA[15:0]=0x00000.

Register 0x111: VC Table Access Control

Bit	Type	Function	Default
31	R/W	RWB	1
30	R	BUSY	X
29	R/W	CC_ClearOnRd	0
28	R/W	AC_ClearOnRd	0
27	R/W	NCC_ClearOnRd	0
26		Unused	X
25		Unused	X
24		Unused	
23	R	DRAM_CRC_ERR	X
22		Unused	
21		Unused	
20		Unused	
19		Unused	
18		Unused	
17		Unused	
16	R/W	Reserved	0
15	R/W	VCRA[15]	0
14	R/W	VCRA[14]	0
13	R/W	VCRA[13]	0
12	R/W	VCRA[12]	0
11	R/W	VCRA[11]	0
10	R/W	VCRA[10]	0
9	R/W	VCRA[9]	0
8	R/W	VCRA[8]	0
7	R/W	VCRA[7]	0
6	R/W	VCRA[6]	0
5	R/W	VCRA[5]	0
4	R/W	VCRA[4]	0
3	R/W	VCRA[3]	0
2	R/W	VCRA[2]	0
1	R/W	VCRA[1]	0
0	R/W	VCRA[0]	0

This register allows the microprocessor to access the VC Table Record indicated by VCRA[16:0], and perform the operation specified by the RWB bit on the data. Writing to this register initiates a microprocessor access request cycle. The VC Table Write Enable Registers 1 and 2 can be used to enable which fields are include in write operations, and should be programmed before this register is written.

Reserved

This bit must be programmed to logic 0.

VCRA[15:0]

This register holds the VC Record Address to be used to address the VC Table internal DRAM through Microprocessor initiated accesses. It identifies the desired VC Table entry.

DRAM_CRC_ERR

When this bit is logic 1, then the CRC of the VC being read was incorrect. This bit is valid after a read or write request has been made and the BUSY bit has gone low. This bit is valid either on a read, or on a write (if any of the Write Mask bits are logic 0). Because write or a clear-on-read operation will correct the DRAM CRC, it is important that the status of this bit be checked.

CC_CLRONRD

If CC_CLRONRD is logic 1, then after a read access, the Cell Count fields of the VC table are automatically written to all '0'. Other bits in the table are preserved in the write back.

If CC_CLRONRD = '0', no write back to clear the count bits is initiated.

AC_CLRONRD

If AC_CLRONRD is logic 1, then after a read access, the Alternate Cell Count fields of the VC table are automatically written to all '0'. Other bits in the table are preserved in the write back.

If AC_CLRONRD = '0', no write back to clear the count bits is initiated.

NCC_CLRONRD

If NCC_CLRONRD is logic 1, then after a read access, the Non-Compliant Count fields of the VC table are automatically written to all '0'. Other bits in the table are preserved in the write back.

If NCC_CLRONRD = '0', no write back to clear the count bits is initiated.

BUSY

The BUSY bit is high while a Microprocessor initiated access request to the DRAM is pending. This register should be polled until the BUSY bit goes low before another microprocessor access request is initiated. A microprocessor access request will be completed within 220 SYSCLK cycles. If the STANDBY bit in the S/UNI-ATLAS-3200 Master Configuration register is a logic 1, the access time is reduced to less than 22 SYSCLK cycles.

RWB

The RWB bit selects the operation to be performed on the addressed VC Table: when RWB is set to a logic 1, a read from the DRAM is requested; when RWB is set to a logic 0, a write to the DRAM is requested.

Register 0x112: VC Table Write Enable 1

Bit	Type	Function	Default
31	R/W	Unused	X
30	R/W	Wr_Action2	1
29	R/W	Wr_Inc2	1
28	R/W	Wr_Limit2	1
27	R/W	Wr_Action1	1
26	R/W	Wr_Inc1	1
25	R/W	Wr_Limit1	1
24	R/W	Wr_Field_B	1
23	R/W	Wr_VPI	1
22	R/W	Wr_VCI	1
21	R/W	Wr_Bwds_VCRA	1
20	R/W	Reserved	0
19	R/W	Wr_Status	1
18	R/W	Wr_Config	1
17	R/W	Wr_OAM_Config	1
16	R/W	Wr_Internal_Status	1
15	R/W	Wr_Police_Config	1
14	R/W	Wr_Max_Fr_Len	1
13	R/W	Wr_Unused1	1
12	R/W	Wr_GFR_State	1
11	R/W	Wr_Police_Rsvd	1
10	R/W	Wr_Ete_Rx_DT	1
9	R/W	Wr_Seg_Rx_DT	1
8	R/W	Wr_Alt_Count_1	1
7	R/W	Wr_Alt_Count_2	1
6	R/W	Wr_Cell_Count_1	1
5	R/W	Wr_Cell_Count_2	1
4	R/W	Wr_Unused3	1
3	R/W	Wr_Rem_Fr_Cnt	1
2	R/W	Wr_Non_Comp_1	1
1	R/W	Wr_Non_Comp_2	1
0	R/W	Wr_Non_Comp_3	1

The bits in this register are write enables. When a write access is requested via the VC Table Access Control Register, then those fields which have their write enable set to logic 1 will be altered by the write, and those which have their write enable set to logic 0 will retain their previous values The fields correspond to the fields described in Table 8, the VC Record Table. Unused_1 and Unused_3 refer to the reserved bits in Row1 and Row 3 respectively; the Reserved bit should always be programmed to logic 0 for proper operation, because it controls writing to (as opposed to automatic generation of) CRC-10 for the VC Record table. The Wr_Bwds_VCRA bit also controls the writing of the two reserved bits adjacent to the Bwds_VCRA field.

Register 0x113: VC Table Write Enable 2

Bit	Type	Function	Default
31:11	R/W	Unused	X
10	R/W	Wr_TAT2	1
9	R/W	Wr_TAT1	1
8	R/W	Wr_Unused4	1
7	R/W	Wr_Trans_VPI	1
6	R/W	Wr_Trans_VCI	1
5	R/W	Wr_Trans_HEC	1
4	R/W	Wr_Trans_UDF	1
3	R/W	Wr_Trans_PrePo_1	1
2	R/W	Wr_Trans_PrePo_2	1
1	R/W	Wr_Seg_DL	1
0	R/W	Wr_Ete_DL	1

The bits in this register are write enables. When a write access is requested via the VC Table Access Control Register, then those fields which have their write enable set to logic 1 will be altered by the write, and those which have their write enable set to logic 0 will retain their previous values The fields correspond to the fields described in Table 8, the VC Record Table. Unused4 refers to the unused bits in Row4.

Register 0x114: VC Table Data Row 0, Word 0 (LSW) (RAM Data [31:0])

Bit	Type	Function	Default
31	R/W	Row0_Data [31]	0
30	R/W	Row0_Data [30]	0
29	R/W	Row0_Data [29]	0
28	R/W	Row0_Data [28]	0
27	R/W	Row0_Data [27]	0
26	R/W	Row0_Data [26]	0
25	R/W	Row0_Data [25]	0
24	R/W	Row0_Data [24]	0
23	R/W	Row0_Data [23]	0
22	R/W	Row0_Data [22]	0
21	R/W	Row0_Data [21]	0
20	R/W	Row0_Data [20]	0
19	R/W	Row0_Data [19]	0
18	R/W	Row0_Data [18]	0
17	R/W	Row0_Data [17]	0
16	R/W	Row0_Data [16]	0
15	R/W	Row0_Data[15]	0
14	R/W	Row0_Data[14]	0
13	R/W	Row0_Data [13]	0
12	R/W	Row0_Data [12]	0
11	R/W	Row0_Data [11]	0
10	R/W	Row0_Data [10]	0
9	R/W	Row0_Data [9]	0
8	R/W	Row0_Data [8]	0
7	R/W	Row0_Data [7]	0
6	R/W	Row0_Data [6]	0
5	R/W	Row0_Data [5]	0
4	R/W	Row0_Data [4]	0
3	R/W	Row0_Data [3]	0
2	R/W	Row0_Data [2]	0
1	R/W	Row0_Data [1]	0
0	R/W	Row0_Data [0]	0

For writes, this register contains data to be written to word 0 of Row 0 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from word 0 of Row 0 of the VC Table Record specified by VCRA[15:0].

Register 0x115: VC Table Data Row 0, Word 1 (RAM Data [63:32])

Bit	Type	Function	Default
31	R/W	Row0_Data[63]	0
30	R/W	Row0_Data[62]	0
29	R/W	Row0_Data[61]	0
28	R/W	Row0_Data[60]	0
27	R/W	Row0_Data[59]	0
26	R/W	Row0_Data[58]	0
25	R/W	Row0_Data[57]	0
24	R/W	Row0_Data[56]	0
23	R/W	Row0_Data[55]	0
22	R/W	Row0_Data[54]	0
21	R/W	Row0_Data[53]	0
20	R/W	Row0_Data[52]	0
19	R/W	Row0_Data[51]	0
18	R/W	Row0_Data[50]	0
17	R/W	Row0_Data[49]	0
16	R/W	Row0_Data[48]	0
15	R/W	Row0_Data[47]	0
14	R/W	Row0_Data[46]	0
13	R/W	Row0_Data[45]	0
12	R/W	Row0_Data[44]	0
11	R/W	Row0_Data[43]	0
10	R/W	Row0_Data[42]	0
9	R/W	Row0_Data[41]	0
8	R/W	Row0_Data[40]	0
7	R/W	Row0_Data[39]	0
6	R/W	Row0_Data[38]	0
5	R/W	Row0_Data[37]	0
4	R/W	Row0_Data[36]	0
3	R/W	Row0_Data[35]	0
2	R/W	Row0_Data[34]	0
1	R/W	Row0_Data[33]	0
0	R/W	Row0_Data[32]	0

For writes, this register contains data to be written to word 1 of Row 0 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from word 1 of Row 0 of the VC Table Record specified by VCRA[15:0].

Register 0x116: VC Table Data Row 0, Word 2 (RAM Data [95:64])

Bit	Type	Function	Default
31	R/W	Row0_Data[95]	0
30	R/W	Row0_Data[94]	0
29	R/W	Row0_Data[93]	0
28	R/W	Row0_Data[92]	0
27	R/W	Row0_Data[91]	0
26	R/W	Row0_Data[90]	0
25	R/W	Row0_Data[89]	0
24	R/W	Row0_Data[88]	0
23	R/W	Row0_Data[87]	0
22	R/W	Row0_Data[86]	0
21	R/W	Row0_Data[85]	0
20	R/W	Row0_Data[84]	0
19	R/W	Row0_Data[83]	0
18	R/W	Row0_Data[82]	0
17	R/W	Row0_Data[81]	0
16	R/W	Row0_Data[80]	0
15	R/W	Row0_Data[79]	0
14	R/W	Row0_Data[78]	0
13	R/W	Row0_Data[77]	0
12	R/W	Row0_Data[76]	0
11	R/W	Row0_Data[75]	0
10	R/W	Row0_Data[74]	0
9	R/W	Row0_Data[73]	0
8	R/W	Row0_Data[72]	0
7	R/W	Row0_Data[71]	0
6	R/W	Row0_Data[70]	0
5	R/W	Row0_Data[69]	0
4	R/W	Row0_Data[68]	0
3	R/W	Row0_Data[67]	0
2	R/W	Row0_Data[66]	0
1	R/W	Row0_Data[65]	0
0	R/W	Row0_Data[64]	0

For writes, this register contains data to be written to word 2 of Row 0 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from word 2 of Row 0 of the VC Table Record specified by VCRA[15:0].

Register 0x117: VC Table Data Row 0, Word 3 (MSW) (RAM Data [127:96])

Bit	Type	Function	Default
31	R/W	Row0_Data[127]	0
30	R/W	Row0_Data[126]	0
29	R/W	Row0_Data[125]	0
28	R/W	Row0_Data[124]	0
27	R/W	Row0_Data[123]	0
26	R/W	Row0_Data[122]	0
25	R/W	Row0_Data[121]	0
24	R/W	Row0_Data[120]	0
23	R/W	Row0_Data[119]	0
22	R/W	Row0_Data[118]	0
21	R/W	Row0_Data[117]	0
20	R/W	Row0_Data[116]	0
19	R/W	Row0_Data[115]	0
18	R/W	Row0_Data[114]	0
17	R/W	Row0_Data[113]	0
16	R/W	Row0_Data[112]	0
15	R/W	Row0_Data[111]	0
14	R/W	Row0_Data[110]	0
13	R/W	Row0_Data[109]	0
12	R/W	Row0_Data[108]	0
11	R/W	Row0_Data[107]	0
10	R/W	Row0_Data[106]	0
9	R/W	Row0_Data[105]	0
8	R/W	Row0_Data[104]	0
7	R/W	Row0_Data[103]	0
6	R/W	Row0_Data[102]	0
5	R/W	Row0_Data[101]	0
4	R/W	Row0_Data[100]	0
3	R/W	Row0_Data[99]	0
2	R/W	Row0_Data[98]	0
1	R/W	Row0_Data[97]	0
0	R/W	Row0_Data[96]	0

For writes, this register contains data to be written to word 3 of Row 0 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from word 3 of Row 0 of the VC Table Record specified by VCRA[15:0].

Register 0x118: VC Table Data Row 1, Word 0 (LSW) (RAM Data [31:0])

For writes to the VC table, this and the next three registers contain data to be written to Row 1 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from Row 1 of the VC Table Record specified by VCRA[15:0].

Register 0x119: VC Table Data Row 1, Word 1 (RAM Data [63:32])

Register 0x11A: VC Table Data Row 1, Word 2 (RAM Data [95:64])

Register 0x11B: VC Table Data Row 1, Word 3 (MSW) (RAM Data [127:96])

Register 0x11C: VC Table Data Row 2, Word 0 (LSW) (RAM Data [31:0])

For writes to the VC table, this and the next three registers contain data to be written to Row 2 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from Row 2 of the VC Table Record specified by VCRA[15:0].

Register 0x11D: VC Table Data Row 2, Word 1 (RAM Data [63:32])

Register 0x11E: VC Table Data Row 2, Word 2 (RAM Data [95:64])

Register 0x11F: VC Table Data Row 2, Word 3 (MSW) (RAM Data [127:96])

Register 0x120: VC Table Data Row 3, Word 0 (LSW) (RAM Data [31:0])

For writes to the VC table, this and the next three registers contain data to be written to Row 3 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from Row 3 of the VC Table Record specified by VCRA[15:0].

Register 0x121: VC Table Data Row 3, Word 1 (RAM Data [63:32])

Register 0x122: VC Table Data Row 3, Word 2 (RAM Data [95:64])

Register 0x123: VC Table Data Row 3, Word 3 (MSW) (RAM Data [127:96])

Register 0x124: VC Table Data Row 4 Word 0 (LSW) (RAM Data [31:0])

For writes to the VC table, this and the next three registers contain data to be written to Row 4 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from Row 4 of the VC Table Record specified by VCRA[15:0].

Register 0x125: VC Table Data Row 4, Word 1 (RAM Data [63:32])

Register 0x126: VC Table Data Row 4, Word 2 (RAM Data [95:64])

Register 0x127: VC Table Data Row 4, Word 3 (MSW) (RAM Data [127:96])

Register 0x128: VC Table Data Row 5 Word 0 (LSW) (RAM Data [31:0])

For writes to the VC table, this and the next three registers contain data to be written to Row 5 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from Row 5 of the VC Table Record specified by VCRA[15:0].

Register 0x129: VC Table Data Row 5, Word 1 (RAM Data [63:32])

Register 0x12A: VC Table Data Row 5, Word 2 (RAM Data [95:64])

Register 0x12B: VC Table Data Row 5, Word 3 (MSW) (RAM Data [127:96])

Register 0x12C: VC Table Data Row 6 Word 0 (LSW) (RAM Data [31:0])

For writes to the VC table, this and the next three registers contain data to be written to Row 6 of the VC Table Record specified by VCRA[15:0]. The actual writes will take into account VC Table Write Enable Registers 1 and 2. For reads this register contains the data that was read from Row 6 of the VC Table Record specified by VCRA[15:0].

Register 0x12D: VC Table Data Row 6, Word 1 (RAM Data [63:32])

Register 0x12E: VC Table Data Row 6, Word 2 (RAM Data [95:64])

Register 0x12F: VC Table Data Row 6, Word 3 (MSW) (RAM Data [127:96])

11.5.4 Policing

Register 0x130: Per-VC Non-Compliant Cell Counting Configuration

Bit	Type	Function	Default
31:24		Unused	X
23	R/W	GFR_NCOUNT3[3]	0
22	R/W	GFR_NCOUNT3[2]	0
21	R/W	GFR_NCOUNT3[1]	0
20	R/W	GFR_NCOUNT3[0]	0
19	R/W	GFR_NCOUNT2[3]	0
18	R/W	GFR_NCOUNT2[2]	0
17	R/W	GFR_NCOUNT2[1]	0
16	R/W	GFR_NCOUNT2[0]	0
15	R/W	GFR_NCOUNT1[3]	0
14	R/W	GFR_NCOUNT1[2]	0
13	R/W	GFR_NCOUNT1[1]	0
12	R/W	GFR_NCOUNT1[0]	0
11	R/W	NCOUNT3[3]	0
10	R/W	NCOUNT3[2]	0
9	R/W	NCOUNT3[1]	0
8	R/W	NCOUNT3[0]	0
7	R/W	NCOUNT2[3]	0
6	R/W	NCOUNT2[2]	0
5	R/W	NCOUNT2[1]	0
4	R/W	NCOUNT2[0]	0
3	R/W	NCOUNT1[3]	0
2	R/W	NCOUNT1[2]	0
1	R/W	NCOUNT1[1]	0
0	R/W	NCOUNT1[0]	0

NCOUNTx[3:0]

The NCOUNTx[3:0] bits determine how the per-connection Non-Compliant cell counts #1 through #3 of the VC Table is defined:

NCOUNTx[3:0]	Definition
0000	Non-compliant CLP=0 cells.
0001	Non-compliant CLP=0+1 cells.
0010	Discarded CLP=0 cells.
0011	Discarded CLP=0+1 cells.
0100	Tagged CLP=0 cells which are not discarded
0101 … 1001	Reserved

NCOUNTx[3:0]	Definition
1010	Total CLP=0 AAL5 Frames Received
1011	Total CLP=0+1 AAL5 Frames Received
1100	Total cells non-compliant to GCRA1
1101	Total cells non-compliant to GCRA2
1110	Total cells non-compliant to the PHY GCRA
1111	Reserved

GFR_NCOUNTx[3:0]

The GFR_NCOUNTx[3:0] bits determine how the per-connection Non-Compliant cell counts #1 through #3 of the VC Table are defined for connections with GFR policing enabled (GFR = 1):

NCOUNTx[3:0]	Definition
0000	Non-compliant CLP=0 cells.
0001	Non-compliant CLP=0+1 cells.
0010	Discarded CLP=0 cells.
0011	Discarded CLP=0+1 cells.
0100	Tagged CLP=0 cells which are not discarded
0101	Non-compliant CLP=0 frames (GFR only)
0110	Non-compliant CLP=0+1 frames (GFR only)
0111	Partially or Completely Discarded CLP=0 frames (GFR Only)
1000	Partially or Completely Discarded CLP=0+1 frames (GFR Only)
1001	Tagged CLP=0 Frames which are not discarded (GFR Only)
1010	Total CLP=0 AAL5 Frames Received
1011	Total CLP=0+1 AAL5 Frames Received
1100	Total cells non-compliant to GCRA1
1101	Total cells non-compliant to GCRA2
1110	Total cells non-compliant to the PHY GCRA
1111	Reserved

Register 0x131: Connection Policing Configuration 1 & 2

Bit	Type	Function	Default
31	R/W	Cfg2_GCRA2[7]	0
30	R/W	Cfg2_GCRA2[6]	0
29	R/W	Cfg2_GCRA2[5]	0
28	R/W	Cfg2_GCRA2[4]	0
27	R/W	Cfg2_GCRA2[3]	0
26	R/W	Cfg2_GCRA2[2]	0
25	R/W	Cfg2_GCRA2[1]	0
24	R/W	Cfg2_GCRA2[0]	0
23	R/W	Cfg2_GCRA1[7]	0
22	R/W	Cfg2_GCRA1[6]	0
21	R/W	Cfg2_GCRA1[5]	0
20	R/W	Cfg2_GCRA1[4]	0
19	R/W	Cfg2_GCRA1[3]	0
18	R/W	Cfg2_GCRA1[2]	0
17	R/W	Cfg2_GCRA1[1]	0
16	R/W	Cfg2_GCRA1[0]	0
15	R/W	Cfg1_GCRA2[7]	0
14	R/W	Cfg1_GCRA2[6]	0
13	R/W	Cfg1_GCRA2[5]	0
12	R/W	Cfg1_GCRA2[4]	0
11	R/W	Cfg1_GCRA2[3]	0
10	R/W	Cfg1_GCRA2[2]	0
9	R/W	Cfg1_GCRA2[1]	0
8	R/W	Cfg1_GCRA2[0]	0
7	R/W	Cfg1_GCRA1[7]	0
6	R/W	Cfg1_GCRA1[6]	0
5	R/W	Cfg1_GCRA1[5]	0
4	R/W	Cfg1_GCRA1[4]	0
3	R/W	Cfg1_GCRA1[3]	0
2	R/W	Cfg1_GCRA1[2]	0
1	R/W	Cfg1_GCRA1[1]	0
0	R/W	Cfg1_GCRA1[0]	0

The Cfg1 configuration is selected if the per-connection PolicingConfiguration[2:0]=000. The Cfg2 configuration is selected if the per-connection PolicingConfigSelect[2:0] =001

GCRA1[7:0]

The following table indicates upon which cell streams the first policing instance acts:

Cell Type	RM		Segment OAM		End-to-End OAM		User	
CLP Bit	0	1	0	1	0	1	0	1
Reg Bit	GCRA1 [0]	GCRA1 [1]	GCRA1 [2]	GCRA1 [3]	GCRA1 [4]	GCRA1 [5]	GCRA1 [6]	GCRA1 [7]

A logic 1 written to any of the GCRA1[7:0] bits enables GCRA1 policing for that particular cell stream. For example, to enable cell rate policing for GCRA1 on the user CLP=0+1 cell stream, the register configuration would be GCRA1[7:0]=11000000. If GCRA1[7:0] = 00000000, the first GCRA policing instance is globally disabled.

Note that F5 OAM and RM cells are considered user cells when being policed at the F4 level, which occurs if the VC is an F4, or if the VP_POLICE feature is being used.

GCRA2[7:0]

These register bits control upon which cell streams the second GCRA instance acts. These register bits are programmed in exactly the same manner as described above.

Register 0x132: Connection Policing Configuration 3 & 4

Register 0x133: Connection Policing Configuration 5 & 6

Register 0x134: Connection Policing Configuration 7 & 8

Register 0x140: PHY Policing Enable 1

Bit	Type	Function	Default
31	R/W	PolicePHY31	0
30	R/W	PolicePHY30	0
29	R/W	PolicePHY29	0
28	R/W	PolicePHY28	0
27	R/W	PolicePHY27	0
26	R/W	PolicePHY26	0
25	R/W	PolicePHY25	0
24	R/W	PolicePHY24	0
23	R/W	PolicePHY23	0
22	R/W	PolicePHY22	0
21	R/W	PolicePHY21	0
20	R/W	PolicePHY20	0
19	R/W	PolicePHY19	0
18	R/W	PolicePHY18	0
17	R/W	PolicePHY17	0
16	R/W	PolicePHY16	0
15	R/W	PolicePHY15	0
14	R/W	PolicePHY14	0
13	R/W	PolicePHY13	0
12	R/W	PolicePHY12	0
11	R/W	PolicePHY11	0
10	R/W	PolicePHY10	0
9	R/W	PolicePHY9	0
8	R/W	PolicePHY8	0
7	R/W	PolicePHY7	0
6	R/W	PolicePHY6	0
5	R/W	PolicePHY5	0
4	R/W	PolicePHY4	0
3	R/W	PolicePHY3	0
2	R/W	PolicePHY2	0
1	R/W	PolicePHY1	0
0	R/W	PolicePHY0	0

PolicePHYx

The PolicePHYx bits enable the S/UNI-ATLAS-3200 per-PHY policing for PHYs 0 through 31. If PolicePHYx is logic 1, the per-PHY policing is enabled on PHYx. All connections associated with PHYx may have per-PHY policing enabled. The PHY Police bit in the VC Table must also be set to logic 1 for a connection to be per-PHY policed as well as policed by the per-connection leaky buckets. If PolicePHYx is logic 0, per-PHY policing for PHYx is disabled.

If per-PHY policing is enabled, it is the responsibility of the management software to setup the internal per-PHY Policing RAM.

Register 0x141: PHY Policing Enable 2

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	PolicePHY47	0
14	R/W	PolicePHY46	0
13	R/W	PolicePHY45	0
12	R/W	PolicePHY44	0
11	R/W	PolicePHY43	0
10	R/W	PolicePHY42	0
9	R/W	PolicePHY41	0
8	R/W	PolicePHY40	0
7	R/W	PolicePHY39	0
6	R/W	PolicePHY38	0
5	R/W	PolicePHY37	0
4	R/W	PolicePHY36	0
3	R/W	PolicePHY35	0
2	R/W	PolicePHY34	0
1	R/W	PolicePHY33	0
0	R/W	PolicePHY32	0

PolicePHYx

The PolicePHYx bits enable the S/UNI-ATLAS-3200 per-PHY policing for PHYs 32 through 47. If PolicePHYx is logic 1, the per-PHY policing is enabled on PHYx. All connections associated with PHYx may have per-PHY policing enabled. The PHY Police bit in the VC Table must also be set to logic 1 for a connection to be per-PHY policed as well as policed by the per-connection leaky buckets. If PolicePHYx is logic 0, per-PHY policing for PHYx is disabled.

If per-PHY policing is enabled, it is the responsibility of the management software to setup the internal per-PHY Policing RAM.

Register 0x142: PHY Policing Configuration

Bit	Type	Function	Default
31	R/W	Config4GCRA[7]	0
30	R/W	Config4GCRA[6]	0
29	R/W	Config4GCRA[5]	0
28	R/W	Config4GCRA[4]	0
27	R/W	Config4GCRA[3]	0
26	R/W	Config4GCRA[2]	0
25	R/W	Config4GCRA[1]	0
24	R/W	Config4GCRA[0]	0
23	R/W	Config3GCRA[7]	0
22	R/W	Config3GCRA[6]	0
21	R/W	Config3GCRA[5]	0
20	R/W	Config3GCRA[4]	0
19	R/W	Config3GCRA[3]	0
18	R/W	Config3GCRA[2]	0
17	R/W	Config3GCRA[1]	0
16	R/W	Config3GCRA[0]	0
15	R/W	Config2GCRA[7]	0
14	R/W	Config2GCRA[6]	0
13	R/W	Config2GCRA[5]	0
12	R/W	Config2GCRA[4]	0
11	R/W	Config2GCRA[3]	0
10	R/W	Config2GCRA[2]	0
9	R/W	Config2GCRA[1]	0
8	R/W	Config2GCRA[0]	0
7	R/W	Config1GCRA[7]	0
6	R/W	Config1GCRA[6]	0
5	R/W	Config1GCRA[5]	0
4	R/W	Config1GCRA[4]	0
3	R/W	Config1GCRA[3]	0
2	R/W	Config1GCRA[2]	0
1	R/W	Config1GCRA[1]	0
0	R/W	Config1GCRA[0]	0

Config1GCRA[7:0]

The following table indicates upon which cell streams the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=00):

Cell Type	RM		Segment OAM		End-to-End OAM		User	
CLP Bit	0	1	0	1	0	1	0	1
Reg Bit	Config1 GCRA[0]	Config1 GCRA[1]	Config1 GCRA[2]	Config1 GCRA[3]	Config1 GCRA[4]	Config1 GCRA[5]	Config1 GCRA[6]	Config1 GCRA[7]

A logic 1 written into any of the Config1GCRA1[7:0] register bits enables the per-PHY policing on that particular cell stream.

Config2GCRA[7:0]

These register bits indicate the cell streams upon which the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=01). These register bits are programmed in the same manner as listed above.

Config3GCRA[7:0]

These register bits indicate the cell streams upon which the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=10). These register bits are programmed in the same manner as listed above.

Config4GCRA[7:0]

These register bits indicate the cell streams upon which the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=11). These register bits are programmed in the same manner as listed above.

Register 0x143: Per-PHY Non-Compliant Cell Counting Configuration

Bit	Type	Function	Default
31:12		Unused	X
11	R/W	PHYNCOUNT3[3]	0
10	R/W	PHYNCOUNT3[2]	0
9	R/W	PHYNCOUNT3[1]	0
8	R/W	PHYNCOUNT3[0]	0
7	R/W	PHYNCOUNT2[3]	0
6	R/W	PHYNCOUNT2[2]	0
5	R/W	PHYNCOUNT2[1]	0
4	R/W	PHYNCOUNT2[0]	0
3	R/W	PHYNCOUNT1[3]	0
2	R/W	PHYNCOUNT1[2]	0
1	R/W	PHYNCOUNT1[1]	0
0	R/W	PHYNCOUNT1[0]	0

PHYNCOUNTx[3:0]

The PHYNCOUNTx[3:0] bits determine how the per-PHY Non-Compliant Cell Counts #1 through #3 of the PHY Policing RAM is defined:

PHYNCOUNTx[3:0]	Definition
0000	Non-compliant CLP=0 cells.
0001	Non-compliant CLP=0+1 cells.
0010	Discarded CLP=0 cells.
0011	Discarded CLP=0+1 cells.
0100	Tagged CLP=0 cells which are not discarded
0101 … 1001	Reserved
1010	Total CLP=0 AAL5 Frames Received
1011	Total CLP=0+1 AAL5 Frames Received
1100	Total cells non-compliant to GCRA1
1101	Total cells non-compliant to GCRA2
1110	Total cells non-compliant to the PHY GCRA
1111	Reserved

Register 0x144: PHY Policing RAM Address and Access Control

Bit	Type	Function	Default
31:19		Unused	X
18	R/W	RWB	1
17	R	BUSY	X
16	R/W	CLRONRD	0
15	R/W	Wr_PhyConfig	0
14	R/W	Wr_PhyNonComp3	0
13	R/W	Wr_PhyNonComp2	0
12	R/W	Wr_PhyNonComp1	0
11	R/W	Wr_Reserved	0
10	R/W	Wr_PHYI	0
9	R/W	Wr_PhyL	0
8	R/W	Wr_PhyTAT	0
7	R/W	Unused	0
6	R/W	Unused	0
5	R/W	PHYAddr[5]	0
4	R/W	PHYAddr[4]	0
3	R/W	PHYAddr[3]	0
2	R/W	PHYAddr[2]	0
1	R/W	PHYAddr[1]	0
0	R/W	PHYAddr[0]	0

PHYAddr[5:0]

The PHYAddr[5:0] bits indicate which of the per-PHY RAM locations is going to be accessed. PHYAddr[5:0]=000000 holds the policing parameters and non-compliant cell counts for PHY 1, and PHYAddr[5:0]=101111 holds the policing parameters and non-compliant cell counts for PHY48.

Wr_PhyTAT

When Wr_PhyTAT is logic 1, then a write access to the PHY Policing RAM will write to the PhyTAT field. When it is logic 0, the contents of PhyTAT will be unchanged after a write access. These bits should be written to zero on setup and left alone thereafter.

Wr_PhyL

When Wr_PhyL is logic 1, then a write access to the PHY Policing RAM will write to the PhyL field and the two Unused bits contiguous with it. When it is logic 0, the contents of PhyL and the Unused bits will be unchanged after a write access.

Wr_PhyI

When Wr_PhyI is logic 1, then a write access to the PHY Policing RAM will write to the PhyI field. When it is logic 0, the contents of PhyI will be unchanged after a write access.

Wr_Reserved

When Wr_Reserved is logic 1, then a write access to the PHY Policing RAM will write to the Reserved field. When it is logic 0, the contents of the Reserved field will be unchanged after a write access. These bits should be written to zero on setup and left alone thereafter.

Wr_PhyNonComp1

When Wr_PhyNonComp1 is logic 1, then a write access to the PHY Policing RAM will write to the PHY Non-Compliant Count 1 field. When it is logic 0, the contents of PHY Non-Compliant Count 1 will be unchanged after a write access.

Wr_PhyNonComp2

When Wr_PhyNonComp2 is logic 1, then a write access to the PHY Policing RAM will write to the PHY Non-Compliant Count 2 field. When it is logic 0, the contents of PHY Non-Compliant Count 2 will be unchanged after a write access.

Wr_PhyNonComp3

When Wr_PhyNonComp1 is logic 3, then a write access to the PHY Policing RAM will write to the PHY Non-Compliant Count 3 field. When it is logic 0, the contents of PHY Non-Compliant Count 3 will be unchanged after a write access.

Wr_PhyConfig

When Wr_PhyConfig is logic 1, then a write access to the PHY Policing RAM will write to the PHY Action, PHY Police Config, PHY VC Count, and PHY Policing Rollover FIFO Enable fields, as well as the 10 Unused bits in Row 3.. When it is logic 0, the contents of these fields will be unchanged after a write access.

CLRONRD

If the CLRONRD bit is logic 1, then the per-PHY non-compliant cell counts are cleared after a read access to a per-PHY Policing RAM location is performed. If CLRONRD is logic 0, then a clearing write is not performed when the per-PHY non-compliant cell counts are accessed.

BUSY

After a read or write access is initiated, the BUSY bit is asserted until the access has been completed. A read or write access will be completed within 220 SYSCLK cycles.

RWB

This bit indicates whether a read or write access is to be performed. If logic 0, a read access is initiated when this register is written to. If logic 1, a write access is initiated.

Register 0x145: PHY Policing RAM Data Row 0

Bit	Type	Function	Default
31	R/W	PhyPoliceRow0[31]	0
30	R/W	PhyPoliceRow0[30]	0
29	R/W	PhyPoliceRow0[29]	0
28	R/W	PhyPoliceRow0[28]	0
27	R/W	PhyPoliceRow0[27]	0
26	R/W	PhyPoliceRow0[26]	0
25	R/W	PhyPoliceRow0[25]	0
24	R/W	PhyPoliceRow0[24]	0
23	R/W	PhyPoliceRow0[23]	0
22	R/W	PhyPoliceRow0[22]	0
21	R/W	PhyPoliceRow0[21]	0
20	R/W	PhyPoliceRow0[20]	0
19	R/W	PhyPoliceRow0[19]	0
18	R/W	PhyPoliceRow0[18]	0
17	R/W	PhyPoliceRow0[17]	0
16	R/W	PhyPoliceRow0[16]	0
15	R/W	PhyPoliceRow0[15]	0
14	R/W	PhyPoliceRow0[14]	0
13	R/W	PhyPoliceRow0[13]	0
12	R/W	PhyPoliceRow0[12]	0
11	R/W	PhyPoliceRow0[11]	0
10	R/W	PhyPoliceRow0[10]	0
9	R/W	PhyPoliceRow0[9]	0
8	R/W	PhyPoliceRow0[8]	0
7	R/W	PhyPoliceRow0[7]	0
6	R/W	PhyPoliceRow0[6]	0
5	R/W	PhyPoliceRow0[5]	0
4	R/W	PhyPoliceRow0[4]	0
3	R/W	PhyPoliceRow0[3]	0
2	R/W	PhyPoliceRow0[2]	0
1	R/W	PhyPoliceRow0[1]	0
0	R/W	PhyPoliceRow0[0]	0

PHYPoliceRow0[31:0]

This is the 32-bits of data to be written into Row 0 of the per-PHY Policing RAM, or the data read from Row 0 of the RAM when a read request has been completed. If data are to be written into the RAM, then this register must be written to before the PHY Policing Access and Control register is written. If data are to be read, then the BUSY bit of the PHY Policing Access and Control register must be deasserted before these data are valid.

Register 0x146: PHY Policing RAM Data Row 1

Bit	Type	Function	Default
31	R/W	PhyPoliceRow1[31]	0
30	R/W	PhyPoliceRow1[30]	0
29	R/W	PhyPoliceRow1[29]	0
28	R/W	PhyPoliceRow1[28]	0
27	R/W	PhyPoliceRow1[27]	0
26	R/W	PhyPoliceRow1[26]	0
25	R/W	PhyPoliceRow1[25]	0
24	R/W	PhyPoliceRow1[24]	0
23	R/W	PhyPoliceRow1[23]	0
22	R/W	PhyPoliceRow1[22]	0
21	R/W	PhyPoliceRow1[21]	0
20	R/W	PhyPoliceRow1[20]	0
19	R/W	PhyPoliceRow1[19]	0
18	R/W	PhyPoliceRow1[18]	0
17	R/W	PhyPoliceRow1[17]	0
16	R/W	PhyPoliceRow1[16]	0
15	R/W	PhyPoliceRow1[15]	0
14	R/W	PhyPoliceRow1[14]	0
13	R/W	PhyPoliceRow1[13]	0
12	R/W	PhyPoliceRow1[12]	0
11	R/W	PhyPoliceRow1[11]	0
10	R/W	PhyPoliceRow1[10]	0
9	R/W	PhyPoliceRow1[9]	0
8	R/W	PhyPoliceRow1[8]	0
7	R/W	PhyPoliceRow1[7]	0
6	R/W	PhyPoliceRow1[6]	0
5	R/W	PhyPoliceRow1[5]	0
4	R/W	PhyPoliceRow1[4]	0
3	R/W	PhyPoliceRow1[3]	0
2	R/W	PhyPoliceRow1[2]	0
1	R/W	PhyPoliceRow1[1]	0
0	R/W	PhyPoliceRow1[0]	0

PHYPoliceRow1[31:0]

This is the 32-bits of data to be written into Row 1 of the per-PHY Policing RAM, or the data read from Row 1 of the RAM when a read request has been completed. If data are to be written into the RAM, then this register must be written to before the PHY Policing Access and Control register is written. If data are to be read, then the BUSY bit of the PHY Policing Access and Control register must be deasserted before these data are valid.

Register 0x147: PHY Policing RAM Data Row 2

Bit	Type	Function	Default
31	R/W	PhyPoliceRow2[31]	0
30	R/W	PhyPoliceRow2[30]	0
29	R/W	PhyPoliceRow2[29]	0
28	R/W	PhyPoliceRow2[28]	0
27	R/W	PhyPoliceRow2[27]	0
26	R/W	PhyPoliceRow2[26]	0
25	R/W	PhyPoliceRow2[25]	0
24	R/W	PhyPoliceRow2[24]	0
23	R/W	PhyPoliceRow2[23]	0
22	R/W	PhyPoliceRow2[22]	0
21	R/W	PhyPoliceRow2[21]	0
20	R/W	PhyPoliceRow2[20]	0
19	R/W	PhyPoliceRow2[19]	0
18	R/W	PhyPoliceRow2[18]	0
17	R/W	PhyPoliceRow2[17]	0
16	R/W	PhyPoliceRow2[16]	0
15	R/W	PhyPoliceRow2[15]	0
14	R/W	PhyPoliceRow2[14]	0
13	R/W	PhyPoliceRow2[13]	0
12	R/W	PhyPoliceRow2[12]	0
11	R/W	PhyPoliceRow2[11]	0
10	R/W	PhyPoliceRow2[10]	0
9	R/W	PhyPoliceRow2[9]	0
8	R/W	PhyPoliceRow2[8]	0
7	R/W	PhyPoliceRow2[7]	0
6	R/W	PhyPoliceRow2[6]	0
5	R/W	PhyPoliceRow2[5]	0
4	R/W	PhyPoliceRow2[4]	0
3	R/W	PhyPoliceRow2[3]	0
2	R/W	PhyPoliceRow2[2]	0
1	R/W	PhyPoliceRow2[1]	0
0	R/W	PhyPoliceRow2[0]	0

PHYPoliceRow2[31:0]

This is the 32-bits of data to be written into Row 2 of the per-PHY Policing RAM, or the data read from Row 2 of the RAM when a read request has been completed. If data are to be written into the RAM, then this register must be written to before the PHY Policing Access and Control register is written. If data are to be read, then the BUSY bit of the PHY Policing Access and Control register must be deasserted before these data are valid.

Register 0x148: PHY Policing RAM Data Row 3

Bit	Type	Function	Default
31	R/W	PhyPoliceRow3[31]	0
30	R/W	PhyPoliceRow3[30]	0
29	R/W	PhyPoliceRow3[29]	0
28	R/W	PhyPoliceRow3[28]	0
27	R/W	PhyPoliceRow3[27]	0
26	R/W	PhyPoliceRow3[26]	0
25	R/W	PhyPoliceRow3[25]	0
24	R/W	PhyPoliceRow3[24]	0
23	R/W	PhyPoliceRow3[23]	0
22	R/W	PhyPoliceRow3[22]	0
21	R/W	PhyPoliceRow3[21]	0
20	R/W	PhyPoliceRow3[20]	0
19	R/W	PhyPoliceRow3[19]	0
18	R/W	PhyPoliceRow3[18]	0
17	R/W	PhyPoliceRow3[17]	0
16	R/W	PhyPoliceRow3[16]	0
15	R/W	PhyPoliceRow3[15]	0
14	R/W	PhyPoliceRow3[14]	0
13	R/W	PhyPoliceRow3[13]	0
12	R/W	PhyPoliceRow3[12]	0
11	R/W	PhyPoliceRow3[11]	0
10	R/W	PhyPoliceRow3[10]	0
9	R/W	PhyPoliceRow3[9]	0
8	R/W	PhyPoliceRow3[8]	0
7	R/W	PhyPoliceRow3[7]	0
6	R/W	PhyPoliceRow3[6]	0
5	R/W	PhyPoliceRow3[5]	0
4	R/W	PhyPoliceRow3[4]	0
3	R/W	PhyPoliceRow3[3]	0
2	R/W	PhyPoliceRow3[2]	0
1	R/W	PhyPoliceRow3[1]	0
0	R/W	PhyPoliceRow3[0]	0

PHYPoliceRow3[31:0]

This is the 32-bits of data to be written into Row 3 of the per-PHY Policing RAM, or the data read from Row 3 of the RAM when a read request has been completed. If data are to be written into the RAM, then this register must be written to before the PHY Policing Access and Control register is written. If data are to be read, then the BUSY bit of the PHY Policing Access and Control register must be deasserted before these data are valid.

11.5.5 OAM Fault Management

Register 0x151: OAM Defect Location Octets 3 to 0

Bit	Type	Function	Default
31	R/W	DL[31]	0
30	R/W	DL[30]	1
29	R/W	DL[29]	1
28	R/W	DL[28]	0
27	R/W	DL[27]	1
26	R/W	DL [26]	0
25	R/W	DL[25]	1
24	R/W	DL[24]	0
23	R/W	DL[23]	0
22	R/W	DL[22]	1
21	R/W	DL[21]	1
20	R/W	DL[20]	0
19	R/W	DL[19]	1
18	R/W	DL[18]	0
17	R/W	DL[17]	1
16	R/W	DL[16]	0
15	R/W	DL[15]	0
14	R/W	DL[14]	1
13	R/W	DL[13]	1
12	R/W	DL[12]	0
11	R/W	DL[11]	1
10	R/W	DL[10]	0
9	R/W	DL[9]	1
8	R/W	DL[8]	0
7	R/W	DL[7]	0
6	R/W	DL[6]	1
5	R/W	DL[5]	1
4	R/W	DL[4]	0
3	R/W	DL[3]	1
2	R/W	DL[2]	0
1	R/W	DL[1]	1
0	R/W	DL[0]	0

DL[31:0]

This register contains the Defect Location data LSB which is inserted into

AIS cells generated due to PHY AIS, Send_AIS_* and due to declaration of CC alarm. The Defect Location is also inserted into RDI cells when the PHY_RDI, Send_RDI_Segment or Send_RDI_End_to_End register bits are asserted (i.e. forced insertion of RDI cells rather than generation of RDI cells as a -result of AUTO_RDI) and when RDI cells are generated as a result of the CC_AIS_RDI process. This is the least significant 32-bits of the Defect Location field. Note the Defect Location defaults to 6A6A6A6A6A6A6A6A6A6A6A6A6A6A6A hex.

Register 0x152: Defect Location Octets 7 to 4

Register 0x153: Defect Location Octets 11 to 8

Register 0x154: Defect Location Octets 15 to 12

Register 0x155: Per-PHY AIS Cell Generation Control 1

Bit	Type	Function	Default
31	R/W	AIS31	0
30	R/W	AIS30	0
29	R/W	AIS29	0
28	R/W	AIS28	0
27	R/W	AIS27	0
26	R/W	AIS26	0
25	R/W	AIS25	0
24	R/W	AIS24	0
23	R/W	AIS23	0
22	R/W	AIS22	0
21	R/W	AIS21	0
20	R/W	AIS20	0
19	R/W	AIS19	0
18	R/W	AIS18	0
17	R/W	AIS17	0
16	R/W	AIS16	0
15	R/W	AIS15	0
14	R/W	AIS14	0
13	R/W	AIS13	0
12	R/W	AIS12	0
11	R/W	AIS11	0
10	R/W	AIS10	0
9	R/W	AIS9	0
8	R/W	AIS8	0
7	R/W	AIS7	0
6	R/W	AIS6	0
5	R/W	AIS5	0
4	R/W	AIS4	0
3	R/W	AIS3	0
2	R/W	AIS2	0
1	R/W	AIS1	0
0	R/W	AIS0	0

AISx

AISx enables the generation of AIS cells for PHY x, where x is from 31 to 0. If AISx is a logic 1, AIS cells are generated to the Output Cell Interface once per second (nominally) for every connection associated with PHYx which is not an end-to-end point. Segment AIS cells will be generated if the SegmentFlow bit is logic 1 in the OAM Configuration field of the VC table; Otherwise, end-to-end AIS cells are generated. If AISx is a logic 0, AIS cell generation on a per-PHY basis is disabled. The PHYID[5:0] field in the VC Table identifies a connection's associated PHY.

Register 0x156: Per-PHY AIS Cell Generation Control 2

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	AIS47	0
14	R/W	AIS46	0
13	R/W	AIS45	0
12	R/W	AIS44	0
11	R/W	AIS43	0
10	R/W	AIS42	0
9	R/W	AIS41	0
8	R/W	AIS40	0
7	R/W	AIS39	0
6	R/W	AIS38	0
5	R/W	AIS37	0
4	R/W	AIS36	0
3	R/W	AIS35	0
2	R/W	AIS34	0
1	R/W	AIS33	0
0	R/W	AIS32	0

AISx

AISx enables the generation of AIS cells for PHY x, where x is from 47 to 32. If AISx is a logic 1, AIS cells are generated to the Output Cell Interface once per second (nominally) for every connection associated with PHYx which is not an end-to-end point. Segment AIS cells will be generated if the SegmentFlow bit is logic 1 in the OAM Configuration field of the VC table; Otherwise, end-to-end AIS cells are generated. If AISx is a logic 0, AIS cell generation on a per-PHY basis is disabled. The PHYID[5:0] field in the VC Table identifies a connection's associated PHY.

Register 0x157: Per-PHY RDI Cell Generation Control 1

Bit	Type	Function	Default
31	R/W	RDI31	0
30	R/W	RDI30	0
29	R/W	RDI29	0
28	R/W	RDI28	0
27	R/W	RDI27	0
26	R/W	RDI26	0
25	R/W	RDI25	0
24	R/W	RDI24	0
23	R/W	RDI23	0
22	R/W	RDI22	0
21	R/W	RDI21	0
20	R/W	RDI20	0
19	R/W	RDI19	0
18	R/W	RDI18	0
17	R/W	RDI17	0
16	R/W	RDI16	0
15	R/W	RDI15	0
14	R/W	RDI14	0
13	R/W	RDI13	0
12	R/W	RDI12	0
11	R/W	RDI11	0
10	R/W	RDI10	0
9	R/W	RDI9	0
8	R/W	RDI8	0
7	R/W	RDI7	0
6	R/W	RDI6	0
5	R/W	RDI5	0
4	R/W	RDI4	0
3	R/W	RDI3	0
2	R/W	RDI2	0
1	R/W	RDI1	0
0	R/W	RDI0	0

RDIx

RDIx enables the generation of RDI cells on a per-PHY basis for PHY x, where x is from 31 to 0. If RDIx is a logic 1, RDI cells for every connection (which is configured as an OAM end point) associated with PHY x, are generated once per second (nominally) to the backwards direction S/UNI-ATLAS-3200 (through the Output Backward OAM Cell Interface). Segment RDI will be generated at Segment End Points, and End-to-end RDI at end-to-end points. Both kinds of cells will be generated at dual end points. If RDIx is a logic 0, RDI cell generation on a per-PHY basis is disabled. The PHYID[5:0] field in the VC Table identifies a connection's associated PHY.

Register 0x158: Per-PHY RDI Cell Generation Control 2

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	RDI47	0
14	R/W	RDI46	0
13	R/W	RDI45	0
12	R/W	RDI44	0
11	R/W	RDI43	0
10	R/W	RDI42	0
9	R/W	RDI41	0
8	R/W	RDI40	0
7	R/W	RDI39	0
6	R/W	RDI38	0
5	R/W	RDI37	0
4	R/W	RDI36	0
3	R/W	RDI35	0
2	R/W	RDI34	0
1	R/W	RDI33	0
0	R/W	RDI32	0

RDIx

RDIx enables the generation of RDI cells on a per-PHY basis for PHY x, where x is from 47 to 32. If RDIx is a logic 1, RDI cells for every connection (which is configured as an OAM end point) associated with PHY x, are generated once per second (nominally) to the Backwards Direction S/UNI-ATLAS-3200 via the Output Backwards Cell Interface. Segment RDI will be generated at Segment End Points, and End-to-end RDI at end-to-end points. Both kinds of cells will be generated at dual end points. If RDIx is a logic 0, RDI cell generation on a per-PHY basis is disabled. The PHYID[5:0] field in the VC Table identifies a connection's associated PHY.

Register 0x159: Per-PHY APS Indication 1

Bit	Type	Function	Default
31	R/W	APS31	1
30	R/W	APS30	1
29	R/W	APS29	1
28	R/W	APS28	1
27	R/W	APS27	1
26	R/W	APS26	1
25	R/W	APS25	1
24	R/W	APS24	1
23	R/W	APS23	1
22	R/W	APS22	1
21	R/W	APS21	1
20	R/W	APS20	1
19	R/W	APS19	1
18	R/W	APS18	1
17	R/W	APS17	1
16	R/W	APS16	1
15	R/W	APS15	1
14	R/W	APS14	1
13	R/W	APS13	1
12	R/W	APS12	1
11	R/W	APS11	1
10	R/W	APS10	1
9	R/W	APS9	1
8	R/W	APS8	1
7	R/W	APS7	1
6	R/W	APS6	1
5	R/W	APS5	1
4	R/W	APS4	1
3	R/W	APS3	1
2	R/W	APS2	1
1	R/W	APS1	1
0	R/W	APS0	1

APSx

The APSx register bits indicate that automatic protection switching for PHY x exists, where x is from 31 to 0. If APSx is logic 1, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will not be generated. If APSx is logic 0, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will be generated (assuming that end-to-end VPC-AIS cells are not being received). The PHYID[5:0] field in the VC Table identifies the PHY device associated with a connection.

Register 0x15A: Per-PHY APS Indication 2

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	APS47	1
14	R/W	APS46	1
13	R/W	APS45	1
12	R/W	APS44	1
11	R/W	APS43	1
10	R/W	APS42	1
9	R/W	APS41	1
8	R/W	APS40	1
7	R/W	APS39	1
6	R/W	APS38	1
5	R/W	APS37	1
4	R/W	APS36	1
3	R/W	APS35	1
2	R/W	APS34	1
1	R/W	APS33	1
0	R/W	APS32	1

APSx

The APSx register bits indicate that automatic protection switching for PHY x exists, where x is from 47 to 32. If APSx is logic 1, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will not be generated. If APSx is logic 0, then when a segment VP-AIS cell is terminated, and end-to-end VP-AIS cell will be generated. The PHYID[5:0] field in the VC Table identifies the PHY device associated with a connection.

11.5.6 OAM Loopback

Register 0x160: OAM Loopback Location ID Octets 3 to 0

Bit	Type	Function	Default
31	R/W	LLID[31]	0
30	R/W	LLID[30]	1
29	R/W	LLID[29]	1
28	R/W	LLID[28]	0
27	R/W	LLID[27]	1
26	R/W	LLID [26]	0
25	R/W	LLID[25]	1
24	R/W	LLID[24]	0
23	R/W	LLID[23]	0
22	R/W	LLID[22]	1
21	R/W	LLID[21]	1
20	R/W	LLID[20]	0
19	R/W	LLID[19]	1
18	R/W	LLID[18]	0
17	R/W	LLID[17]	1
16	R/W	LLID[16]	0
15	R/W	LLID[15]	0
14	R/W	LLID[14]	1
13	R/W	LLID[13]	1
12	R/W	LLID[12]	0
11	R/W	LLID[11]	1
10	R/W	LLID[10]	0
9	R/W	LLID[9]	1
8	R/W	LLID[8]	0
7	R/W	LLID[7]	0
6	R/W	LLID[6]	1
5	R/W	LLID[5]	1
4	R/W	LLID[4]	0
3	R/W	LLID[3]	1
2	R/W	LLID[2]	0
1	R/W	LLID[1]	1
0	R/W	LLID[0]	0

LLID[31:0]

This register contains the LSB of the Loopback Location ID which the S/UNI-ATLAS-3200 will compare against when determining whether to loop back (in the case of outgoing Loopback cells) or extract (in the case of returning Loopback cells) loopback cells. The default of 6A6A…6A6A hex effectively disables this feature, as cells with this loopback ID are not permitted to be looped back.

Register 0x161: Loopback Location ID Octets 7 to 4

Register 0x162: Loopback Location ID Octets 11 to 8

Register 0x163: Loopback Location ID Octets 15 to 12

11.5.7 OAM Performance Management

Register 0x170: Performance Management RAM Record Address, Word Select and Access Control

Bit	Type	Function	Default
31-25		Unused	X
24	R/W	PM Bank	0
23	R/W	PM Addr[7]	0
22	R/W	PM Addr[6]	0
21	R/W	PM Addr[5]	0
20	R/W	PM Addr[4]	0
19	R/W	PM Addr[3]	0
18	R/W	PM Addr[2]	0
17	R/W	PM Addr[1]	0
16	R/W	PM Addr[0]	0
15	R/W	RWB	1
14	R	BUSY	X
13	R/W	ClrOnRd_Row[7]	0
12	R/W	ClrOnRd_Row[6]	0
11	R/W	ClrOnRd_Row[5]	0
10	R/W	ClrOnRd_Row[4]	0
9	R/W	ClrOnRd_Row[3]	0
8	R/W	Wr_PM_Row[7]	0
7	R/W	Wr_PM_Row[6]	0
6	R/W	Wr_PM_Row[5]	0
5	R/W	Wr_PM_Row[4]	0
4	R/W	Wr_PM_Row[3]	0
3	R/W	Wr_PM_Row[2]	0
2	R/W	Wr_PM_Row[1]	0
1	R/W	Wr_PM_Row[0]	0
0	R/W	Wr_PM_Config	0

PM Bank

The PM Bank bit determines which bank of PM data will be accessed. If this bit is logic 0, the PM Addr[7:0] field will access the desired data for the first bank of internal PM RAM. If this bit is logic 1, the PM Addr[7:0] field will access the desired data for the second bank of internal PM Ram.

PM Addr[7:0]

This field specifies which of the 256 possible PM Sessions to access. The PM Bank bit determines whether Bank 1 or Bank 2 of a particular PM Address will be selected.

Wr_PM_Config

When this field is logic 1, then when a write operation is requested to the PM Internal RAM, the PM Configuration and Status Field in Row 0 of the PM RAM will be written to. When this field is logic 0, then a write operation will not alter the PM Configuration and Status Field in Row 0.

Wr_PM_Row[7:0]

The PM Row mask is used to select which rows of the PM Internal RAM data will be written during a write operation, or cleared during a read operation. If any of PM Row WM[7:0] are '0' during a write operation, the corresponding row will not be altered by the write operation. All rows for which PM Row WM[x] is 1 will be altered by write operations, except for the PM Configuration and Status Register in row 0, which is separately controlled by Wr_PM_Config.

ClrOnRd_Row[7:3]

When ClrOnRd_Row[x] is set to logic 1, then a read access will cause all counts in that row to be cleared to 0, except for those counts (e.g. Fwd SECBC and Bwd SECBC) which are naturally rolling counts. Rows 0, 1, and 2 contain no clearable counts, so they do not have ClrOnRd bits. If ClrOnRd_Row[x] is set to logic 0, then a read will not change the values in that row.

BUSY

The BUSY bit is high while a Microprocessor initiated access request to the PM RAM data is pending the BUSY bit is deasserted only after all the access required has been completed. This register should be polled until the BUSY bit goes low before another microprocessor access request is initiated. A microprocessor access request will be completed within 220 SYSCLK cycles

RWB

The RWB bit selects the operation to be performed on the addressed PM Ram Data: when RWB is set to a logic 1, a read from the internal SRAM is requested; when RWB is set to a logic 0, a write to the internal SRAM is requested.

Register 0x171: Performance Management RAM Row 0 Word 0 (LSW)

Bit	Type	Function	Default
31	R/W	PM_Row0[31]	0
30	R/W	PM_Row0[30]	0
29	R/W	PM_Row0[29]	0
28	R/W	PM_Row0[28]	0
27	R/W	PM_Row0[27]	0
26	R/W	PM_Row0[26]	0
25	R/W	PM_Row0[25]	0
24	R/W	PM_Row0[24]	0
23	R/W	PM_Row0[23]	0
22	R/W	PM_Row0[22]	0
21	R/W	PM_Row0[21]	0
20	R/W	PM_Row0[20]	0
19	R/W	PM_Row0[19]	0
18	R/W	PM_Row0[18]	0
17	R/W	PM_Row0[17]	0
16	R/W	PM_Row0[16]	0
15	R/W	PM_Row0[15]	0
14	R/W	PM_Row0[14]	0
13	R/W	PM_Row0[13]	0
12	R/W	PM_Row0[12]	0
11	R/W	PM_Row0[11]	0
10	R/W	PM_Row0[10]	0
9	R/W	PM_Row0[9]	0
8	R/W	PM_Row0[8]	0
7	R/W	PM_Row0[7]	0
6	R/W	PM_Row0[6]	0
5	R/W	PM_Row0[5]	0
4	R/W	PM_Row0[4]	0
3	R/W	PM_Row0[3]	0
2	R/W	PM_Row0[2]	0
1	R/W	PM_Row0[1]	0
0	R/W	PM_Row0[0]	0

This register contains either the data to be written into the PM RAM Row 0 Word 0 (LSW) or the data read from the internal PM RAM when a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written. If data is to be read from the PM RAM, this register contains the data from Row 0 Word 0 (LSW) after the internal SRAM access is completed.

Register 0x172: Performance Management RAM Row 0 Word 1

Bit	Type	Function	Default
31	R/W	PM_Row0[63]	0
30	R/W	PM_Row0[62]	0
29	R/W	PM_Row0[61]	0
28	R/W	PM_Row0[60]	0
27	R/W	PM_Row0[59]	0
26	R/W	PM_Row0[58]	0
25	R/W	PM_Row0[57]	0
24	R/W	PM_Row0[56]	0
23	R/W	PM_Row0[55]	0
22	R/W	PM_Row0[54]	0
21	R/W	PM_Row0[53]	0
20	R/W	PM_Row0[52]	0
19	R/W	PM_Row0[51]	0
18	R/W	PM_Row0[50]	0
17	R/W	PM_Row0[49]	0
16	R/W	PM_Row0[48]	0
15	R/W	PM_Row0[47]	0
14	R/W	PM_Row0[46]	0
13	R/W	PM_Row0[45]	0
12	R/W	PM_Row0[44]	0
11	R/W	PM_Row0[43]	0
10	R/W	PM_Row0[42]	0
9	R/W	PM_Row0[41]	0
8	R/W	PM_Row0[40]	0
7	R/W	PM_Row0[39]	0
6	R/W	PM_Row0[38]	0
5	R/W	PM_Row0[37]	0
4	R/W	PM_Row0[36]	0
3	R/W	PM_Row0[35]	0
2	R/W	PM_Row0[34]	0
1	R/W	PM_Row0[33]	0
0	R/W	PM_Row0[32]	0

This register contains either the data to be written into the PM RAM Row 0 Word 1 or the data read from the internal PM RAM when a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written. If data is to be read from the PM RAM, this register contains the data from Row 0 Word 1 after the internal SRAM access is completed.

Register 0x173: Performance Management RAM Row 0 Word 2 (MSW)

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	PM_Row0[79]	0
14	R/W	PM_Row0[78]	0
13	R/W	PM_Row0[77]	0
12	R/W	PM_Row0[76]	0
11	R/W	PM_Row0[75]	0
10	R/W	PM_Row0[74]	0
9	R/W	PM_Row0[73]	0
8	R/W	PM_Row0[72]	0
7	R/W	PM_Row0[71]	0
6	R/W	PM_Row0[70]	0
5	R/W	PM_Row0[69]	0
4	R/W	PM_Row0[68]	0
3	R/W	PM_Row0[67]	0
2	R/W	PM_Row0[66]	0
1	R/W	PM_Row0[65]	0
0	R/W	PM_Row0[64]	0

This register contains either the data to be written into the PM RAM Row 0 Word 2 or the data read from the internal PM RAM when a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written. If data is to be read from the PM RAM, this register contains the data from Row 0 Word 2 after the internal SRAM access is completed.

Register 0x174: Performance Management RAM Row 1 Word 0 (LSW)

Register 0x175: Performance Management RAM Row 1 Word 1

Register 0x176: Performance Management RAM Row 1 Word 2 (MSW)

These registers contain either the data to be written into the PM RAM Row 1, or contains the data read from the internal PM RAM Row 1 after a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written.

Register 0x177: Performance Management RAM Row 2 Word 0 (LSW)

Register 0x178: Performance Management RAM Row 2 Word 1

Register 0x179: Performance Management RAM Row 2 Word 2 (MSW)

These registers contain either the data to be written into the PM RAM Row 2, or contains the data read from the internal PM RAM Row 2 after a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written.

Register 0x17A: Performance Management RAM Row 3 Word 0 (LSW)

Register 0x17B: Performance Management RAM Row 3 Word 1

Register 0x17C: Performance Management RAM Row 3 Word 2 (MSW)

These registers contain either the data to be written into the PM RAM Row 3, or contains the data read from the internal PM RAM Row 3 after a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written.

Register 0x17D: Performance Management RAM Row 4 Word 0 (LSW)

Register 0x17E: Performance Management RAM Row 4 Word 1

Register 0x17F: Performance Management RAM Row 4 Word 2 (MSW)

These registers contain either the data to be written into the PM RAM Row 4, or contains the data read from the internal PM RAM Row 4 after a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written.

Register 0x180: Performance Management RAM Row 5 Word 0 (LSW)

Register 0x181: Performance Management RAM Row 5 Word 1

Register 0x182: Performance Management RAM Row 5 Word 2 (MSW)

These registers contain either the data to be written into the PM RAM Row5, or contains the data read from the internal PM RAM Row 5 after a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written.

Register 0x183: Performance Management RAM Row 6 Word 0 (LSW)

Register 0x184: Performance Management RAM Row 6 Word 1

Register 0x185: Performance Management RAM Row 6 Word 2 (MSW)

These registers contain either the data to be written into the PM RAM Row 6, or contains the data read from the internal PM RAM Row 6 after a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written.

Register 0x186: Performance Management RAM Row 7 Word 0 (LSW)

Register 0x187: Performance Management RAM Row 7 Word 1

Register 0x188: Performance Management RAM Row 7 Word 2 (MSW)

These registers contain either the data to be written into the PM RAM Row 7, or contains the data read from the internal PM RAM Row 7 after a read request has been completed. If data is to be written to the PM RAM, it must be written to this register before the PM RAM Select and Access Control registers are written.

Register 0x189: Performance Management Threshold A

Bit	Type	Function	Default
31	R/W	MERROR[3]	0
30	R/W	MERROR[2]	0
29	R/W	MERROR[1]	0
28	R/W	MERROR[0]	0
27		Unused	X
26		Unused	X
25	R/W	MMISINS[11]	0
24	R/W	MMISINS[10]	0
23	R/W	MMISINS[9]	0
22	R/W	MMISINS[8]	0
21	R/W	MMISINS[7]	0
20	R/W	MMISINS[6]	0
19	R/W	MMISINS[5]	0
18	R/W	MMISINS[4]	0
17	R/W	MMISINS[3]	0
16	R/W	MMISINS[2]	0
15	R/W	MMISINS[1]	0
14	R/W	MMISINS[0]	0
13		Unused	X
12		Unused	X
11	R/W	MLOST[11]	0
10	R/W	MLOST[10]	0
9	R/W	MLOST[9]	0
8	R/W	MLOST[8]	0
7	R/W	MLOST[7]	0
6	R/W	MLOST[6]	0
5	R/W	MLOST[5]	0
4	R/W	MLOST[4]	0
3	R/W	MLOST[3]	0
2	R/W	MLOST[2]	0
1	R/W	MLOST[1]	0
0	R/W	MLOST[0]	0

This is the first of four Threshold Registers. These threshold registers are addressed by the Threshold_Select[1:0] field of the PM Configuration field of the PM RAM data. Note, these thresholds apply to both Forward Monitoring and Backward Reporting cells.

MMISINS[11:0]

MMISINS[11:0] is the binary representation of the threshold of misinserted cells per Performance Management block required to declare a Severely Errored Cell Block of Misinserted Cells (SECB Misinserted). The number of misinserted cells is not counted if this threshold is exceeded (the SECB Misinserted counter will be incremented instead). If MMISINS[11:0] is a binary zero, SECB Misinserted is not declared as a result of excessive misinserted cells.

MERROR[3:0]

MERROR[3:0] is the binary representation of the threshold of BIP-16 violations per Performance Management block required to declare a Severely Errored Cell Block for Errored cells (SECB Errored). Errored cell counts are not accumulated if this threshold is exceeded (the SECB Errored count will be incremented instead). If MERROR[3:0] is a binary zero, the SECB Errored cell count is not declared as a result of excessive BIP-16 violations.

MLOST[11:0]

MLOST[11:0] is the binary representation of the threshold of lost cells per Performance Management block required to declare a Severely Errored Cell Block of Lost Cells (SECB Lost). The number of lost cells is not counted if this threshold is exceeded (the SECB Lost counter will be incremented instead). If MLOST[11:0] is a binary zero, SECB Lost is not declared as a result of excessive lost cells.

Register 0x18A: Performance Management Threshold B

Register 0x18B: Performance Management Threshold C

Register 0x18C: Performance Management Threshold D

11.5.8 Change of Connection State FIFO

Register 0x190: VC Table Change of Connection State FIFO Status

Bit	Type	Function	Default
31:3		Unused	X
2	R	COSFULL	X
1	R	COSVALID	X
0	R	COSBUSY	X

The COSVALID and COSBUSY register bits indicate whether or not the data in the Change Of State Data register is valid. The COS FIFO read pointer is updated when the Change of Connection State FIFO Data register is read.

COSBUSY

If COSBUSY is logic 1, the COS FIFO read-pointer is being updated. When BUSY is asserted, the COSVALID bit is undefined. When COSBUSY is deasserted, the state of the COSVALID bit is defined.

COSVALID

If this bit is logic 1, the data in the VC Table Change of Connection Status Data Register is valid. The COSVALID bit is defined only when the COSBUSY bit is logic 0.

COSFULL

If this register bit is logic 1, the Change of State FIFO is full, and no more change of connection state data can be written into the FIFO. This will suspend the background process which monitors connection for change in connection state. It is the responsibility of the management software to ensure this register is read often enough to ensure the notification of changes in connection state are compliant to Bellcore and ITU standards.

Register 0x191: VC Table Change of Connection State FIFO Data

Bit	Type	Function	Default
31:0	R	COSDATA[31:0]	X

The COS FIFO read pointer is updated when this register is read. COSDATA is valid if the COSVALID bit is logic 1 and BUSY bit is logic 0.

COSDATA[28:17]

The COSDATA[28:17] field contains the End-point information and Status field of a connection whose address is identified by the COSDATA[15:0] register. The presence of data in this register indicates that the connection has undergone a change in connection state. The formatting of the FIFO entries is described in Table 34 in Section 10.15.

COSDATA[15:0]

This register contains the 16-bit connection ID of a connection in the VC Table which has undergone a change in connection state. The formatting of the FIFO entries is described in Table 34 in Section 10.15.

11.5.9 Count Rollover FIFO

Register 0x198: Count Rollover FIFO Status

Bit	Type	Function	Default
31:3		Unused	X
2	R	CRFULL	X
1	R	CRVALID	X
0	R	CRBUSY	X

The CRVALID and BUSY register bits indicate whether or not the data in the Count Rollover Data register are valid. The CR FIFO read pointer is updated when the Count Rollover FIFO Data register is read.

CRBUSY

If BUSY is logic 1, the CR FIFO read-pointer is being updated. When BUSY is asserted, the CRVALID bit is undefined. When BUSY is deasserted, the state of the CRVALID bit is defined.

CRVALID

If this bit is logic 1, the data in the Count Rollover FIFO Data register is valid. The CRVALID bit is defined only when the BUSY bit is logic 0.

CRFULL

If this register bit is logic 1, the Count Rollover FIFO is full, and no more rollover data can be written into the FIFO. This will result in those counts which would normally cause entries to be made to saturate rather than rolling over.

Register 0x199: Count Rollover FIFO Data

Bit	Type	Function	Default
31	R	Source[2]	X
30	R	Source[1]	X
29	R	Source[0]	X
28	R	CRDATA[28]	X
27	R	CRDATA[27]	X
26	R	CRDATA[26]	X
25	R	CRDATA[25]	X
24	R	CRDATA[24]	X
23	R	CRDATA[23]	X
22	R	CRDATA[22]	X
21	R	CRDATA[21]	X
20	R	CRDATA[20]	X
19	R	CRDATA[19]	X
18	R	CRDATA[18]	X
17	R	CRDATA[17]	X
16	R	CRDATA[16]	X
15	R	CRDATA[15]	X
14	R	CRDATA[14]	X
13	R	CRDATA[13]	X
12	R	CRDATA[12]	X
11	R	CRDATA[11]	X
10	R	CRDATA[10]	X
9	R	CRDATA[9]	X
8	R	CRDATA[8]	X
7	R	CRDATA[7]	X
6	R	CRDATA[6]	X
5	R	CRDATA[5]	X
4	R	CRDATA[4]	X
3	R	CRDATA[3]	X
2	R	CRDATA[2]	X
1	R	CRDATA[1]	X
0	R	CRDATA[0]	X

The CRVALID and CRBUSY register bits indicate whether or not the data in this register are valid. The CR FIFO read pointer is updated when this register is read.

SOURCE[2:0]

The Source field identifies which of four possible sources the entry comes from. The Source field determines the format of the CRDATA[26:0]. The Source field is encoded as follows:

000	per-VC generic or policing counts
001	per-PHY counts
010	PM Counts from Bank 0
011	PM Counts from Bank 1
1XX	Reserved

CRDATA[28:0]

The format of the CRDATA[28:0] depends on the source. See section 11.5.9 for details on the Count Rollover FIFO data.

11.5.10 Per PHY Statistics

Register 0x1A0: Per-PHY Counter Configuration

Bit	Type	Function	Default
31:5		Unused	
4	R/W	Cnt_NZ_GFC	1
3	R/W	Cnt_EFCI	0
2	R/W	Cnt_Undef_OAM	0
1	R/W	Cnt_Rsvd_VCI_PTI	0
0	R/W	PHY Rollover_FIFO_EN	0

PHY Rollover_FIFO_EN

If this bit is logic 1, all per-PHY counts cause entries to be made in the Count Rollover FIFO when their MSBs become logic 1. The MSB is reset to logic 0 when the FIFO entry is successfully made. It is the responsibility of the management software either to ensure the per-PHY counts are polled often enough to ensure they do not saturate, or to read the Count Rollover FIFO. If this bit is logic 0, all per-PHY counts saturate at all ones.

Cnt_Rsvd_VCI_PTI

The Cnt_Rsvd_VCI_PTI controls the counting of F4 cells with VCI values of 0 or between 7 and 15, inclusive, and all cells with PTI = 7. If Cnt_Rsvd_VCI_PTI is a logic 1, these cells are included in the count of Invalid VPI/VCI/PTI cells. If this bit is logic 0, only cells that cannot be searched to a valid, active connection are counted in this count. In any event, cells with an invalid VCI or PTI cause the INVALI interrupt to be asserted.

Cnt_Undef_OAM

If the Cnt_Undef_OAM bit is a logic 1, OAM cells with undefined OAM Type and Function Type fields are accumulated in the per-PHY count of errored OAM/RM cells. If Cnt_Undef_OAM is a logic 0, only OAM or RM cells with CRC-10 errors cause the per-PHY errored OAM/RM cell count to increment. The OAMERRI interrupt is also asserted when an OAM cell with an undefined OAM Type Function Type field is received.

Cnt_EFCI

If the Cnt_EFCI bit is logic 1, then with a PTI of 010 or 011 (which is the Explicit Forward Congestion Indication) are accumulated in the per-PHY count of EFCI/Non-Zero GFC cells. If this bit is logic 0, cells with EFCI are not accumulated.

Cnt_NZ_GFC

If the Cnt_NZ_GFC bit is logic 1, then cells which arrive on a UNI which have a non-zero GFC field are accumulated in the per-PHY count of EFCI/Non-Zero GFC cells. If this bit is logic 0, cells with non-zero GFC are not accumulated.

Register 0x1A1: Per-PHY Counter Control

Bit	Type	Function	Default
31:18	R	Unused	X
17	R/W	RWB	1
16	R	BUSY	X
15	R/W	CLP0_CLRONRD	0
14	R/W	CLP1_CLRONRD	0
13	R/W	RM_CLRONRD	0
12	R/W	OAM_CLRONRD	0
11	R/W	INVOAMRM_CLRONRD	0
10	R/W	INVAL_CLRONRD	0
9	R/W	NZGFC_CLRONRD	0
8	R/W	TO_CLRONRD	0
7:6	R	Reserved	0
5:0	R/W	PHYID[5:0]	0

A write to this register initiates an access to the Per-PHY counting RAM. The RWB bit determines if this access is a read or a write. While the transfer is pending, the BUSY bit will be high. The BUSY bit will go low when the transfer into the holding registers is complete.

PHYID[5:0]

The PHYID field determines which PHYs counts get read or written. PHY ID's greater than 47 will not result in any action and the holding registers will stay unchanged.

BUSY

When the BUSY bit is active it indicates that an access request to the PHY counts is pending. While this bit is high the contents of the holding registers is undefined. After writing to this register to initiate an access, the microprocessor should poll this register and wait for the BUSY to go low before reading the counts from the holding register. An access to the PHY counts is typically completed within 22 cycles.

CLP0_CLRONRD

If CLP0_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the CLP0 count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

CLP1_CLRONRD

If CLP1_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the CLP1 count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

RM_CLRONRD

If RM_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the Valid RM Cells count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

OAM_CLRONRD:

If OAM_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the Valid OAM Cells count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

INVOAMRM_CLRONRD

If INVOAMRM_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the Invalid OAM and RM Cells count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

INVAL_CLRONRD:

If INVAL_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the Invalid VPI/VCI/PTI count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

NZGFC_CLRONRD

If NZGFC_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the Non-Zero GFC and EFCI count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

TO_CLRONRD

If TO_CLRONRD is logic 1, then after a read of a set of PHY counts, a write is automatically initiated to set the Timed Out Cells count to 0. The writes are done in such a way that no counts are missed. If CLRONRD = '0', no write back to clear the count bits is initiated.

RWB

The RWB bit selects the operation to be performed on the addressed PHY. When RWB is set to a logic 1, a read of the PHY counts is requested; when RWB is set to a logic 0, a write to the PHY counts is requested.

Register 0x1A8: Per-PHY CLP0 Cell Count Holding Register

Bit	Type	Function	Default
31	R/W	CLP0[31]	X
30	R/W	CLP0[30]	X
29	R/W	CLP0[29]	X
28	R/W	CLP0[28]	X
27	R/W	CLP0[27]	X
26	R/W	CLP0[26]	X
25	R/W	CLP0[25]	X
24	R/W	CLP0[24]	X
23	R/W	CLP0[23]	X
22	R/W	CLP0[22]	X
21	R/W	CLP0[21]	X
20	R/W	CLP0[20]	X
19	R/W	CLP0[19]	X
18	R/W	CLP0[18]	X
17	R/W	CLP0[17]	X
16	R/W	CLP0[16]	X
15	R/W	CLP0[15]	X
14	R/W	CLP0[14]	X
13	R/W	CLP0[13]	X
12	R/W	CLP0[12]	X
11	R/W	CLP0[11]	X
10	R/W	CLP0[10]	X
9	R/W	CLP0[9]	X
8	R/W	CLP0[8]	X
7	R/W	CLP0[7]	X
6	R/W	CLP0[6]	X
5	R/W	CLP0[5]	X
4	R/W	CLP0[4]	X
3	R/W	CLP0[3]	X
2	R/W	CLP0[2]	X
1	R/W	CLP0[1]	X
0	R/W	CLP0[0]	X

CLP0[31:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of CLP=0 cells received on the specified PHYID. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the count of CLP = 0 cells received on the specified PHYID to the value in this register.

Register 0x1A9: Per PHY CLP1 Cell Count Holding Register

CLP1[31:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of CLP=1 cells received on the specified PHYID. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the count of CLP = 1 cells received on the specified PHYID to the value in this register.

Register 0x1AA: Per PHY Valid RM Cell Counts Holding Register

RM[15:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of RM cells with valid CRCs received on the specified PHYID. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the count of "valid RM cells with valid CRCs" received on the specified PHYID to the value in this register.

Register 0x1AB: Per PHY Valid OAM Cell Counts Holding Register

OAM[15:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of defined OAM cells with valid CRCs received on the specified PHYID. Undefined OAM cells (i.e. those with a OAM and Function Type not defined by 1.610-1999) are not counted in this register; they may optionally be counted in the Per-PHY Errored OAM/RM Cell Count. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the count of "OAM cells with valid CRCs" received on the specified PHYID to the value in this register.

Register 0x1AC: Per PHY Errored OAM/RM Cell Counts Holding Register

BADOAM[15:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of OAM or RM cells with invalid crc's received on the specified PHYID. If the Cnt_Undef_OAM bit is logic 1 in the Per-PHY Counter Configuration register, then this count also includes OAM cells with an undefined OAM Type or Function Type. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the count of "Errored OAM or RM" received on the specified PHYID to the value in this register.

Register 0x1AD: Per PHY Invalid VPI/VCI/PTI Cell Counts Holding Register

BADVPIVCI[15:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of cells from the specified PHYID which did not successfully complete the search, which terminated on an unprovisioned or inactive connection, or which contained an invalid VCI or PTI. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the count of "cells from the specified PHYID which did not successfully complete the search" to the value in this register.

Register 0x1AE: Per-PHY EFCI/Non-Zero GFC Cell Count Holding Register

EFCI_NZGFC[15:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of cells received at UNI connections on the specified PHYID with a non-zero GFC field, and/or cells with Explicit Forward Congestion Indication set in their PTI field, depending on the setting of the Cnt_EFCI and Cnt_NZ_GFC bits. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the "EFCI and/or Non-Zero GFC UNI cells" count of the specified PHY to the value in this register.

Register 0x1AF: Per-PHY Timed-Out Cell Count Holding Register

TIMEOUT [15:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the count of cells that timed-out of the BCIF, MCIF, Forward PM, or AIS/CC processes due to their PHY being unable to accept them. If the ClrOnRd bit was set, the internal count will also be reset to zero to start a fresh counting cycle. This transfer and reset will be done in a manner that ensures that no events are lost.

A write to the Per PHY Counter Control register with RWB = 0 will set the "Timed-Out Cells" count of the specified PHY to the value in this register.

Register 0x1B0: Per PHY Last Unknown VPI & VCI Holding Register

Bit	Type	Function	Default
31:28		Unused	X
27	R	UNK_VPI[11]	X
26	R	UNK_VPI[10]	X
25	R	UNK_VPI[9]	X
24	R	UNK_VPI[8]	X
23	R	UNK_VPI[7]	X
22	R	UNK_VPI[6]	X
21	R	UNK_VPI[5]	X
20	R	UNK_VPI[4]	X
19	R	UNK_VPI[3]	X
18	R	UNK_VPI[2]	X
17	R	UNK_VPI[1]	X
16	R	UNK_VPI[0]	X
15	R	UNK_VCI[15]	X
14	R	UNK_VCI[14]	X
13	R	UNK_VCI[13]	X
12	R	UNK_VCI[12]	X
11	R	UNK_VCI[11]	X
10	R	UNK_VCI[10]	X
9	R	UNK_VCI[9]	X
8	R	UNK_VCI[8]	X
7	R	UNK_VCI[7]	X
6	R	UNK_VCI[6]	X
5	R	UNK_VCI[5]	X
4	R	UNK_VCI[4]	X
3	R	UNK_VCI[3]	X
2	R	UNK_VCI[2]	X
1	R	UNK_VCI [1]	X
0	R	UNK_VCI[0]	X

UNK_VCI[15:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the VCI of the last cell from the specified PHYID which failed the search (due to a search error, an unprovisioned connection, or an inactive connection). The ClrOnRd bit is not relevant for this register and has no effect.

A write to the Per PHY Counter Control register with RWB = 0 will have no effect on this register.

UNK_VPI[11:0]

A write to the Per PHY Counter Control register with RWB = 1 will load this register with the VPI of the last cell from the specified PHYID which failed the search. The ClrOnRd bit is not relevant for this register and has no effect. A write to the Per PHY Counter Control register with RWB = 0 will have no effect on this register.

Register 0x1C0: Reserved

Bit	Type	Function	Default
31:4		Unused	X
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	1

Reserved

This register must be programmed to 0x1 for correct operation.

11.6 Rx Link Interface

The RxLink Interface registers should be left in their default state when the RxLink is not being used (i.e. when Egress_IngressB is logic 1 in the S/UNI-ATLAS-3200 Master Configuration Register).

Register 0x200: RxL Configuration

Bit	Type	Function	Default
31:16		Unused	X
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	POSTLEN[1]	0
8	R/W	POSTLEN[0]	0
7		Unused	X
6	R/W	INBANDADDR	1
5	R/W	PRELEN[1]	0
4	R/W	PRELEN[0]	0
3	R/W	PAREN	0
2	R/W	HEC	0
1	R/W	ODDPARITY	0
0	R/W	RXLRST	1

RXLRST

The RXLRST bit is used to reset the RxLink block circuitry. When RXLRST is set to logic zero, the RxLink block operates normally. When RXLRST is set to logic one, the RxLink block is held in reset, apart from Normal Mode registers which may be accessed for purposes of initialization.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is checked by the RxLink. Set this bit to '1' in order to check odd parity. Set this bit to '0' to check even parity. This bit is global and affects all PHY channels. This bit can be changed during operation.

PAREN

The PAREN bit is used to indicate whether parity errored cells or packets are marked as errored. When PAREN is '1', parity-errored cells and packets will be marked. When the value is '0', errored cells and packets will not be marked. This bit cannot be changed during operation and can only be changed when RXLRST is logic 1. Packets marked in error will be marked using RPP_ERR when they are transmitted. Parity errors have no effect on the processing of ATM cells.

HEC

The HEC bit is used to indicate whether the HEC/UDF word is included in ATM cells. When the value is '1', the ATM cells contain the HEC/UDF word. When the value is '0', the ATM cells do not contain the HEC/UDF word. In any event, the HEC is undefined at the ATM layer, and will not be checked by RxLink. This bit cannot be changed during operation and can only be changed when RXLRST is logic one.

PRELEN[1:0]

The PRELEN bits are used to indicate the size of the prepend applied to ATM cells. A value of '00' indicates no prepend word. A value of '01' indicates 1 prepend word. A value of '10' indicates 2 prepend words. A value of '11' is invalid. These bits cannot be changed during operation and can only be changed when RXLRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

INBANDADDR

The INBANDADDR bit is used only in POS-PHY mode to indicate whether the in band address is expected on the interface. This bit is useful in single phy applications where the in band addressing is optional and the Link Layer device does not send an address in band since there is only one phy. A setting of '1' means that the address is expected on RDAT when RSX is asserted. A setting of '0' means that RSX is not used and a PHYID of "000000" is assigned to all traffic on the POS PHY interface. This bit cannot be changed during operation and can only be changed when RXLRST is logic one.

POSTLEN[1:0]

The POSTLEN bits are used to indicate the size of the postpend applied to the ATM cells. A value of '00' indicates no postpend word. A value of '01' indicates 1 postpend word. A value of '10' indicates 2 postpend words. A value of '11' is invalid. These bits cannot be changed during operation and can only be changed when RXLRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

Register 0x201: RxL Interrupt Enable

Bit	Type	Function	Default
31:4		Unused	X
3	R/W	RDTFERRE	0
2	R/W	RERRE	0
1	R/W	PARERRE	0
0	R/W	FIFOTHE	0

A value of '0' masks the corresponding interrupt from asserting INTB. A setting of '1' unmasks the interrupt enabling the assertion of INTB. The enable bits correspond in bit location to the interrupts described in RxL Interrupt register.

Register 0x202: RxL Interrupt

Bit	Type	Function	Default
31:4		Unused	X
3	R	RDTFERRI	X
2	R	RERRI	X
1	R	PARERRI	X
0	R	FIFOTHI	X

The bits in this register indicate that a given event has occurred since the last time this register was read. The bits are cleared on microprocessor read.

FIFOTHI

The FIFOTH (Throttling) bit is set when there is cell available from a PHY port and no cell space available in the SDQ FIFO for that port. The Rx Link must throttle the PHY at this point. This is just an indicative interrupt.

PARERRI

The PARERR bit is set if there is a parity error on the UL3 or POS-PHY bus. Cells and packets received with parity errors will be marked as errored if the PAREN bit is logic 1 in the RxL Configuration register..

RERRI

This bit is set if the current POS packet is in error. This bit is set when RERR interface signal is asserted along with REOP and RVAL signals.

RDTFERRI

The RDTFERRI bit is used to indicate that the value of RDAT[31:24] during the RSX cycle was not equal to the value of ATM_FIELD or POS_FIELD, depending on whether the PHY is expected to be an ATM or a Packet PHY. The interrupt is advisory only. This bit is cleared on microprocessor read.

Register 0x208: RxL PHY Indirect Address

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	X
14	R/W	CONFIG_RWB	1
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	
5	R/W	PHY_ADDR[5]	0
4	R/W	PHY_ADDR[4]	0
3	R/W	PHY_ADDR[3]	0
2	R/W	PHY_ADDR[2]	0
1	R/W	PHY_ADDR[1]	0
0	R/W	PHY_ADDR[0]	0

The RxL PHY Indirect Address register is an indirect address register used along with the RxL PHY Indirect Data.

PHY_ADDR[5:0]

The PHY_ADDR register indicates the indirect address to read or write the RxL PHY Indirect Data, depending on the setting of CONFIG_RWB.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed, and the data for PHY_ADDR will be placed in the RxL PHY DATA register. A value of '0' means that a write of the information in RxL PHY DATA will be performed at address PHY_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0x209: RxL PHY Indirect Data

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5	R/W	PORT_X_MAP[5]	0
4	R/W	PORT_X_MAP[4]	0
3	R/W	PORT_X_MAP[3]	0
2	R/W	PORT_X_MAP[2]	0
1	R/W	PORT_X_MAP[1]	0
0	R/W	PORT_X_MAP[0]	0

The RxL PHY Indirect Data register is used along with the RxL PHY Indirect Address register to program the PHY channels.

PORT X MAP

The PORT_X_MAP bits are used to translate PHY addresses. On powerup, each PHY port will map to the corresponding PHYID in the FIFO. If translation is needed, then the location for the external (UL3 or POS-PHY3 bus) PHY address must be programmed with the value of the desired internal FIFO PHYID. The RxLink calendar always refers to the external PHYID; the rest of the device will act on the translated PHYID. PORT_X_MAP must not be written to a value greater than 47.

Register 0x20A: RxL Calendar Length

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6	R/W	CALENDAR_LENGTH[6]	0
5	R/W	CALENDAR_LENGTH[5]	0
4	R/W	CALENDAR_LENGTH[4]	0
3	R/W	CALENDAR_LENGTH[3]	0
2	R/W	CALENDAR_LENGTH[2]	0
1	R/W	CALENDAR_LENGTH[1]	0
0	R/W	CALENDAR_LENGTH[0]	0

This register is used in UTOPIA mode for polling and servicing. A description of the calendar is provided in Section 10.1.5

CALENDAR_LENGTH[6:0]

The CALENDAR_LENGTH register is provided to program the length of calendar used for polling and servicing up to a maximum of 128 entries. *Updating the calendar length during cell flow can cause overflows of the SDQ or underruns of the attached PHY device.*

Register 0x20B: RxL Calendar Indirect Address and Data

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	X
14	R/W	CALENDAR_ADDR[6]	0
13	R/W	CALENDAR_ADDR[5]	0
12	R/W	CALENDAR_ADDR[4]	0
11	R/W	CALENDAR_ADDR[3]	0
10	R/W	CALENDAR_ADDR[2]	0
9	R/W	CALENDAR_ADDR[1]	0
8	R/W	CALENDAR_ADDR[0]	0
7	R/W	CONFIG_RWB	1
6		Unused	X
5	R/W	CALENDAR_DATA[5]	0
4	R/W	CALENDAR_DATA[4]	0
3	R/W	CALENDAR_DATA[3]	0
2	R/W	CALENDAR_DATA[2]	0
1	R/W	CALENDAR_DATA[1]	0
0	R/W	CALENDAR_DATA[0]	0

The RxL Calendar Indirect Address Data register is an indirect register used to program the polling and servicing calendar described in Section 10.1.5. The RxL block performs polling and servicing in UTOPIA mode only.

CALENDAR_DATA[5:0]

The CALENDAR_DATA register is provided to program the sequence calendar with the PHY ids. The calendar consists of a maximum of 128 entries where the CALENDAR_ADDR is used to access one of the 128 entries to either write or read CALENDAR_DATA. The length of the calendar is set in the RxL Calendar Length register. *Updating the calendar entries during cell flow can cause overflows of the SDQ or underruns of the attached PHY device.*

CALENDAR_ADDR[6:0]

The CALENDAR_ADDR register is an indirect address register that is used with CALENDAR_DATA register. The two registers together allow indirect address reads and writes to the polling and servicing calendar. The CALENDAR_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register bit specifies whether a read or write is to be performed. A value of '1' means that a read is to be performed on the data at CALENDAR_ADDR and will be placed in the CALENDAR_DATA register. A value of '0' means that a write of the information in CALENDAR_DATA will be performed at address CALENDAR_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further accesses.

Register 0x20C: RxL Data Type Field

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	POS_FIELD[7]	0
14	R/W	POS_FIELD[6]	0
13	R/W	POS_FIELD[5]	0
12	R/W	POS_FIELD[4]	0
11	R/W	POS_FIELD[3]	0
10	R/W	POS_FIELD[2]	0
9	R/W	POS_FIELD[1]	0
8	R/W	POS_FIELD[0]	1
7	R/W	ATM_FIELD[7]	0
6	R/W	ATM_FIELD[6]	0
5	R/W	ATM_FIELD[5]	0
4	R/W	ATM_FIELD[4]	0
3	R/W	ATM_FIELD[3]	0
2	R/W	ATM_FIELD[2]	0
1	R/W	ATM_FIELD[1]	0
0	R/W	ATM_FIELD[0]	0

The RxL Data Type Field is used in POS mode of operation only and is provided as a means to identify the type of traffic, ATM or packet data, being sent over POS-PHY.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cells being transferred over POS-PHY. Whenever a packet arrives on a PHY expected to be an ATM PHY, RDAT[31:24] should match ATM_FIELD during the RSX cycle. Otherwise, an interrupt (RDTFERRI) is signaled to indicate POS data type mismatch. These bits can be changed during operation.

POS_FIELD[7:0]

The POS_FIELD register is provided to identify ATM cells being transferred over POS-PHY. Whenever a packet arrives on a PHY expected to be an Packet PHY, RDAT[31:24] should match POS_FIELD during the RSX cycle. Otherwise, an interrupt (RDTFERRI) is signaled to indicate POS data type mismatch. These bits can be changed during operation.

11.7 Tx PHY Interface

The TxPhy Interface registers should be left in their default state when the TxPhy is not being used (i.e. when Egress_IngressB is logic 0 in the S/UNI-ATLAS-3200 Master Configuration Register).

Register 0x220: TxP Configuration

Bit	Type	Function	Default
31:16		Unused	X
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	POSTLEN[1]	0
8	R/W	POSTLEN[0]	0
7		Unused	X
6	R/W	INBANDADDR	1
5	R/W	PRELEN[1]	0
4	R/W	PRELEN[0]	0
3	R/W	PAREN	0
2	R/W	HEC	0
1	R/W	ODDPARITY	0
0	R/W	TXPRST	1

TXPRST

The TXPRST bit is used to reset the TXPHY block circuitry. When TXPRST is set to logic zero, the TxPHY block operates normally. When TXPRST is set to logic one, the TxPHY block circutry is held in reset, except for the Normal Mode registers which may be accessed for purposes of initialization.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is expected on the TPx_DAT bus. Set this bit to ‘1’ in order to check for odd parity. Set this bit to ‘0’ to generate even parity. This bit is global and affects all PHY channels. This bit can be altered during operation.

PAREN

The PAREN bit is used to indicate whether parity errored cells or packets are marked as errored. When PAREN is '1', parity-errored cells and packets will be marked. When the value is '0', errored cells and packets will not be marked. This bit cannot be changed during operation and can only be changed when TXPRST is logic 1. Packets marked in error will be marked using TLP_ERR when they are transmitted. Parity errors have no effect on the processing of ATM cells.

HEC

The HEC bit is used to indicate whether the HEC/UDF word is included in ATM cells. When the value is '1', the ATM cells contain the HEC/UDF word. When the value is '0', the ATM cels do not contain the HEC/UDF word. In any event, the HEC is undefined at the ATM layer, and will not be checked by TxPhy. This bit cannot be changed during operation and can only be changed when TXPRST is logic one.

PRELEN[1:0]

The PRELEN bits are used to indicate the size of the prepend applied to ATM cells. A value of '00' indicates no prepend word. A value of '01' indicates 1 prepend word. A value of '10' indicates 2 prepend words. A value of '11' is invalid. These bits cannot be changed during operation and can only be changed when TXPRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

INBANDADDR

The INBANDADDR bit is used only in POS-PHY mode to indicate whether the in band address is expected on the interface. This bit is useful in single PHY applications where the in band addressing is optional and the Link Layer device may not send an address in band since there is only one PHY. A setting of '1' means that the address is expected on TPP_DAT when TPP_SX is asserted. A setting of '0' means that TPP_SX is not used and a PHYID of "000000" is assigned to all traffic on the POS PHY interface. This bit cannot be changed during operation and can only be changed when TXPRST is logic one.

POSTLEN[1:0]

The POSTLEN bits are used to indicate the size of the postpend applied to the ATM cells. A value of '00' indicates no postpend word. A value of '01' indicates 1 postpend word. A value of '10' indicates 2 postpend words. A value of '11' is invalid. These bits cannot be changed during operation and can only be changed when TXPRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

Register 0x221: TxP Interrupt

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2	R	TDTFERRI	X
1	R	TPARERRI	X
0	R	RUNTCELLI	X

RUNTCELLI

RUNTCELLI is set if TPU_ENB is deasserted before the end of the cell transfer, resulting in a partial cell transfer. These cells are be marked as errored, and may be discarded or routed to the microprocessor by the Cell Processor. This error can be caused by incorrectly setting the size of the cell expected by this interface. Check that the HEC, pre and post word registers are properly set.

TPARERRI

The TPARERR bit is used to indicate that a Parity Error was observed on the incoming TPx_DAT bus since the last time the interrupt was read. The cell may be marked errored and sent on to the SDQ. This bit is cleared on microprocessor read.

TDTFERRI

The TDTFERRI bit is used to indicate that the value of TPP_DAT[31:24] during the TPP_SX cycle was not equal to the value of ATM_FIELD or POS_FIELD, depending on whether the PHY is expected to be an ATM or a Packet PHY. The interrupt is advisory only. This bit is cleared on microprocessor read.

Register 0x222: TxP Interrupt Enable

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2	R/W	TDTFERRE	X
1	R/W	TPARERRE	X
0	R/W	RUNTCELLE	X

A value of '0' masks the corresponding interrupt from asserting INTB. A setting of '1' unmasks the interrupt enabling the assertion of INTB. The enable bits correspond in bit location to the interrupts described in RxL Interrupt register.

Register 0x223: TxP Data Type Field

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	POS_FIELD[7]	0
14	R/W	POS_FIELD[6]	0
13	R/W	POS_FIELD[5]	0
12	R/W	POS_FIELD[4]	0
11	R/W	POS_FIELD[3]	0
10	R/W	POS_FIELD[2]	0
9	R/W	POS_FIELD[1]	0
8	R/W	POS_FIELD[0]	1
7	R/W	ATM_FIELD[7]	0
6	R/W	ATM_FIELD[6]	0
5	R/W	ATM_FIELD[5]	0
4	R/W	ATM_FIELD[4]	0
3	R/W	ATM_FIELD[3]	0
2	R/W	ATM_FIELD[2]	0
1	R/W	ATM_FIELD[1]	0
0	R/W	ATM_FIELD[0]	0

The TxP Data Type Field is used in POS mode of operation only and is provided as a means to identify the type of traffic, ATM or packet data, being sent over POS-PHY.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cells being transferred over POS-PHY. Whenever a packet arrives on a PHY expected to be an ATM PHY, TDAT[31:24] should match ATM_FIELD during the TSX cycle. Otherwise, an interrupt (TDTFERRI) is signaled to indicate POS data type mismatch. These bits can be changed during operation.

POS_FIELD[7:0]

The POS_FIELD register is provided to identify ATM cells being transferred over POS-PHY. Whenever a packet arrives on a PHY expected to be an Packet PHY, TDAT[31:24] should match POS_FIELD during the TSX cycle. Otherwise, an interrupt (TDTFERRI) is signaled to indicate POS data type mismatch. These bits can be changed during operation.

11.8 Input Scalable Data Queue

Register 0x240: Input SDQ Control

Bit	Type	Function	Default
31:2		Unused	X
1	R	TIP	X
0	R/W	SDQRST	1

SDQRST

This bit is used to reset the SDQ. The SDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

TIP

This bit is asserted after the S/UNI-ATLAS-3200 Identity/Load Counts Register or any of the Input SDQ Count registers is written to, and goes low once the per-PHY and aggregate counts in the Input SDQ counting registers are valid.

Register 0x241: Input SDQ Interrupts

Bit	Type	Function	Default
31:12		Unused	X
11		UNDI	X
10		EOPI	X
9		SOPI	X
8		OFLI	X
7: 4		Unused	X
3	R/W	UNDE	0
2	R/W	EOPE	0
1	R/W	SOPE	0
0	R/W	OFLE	0

OFLE:

When this bit is set to 1, FIFO overflows cause INTB to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

EOPE

When this bit is set to 1, bad EOP signals cause INTB to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

SOPE:

When this bit is set to 1, bad SOP signals cause INTB to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

UNDRUNE

When this bit is set to 1, FIFO under-runs cause INTB to be asserted. If this bit is set to 0, FIFO under-runs do not cause INTB to be asserted.

OFLI

This bit is set when any of the configured FIFOs overflows. The FIFO that caused this interrupt is available in OFL_FIFO[5:0] in the FIFO overflow ID register. This bit is cleared when this register is read.

SOPI

This bit is set when two SOPs arrive consecutively on the same FIFO without being separated by an EOP. The FIFO that caused the interrupt is available in SOP_FIFO[5:0] in the FIFO SOP error ID register. This bit is cleared when this register is read.

EOPI

This bit is set when two EOPs arrive consecutively on the same FIFO without being separated by a SOP. The FIFO that caused the interrupt is available in EOP_FIFO[5:0] in the FIFO EOP error ID register. This bit is cleared when this register is read.

UNDI

This bit is set when data is requested from an empty FIFO, i.e. when the FIFO underruns. The FIFO that caused this interrupt is available in UND_FIFO[5:0] in the FIFO under-run ID register. This bit is cleared when this register is read. This interrupt should never occur, because it would indicate an error internal to the device.

Register 0x242: Input SDQ Interrupt ID

This register identifies the FIFOs associated with individual interrupts. Because reading the interrupts causes them to be cleared, it is preferable to read the Interrupt ID register first and then the Interrupt register.

Bit	Type	Function	Default
31:30		Unused	X
29:24	R	UND_FIFO[5:0]	X
23:22		Unused	X
21:16	R	EOP_FIFO[5:0]	X
15:14		Unused	X
13:8	R	SOP_FIFO[5:0]	X
7:6		Unused	X
5:0	R	OFL_FIFO[5:0]	X

OFL_FIFO[5:0]

Whenever OFLI becomes logic 1, these bits are loaded with the FIFO that overflowed. Once OFLI becomes logic 1, this value will not change until OFLI is cleared, and then becomes logic 1 again.

SOP_FIFO[5:0]

Whenever SOPI becomes logic 1, these bits are loaded with the FIFO that received two consecutive SOPs without an intervening EOP. Once SOPI becomes logic 1, this value will not change until SOPI is cleared, and then becomes logic 1 again.

EOP_FIFO[5:0]

Whenever EOPI becomes logic 1, these bits are loaded with the FIFO that received two consecutive EOPs without an intervening SOP. Once EOPI becomes logic 1, this value will not change until EOPI is cleared, and then becomes logic 1 again.

UND_FIFO[5:0]

Whenever UNDI becomes logic 1, these bits are loaded with the FIFO that underflowed. Once UNDI becomes logic 1, this value will not change until UNDI is cleared, and then becomes logic 1 again.

Register 0x244: Input SDQ Indirect Address

Writing to this register initialtes a read or write access (based on RWB) to a set of indirect registers that set up the FIFOs for each PHY: Input SDQ Indirect Configuration, Input SDQ Buffer and Data Available Threshold and Input SDQ Indirect Cell Count. FIFOs must be configured according to a set of rules defined in Section 13.1. In order to change the current setup of a FIFO, it is recommended that the user read the existing setup information first, makes any modifications as required, and write back the new configuration .

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	0
14	R/W	RWB	1
13	R/W	FLUSH	1
12	R	EMPTY	1
11:6		Unused	X
5:0	R/W	PHYID[5:0]	0

PHYID[5:0]

This is a 6-bit number that is used to describe the current FIFO being addressed by the Input SDQ FIFO Indirect Configuration and Indirect Cells and Packets Count Register. The range of FIFO numbers that can be used is 0 to 47.

EMPTY

This read-only bit indicates if the requested FIFO is empty or not. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in the FIFO Indirect Address register has no data available to be read out. This bit reflects the read-side perspective and will not react immediately to writes. Before reconfiguring a disabled FIFO, this bit needs to be sampled at 1, indicating that the FIFO is currently empty. A non-empty FIFO can be forced empty by writing FLUSH to logic 1.

FLUSH

FLUSH is an indirect configuration register bit. When RWB = 0, the value written to this bit will be written to the FLUSH bit for the specified PHYID. A logic 1 on FLUSH causes the SDQ to discard all the current data in the specified FIFO; a logic 0 must be written to the FIFO in order for it to begin processing data again. FLUSH is typically used when a non-empty FIFO needs to be reconfigured.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] will become available in the EMPTY bit, the Input SDQ Indirect Configuration register, and the Input SDQ Indirect Cell and Packet Count registers. When this bit is set to 0, the user is writing the configuration of a FIFO. The SDQ latches in the data in the Input SDQ Indirect Configuration and the FLUSH bit into the configuration for the specified FIFO.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the access is complete, the information for the FIFO is now available in the EMPTY bit, the Input SDQ Indirect Configuration Register, and the Input SDQ Cells and Packets Count register, and another access can be initiated.

Register 0x245: Input SDQ Indirect Configuration

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	FIFO_ENBL	0
14	R/W	FIFO_TYPE	0
13:7	R/W	FIFO_SIZE[6:0]	0000001
6:0	R/W	FIFO_PTR[6:0]	0000000

FIFO_PTR[6:0]

This 7-bit pointer specifies where a FIFO starts in the 3072-word SRAM space. It is specified in blocks, where a block is defined as 32 words (128 bytes). The range of this pointer should be 0 to 95; any other values will cause unpredictable effects. This pointer is calculated and programmed based on the number of FIFOs required by the system and the size of each FIFO. The rules governing this calculation are stated in section 13.1.

FIFO_SIZE[6:0]

This 7-bit number denotes the size of a FIFO in blocks. The size of a FIFO is related to the bandwidth. Table 41 shows the suggested FIFO size based on the PHY bandwidth. Since there are altogether 96 blocks in the SRAM, the legal range for this number is 1 to 96; settings outside this range are reserved and may cause unpredictable effects.

Table 41 Suggested FIFO Size Encoding

FIFO Size (blocks)	FIFO Size (cells)	Bandwidth
1	2	Below STS-1
2	4	STS-1 or less
6	12	STS-3
24	48	STS-12 or STS-48
96	192	STS-48

FIFO_TYPE

This bit must be set to logic 0 for all FIFOs in the Input SDQ to indicate that ATM Cells are being handled.

FIFO_ENBL

This bit enables individual FIFOs. Writing a ‘0’ to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but data can be read from it until it is drained completely. In order to reconfigure a FIFO during operation, it should be disabled and drained; a FIFO can be drained immediately through the use of the FLUSH bit. By default, all the FIFOs are disabled. Only ATM PHYs should be enabled in the Input SDQ.

It is recommended that all FIFOs that are disabled also have the FLUSH bit set to logic 1. This will tend to eliminate spurious interrupts.

Register 0x246: Input SDQ Cells and Packets Count

This register is used to read the count of the number of cells in the FIFO addressed by the Input SDQ Indirect Address Register. The count reflects the write-side perspective, and will not react immediately to reads. The counts are latched when the S/UNI-ATLAS-3200 Identity / Load Counts Register is written to, or when any of the Input SDQ Count registers are written to. While the transfer is in progress, the TIP bit is asserted in the Input SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. Once TIP goes low, the count for the PHY specified in the Input SDQ Address register will be placed in this register.

The recommended sequence for using this register is:

1. Program the desired PHYID in the Input SDQ Address Register. Typically this would be done while setting RWB = 1.

2. Execute a write to this register

3. Poll TIP in the Input SDQ Control Register until it becomes 0.

4. Read the value in this register.

Bit	Type	Function	Default
31:12		Unused	X
11:0	R	COUNT[11:0]	0

COUNT[11:0]

This read-only field holds the last sampled count for the FIFO requested by PHYID[5:0] in the FIFO indirect address register. Since each FIFO can hold up to 3072 POS packets or 192 ATM cells, this count does not saturate or roll over.

Register 0x247: Input SDQ Cells Accepted Aggregate Count

Bit	Type	Function	Default
31:0	R	ACOUNT[31:0]	0

This read-only field contains the aggregate count of all the ATM cells accepted by the Input SDQ. This register is latched when a write is performed to the S/UNI-ATLAS-3200 Identity / Load Counts Register or to any of the Input SDQ counter registers. After the count is latched into the register, the internal counter is reset to 0 and starts counting again.

During the latching of this and other counters, the TIP bit is asserted in the Input SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. The update does not cause the counter to lose any events – the events after the latching are included in the subsequent count value.

ACOUNT[31:0]

ACOUNT is a 32-bit aggregate counter which records the number of cells or packets accepted by the Input SDQ since last read. It saturates at the maximum value.

Register 0x248: Input SDQ Cells Dropped Aggregate Count

Bit	Type	Function	Default
31:16		Unused	X
15:0	R	DCOUNT[15:0]	0

This read-only field contains the aggregate count of all the ATM cells dropped by the Input SDQ due to overflow or transfer errors. This register is latched when a write is performed to the S/UNI-ATLAS-3200 Identity / Load Counts Register or to any of the Input SDQ counter registers. After the count is latched into the register, the internal counter is reset to 0 and starts counting again.

During the latching of this and other counters, the TIP bit is asserted in the Input SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. The update does not cause the counter to lose any events – the events after the latching are included in the subsequent count value.

DCOUNT[15:0]

ACOUNT is a 16-bit aggregate counter which records the number of cells or packets dropped by the Input SDQ since last read. It saturates at the maximum value.

11.9 Rx PHY Interface

The RxPhy Interface registers should be left in their default state when the RxPhy is not being used (i.e. when Egress_IngressB is logic 1 in the S/UNI-ATLAS-3200 Master Configuration Register).

Register 0x260: RxP Configuration

Bit	Type	Function	Default
31:16		Unused	X
15		Unused	X
14		Unused	X
13	R/W	RSXPAUSE[1]	0
12	R/W	RSXPAUSE[0]	0
11		Unused	X
10		Unused	X
9	R/W	POSTLEN[1]	0
8	R/W	POSTLEN[0]	0
7		Unused	X
6		Unused	X
5	R/W	PRELEN[1]	0
4	R/W	PRELEN[0]	0
3	R/W	SERVEOVRD	0
2	R/W	HEC	0
1	R/W	ODDPARITY	0
0	R/W	RXPRST	1

RXPRST

The RXPRST bit is used to reset the RxPhy block circuitry. When RXPRST is set to logic zero, the RxPhy block operates normally. When RXPRST is set to logic one, the RxPhy block is held in reset, apart from Normal Mode registers which may be accessed for purposes of initialization.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is generated by the RxPhy. Set this bit to ‘1’ in order to generate odd parity. Set this bit to ‘0’ to generate even parity. This bit is global and affects all PHY channels. This bit can be altered during operation.

HEC

The HEC bit is used to indicate whether the HEC/UDF word is included in ATM cells. When the value is ‘1’, the ATM cells contain the HEC/UDF word. When the value is ‘0’, the ATM cells do not contain the HEC/UDF word. In any event, the HEC is undefined at the ATM layer, and will not be calculated by RxPhy. This bit cannot be changed during operation and can only be changed when RXPRST is logic one.

SERVEOVRD

The SERVEOVRD bit is used to configure whether Servicing Override is performed in UTOPIA. Normally, the switch or TM device is responsible for polling and servicing the FIFOs of this interface. The servicing Override option allows this interface to appear as a single PHY to the switch or TM, with the RxPhy block choosing which PHY queues to service, using the Polling and Servicing Calendar. When the value is ‘1’, the servicing override is engaged. When the value is ‘0’, the servicing override is not engaged and expects normal MPHY polling and servicing from the switch or TM. This bit cannot be changed during operation and can only be changed when RXPRST is logic one.

PRELEN[1:0]

The PRELEN bits are used to indicate the size of the prepend applied to the ATM cells to external blocks. A value of ‘00’ indicates no prepend word. A value of ‘01’ indicates 1 prepend word. A value of ‘10’ indicates 2 prepend words A value of ‘11’ is invalid. These bits cannot be changed during operation and can only be changed when RXPRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

POSTLEN[1:0]

The POSTLEN bits are used to indicate the size of the postpend applied to the ATM cells. A value of ‘00’ indicates no postpend word. A value of ‘01’ indicates 1 postpend word. A value of ‘10’ indicates 2 postpend words. A value of ‘11’ is invalid. These bits cannot be changed during operation and can only be changed when RXPRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

RSXPAUSE[1:0]

RSXPAUSE bits control the number of clocks to pause between transfers as per POS-PHY Level 3 specification. These bits are effective in POS mode only. The default setting is ‘00’ meaning no pause will occur between transfers resulting in maximum bandwidth usage. As setting of ‘01’ indicates 1 clock between transfers and a setting of ‘10’ indicates 2 clocks between transfers. A setting of ‘11’ is reserved. These bits cannot be changed during operation and can only be changed when RXPRST is logic one.

Register 0x261: RxP Interrupt

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1		Unused	X
0	R	RUNTCELLI	X

RUNTCELLI

RUNTCELLI is set if RPU_ENB is deasserted before the end of the cell transfer, resulting in a partial cell transfer. If this occurs, the remainder of the cell is discarded. This error can be caused by incorrectly setting the size of the cell expected by this interface. Check that the HEC, pre and post word registers are properly set.

Register 0x262: RxP Interrupt Enable

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1		Unused	X
0	R/W	RUNTCELLE	0

A value of '0' masks the corresponding interrupt from asserting INTB. A setting of '1' unmasks the interrupt enabling the assertion of INTB. The enable bits correspond in bit location to the interrupts described in RxP Interrupt register.

Register 0x263: RxP PHY Indirect Address and Data

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	X
14	R/W	CONFIG_RWB	1
13	R/W	PHY_ADDR[5]	0
12	R/W	PHY_ADDR[4]	0
11	R/W	PHY_ADDR[3]	0
10	R/W	PHY_ADDR[2]	0
9	R/W	PHY_ADDR[1]	0
8	R/W	PHY_ADDR[0]	0
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R/W	BURST_SIZE[3]	0
2	R/W	BURST_SIZE[2]	0
1	R/W	BURST_SIZE[1]	1
0	R/W	BURST_SIZE[0]	1

The RxL Calendar Indirect Address and Data register is an indirect register used to program the POS-PHY burst sizes.

BURST_SIZE[3:0]

The BURST_SIZE data register specifies the maximum number of 16-byte blocks allowed to be transferred on a PHY in POS-PHY mode before the next PHY in the calendar is automatically selected. A burst is automatically terminated at the end of a packet, or when the FIFO becomes empty. The maximum number of blocks in a burst is BURST_SIZE + 1, so that the minimum Burst Size is 1 block (16 bytes), and the maximum burst size is 16 blocks (256 bytes). For PHYs carrying ATM cells over POS-PHY, BURST_SIZE must be set to the default 0x3. This register is used only in POS mode, and may be changed during operation.

PHY_ADDR[5:0]

The PHY_ADDR register specifies the PHY for which an indirect read or write of the BURST_SIZE field is to occur, depending on the value of CONFIG_RWB. The PHY_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data for PHY_ADDR, which will be placed in the BURST_SIZE register. A value of '0' means that a write of the information in BURST_SIZE will be performed at address PHY_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0x264: RxP Calendar Length

Bit	Type	Function	Default
31:8		Unused	X
6	R/W	CALENDAR_LENGTH[6]	0
5	R/W	CALENDAR_LENGTH[5]	0
4	R/W	CALENDAR_LENGTH[4]	0
3	R/W	CALENDAR_LENGTH[3]	0
2	R/W	CALENDAR_LENGTH[2]	0
1	R/W	CALENDAR_LENGTH[1]	0
0	R/W	CALENDAR_LENGTH[0]	0

CALENDAR_LENGTH[6:0]

The CALENDAR_LENGTH register is provided to program the length of calendar used for servicing up to a maximum of 128 entries. The length of the calendar is CALENDAR_LENGTH[6:0] + 1. For example, a CALENDAR_LENGTH[6:0] = “000000” indicates a calendar length of one. A description of the calendar is provided in Section 10.1.5. For maximum efficiency, it is recommended that the RxPhy calendar length be set to at least 64, and preferably as close to 128 as is practical. A shorter set of calendar entries can simply be repeated several times to pad out to a greater length.

Register 0x265: RxP Calendar Indirect Address and Data

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	X
14	R/W	CALENDAR_ADDR[6]	0
13	R/W	CALENDAR_ADDR[5]	0
12	R/W	CALENDAR_ADDR[4]	0
11	R/W	CALENDAR_ADDR[3]	0
10	R/W	CALENDAR_ADDR[2]	0
9	R/W	CALENDAR_ADDR[1]	0
8	R/W	CALENDAR_ADDR[0]	0
7	R/W	CONFIG_RWB	1
6		Unused	X
5	R/W	CALENDAR_DATA[5]	0
4	R/W	CALENDAR_DATA[4]	0
3	R/W	CALENDAR_DATA[3]	0
2	R/W	CALENDAR_DATA[2]	0
1	R/W	CALENDAR_DATA[1]	0
0	R/W	CALENDAR_DATA[0]	0

The RxP Calendar Indirect Address Data register is an indirect register used to program the servicing calendar as described in Section 10.1.5. The RxP block performs polling and servicing in UTOPIA mode.

CALENDAR_DATA[5:0]

The CALENDAR_DATA register is provided to program the sequence calendar with PHY IDs between 0 and 47. The calendar consists of a maximum of 128 entries where the CALENDAR_ADDR is used to access one of the 128 entries to either write or read CALENDAR_DATA. The length of the calendar is set in the RxP Calendar Length register. These bits can be altered during operation.

CALENDAR_ADDR[6:0]

The CALENDAR_ADDR register is an indirect address register that is used with CALENDAR_DATA register. The two registers together allow indirect address reads and writes using a small amount of external address space. The CALENDAR_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register bit specifies whether a read or write is to be performed. A value of '1' means that a read is to be performed on the data at CALENDAR_ADDR and will be placed in the CALENDAR_DATA register. A value of '0' means that a write of the information in CALENDAR_DATA will be performed at address CALENDAR_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further accesses.

Register 0x266: RxP Data Type Field

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	POS_FIELD[7]	0
14	R/W	POS_FIELD[6]	0
13	R/W	POS_FIELD[5]	0
12	R/W	POS_FIELD[4]	0
11	R/W	POS_FIELD[3]	0
10	R/W	POS_FIELD[2]	0
9	R/W	POS_FIELD[1]	0
8	R/W	POS_FIELD[0]	1
7	R/W	ATM_FIELD[7]	0
6	R/W	ATM_FIELD[6]	0
5	R/W	ATM_FIELD[5]	0
4	R/W	ATM_FIELD[4]	0
3	R/W	ATM_FIELD[3]	0
2	R/W	ATM_FIELD[2]	0
1	R/W	ATM_FIELD[1]	0
0	R/W	ATM_FIELD[0]	0

The RxP Data Type Field is used in POS mode of operation only and is provided as a means to identify the type of traffic, ATM or packet data, being sent over POS-PHY.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cells being transferred over POS_PHY. When the outgoing data is of type ATM cell, then the ATM_FIELD is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[7:0]. These bits can be changed during operation.

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data in POS_PHY. When the outgoing data is of type packet, then the POS_FIELD is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[7:0]. These bits can be changed during operation.

11.10 Tx Link Interface

The TxLink Interface registers should be left in their default state when the TxLink is not being used (i.e. when Egress_IngressB is logic 0 in the S/UNI-ATLAS-3200 Master Configuration Register).

Register 0x280: TxL Configuration

Bit	Type	Function	Default
31:16		Unused	X
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	POSTLEN[1]	0
8	R/W	POSTLEN[0]	0
7		Unused	X
6		Unused	X
5	R/W	PRELEN[1]	0
4	R/W	PRELEN[0]	0
3	R/W	USE_STPA	0
2	R/W	HEC	0
1	R/W	ODDPARITY	0
0	R/W	TXLRST	1

TXLRST

The TXLRST bit is used to reset the TxLink block circuitry. When TXLRST is set to logic zero, the TxLink block operates normally. When TXLRST is set to logic one, the TxLink block circutry is held in reset, except for the Normal Mode registers which may be accessed for purposes of initialization.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is generated by the TxLink. Set this bit to '1' in order to generate odd parity. Set this bit to '0' to generate even parity. This bit is global and affects all PHY channels. This bit can be changed during operation.

HEC

The HEC bit is used to indicate whether the HEC/UDF word is included in ATM cells. When the value is '1', the ATM cells contain the HEC/UDF word. When the value is '0', the ATM cells do not contain the HEC/UDF word. In any event, the HEC is undefined at the ATM layer, and will not be calculated by RxLink. This bit cannot be changed during operation and can only be changed when RXLRST is logic one.

USE_STPA

The USE_STPA bit is used to indicate whether the TxLink will recognize transitions on the TLP_STPA pin. When USE_STPA is logic 0, TLP_STPA is ignored and transfers are based solely on TLP_PTPA. If USE_STPA is logic 1, then on sampling STPA high, the TxLink will immediately cease transferring data. The TLP_STPA signal is valid 3 clocks after TSX is driven on the interface by the LINK device; TxLink stops transmitting data three cycles after

PRELEN[1:0]

The PRELEN bits are used to indicate the size of the prepend applied to the ATM cells to external blocks. A value of '00' indicates no prepend word. A value of '01' indicates 1 prepend word. A value of '10' indicates 2 prepend words A value of '11' is invalid. These bits cannot be changed during operation and can only be changed when RXPRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

POSTLEN[1:0]

The POSTLEN bits are used to indicate the size of the postpend applied to the ATM cells. A value of '00' indicates no postpend word. A value of '01' indicates 1 postpend word. A value of '10' indicates 2 postpend words. A value of '11' is invalid. These bits cannot be changed during operation and can only be changed when RXPRST is logic one. These bits apply to all PHY channels. The sum of PRELEN + POSTLEN must not exceed 2, or correct operation is not guaranteed.

Register 0x281: TxL Interrupt Enable

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	R/W	TERRE	0
0	R/W	TCAERRE	0

A value of '0' masks the corresponding interrupt from asserting INTB. A setting of '1' unmasks the interrupt enabling the assertion of INTB. The enable bits correspond in bit location to the interrupts described in RxP Interrupt register.

Register 0x282: TxL Interrupt

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	R	TERRI	0
0	R	TCAERRI	0

The bits in this register are indicate that the corresponding event has occurred since the last time this register was read. The bits in this register are cleared when the register is read.

TCAERRI

In UTOPIA mode, the TCAERR bit is set if the PHY layer device does not respond with asserted TLU_CLAV after the TxLink selects the PHY for transfer. Because PHYs are not selected unless they have previously indicated a cell buffer available, this condition indicates an error. If this case occurs, the cell will be transmitted anyway. This bit is not used in POS-PHY mode.

TERRI

This bit is set if the current POS packet from SDQ is in error. This bit is set whenever TxLink asserts TERR along with TEOP signal.

Register 0x286: TxL Data Type Field

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	POS_FIELD[7]	0
14	R/W	POS_FIELD[6]	0
13	R/W	POS_FIELD[5]	0
12	R/W	POS_FIELD[4]	0
11	R/W	POS_FIELD[3]	0
10	R/W	POS_FIELD[2]	0
9	R/W	POS_FIELD[1]	0
8	R/W	POS_FIELD[0]	1
7	R/W	ATM_FIELD[7]	0
6	R/W	ATM_FIELD[6]	0
5	R/W	ATM_FIELD[5]	0
4	R/W	ATM_FIELD[4]	0
3	R/W	ATM_FIELD[3]	0
2	R/W	ATM_FIELD[2]	0
1	R/W	ATM_FIELD[1]	0
0	R/W	ATM_FIELD[0]	0

The TxL Data Type Field is used in POS mode of operation only and is provided as a means to identify the type of traffic, ATM or packet data, being sent over POS-PHY.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cell being transferred over POS_PHY. When the outgoing data is of type ATM cell, then the ATM_FIELD is inserted in TLP_DAT[31:24] at the cycle in which the in-band address is inserted in TLP_DAT[5:0]. These bits can be altered during operation.

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data in POS_PHY. When the outgoing data is of type packet, then the POS_FIELD is inserted in TLP_DAT[31:24] at the cycle in which the in-band address is inserted in TLP_DAT[5:0]. These bits can be altered during operation.

Register 0x288: TxL PHY Indirect Address

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	X
14	R/W	CONFIG_RWB	1
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5	R/W	PHY_ADDR[5]	0
4	R/W	PHY_ADDR[4]	0
3	R/W	PHY_ADDR[3]	0
2	R/W	PHY_ADDR[2]	0
1	R/W	PHY_ADDR[1]	0
0	R/W	PHY_ADDR[0]	0

The TxL PHY Indirect Address register is an indirect address register used along with the TxL PHY Indirect Data.

PHY_ADDR[5:0]

The PHY_ADDR register specifies the PHY for which an indirect read or write on the TxL PHY Indirect Data register is to occur, depending on the value of CONFIG_RWB. The PHY_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data for PHY_ADDR and will be placed in the TxL PHY Indirect DATA register. A value of '0' means that a write of the information in TxL PHY Indirect DATA will be performed at address PHY_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further accesses.

Register 0x289: TxL PHY Indirect Data

Bit	Type	Function	Default
31:14		Unused	X
13	R/W	PORT_X_MAP[5]	0
12	R/W	PORT_X_MAP[4]	0
11	R/W	PORT_X_MAP[3]	0
10	R/W	PORT_X_MAP[2]	0
9	R/W	PORT_X_MAP[1]	0
8	R/W	PORT_X_MAP[0]	0
7	R/W	Unused	0
6	R/W	Unused	0
5	R/W	Unused	0
4	R/W	Unused	0
3	R/W	BURST_SIZE[3]	0
2	R/W	BURST_SIZE[2]	0
1	R/W	BURST_SIZE[1]	1
0	R/W	BURST_SIZE[0]	1

The TxL PHY Indirect Data register is an indirect access register along with the TxL PHY Indirect Address.

BURST_SIZE[3:0]

The BURST_SIZE data register specifies the maximum number of 16-byte blocks allowed to be transferred on a PHY in POS-PHY mode before the next PHY in the calendar is automatically selected. A burst is automatically terminated at the end of a packet, or when the FIFO becomes empty. The maximum number of blocks in a burst is BURST_SIZE + 1, so that the minimum Burst Size is 1 block (16 bytes), and the maximum burst size is 16 blocks (256 bytes). For PHYs carrying ATM cells over POS-PHY, BURST_SIZE must be set to the default 0x3. This register is used only in POS mode, and may be changed during operation.

PORT X MAP

The PORT_X_MAP bits are used to translate PHY addresses. On powerup, each internal FIFO PHYID will map to the identical PHY port. If translation is needed, then the location for the external (UL3 or POS-PHY3 bus) PHY address must be programmed with the value of the desired internal FIFO PHYID. The TxLink calendar always refers to the external PHYID; the rest of the device will act on the internal FIFO PHYID. If the PHYID is written to a value greater then 47, then data on that PHY is ignored.

Register 0x28A: TxL Calendar Length

Bit	Type	Function	Default
31: 7		Unused	X
6	R/W	CALENDAR_LENGTH[6]	0
5	R/W	CALENDAR_LENGTH[5]	0
4	R/W	CALENDAR_LENGTH[4]	0
3	R/W	CALENDAR_LENGTH[3]	0
2	R/W	CALENDAR_LENGTH[2]	0
1	R/W	CALENDAR_LENGTH[1]	0
0	R/W	CALENDAR_LENGTH[0]	0

The register is used in both POS and UTOPIA mode of operation to control the weighted round-robin polling and servicing algorithm. . A description of the calendar is provided in Section 10.1.5

Generally, the calendar should be set up at device initialization and subsequently be left unchanged. When the calendar length, or a calendar entry is updated during cell or packet flow, there may be an impact on polling, which may result in an overrun of the PHY device, or a spurious TCA Error interrupt. The overrun may occur on any PHY that is currently transferring data. This impact will be avoided if USE_STPA is logic one while the calendar is being updated

CALENDAR_LENGTH[6:0]

The CALENDAR_LENGTH register is provided to program the length of calendar used for polling and servicing up to a maximum of 128 entries. . The length of the calendar is CALENDAR_LENGTH[6:0] + 1. For example, a CALENDAR_LENGTH[6:0] = “000000” indicates a calendar length of one. (See Register 0x28B).

Register 0x28B: TxL Calendar Indirect Address and Data

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	X
14	R/W	CALENDAR_ADDR[6]	0
13	R/W	CALENDAR_ADDR[5]	0
12	R/W	CALENDAR_ADDR[4]	0
11	R/W	CALENDAR_ADDR[3]	0
10	R/W	CALENDAR_ADDR[2]	0
9	R/W	CALENDAR_ADDR[1]	0
8	R/W	CALENDAR_ADDR[0]	0
7	R/W	CONFIG_RWB	1
6		Unused	X
5	R/W	CALENDAR_DATA[5]	0
4	R/W	CALENDAR_DATA[4]	0
3	R/W	CALENDAR_DATA[3]	0
2	R/W	CALENDAR_DATA[2]	0
1	R/W	CALENDAR_DATA[1]	0
0	R/W	CALENDAR_DATA[0]	0

The TxL Calendar Indirect Address Data register is an indirect address and data register. The register is used in both POS and UTOPIA mode of operation to control the weighted round-robin polling and servicing algorithm. . A description of the calendar is provided in Section 10.1.5.

Generally, the calendar should be set up at device initialization and subsequently be left unchanged. When the calendar length, or a calendar entry is updated during cell or packet flow, there may be an impact on polling, which may result in an overrun of the PHY device, or a spurious TCA Error interrupt. The overrun may occur on any PHY that is currently transferring data. This impact will be avoided if USE_STPA is logic one while the calendar is being updated

CALENDAR_DATA[5:0]

The CALENDAR_DATA register is provided to program the sequence calendar with PHY ids between 0 and 47. The calendar consists of a maximum of 128 entries where the CALENDAR_ADDR is used to access one of the 128 entries to either write or read CALENDAR_DATA. The length of the calendar is set in the TxL Calendar Length register.

CALENDAR_ADDR[6:0]

The CALENDAR_ADDR register is an indirect address register that is used with CALENDAR_DATA register. The CALENDAR_ADDR field determines the position in the calendar which is to be written or read.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read of the calendar is to be performed at CALENDAR_ADDR and the data will be placed in the CALENDAR_DATA register. A value of '0' means that a write of the information in CALENDAR_DATA will be performed at address CALENDAR_ADDR of the calendar.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means an operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

11.11 Output Scalable Data Queue

Register 0x2A0: Output SDQ Control

Bit	Type	Function	Default
31:2		Unused	X
1	R	TIP	X
0	R/W	SDQRST	1

SDQRST

This bit is used to reset the SDQ. The SDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

TIP

This bit is asserted after the S/UNI-ATLAS-3200 Identity/Load Counts Register or any of the Output SDQ Count registers is written to, and goes low once the per-PHY and aggregate counts in the Output SDQ counting registers are valid.

Register 0x2A1: Output SDQ Interrupts

Bit	Type	Function	Default
31:12		Unused	X
11		UNDI	X
10		EOPI	X
9		SOPI	X
8		OFLI	X
7: 4		Unused	X
3	R/W	UNDE	0
2	R/W	EOPE	0
1	R/W	SOPE	0
0	R/W	OFLE	0

OFLE

When this bit is set to 1, FIFO overflows cause INTB to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

EOPE

When this bit is set to 1, bad EOP signals cause INTB to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

SOPE

When this bit is set to 1, bad SOP signals cause INTB to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

UNDRUNE

When this bit is set to 1, FIFO under-runs cause INTB to be asserted. If this bit is set to 0, FIFO under-runs do not cause INTB to be asserted.

OFLI

This bit is set when any of the configured FIFOs overflows. The FIFO that caused this interrupt is available in OFL_FIFO[5:0] in the FIFO overflow ID register. This bit is cleared when this register is read. This interrupt should never occur, since it would indicate an error internal to the device.

SOPI

This bit is set when two SOPs arrive consecutively on the same FIFO without being separated by an EOP. The FIFO that caused the interrupt is available in SOP_FIFO[5:0] in the FIFO SOP error ID register. This bit is cleared when this register is read. This interrupt should never occur, since it would indicate an error internal to the device.

EOPI

This bit is set when two EOPs arrive consecutively on the same FIFO without being separated by a SOP. The FIFO that caused the interrupt is available in EOP_FIFO[5:0] in the FIFO EOP error ID register. This bit is cleared when this register is read. This interrupt should never occur, since it would indicate an error internal to the device.

UNDI

This bit is set when data is requested from an empty FIFO, i.e. when the FIFO underruns. The FIFO that caused this interrupt is available in UND_FIFO[5:0] in the FIFO under-run ID register. This bit is cleared when this register is read.

Register 0x2A2: Output SDQ Interrupt ID

This register identifies the FIFOs associated with individual interrupts. Because reading the interrupts causes them to be cleared, it is preferable to read the Interrupt ID register first and then the Interrupt register.

Bit	Type	Function	Default
31:30		Unused	X
29:24	R	UND_FIFO[5:0]	X
23:22		Unused	X
21:16	R	EOP_FIFO[5:0]	X
15:14		Unused	X
13:8	R	SOP_FIFO[5:0]	X
7:6		Unused	X
5:0	R	OFL_FIFO[5:0]	X

OFL_FIFO[5:0]

Whenever OFLI becomes logic 1, these bits are loaded with the FIFO that overflowed. Once OFLI becomes logic 1, this value will not change until OFLI is cleared, and then becomes logic 1 again.

SOP_FIFO[5:0]

Whenever SOPI becomes logic 1, these bits are loaded with the FIFO that received two consecutive SOPs without an intervening EOP. Once SOPI becomes logic 1, this value will not change until SOPI is cleared, and then becomes logic 1 again.

EOP_FIFO[5:0]

Whenever EOPI becomes logic 1, these bits are loaded with the FIFO that received two consecutive EOPs without an intervening SOP. Once EOPI becomes logic 1, this value will not change until EOPI is cleared, and then becomes logic 1 again.

UND_FIFO[5:0]

Whenever UNDI becomes logic 1, these bits are loaded with the FIFO that underflowed. Once UNDI becomes logic 1, this value will not change until UNDI is cleared, and then becomes logic 1 again.

Register 0x2A4: Output SDQ Indirect Address

Writing to this register initiates a read or write access (based on RWB) to a set of indirect registers that set up the FIFOs for each PHY: Output SDQ Indirect Configuration, Output SDQ Buffer and Data Available Threshold and Output SDQ Indirect Cell Count. FIFOs must be configured according to a set of rules defined in Section 13.1. In order to change the current setup of a FIFO, it is recommended that the user read the existing setup information first, makes any modifications as required, and write back the new configuration .

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	0
14	R/W	RWB	1
13	R/W	FLUSH	1
12	R	EMPTY	1
11:6		Unused	X
5:0	R/W	PHYID[5:0]	0

PHYID[5:0]

This is a 6-bit number that is used to describe the current FIFO being addressed by the Output SDQ FIFO Indirect Configuration and the Output SDQ Cells and Packets Count Register. The range of FIFO numbers that can be used is 0 to 47.

EMPTY

This read-only bit indicates if the requested FIFO is empty or not. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in the FIFO Indirect Address register has no data available to be read out. This bit reflects the read-side perspective and will not react immediately to writes.. Before reconfiguring a disabled FIFO, this bit needs to be sampled at 1, indicating that the FIFO is currently empty. A non-empty FIFO can be forced empty by writing FLUSH to logic 1.

FLUSH

FLUSH is an indirect configuration register bit. When RWB = 0, the value written to this bit will be written to the FLUSH bit for the specified PHYID. A logic 1 on FLUSH causes the SDQ to discard all the current data in the specified FIFO; a logic 0 must be written to the FIFO in order for it to begin processing data again. FLUSH is typically used when a non-empty FIFO needs to be reconfigured.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] will become available in the EMPTY bit and the Output SDQ Indirect Configuration register. When this bit is set to 0, the user is writing the configuration of a FIFO. The SDQ latches in the data in the Output SDQ Indirect Configuration and the FLUSH bit into the configuration for the specified FIFO.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the access is complete, the information for the FIFO is now available in the EMPTY bit and the Output SDQ Indirect Configuration Register, and another access can be initiated.

Register 0x2A5: Output SDQ Indirect Configuration

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	FIFO_ENBL	0
14	R/W	FIFO_TYPE	0
13:7	R/W	FIFO_SIZE[6:0]	0000001
6:0	R/W	FIFO_PTR[6:0]	0000000

FIFO_PTR[6:0]

This 7-bit pointer specifies where a FIFO starts in the 3072-word SRAM space. It is specified in blocks, where a block is defined as 32 words (128 bytes). The range of this pointer should be 0 to 95; any other values will cause unpredictable effects. This pointer is calculated and programmed based on the number of FIFOs required by the system and the size of each FIFO. The rules governing this calculation are stated in section 13.1.

FIFO_SIZE[6:0]

This 7-bit number denotes the size of a FIFO in blocks. The size of a FIFO is related to the bandwidth. Table 42 below shows the suggested FIFO size based on the PHY bandwidth. Since there are altogether 96 blocks in the SRAM, the legal range for this number is 1 to 96; settings outside this range are reserved and may cause unpredictable effects.

Table 42 Suggested FIFO Size Encoding

FIFO Size (blocks)	FIFO Size (cells)	Bandwidth
1	2	Below STS-1
2	4	STS-1 or less
6	12	STS-3
24	48	STS-12 or STS-48
96	192	STS-48

FIFO_TYPE

This bit must be set to logic 0 for all FIFOs in the Output SDQ to indicate that ATM Cells are being handled.

FIFO_ENBL

This bit enables individual FIFOs. Writing a ‘0’ to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but data can be read from it until it is drained completely. In order to reconfigure a FIFO during operation, it should be disabled and drained; a FIFO can be drained immediately through the use of the FLUSH bit. By default, all the FIFOs are disabled. Only ATM PHYs should be enabled in the Output SDQ

It is recommended that all FIFOs that are disabled also have the FLUSH bit set to logic 1. This will tend to eliminate spurious interrupts.

Register 0x2A6: Output SDQ Cells and Packets Count

This register is used to read the count of the number of cells in the FIFO specified in the Output SDQ Indirect Address register. The count reflects the write-side perspective, and will not react immediately to reads. The counts are latched when the S/UNI-ATLAS-3200 Identity / Load Counts Register is written to, or when any of the Output SDQ Count registers are written to. While the transfer is in progress, the TIP bit is asserted in the Output SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. Once TIP goes low, the count for the PHY specified in the Output SDQ Address register will be placed in this register.

The recommended sequence for using this register is:

1. Program the desired PHYID in the Output SDQ Indirect Address Register. Typically this would be done while setting RWB = 1.

2. Execute a write to this register

3. Poll TIP in the Output SDQ Control Register until it becomes 0.

4. Read the value in this register.

Bit	Type	Function	Default
31:12		Unused	X
11:0	R	COUNT[11:0]	0

COUNT[11:0]

This read-only field holds the last sampled count for the FIFO requested by PHYID[5:0] in the FIFO indirect address register. Since each FIFO can hold up to 3072 POS packets or 192 ATM cells, this count does not saturate or roll over.

Register 0x2A7: Output SDQ Cells Accepted Aggregate Count

Bit	Type	Function	Default
31:0	R	ACOUNT[31:0]	0

This read-only field contains the aggregate count of all the ATM cells accepted by the Output SDQ. This register is latched when a write is performed to the S/UNI-ATLAS-3200 Identity / Load Counts Register or any of the Output SDQ counter registers. After the count is latched into the register, the internal counter is reset to 0 and starts counting again.

During the latching of this and other counters, the TIP bit is asserted in the Output SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. The update does not cause the counter to lose any events – the events after the latching are included in the subsequent count value.

ACOUNT[31:0]

ACOUNT is a 32-bit aggregate counter which records the number of cells or packets accepted by the Output SDQ since last read. It saturates at the maximum value.

Register 0x2A8: Output SDQ Cells Dropped Aggregate Count

Bit	Type	Function	Default
31:16		Unused	X
15:0	R	DCOUNT[15:0]	0

This read-only field contains the aggregate count of all the ATM cells dropped by the Output SDQ due to overflow or transfer errors. This register is latched when a write is performed to the S/UNI-ATLAS-3200 Identity / Load Counts Register or to any of the Output SDQ counter registers. After the count is latched into the register, the internal counter is reset to 0 and starts counting again.

During the latching of this and other counters, the TIP bit is asserted in the Output SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. The update does not cause the counter to lose any events – the events after the latching are included in the subsequent count value.

DCOUNT[15:0]

ACOUNT is a 16-bit aggregate counter which records the number of cells or packets dropped by the Output SDQ since last read. It saturates at the maximum value.

11.12 Packet Bypass Scalable Data Queue

Register 0x2C0: Bypass SDQ Control

Bit	Type	Function	Default
31:2		Unused	X
1	R	TIP	X
0	R/W	SDQRST	1

SDQRST

This bit is used to reset the SDQ. The SDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

TIP

This bit is asserted after the S/UNI-ATLAS-3200 Identity/Load Counts Register or any of the Bypass SDQ Count registers is written to, and goes low once the per-PHY and aggregate counts in the Bypass SDQ counting registers are valid.

Register 0x2C1: Bypass SDQ Interrupts

Bit	Type	Function	Default
31:12		Unused	X
11		UNDI	X
10		EOPI	X
9		SOPI	X
8		OFLI	X
7: 4		Unused	X
3	R/W	UNDE	0
2	R/W	EOPE	0
1	R/W	SOPE	0
0	R/W	OFLE	0

OFLE

When this bit is set to 1, FIFO overflows cause INTB to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

EOPE

When this bit is set to 1, bad EOP signals cause INTB to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

SOPE

When this bit is set to 1, bad SOP signals cause INTB to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

UNDRUNE

When this bit is set to 1, FIFO under-runs cause INTB to be asserted. If this bit is set to 0, FIFO under-runs do not cause INTB to be asserted.

OFLI

This bit is set when any of the configured FIFOs overflows. The FIFO that caused this interrupt is available in OFL_FIFO[5:0] in the FIFO overflow ID register. This bit is cleared when this register is read.

SOPI

This bit is set when two SOPs arrive consecutively on the same FIFO without being separated by an EOP. The FIFO that caused the interrupt is available in SOP_FIFO[5:0] in the FIFO SOP error ID register. This bit is cleared when this register is read.

EOPI

This bit is set when two EOPs arrive consecutively on the same FIFO without being separated by a SOP. The FIFO that caused the interrupt is available in EOP_FIFO[5:0] in the FIFO EOP error ID register. This bit is cleared when this register is read.

UNDI

This bit is set when data is requested from an empty FIFO, i.e. when the FIFO underruns. The FIFO that caused this interrupt is available in UND_FIFO[5:0] in the FIFO under-run ID register. This bit is cleared when this register is read.

Register 0x2C2: Bypass SDQ Interrupt ID

This register identifies the FIFOs associated with individual interrupts. Because reading the interrupts causes them to be cleared, it is preferable to read the Interrupt ID register first and then the Interrupt register.

Bit	Type	Function	Default
31:30		Unused	X
29:24	R	UND_FIFO[5:0]	X
23:22		Unused	X
21:16	R	EOP_FIFO[5:0]	X
15:14		Unused	X
13:8	R	SOP_FIFO[5:0]	X
7:6		Unused	X
5:0	R	OFL_FIFO[5:0]	X

OFL_FIFO[5:0]

Whenever OFLI becomes logic 1, these bits are loaded with the FIFO that overflowed. Once OFLI becomes logic 1, this value will not change until OFLI is cleared, and then becomes logic 1 again.

SOP_FIFO[5:0]

Whenever SOPI becomes logic 1, these bits are loaded with the FIFO that received two consecutive SOPs without an intervening EOP. Once SOPI becomes logic 1, this value will not change until SOPI is cleared, and then becomes logic 1 again.

EOP_FIFO[5:0]

Whenever EOPI becomes logic 1, these bits are loaded with the FIFO that received two consecutive EOPs without an intervening SOP. Once EOPI becomes logic 1, this value will not change until EOPI is cleared, and then becomes logic 1 again.

UND_FIFO[5:0]

Whenever UNDI becomes logic 1, these bits are loaded with the FIFO that underflowed. Once UNDI becomes logic 1, this value will not change until UNDI is cleared, and then becomes logic 1 again.

Register 0x2C4: Bypass SDQ Indirect Address

Writing to this register initiates a read or write access (based on RWB) to a set of indirect registers that set up the FIFOs for each PHY: Bypass SDQ Indirect Configuration, Bypass SDQ Buffer and Data Available Threshold and Bypass SDQ Indirect Cell Count. FIFOs must be configured according to a set of rules defined in Section 13.1. In order to change the current setup of a FIFO, it is recommended that the user read the existing setup information first, makes any modifications as required, and write back the new configuration .

Bit	Type	Function	Default
31:16		Unused	X
15	R	BUSY	0
14	R/W	RWB	1
13	R/W	FLUSH	1
12	R	EMPTY	1
11:6		Unused	X
5:0	R/W	PHYID[5:0]	0

PHYID[5:0]

This is a 6-bit number that is used to describe the current FIFO being addressed by the Bypass SDQ FIFO Indirect Configuration and the Bypass SDQ Cells and Packets Count Register. The range of FIFO numbers that can be used is 0 to 47.

EMPTY

This read-only bit indicates if the requested FIFO is empty or not. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in the FIFO Indirect Address register has no data available to be read out. This bit reflects the read-side perspective and will not react immediately to writes. Before reconfiguring a disabled FIFO, this bit needs to be sampled at 1, indicating that the FIFO is currently empty. A non-empty FIFO can be forced empty by writing FLUSH to logic 1.

FLUSH

FLUSH is an indirect configuration register bit. When RWB = 0, the value written to this bit will be written to the FLUSH bit for the specified PHYID. A logic 1 on FLUSH causes the SDQ to discard all the current data in the specified FIFO; a logic 0 must be written to the FIFO in order for it to begin processing data again. FLUSH is typically used when a non-empty FIFO needs to be reconfigured.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] will become available in the EMPTY bit and the Bypass SDQ Indirect Configuration register. When this bit is set to 0, the user is writing the configuration of a FIFO. The SDQ latches in the data in the Bypass SDQ Indirect Configuration and the FLUSH bit into the configuration for the specified FIFO.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the access is complete, the information for the FIFO is now available in the EMPTY bit and the Bypass SDQ Indirect Configuration Register, and another access can be initiated.

Register 0x2C5: Bypass SDQ Indirect Configuration

Bit	Type	Function	Default
31:16		Unused	X
15	R/W	FIFO_ENBL	0
14	R/W	FIFO_TYPE	0
13:7	R/W	FIFO_SIZE[6:0]	0000001
6:0	R/W	FIFO_PTR[6:0]	0000000

FIFO_PTR[6:0]

This 7-bit pointer specifies where a FIFO starts in the 3072-word SRAM space. It is specified in blocks, where a block is defined as 32 words (128 bytes). The range of this pointer should be 0 to 95; any other values will cause unpredictable effects. This pointer is calculated and programmed based on the number of FIFOs required by the system and the size of each FIFO. The rules governing this calculation are stated in section 13.1.

FIFO_SIZE[6:0]

This 7-bit number denotes the size of a FIFO in blocks. The size of a FIFO is related to the bandwidth. Table 43 below shows the suggested FIFO size based on the PHY bandwidth. Since there are altogether 96 blocks in the SRAM, the legal range for this number is 2 to 96; settings outside this range are reserved and may cause unpredictable effects.

Table 43 Suggested FIFO Size Encoding

FIFO size (blocks)	FIFO size (bytes)	Bandwidth
1	128	Not Supported
2	256	STS-1 or less
6	768	STS-3
24	3072	STS-12 or STS-48
96	12288	STS-48

Note that packets occupy a number of bytes equal to their packet length rounded up to the next multiple of 4 bytes. A FIFO size of 1 block is not supported.

FIFO_TYPE

This bit must be set to logic 1 for all FIFOs in the Bypass SDQ to indicate that packets are being handled.

FIFO_ENBL

This bit enables individual FIFOs. Writing a ‘0’ to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but data can be read from it until it is drained completely. In order to reconfigure a FIFO during operation, it should be disabled and drained; a FIFO can be drained immediately through the use of the FLUSH bit. By default, all the FIFOs are disabled. Only Packet PHYs should be enabled in the Bypass SDQ.

It is recommended that all FIFOs that are disabled also have the FLUSH bit set to logic 1. This will tend to eliminate spurious interrupts.

Register 0x2C6: Bypass SDQ Cells and Packets Count

This register is used to read the count of the number of packets on the FIFO specified in the Bypass SDQ Address register. The count reflects the write-side perspective, and will not react immediately to reads. The counts are latched when the S/UNI-ATLAS-3200 Identity / Load Counts Register is written to, or when any of the Bypass SDQ Count registers are written to. While the transfer is in progress, the TIP bit is asserted in the Bypass SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. Once TIP goes low, the count for the PHY specified in the Bypass SDQ Address register will be placed in this register.

The recommended sequence for using this register is:

1. Program the desired PHYID in the Bypass SDQ Address Register. Typically this would be done while setting RWB = 1.

2. Execute a write to this register

3. Poll TIP in the Bypass SDQ Control Register until it becomes 0.

4. Read the value in this register.

Bit	Type	Function	Default
31:12		Unused	X
11:0	R	COUNT[11:0]	0

COUNT[11:0]

This read-only field holds the last sampled count for the FIFO requested by PHYID[5:0] in the FIFO indirect address register, at the time the transfer was initiated. Since each FIFO can hold up to 3072 POS packets or 192 ATM cells, this count does not saturate or roll over.

Register 0x2C7: Bypass SDQ Cells Accepted Aggregate Count

Bit	Type	Function	Default
31:0	R	ACOUNT[31:0]	0

This read-only field contains the aggregate count of all the packets accepted by the Bypass SDQ. This register is latched when a write is performed to the S/UNI-ATLAS-3200 Identity / Load Counts Register or any of the Bypass SDQ counter registers. After the count is latched into the register, the internal counter is reset to 0 and starts counting again.

During the latching of this and other counters, the TIP bit is asserted in the Bypass SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. The update does not cause the counter to lose any events – the events after the latching are included in the subsequent count value.

ACOUNT[31:0]

ACOUNT is a 32-bit aggregate counter which records the number of cells or packets accepted by the Bypass SDQ since last read. It saturates at the maximum value.

Register 0x2C8: Bypass SDQ Cells Dropped Aggregate Count

Bit	Type	Function	Default
31:16		Unused	X
15:0	R	DCOUNT[15:0]	0

This read-only field contains the aggregate count of all the packets dropped by the Bypass SDQ due to overflow or transfer errors. This register is latched when a write is performed to the S/UNI-ATLAS-3200 Identity / Load Counts Register or to any of the Bypass SDQ counter registers. After the count is latched into the register, the internal counter is reset to 0 and starts counting again.

During the latching of this and other counters, the TIP bit is asserted in the Bypass SDQ Control Register and S/UNI-ATLAS-3200 Identity / Load Counts Register, and remains high for the interval of the update. TIP goes low once the counts are valid. The update does not cause the counter to lose any events – the events after the latching are included in the subsequent count value.

DCOUNT[15:0]

ACOUNT is a 16-bit aggregate counter which records the number of cells or packets dropped by the Bypass SDQ since last read. It saturates at the maximum value.

12 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-ATLAS-3200. Test mode registers (as opposed to normal mode registers) are selected when TRS (UP_ADDR[11]) is high.

Test mode registers may also be used for board testing. When all of the blocks within the S/UNI-ATLAS-3200 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-ATLAS-3200 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced with the exception of the POUT[7:0] bus via the JTAG test port.

Table 44 Test Mode Register Memory Map

Address	Register
0x000-0x7FF	Normal Mode Registers
0x800	Master Test
0x900	CP Test Register 0
0x901	CP Test Register 1
0x902	CP Test Register 2
…	
0xA00-0xFFF	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x800: Master Test

Bit	Type	Function	Default
7		Unused	X
6		Unused	X
5		Unused	X
4	W	PMCTST	X
3	W	DBCTRL	X
2	R/W	Reserved	0
1	W	HIZDATA	X
0	R/W	HIZIO	0

This register is used to enable S/UNI-ATLAS-3200 test features. All bits, except PMCTST and DS27_53, are reset to zero by a reset of the S/UNI-ATLAS-3200.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-ATLAS-3200 . While the HIZIO bit is a logic one, all output pins of the S/UNI-ATLAS-3200 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

Reserved

This bit must be programmed to logic 0.

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and PMCTST is logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-ATLAS-3200 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the S/UNI-ATLAS-3200 for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-ATLAS-3200 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

12.1 Test Mode 0 Details

In test mode 0, the S/UNI-ATLAS-3200 allows the logic levels on the device inputs to be read through the microprocessor interface and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the Master Configuration and Reset register is set to 02H, and the PMCTST bit in the Master Test register is set to logic one. The following addresses must be written with 00H as well: 821H, 831H, 839H, 841H, 849H, 851H, 901H, A01H, A21H, A41H, A61H, A81H, AA1H, AC1H. In addition, the following addresses must be written with 10H: 040H, 048H, 050H. Clock edges must be provided on inputs SYSCLK, XCLK, BI_CLK, BO_CLK, ICLK, and OCLK when these clocks are not being tested.

Reading the following address locations returns the values being driven on the indicated device inputs:

Table 45 Test Mode 0 Read Map

Addr	Bits[x:y] (31:24)	Bits[x:y] (23:16)	Bits[x:y] (15:8)	Bits[x:y] (7:0)
830H			bi_dat[15:8] (15:8)	bi_dat[7:0] (7:0)
832H				bi_soc (0), bi_par (1), bi_rclav_twrenb (4)
840H				bo_rdenb (2)
90FH				spar[7:0] (7:0)
910H	sdat[31:24] (31:24)	sdat[23:16] (23:16)	sdat[15:8] (15:8)	sdat[7:0] (7:0)
911H	sdat[63:56] (31:24)	sdat[55:48] (23:16)	sdat[47:40] (15:8)	sdat[39:32] (7:0)
A03H			icif_err (8), icif_eop(9), icif_mod[1:0] (11:10), icif_sx (12), icif_soc_sop (13), icif_ctrl (15)	icif_par (7)
A04H			icif_dat[15:8] (15:8)	icif_dat[7:0] (7:0)
A05H			icif_dat[31:24] (15:8)	icif_dat[23:16] (7:0)
A24H			icif_err (8), icif_eop (9), icif_mod[1:0] (11:10), icif_sx (12), icif_soc_sop (13),	icif_ctrl (0), icif_addr[5:0] (6:1), icif_par (7)
A25H			icif_dat[15:8] (15:8)	icif_dat[7:0] (7:0)
A26H			icif_dat[31:24] (15:8)	icif_dat[23:16] (7:0)
A64H				ocif_enb_stpa (0), ocif_addr[5:0] (6:1)
A83H				ocif_enb_stpa (1), ocif_clav_ptpa (2)

Note: [x:y] are chip pin designations while (a:b) are the corresponding register bits.

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations). Some bit may be written from two different locations, and these are designated with a "*". When writing to these locations make sure that the mirror location is written to logic 0:

Table 46 Test Mode 0 Write Map

Addr	Bits[x:y] (31:24)	Bits[x:y] (23:16)	Bits[x:y] (15:8)	Bits[x:y] (7:0)
822H				up_dmareq (0)
832H				bi_rrdenb_tclav (6)
838H		bo_par (16), bo_soc (17), bo_clav (18)	bo_dat[15:8] (15:8)	bo_dat[7:0] (7:0)
A07H				icif_addr[5:0] (5:0)
A27H			icif_clav_ptpa (11)	
A84H				ocif_addr[5:0] (5:0)
A64H			ocif_dat[15:8] (15:8) *	ocif_dat[7:0] (7:0) *
A85H			ocif_dat[15:8] (15:8) *	ocif_dat[7:0] (7:0) *
A65H			ocif_dat[31:24] (15:7) *	ocif_dat[23:16] (7:0) *
A86H			ocif_dat[31:24] (15:7) *	ocif_dat[23:16] (7:0) *
A66H				ocif_par (0) *, ocif_err (1) *, ocif_eop (2) *, ocif_mod[1:0] (4:3) *, ocif_sx (5) *
A67H				ocif_soc_sop (1) *
A83H			ocif_eop (8) *, ocif_err (9) *, ocif_par (10) *, ocif_soc_sop (11) *, ocif_sx (12) *	ocif_mod[1:0] (5:4) *,

Notes

1. [x:y] are chip pin designations while (a:b) are the corresponding register bits
2. * indicates signals that may be written from two different locations. Be careful to have the mirror location written to logic 0.

The following outputs can not be controlled with register writes: sdat[63:0], spar[7:0], icif_enb_stpa, ocif_ctrl.

12.2 JTAG Test Port

The S/UNI-ATLAS-3200 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 47 Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 48 Identification Register

Length	32 bits
Version number	0H
Part Number	7325H
Manufacturer's identification code	0CDH
Device identification	073250CDH

Table 49 Boundary Scan Register

Length - 514 bits

The boundary scan register has an enable register bit for every output and bidirectional register bit. However, in order to integrate the boundary scan chain with the chip core and pad ring it was necessary to select a small number of the boundary scan enables to control all the output and bidirectional pads. For example, the sdat bus is 64 bits wide and therefore has 64 boundary scan enables associated with it. Of these 64 enables only one enable is used, the boundary scan enable associated with the 31st bit of the bus. Consequently, a good portion of the scan chain register bits are unused (marked by a -).

The boundary scan chain numbering begins at 0 with the first bit shifted out on TDO and ends at 513 with the last bit shifted out on TDO.

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
bi_dat[15]		0	IN_CELL	saddr[11]	oeb_ocif_eop	257	OUT_CELL
bi_dat[14]		1	IN_CELL	-		258	
bi_dat[13]		2	IN_CELL	saddr[12]	oeb_ocif_eop	259	OUT_CELL
bi_dat[12]		3	IN_CELL	-		260	
bi_dat[11]		4	IN_CELL	saddr[13]	oeb_ocif_eop	261	OUT_CELL
bi_dat[10]		5	IN_CELL	-		262	
bi_dat[9]		6	IN_CELL	saddr[14]	oeb_ocif_eop	263	OUT_CELL

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
bi_dat[8]		7	IN_CELL	-		264	
bi_dat[7]		8	IN_CELL	saddr[15]	oeb_ocif_eop	265	OUT_CELL
bi_dat[6]		9	IN_CELL	-		266	
bi_dat[5]		10	IN_CELL	saddr[16]	oeb_ocif_eop	267	OUT_CELL
bi_dat[4]		11	IN_CELL	-		268	
bi_dat[3]		12	IN_CELL	saddr[17]	oeb_ocif_eop	269	OUT_CELL
bi_dat[2]		13	IN_CELL	-		270	
bi_dat[1]		14	IN_CELL	srwb	oeb_ocif_eop	271	OUT_CELL
bi_dat[0]		15	IN_CELL	-		272	
bi_par		16	IN_CELL	sceb	oeb_ocif_eop	273	OUT_CELL
bi_soc		17	IN_CELL	-		274	
bi_rrdenb_tclav	oeb_ocif_eop	18	OUT_CELL	spar[0]	oeb_sdat	275	IO_CELL
-		19		-		276	
bi_rclav_twrenb		20	IN_CELL	spar[1]	oeb_sdat	277	IO_CELL
bo_rdenb		21	IN_CELL	-		278	
bo_clav	oeb_ocif_eop	22	OUT_CELL	spar[2]	oeb_sdat	279	IO_CELL
-		23		-		280	
bo_soc	oeb_ocif_eop	24	OUT_CELL	spar[3]	oeb_sdat	281	IO_CELL
-		25		-		282	
bo_par	oeb_ocif_eop	26	OUT_CELL	spar[4]	oeb_sdat	283	IO_CELL
-		27		-		284	
bo_dat[0]	oeb_ocif_eop	28	OUT_CELL	spar[5]	oeb_sdat	285	IO_CELL
-		29		-		286	
bo_dat[1]	oeb_ocif_eop	30	OUT_CELL	spar[6]	oeb_sdat	287	IO_CELL
-		31		-		288	
bo_dat[2]	oeb_ocif_eop	32	OUT_CELL	spar[7]	oeb_sdat	289	IO_CELL
-		33		-		290	
bo_dat[3]	oeb_ocif_eop	34	OUT_CELL	sdat[0]	oeb_sdat	291	IO_CELL
-		35		-		292	
bo_dat[4]	oeb_ocif_eop	36	OUT_CELL	sdat[1]	oeb_sdat	293	IO_CELL
-		37		-		294	
bo_dat[5]	oeb_ocif_eop	38	OUT_CELL	sdat[2]	oeb_sdat	295	IO_CELL
-		39		-		296	
bo_dat[6]	oeb_ocif_eop	40	OUT_CELL	sdat[3]	oeb_sdat	297	IO_CELL
-		41		-		298	
bo_dat[7]	oeb_ocif_eop	42	OUT_CELL	sdat[4]	oeb_sdat	299	IO_CELL
-		43		-		300	

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
bo_dat[8]	oeb_ocif_eop	44	OUT_CELL	sdat[5]	oeb_sdat	301	IO_CELL
-		45		-		302	
bo_dat[9]	oeb_ocif_eop	46	OUT_CELL	sdat[6]	oeb_sdat	303	IO_CELL
-		47		-		304	
bo_dat[10]	oeb_ocif_eop	48	OUT_CELL	sdat[7]	oeb_sdat	305	IO_CELL
-		49		-		306	
bo_dat[11]	oeb_ocif_eop	50	OUT_CELL	sdat[8]	oeb_sdat	307	IO_CELL
-		51		-		308	
bo_dat[12]	oeb_ocif_eop	52	OUT_CELL	sdat[9]	oeb_sdat	309	IO_CELL
-		53		-		310	
bo_dat[13]	oeb_ocif_eop	54	OUT_CELL	sdat[10]	oeb_sdat	311	IO_CELL
-		55		-		312	
bo_dat[14]	oeb_ocif_eop	56	OUT_CELL	sdat[11]	oeb_sdat	313	IO_CELL
-		57		-		314	
bo_dat[15]	oeb_ocif_eop	58	OUT_CELL	sdat[12]	oeb_sdat	315	IO_CELL
-		59		-		316	
intb	oeb_intb	60	OUT_CELL	sdat[13]	oeb_sdat	317	IO_CELL
oeb_intb		61	ENABLE	-		318	
up_rstb		62	IN_CELL	sdat[14]	oeb_sdat	319	IO_CELL
up_wrb		63	IN_CELL	-		320	
up_rdb		64	IN_CELL	sdat[15]	oeb_sdat	321	IO_CELL
up_ale		65	IN_CELL	-		322	
up_csb		66	IN_CELL	sdat[16]	oeb_sdat	323	IO_CELL
up_dmareq	oeb_ocif_eop	67	OUT_CELL	-		324	
-		68		sdat[17]	oeb_sdat	325	IO_CELL
up_busyb	oeb_ocif_eop	69	OUT_CELL	-		326	
-		70		sdat[18]	oeb_sdat	327	IO_CELL
up_addr[0]		71	IN_CELL	-		328	
up_addr[1]		72	IN_CELL	sdat[19]	oeb_sdat	329	IO_CELL
up_addr[2]		73	IN_CELL	-		330	
up_addr[3]		74	IN_CELL	sdat[20]	oeb_sdat	331	IO_CELL
up_addr[4]		75	IN_CELL	-		332	
up_addr[5]		76	IN_CELL	sdat[21]	oeb_sdat	333	IO_CELL
up_addr[6]		77	IN_CELL	-		334	
up_addr[7]		78	IN_CELL	sdat[22]	oeb_sdat	335	IO_CELL
up_addr[8]		79	IN_CELL	-		336	
up_addr[9]		80	IN_CELL	sdat[23]	oeb_sdat	337	IO_CELL
up_addr[10]		81	IN_CELL	-		338	

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
up_addr[11]		82	IN_CELL	sdat[24]	oeb_sdat	339	IO_CELL
up_dat[0]	oeb_up_dat	83	IO_CELL	-		340	
-		84		sdat[25]	oeb_sdat	341	IO_CELL
up_dat[1]	oeb_up_dat	85	IO_CELL	-		342	
-		86		sdat[26]	oeb_sdat	343	IO_CELL
up_dat[2]	oeb_up_dat	87	IO_CELL	-		344	
-		88		sdat[27]	oeb_sdat	345	IO_CELL
up_dat[3]	oeb_up_dat	89	IO_CELL	-		346	
-		90		sdat[28]	oeb_sdat	347	IO_CELL
up_dat[4]	oeb_up_dat	91	IO_CELL	-		348	
-		92		sdat[29]	oeb_sdat	349	IO_CELL
up_dat[5]	oeb_up_dat	93	IO_CELL	-		350	
-		94		sdat[30]	oeb_sdat	351	IO_CELL
up_dat[6]	oeb_up_dat	95	IO_CELL	-		352	
-		96		sdat[31]		353	IO_CELL
up_dat[7]	oeb_up_dat	97	IO_CELL	oeb_sdat		354	ENABLE
-		98		sdat[32]	oeb_sdat	355	IO_CELL
up_dat[8]	oeb_up_dat	99	IO_CELL	-		356	
-		100		sdat[33]	oeb_sdat	357	IO_CELL
up_dat[9]	oeb_up_dat	101	IO_CELL	-		358	
-		102		sdat[34]	oeb_sdat	359	IO_CELL
up_dat[10]	oeb_up_dat	103	IO_CELL	-		360	
-		104		sdat[35]	oeb_sdat	361	IO_CELL
up_dat[11]	oeb_up_dat	105	IO_CELL	-		362	
-		106		sdat[36]	oeb_sdat	363	IO_CELL
up_dat[12]	oeb_up_dat	107	IO_CELL	-		364	
-		108		sdat[37]	oeb_sdat	365	IO_CELL
up_dat[13]	oeb_up_dat	109	IO_CELL	-		366	
-		110		sdat[38]	oeb_sdat	367	IO_CELL
up_dat[14]	oeb_up_dat	111	IO_CELL	-		368	
-		112		sdat[39]	oeb_sdat	369	IO_CELL
up_dat[15]		113	IO_CELL	-		370	
oeb_up_dat		114	ENABLE	sdat[40]	oeb_sdat	371	IO_CELL
up_dat[16]	oeb_up_dat	115	IO_CELL	-		372	
-		116		sdat[41]	oeb_sdat	373	IO_CELL
up_dat[17]	oeb_up_dat	117	IO_CELL	-		374	
-		118		sdat[42]	oeb_sdat	375	IO_CELL
up_dat[18]	oeb_up_dat	119	IO_CELL	-		376	

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
-		120		sdat[43]	oeb_sdat	377	IO_CELL
up_dat[19]	oeb_up_dat	121	IO_CELL	-		378	
-		122		sdat[44]	oeb_sdat	379	IO_CELL
up_dat[20]	oeb_up_dat	123	IO_CELL	-		380	
-		124		sdat[45]	oeb_sdat	381	IO_CELL
up_dat[21]	oeb_up_dat	125	IO_CELL	-		382	
-		126		sdat[46]	oeb_sdat	383	IO_CELL
up_dat[22]	oeb_up_dat	127	IO_CELL	-		384	
-		128		sdat[47]	oeb_sdat	385	IO_CELL
up_dat[23]	oeb_up_dat	129	IO_CELL	-		386	
-		130		sdat[48]	oeb_sdat	387	IO_CELL
up_dat[24]	oeb_up_dat	131	IO_CELL	-		388	
-		132		sdat[49]	oeb_sdat	389	IO_CELL
up_dat[25]	oeb_up_dat	133	IO_CELL	-		390	
-		134		sdat[50]	oeb_sdat	391	IO_CELL
up_dat[26]	oeb_up_dat	135	IO_CELL	-		392	
-		136		sdat[51]	oeb_sdat	393	IO_CELL
up_dat[27]	oeb_up_dat	137	IO_CELL	-		394	
-		138		sdat[52]	oeb_sdat	395	IO_CELL
up_dat[28]	oeb_up_dat	139	IO_CELL	-		396	
-		140		sdat[53]	oeb_sdat	397	IO_CELL
up_dat[29]	oeb_up_dat	141	IO_CELL	-		398	
-		142		sdat[54]	oeb_sdat	399	IO_CELL
up_dat[30]	oeb_up_dat	143	IO_CELL	-		400	
-		144		sdat[55]	oeb_sdat	401	IO_CELL
up_dat[31]	oeb_up_dat	145	IO_CELL	-		402	
-		146		sdat[56]	oeb_sdat	403	IO_CELL
icif_dat[31]	oeb_icif_dat	147	IO_CELL	-		404	
-		148		sdat[57]	oeb_sdat	405	IO_CELL
icif_dat[30]	oeb_icif_dat	149	IO_CELL	-		406	
-		150		sdat[58]	oeb_sdat	407	IO_CELL
icif_dat[29]	oeb_icif_dat	151	IO_CELL	-		408	
-		152		sdat[59]	oeb_sdat	409	IO_CELL
icif_dat[28]	oeb_icif_dat	153	IO_CELL	-		410	
-		154		sdat[60]	oeb_sdat	411	IO_CELL
icif_dat[27]	oeb_icif_dat	155	IO_CELL	-		412	
-		156		sdat[61]	oeb_sdat	413	IO_CELL
icif_dat[26]	oeb_icif_dat	157	IO_CELL	-		414	

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
-		158		sdat[62]	oeb_sdat	415	IO_CELL
icif_dat[25]	oeb_icif_dat	159	IO_CELL	-		416	
-		160		sdat[63]	oeb_sdat	417	IO_CELL
icif_dat[24]	oeb_icif_dat	161	IO_CELL	-		418	
-		162		ocif_dat[31]	oeb_ocif_dat	419	IO_CELL
icif_dat[23]	oeb_icif_dat	163	IO_CELL	-		420	
-		164		ocif_dat[30]	oeb_ocif_dat	421	IO_CELL
icif_dat[22]	oeb_icif_dat	165	IO_CELL	-		422	
-		166		ocif_dat[29]	oeb_ocif_dat	423	IO_CELL
icif_dat[21]	oeb_icif_dat	167	IO_CELL	-		424	
-		168		ocif_dat[28]	oeb_ocif_dat	425	IO_CELL
icif_dat[20]	oeb_icif_dat	169	IO_CELL	-		426	
-		170		ocif_dat[27]	oeb_ocif_dat	427	IO_CELL
icif_dat[19]	oeb_icif_dat	171	IO_CELL	-		428	
-		172		ocif_dat[26]	oeb_ocif_dat	429	IO_CELL
icif_dat[18]	oeb_icif_dat	173	IO_CELL	-		430	
-		174		ocif_dat[25]	oeb_ocif_dat	431	IO_CELL
icif_dat[17]	oeb_icif_dat	175	IO_CELL	-		432	
-		176		ocif_dat[24]	oeb_ocif_dat	433	IO_CELL
icif_dat[16]	oeb_icif_dat	177	IO_CELL	-		434	
-		178		ocif_dat[23]	oeb_ocif_dat	435	IO_CELL
icif_dat[15]	oeb_icif_dat	179	IO_CELL	-		436	
-		180		ocif_dat[22]	oeb_ocif_dat	437	IO_CELL
icif_dat[14]	oeb_icif_dat	181	IO_CELL	-		438	
-		182		ocif_dat[21]	oeb_ocif_dat	439	IO_CELL
icif_dat[13]	oeb_icif_dat	183	IO_CELL	-		440	
-		184		ocif_dat[20]	oeb_ocif_dat	441	IO_CELL
icif_dat[12]	oeb_icif_dat	185	IO_CELL	-		442	
-		186		ocif_dat[19]	oeb_ocif_dat	443	IO_CELL
icif_dat[11]	oeb_icif_dat	187	IO_CELL	-		444	
-		188		ocif_dat[18]	oeb_ocif_dat	445	IO_CELL
icif_dat[10]	oeb_icif_dat	189	IO_CELL	-		446	
-		190		ocif_dat[17]	oeb_ocif_dat	447	IO_CELL
icif_dat[9]	oeb_icif_dat	191	IO_CELL	-		448	
-		192		ocif_dat[16]	oeb_ocif_dat	449	IO_CELL
icif_dat[8]	oeb_icif_dat	193	IO_CELL	-		450	
-		194		ocif_dat[15]	oeb_ocif_dat	451	IO_CELL
icif_dat[7]	oeb_icif_dat	195	IO_CELL	-		452	

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
-		196		ocif_dat[14]	oeb_ocif_dat	453	IO_CELL
icif_dat[6]	oeb_icif_dat	197	IO_CELL	-		454	
-		198		ocif_dat[13]	oeb_ocif_dat	455	IO_CELL
icif_dat[5]	oeb_icif_dat	199	IO_CELL	-		456	
-		200		ocif_dat[12]	oeb_ocif_dat	457	IO_CELL
icif_dat[4]	oeb_icif_dat	201	IO_CELL	-		458	
-		202		ocif_dat[11]	oeb_ocif_dat	459	IO_CELL
icif_dat[3]	oeb_icif_dat	203	IO_CELL	-		460	
-		204		ocif_dat[10]	oeb_ocif_dat	461	IO_CELL
icif_dat[2]	oeb_icif_dat	205	IO_CELL	-		462	
-		206		ocif_dat[9]	oeb_ocif_dat	463	IO_CELL
icif_dat[1]	oeb_icif_dat	207	IO_CELL	-		464	
-		208		ocif_dat[8]	oeb_ocif_dat	465	IO_CELL
icif_dat[0]		209	IO_CELL	-		466	
oeb_icif_dat		210	ENABLE	ocif_dat[7]	oeb_ocif_dat	467	IO_CELL
icif_par		211	IN_CELL	-		468	
icif_eop		212	IN_CELL	ocif_dat[6]	oeb_ocif_dat	469	IO_CELL
icif_soc_sop		213	IN_CELL	-		470	
icif_sx		214	IN_CELL	ocif_dat[5]	oeb_ocif_dat	471	IO_CELL
icif_err		215	IN_CELL	-		472	
icif_mod[1]		216	IN_CELL	ocif_dat[4]	oeb_ocif_dat	473	IO_CELL
icif_mod[0]		217	IN_CELL	-		474	
icif_ctrl		218	IN_CELL	ocif_dat[3]	oeb_ocif_dat	475	IO_CELL
icif_addr[5]	icif_addr_oeb	219	IO_CELL	-		476	
-		220		ocif_dat[2]	oeb_ocif_dat	477	IO_CELL
icif_addr[4]	icif_addr_oeb	221	IO_CELL	-		478	
-		222		ocif_dat[1]	oeb_ocif_dat	479	IO_CELL
icif_addr[3]	icif_addr_oeb	223	IO_CELL	-		480	
-		224		ocif_dat[0]		481	IO_CELL
icif_addr[2]	icif_addr_oeb	225	IO_CELL	oeb_ocif_dat		482	ENABLE
-		226		ocif_par	oeb_ocif_eop	483	OUT_CELL
icif_addr[1]	icif_addr_oeb	227	IO_CELL	-		484	
-		228		ocif_eop		485	OUT_CELL
icif_addr[0]		229	IO_CELL	oeb_ocif_eop		486	ENABLE
icif_addr_oeb		230	ENABLE	ocif_soc_sop	oeb_ocif_eop	487	OUT_CELL
icif_clav_ptpa	oeb_ocif_eop	231	OUT_CELL	-		488	
-		232		ocif_sx	oeb_ocif_eop	489	OUT_CELL
icif_enb_stpa	oeb_ocif_eop	233	OUT_CELL	-		490	

Pin	Enable	Register Bit	Cell Type	Pin	Enable	Register Bit	Cell Type
-		234		ocif_err	oeb_ocif_eop	491	OUT_CELL
saddr[0]	oeb_ocif_eop	235	OUT_CELL	-		492	
-		236		ocif_mod[1]	oeb_ocif_eop	493	OUT_CELL
saddr[1]	oeb_ocif_eop	237	OUT_CELL	-		494	
-		238		ocif_mod[0]	oeb_ocif_eop	495	OUT_CELL
saddr[2]	oeb_ocif_eop	239	OUT_CELL	-		496	
-		240		ocif_clav_ptpa		497	IN_CELL
saddr[3]	oeb_ocif_eop	241	OUT_CELL	ocif_enb_stpa		498	IN_CELL
-		242		ocif_addr[5]	oeb_ocif_addr	499	IO_CELL
saddr[4]	oeb_ocif_eop	243	OUT_CELL	-		500	
-		244		ocif_addr[4]	oeb_ocif_addr	501	IO_CELL
saddr[5]	oeb_ocif_eop	245	OUT_CELL	-		502	
-		246		ocif_addr[3]	oeb_ocif_addr	503	IO_CELL
saddr[6]	oeb_ocif_eop	247	OUT_CELL	-		504	
-		248		ocif_addr[2]	oeb_ocif_addr	505	IO_CELL
saddr[7]	oeb_ocif_eop	249	OUT_CELL	-		506	
-		250		ocif_addr[1]	oeb_ocif_addr	507	IO_CELL
saddr[8]	oeb_ocif_eop	251	OUT_CELL	-		508	
-		252		ocif_addr[0]		509	IO_CELL
saddr[9]	oeb_ocif_eop	253	OUT_CELL	oeb_ocif_addr		510	ENABLE
-		254		ocif_ctrl	oeb_ocif_eop	511	OUT_CELL
saddr[10]	oeb_ocif_eop	255	OUT_CELL	-		512	
-		256		halfsecclk		513	IN_CELL

Notes:

1. OENB is the active low output enable for D[7:0].
2. RDATENB is the active low output enable for RSOC, RDAT[15:0], and RXPRTY[1:0].
3. When set high, INTB will be set to high impedance.
4. HIZ is the active low output enable for all OUT_CELL types except D[7:0], RXPRTY[1:0], RDAT[15:0], and INTB
5. A[7] is the first bit of the boundary scan chain.

Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 21 Input Observation Cell (IN_CELL)

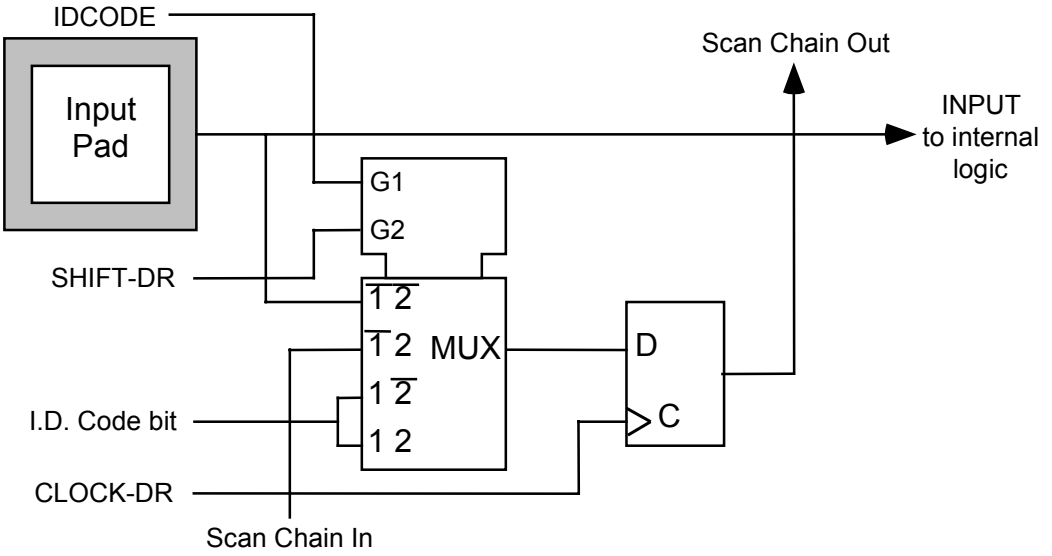


Figure 22 Output Cell (OUT_CELL)

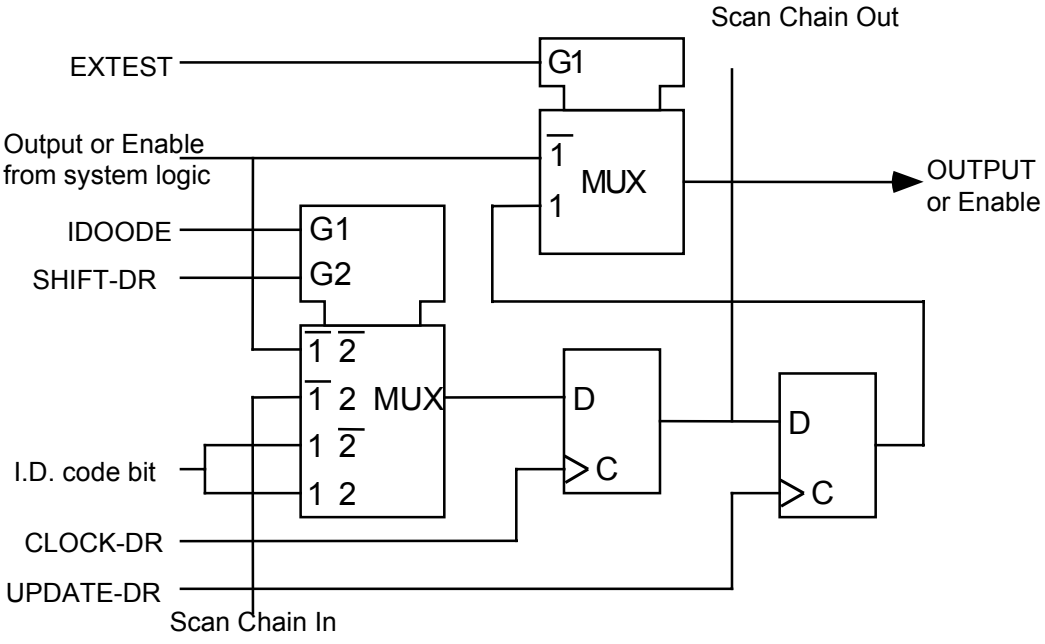


Figure 23 Bidirectional Cell (IO_CELL)

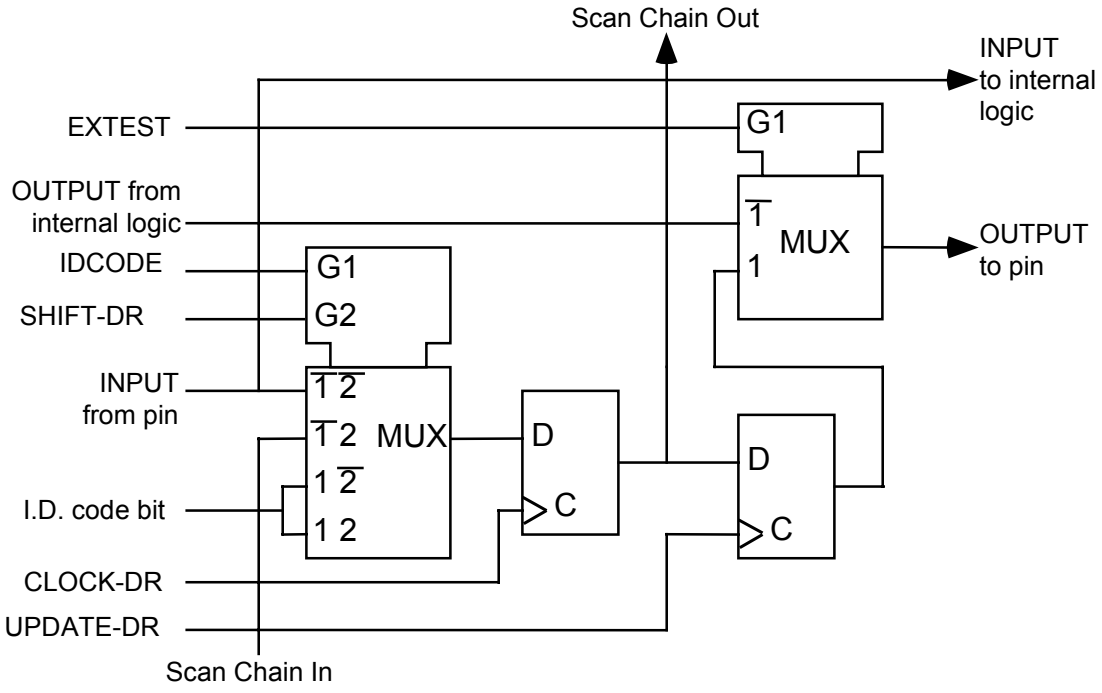
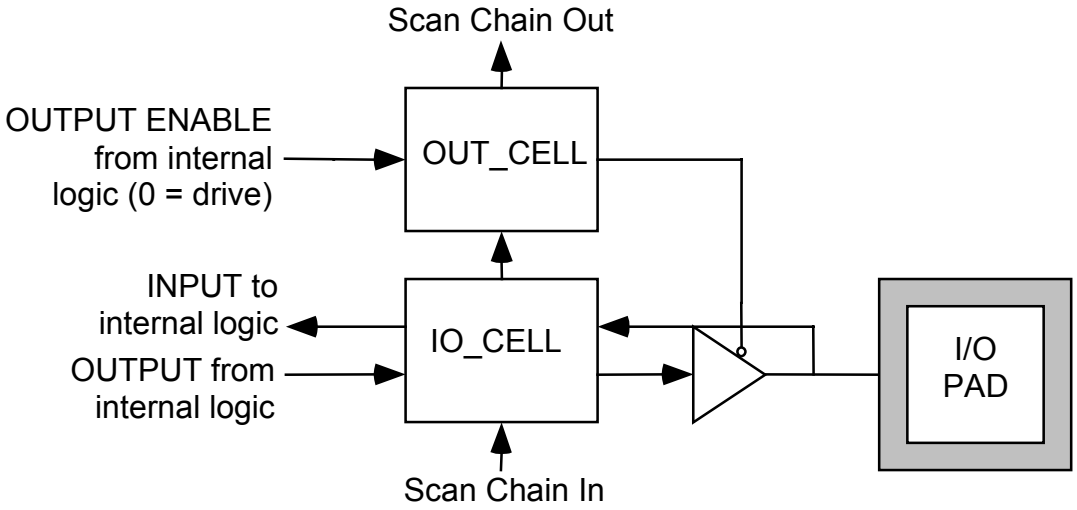


Figure 24 Layout of Output Enable and Bidirectional Cells



13 Operations

13.1 Configuring the Scalable Data Queue

The SDQ supports a number of FIFO sizes, from 128 bytes (equal to 2 ATM cells) to 12,288 bytes (equal to 192 ATM cells). The 12,288-byte total storage can be carved up into a maximum of 48 FIFOs.

In order to configure the SDQ-ATLAS, the user first determines the size of each FIFO in blocks (1 block = 128 bytes) based on the PHYs in the system, and adds them all up. The total number of blocks should be less than or equal to 96. The user then needs to program four things for a given PHY:

FIFO pointer – this is the starting block number, which is an integer from 0 to 95. Since there are 96 blocks in total, this is a 7-bit number, as specified in the FIFO indirect configuration register (FIFO_PTR[6:0] field). There is no restriction on where a PHY's FIFO may start, so long as no FIFOs overlap.

FIFO size – this is the size of a FIFO measured in blocks. Refer to the Suggested FIFO size encoding table below for the values used to specify the FIFO sizes, and a guide to sizing the FIFO based on the bandwidth of the associated PHY. It is up to the discretion of the user to apply this guide to each specific case. Room permitting, it is always acceptable to increase the amount of space for a FIFO. This number is specified in the FIFO indirect configuration register (FIFO_SIZE[6:0] field). Packets occupy a number of bytes equal to their length, rounded up to the next multiple of 4 bytes; ATM cells occupy 64 bytes apiece, regardless of prepends or postpends.

Table 50 Suggested FIFO Size Encoding

FIFO Size (blocks)	FIFO Size (cells)	FIFO Size (bytes)	Bandwidth
1	2	128	Below STS-1
2	4	256	STS-1 or less
6	12	768	STS-3
24	48	3072	STS-12 or STS-48
96	192	12288	STS-48

FIFO type – this is a single bit which sets the FIFO in either POS mode (1) or ATM mode (0). This bit must be set to logic 0 for all PHYs in the Input and Output SDQs, and to logic 1 for all PHYs in the Packet Bypass SDQ. This bit is specified in the FIFO indirect configuration register (FIFO_TYPE field).

FIFO enable – this is a single bit which enables the FIFO (1) or disables the FIFO (0). When the FIFO is disabled, it refuses to accept any data, but data can still be read from it. This bit is specified in the FIFO indirect configuration register (FIFO_ENBL field). Unused PHYs should be left disabled, and should have their FLUSH bit set. Only ATM PHYs should be enabled in the Input and Output SDQs, and only packet PHYs should be enabled in the Bypass SDQ. A FIFO should be disabled and emptied if it is to be reconfigured.

Starting from the FIFO pointer, a FIFO occupies the number of blocks specified by its FIFO size. The user should not configure the FIFO pointers such that two FIFOs overlap. The user can, however, have gaps between consecutive FIFOs. This is useful when the FIFO size needs to be adjusted dynamically.

The following table illustrates the configuration for a typical case. This example involves 3 PHYs that have a bandwidth of STS-12, and are allocated 24 blocks each. In addition, there are 1 STS-3 PHY with a FIFO size of 6 blocks, 6 STS-1 PHYs each with a FIFO size of 2 blocks, and 3 T1 PHYs each with a FIFO size of 1 block. The sum of all the blocks used in this example is 93, which is less than the total number of blocks available, 96.

Table 51 SDQ-ATLAS Configuration Example

PHYID	Bandwidth	FIFO pointer	FIFO size (blocks)	FIFO size (cells)
0	STS-12	0	24	48
1	STS-12	24	24	48
3	STS-3	48	6	12
4	STS-1	54	2	4
5	STS-1	56	2	4
2	STS-12	58	24	48
6	STS-1	82	2	4
7	STS-1	84	2	4
8	STS-1	86	2	4
9	STS-1	88	2	4
12	T1	90	1	2
10	T1	91	1	2
15	T1	92	1	2

Blocks 93 to 95 are not used in this example. Potentially, users can configure three more 1-block FIFOs, or one more 1-block FIFO and one more 2-block FIFO, or to enlarge PHY #15 to 4 blocks, and so on. Note that the FIFOs are not required to be adjacent to each other; gaps are allowed between FIFOs. For example, PHY #10 could start at block 93.

The SDQ cannot detect errors due to user misconfiguration. If the user sets up FIFOs that overlap each other, or start at an illegal FIFO position (e.g. a number greater than 95) or with an illegal FIFO size (i.e. 0, 97-127), the results will be unpredictable.

In terms of the actual programming sequence for a given FIFO, the recommended sequence is as follows:

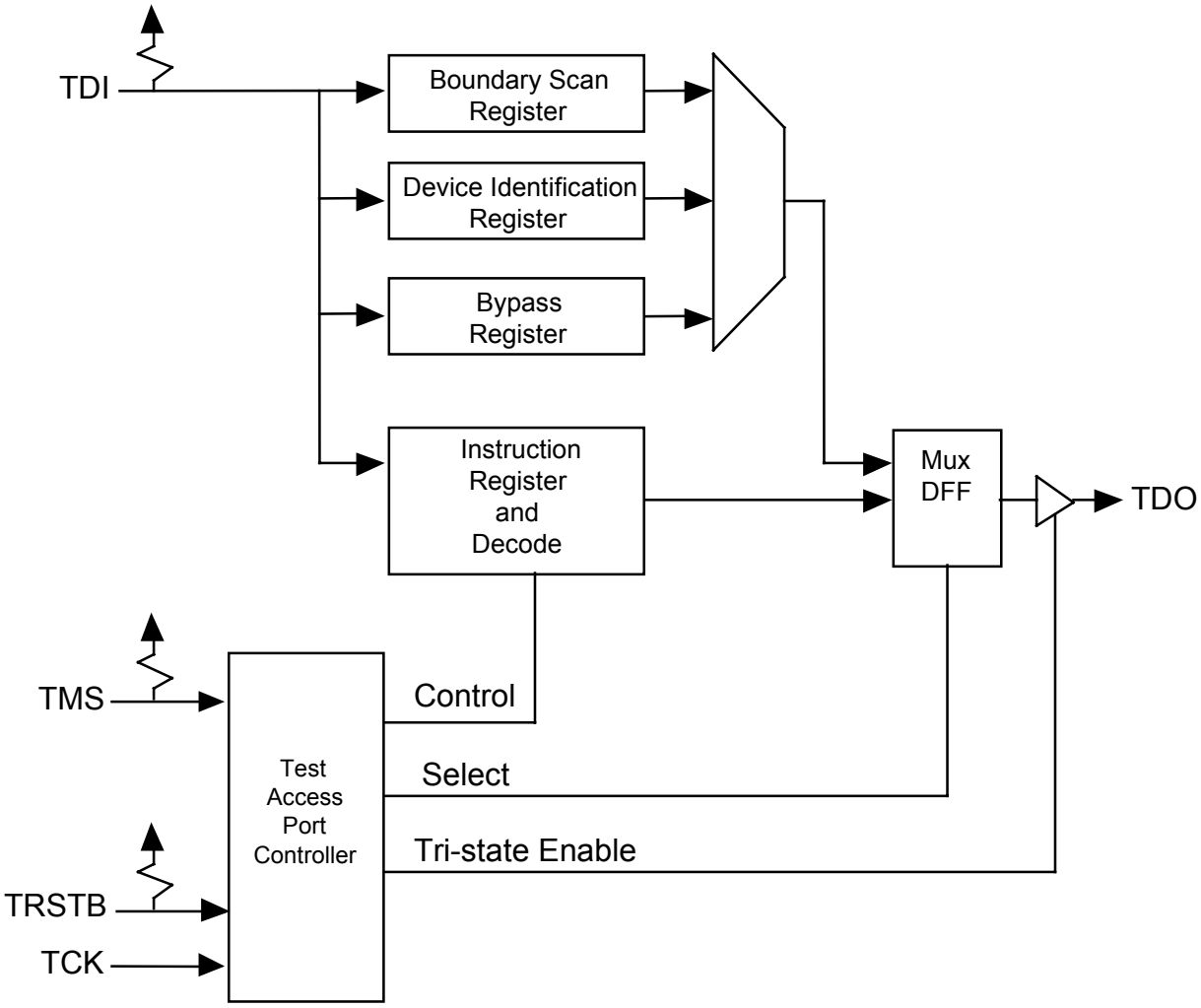
1. Read the Indirect Address register until BUSY = 0
2. Write the desired values into the Indirect Configuration register
3. Write to the Indirect Address register with RWB = 0, PHYID = desired PHY, and FLUSH = 1
4. Poll the Indirect Address register until BUSY = 0
5. Write to the Indirect Address register with RWB = 0, PHYID = desired PHY, and FLUSH = 0

When reconfiguring the SDQ while traffic is passing through, all FIFOs that are being affected by the reconfiguration should be disabled and flushed, and held that way until the reconfiguration is complete. FIFOs unaffected by the reconfiguration will continue to carry traffic normally.

13.2 JTAG Support

The S/UNI-ATLAS-3200 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown:

Figure 25 Boundary Scan Architecture



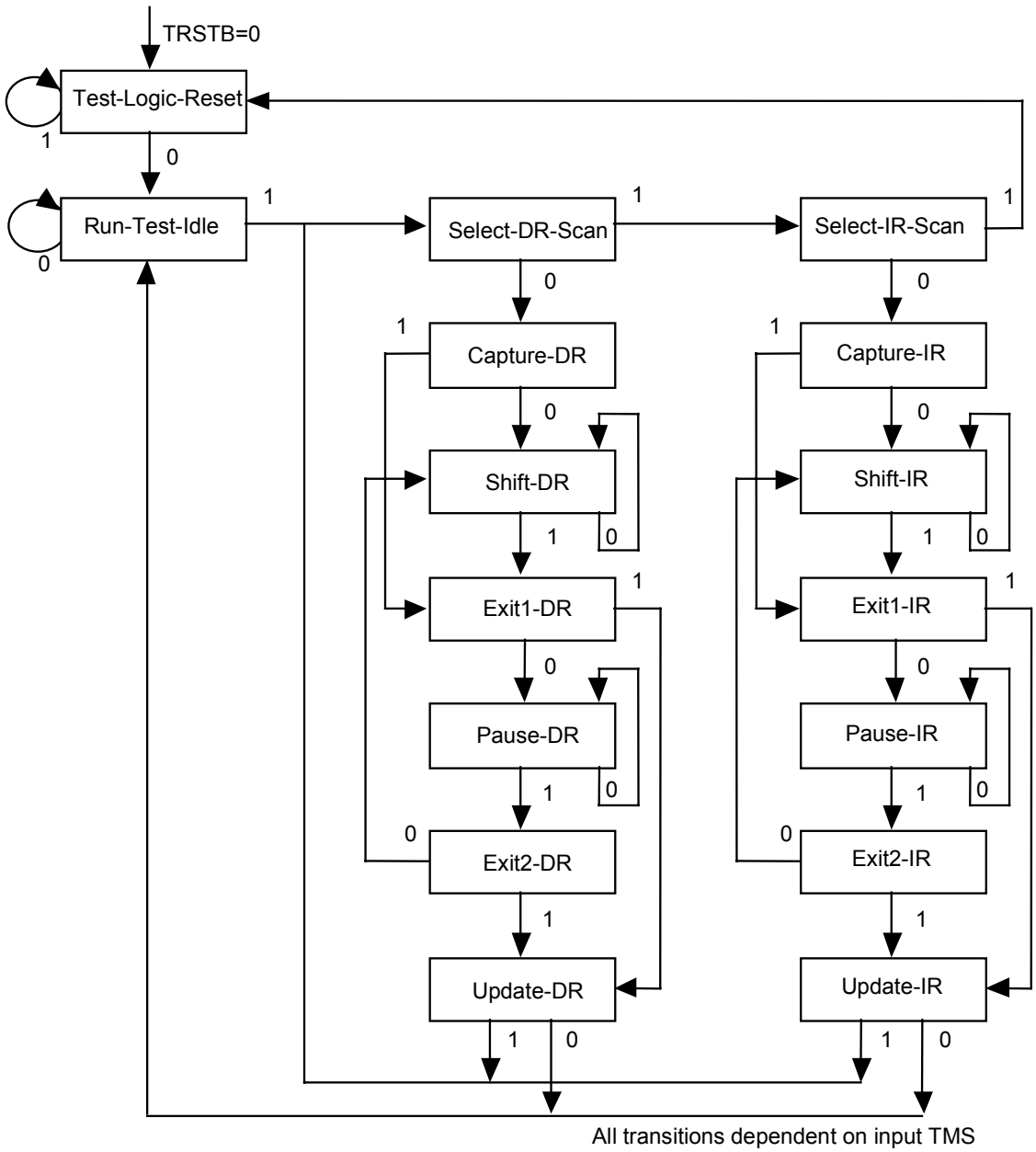
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.2.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described:

Figure 26 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.3 Board Design Recommendations

Recommendations for board design are contained in the S/UNI-ATLAS-3200 with MACH-48 Reference Design, PMC-2000718.

14 Functional Timing

14.1 POS-PHY Level 3

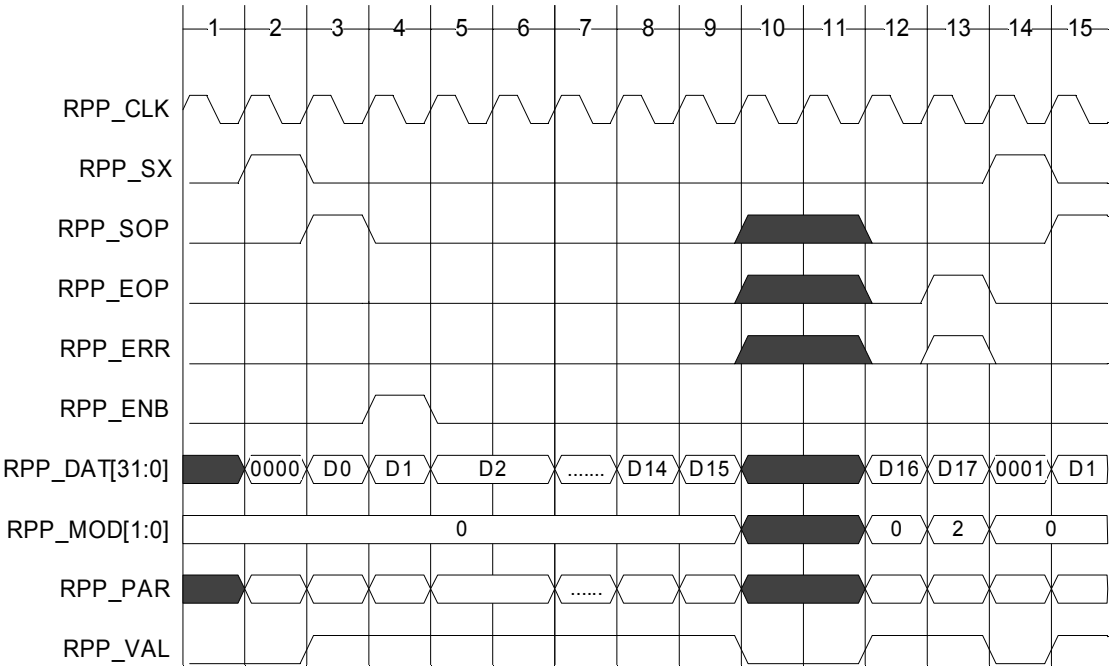
14.1.1 Ingress Packet Interface

When the S/UNI-ATLAS-3200 is required to carry a mix of cells and packets, a POS-PHY Level 3 interface is used. In the ingress direction, the S/UNI-ATLAS-3200 provides an Rx PHY interface on the system side, and an Rx Link interface on the PHY side. Selection of ingress vs. egress mode and POS vs UL3 signalling must be performed at startup.

Figure 27 illustrates the operation of the interface. The figure is valid for both the RxLink and RxPHY blocks (on input and output, respectively), with the 'x' in the signal names replaced with 'L' for the RxLink and 'P' for RxPHY.

The POS-PHY Receive Interface is controlled by the PHY Layer. It is presumed that the Link Layer device can accept data at full line rate, so backpressure is limited to a single RxP_ENB signal. At the beginning of a transfer, RxP_SX is asserted to indicate that the PHY address is on RxP_DAT. In the subsequent cycle, RxP_SOP is asserted to mark the first word of the packet. At any time, the PHY layer may pause the transfer by deasserting RxP_VAL. At the end of a packet, RxP_MOD becomes valid to indicate how many of the final 4 bytes (between 1 and 4) are valid. RxP_ERR may be asserted in this cycle to indicate that the packet is in error. PHY devices generally assert RERR to indicate that HDLC abort flags rather than normal HDLC flags were received at the end of a packet; S/UNI-ATLAS-3200 will assert RPP_RERR when transmitting packets if RLP_RERR was asserted when the packet was received or, configurably, if an interface error such as a parity error was detected.

Figure 27 POS-PHY Level 3 Ingress Logical Timing



On the RxLink interface, the S/UNI-ATLAS-3200 will deassert RLP_RDENB to pause a transaction if any of the per-PHY queues backs up. However, so long as S/UNI-ATLAS-3200 is properly provisioned, and RPP_RDENB is never asserted to S/UNI-ATLAS-3200 by the switch or TM, then this will not occur.

On the RxPHY interface, the S/UNI-ATLAS-3200 will not update its outputs when it samples RPP_ENB deasserted.

Transferring cells over this interface is just like transferring packets. The length of the cells is programmed into the RxPHY and RxLink blocks so that they can correctly generate and interpret the packet, but as far as the interface is concerned, ATM cells are simply 52, 56, 60, or 64-byte packets. There exists an option, using the ATM_FIELD and POS_FIELD bits in the RxPHY and RxLink blocks, to insert and check an identifier in the top 8 bits of RDAT during the RLP_SX cycle, which identifies ATM vs packet data. This feature is useful in detecting misconfigurations in the selection of packet vs. ATM PHYs.

RxLink POS-PHY Logical Timing

In the Ingress direction, the S/UNI-ATLAS-3200 input cell/packet interface acts as a Receive Link Layer device, and the upstream device acts as a PHY layer device, for the purposes of POS-PHY level 3 transfers.

Figure 28 RxLink POS-PHY Packet Transfer

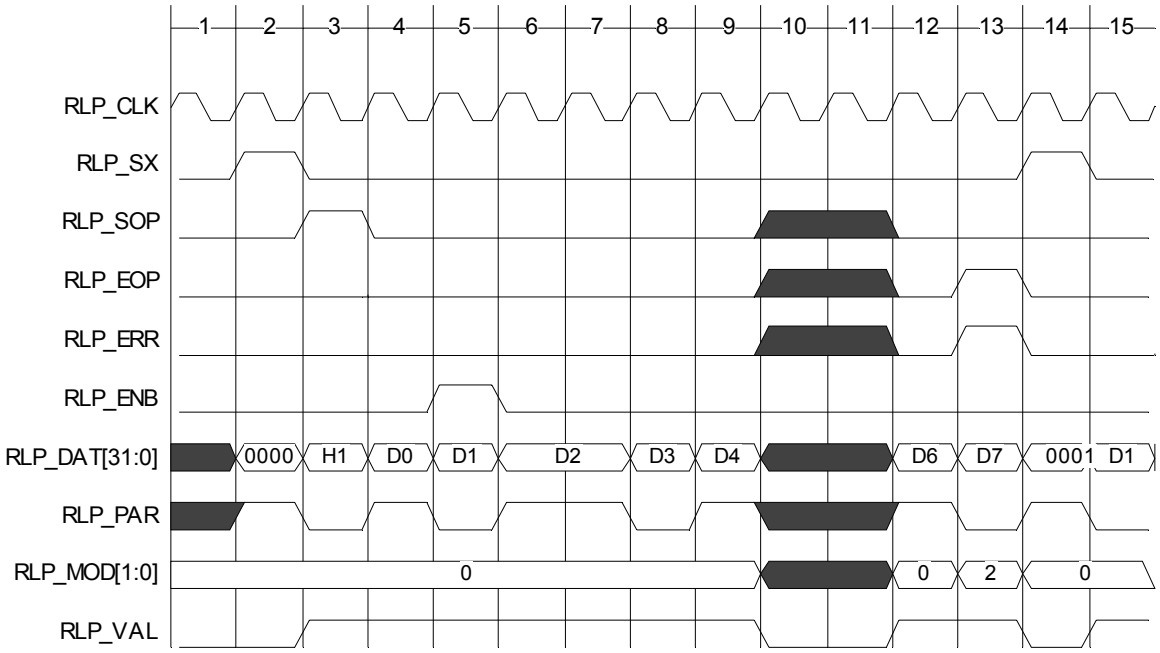


Figure 28 is an example of a multi-port PHY device with at least two channels. The PHY informs the S/UNI-ATLAS-3200 of the port address of the selected FIFO by asserting RLP_SX with the port address on the RLP_DAT bus in cycle 2. The Link Layer may pause the Receive Interface at any time by deasserting the RLP_ENB signal. The end of the packet is indicated with the RLP_EOP signal. The next transfer starts by asserting RLP_SX in cycle 14. If an error occurred during the reception of the packet, the RLP_ERR would be asserted with RLP_EOP.

Figure 29 RxLink back to back POS-PHY Packet Transfer

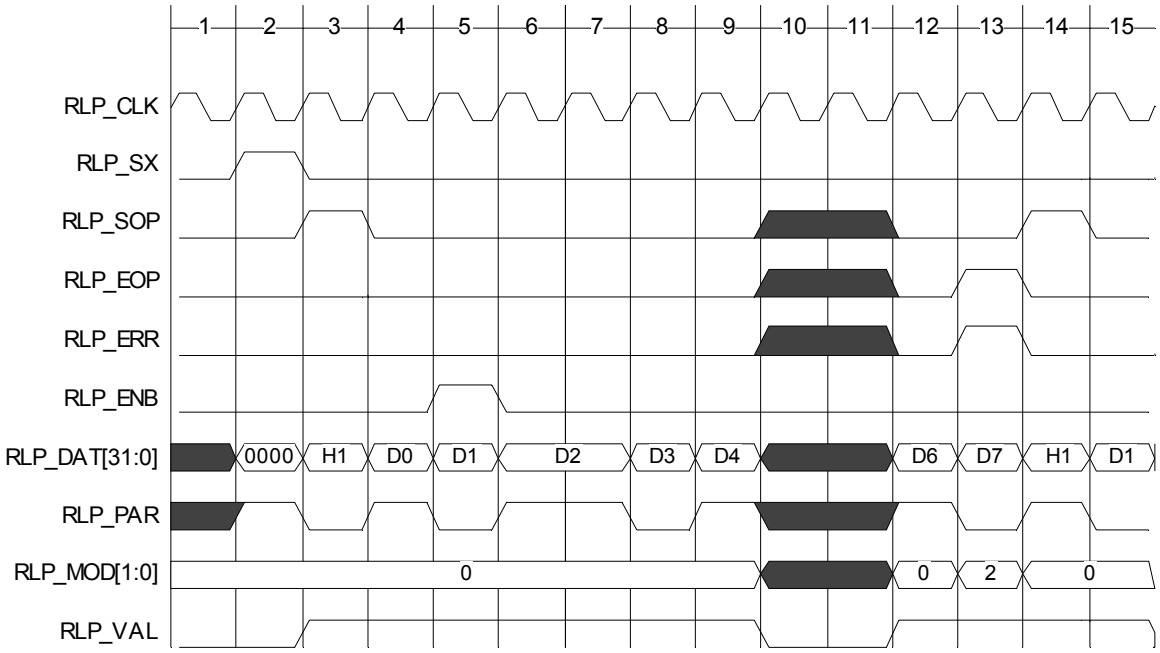


Figure 29 is an example of a multi-port PHY device performing a back to back packet transfer. The PHY informs the S/UNI-ATLAS-3200 of the port address of the selected FIFO by asserting RLP_SX with the port address on the RLP_DAT bus. The Link Layer may pause the Receive Interface at any time by deasserting the RLP_ENB signal. The end of the packet is indicated with the RLP_EOP signal. Thus, the next subsequent FIFO transfer for this port would be the start of the next packet. If an error occurred during the reception of the packet, the RLP_ERR would be asserted with RLP_EOP.

Figure 30 RxLink POS-PHY ATM Cell Transfer

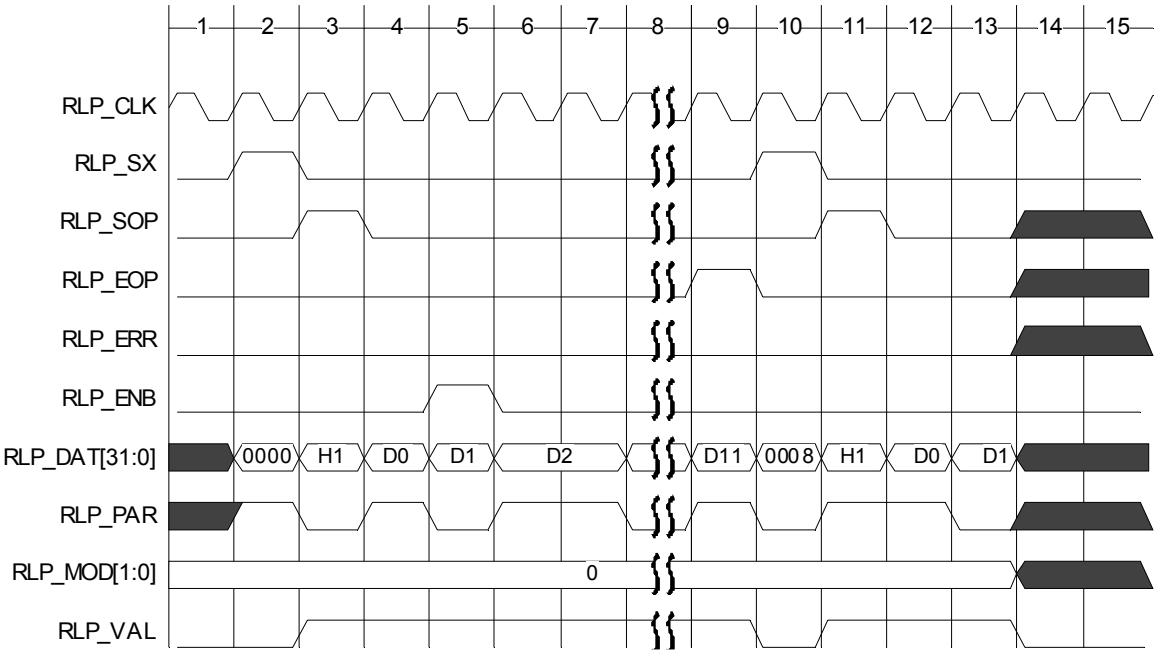


Figure 30 is an example of ATM cells being transferred over the POS-PHY interface. The transfer is initiated with RLP_SX and the address insertion on the RLP_DAT bus. After 3 clocks, the link layer decides to pause the transfer with the deassertion RLP_ENB. The PHY layer must discontinue transfer immediately as shown, holding D2 on the RLP_DAT bus. Transfer commences when the RLP_ENB signal is asserted. Cell traffic continues to flow until the PHY layer has run out of data, at which time it deasserts RLP_VAL. S/UNI-ATLAS-3200 may pause a transfer via RLP_ENB in the middle of a cell or packet; however, generally speaking S/UNI-ATLAS-3200 will not need to do so as long as no backpressure is applied at the output of the device, and the device is properly configured.

Cells and packets may be interleaved, but must be on separate PHYs.

RxPhy POS-PHY Logical Timing

In the ingress direction, the S/UNI-ATLAS-3200 output cell/packet interface acts as a Receive PHY layer device, and the downstream device acts as a Link Layer device, for the purposes of POS-PHY Level 3 cell transfer.

The POS-PHY Receive Interface is controlled by the S/UNI-ATLAS-3200 PHY Layer device. All signals must be updated and sampled using RPP_CLK. The RPP_DAT bus, RPP_PAR, RPP_MOD, RPP_SOP, RPP_EOP and RPP_ERR signals are valid in cycles for which RPP_VAL is high. Outputs will not be updated by the POS-PHY Receive PHY interface when it samples RPP_ENB deasserted. In the example below, RPP_ENB is deasserted by the Link Layer in cycle 4. The S/UNI-ATLAS-3200 interface samples it in cycle 5, and does not update the interface in cycle 6. When transferring data, RPP_VAL is asserted and remains high until the internal FIFO of the PHY layer device is empty, or a complete burst is transferred. A burst always ends at an EOP. The RPP_SX signal is valid in the cycle for which RPP_VAL is low and RPP_ENB was low in the previous cycle.

Figure 31 RxPHY POS-PHY Packet Transfer

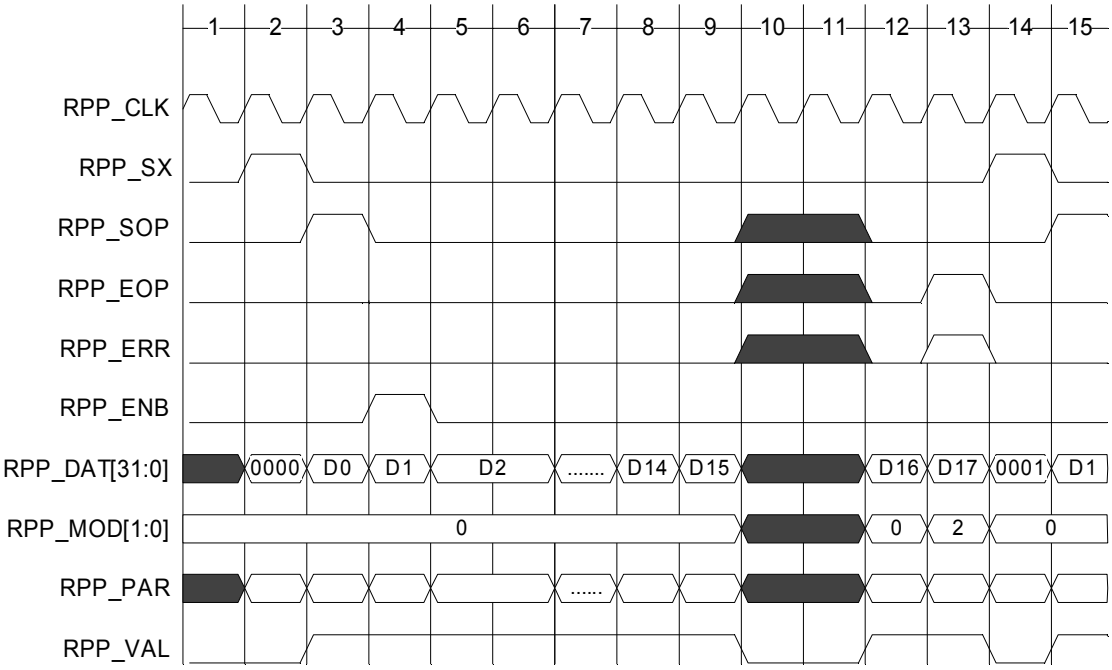


Figure 31 is an example of a multi-port PHY device with at least two channels. The PHY informs the Link Layer device of the port address of the selected FIFO by asserting RPP_SX with the port address on the RPP_DAT bus. The Link Layer may pause the Receive Interface at any time by deasserting the RPP_ENB signal. The end of the packet is indicated with the RPP_EOP signal, along with any error condition on RPP_ERR. The Receive POS-PHY interface bursts data in 16 word bursts. A burst always ends at an EOP, and RSX is always asserted before the start of another burst. The Receive PHY interface selects PHY 1 for the next burst, which starts at cycle 15.

Figure 32 RxPhy POS-PHY ATM Cell Transfer

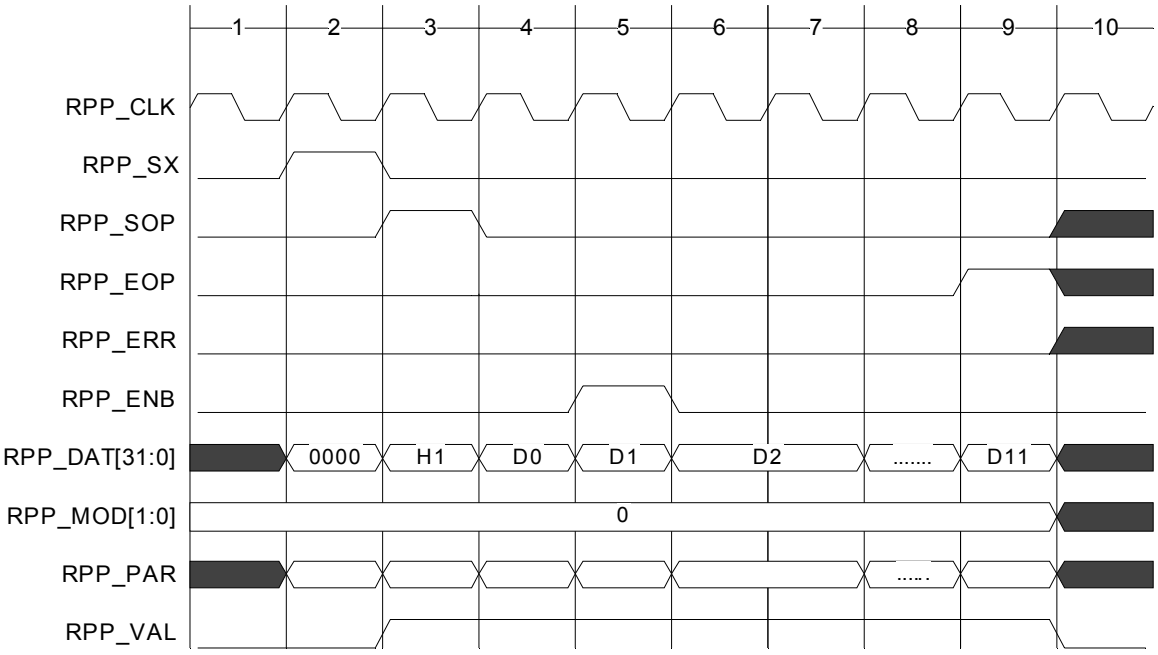


Figure 32 is an example of 52-byte ATM cells being transferred over the POS-PHY interface. The transfer is initiated with RPP_SX and the address insertion on the RPP_DAT bus. After 3 clocks, the link layer decides to pause the transfer by deasserting RPP_ENB. The S/UNI-ATLAS-3200 discontinues the transfer immediately as shown, holding D2 on the RPP_DAT bus. Unless paused by RPP_ENB, the S/UNI-ATLAS-3200 always transfers entire cells, ending with an RPP_EOP. A new RPP_SX selection cycle will occur before another cell or packet is transferred.. Cells and packets may be interleaved, but must be on separate PHYs.

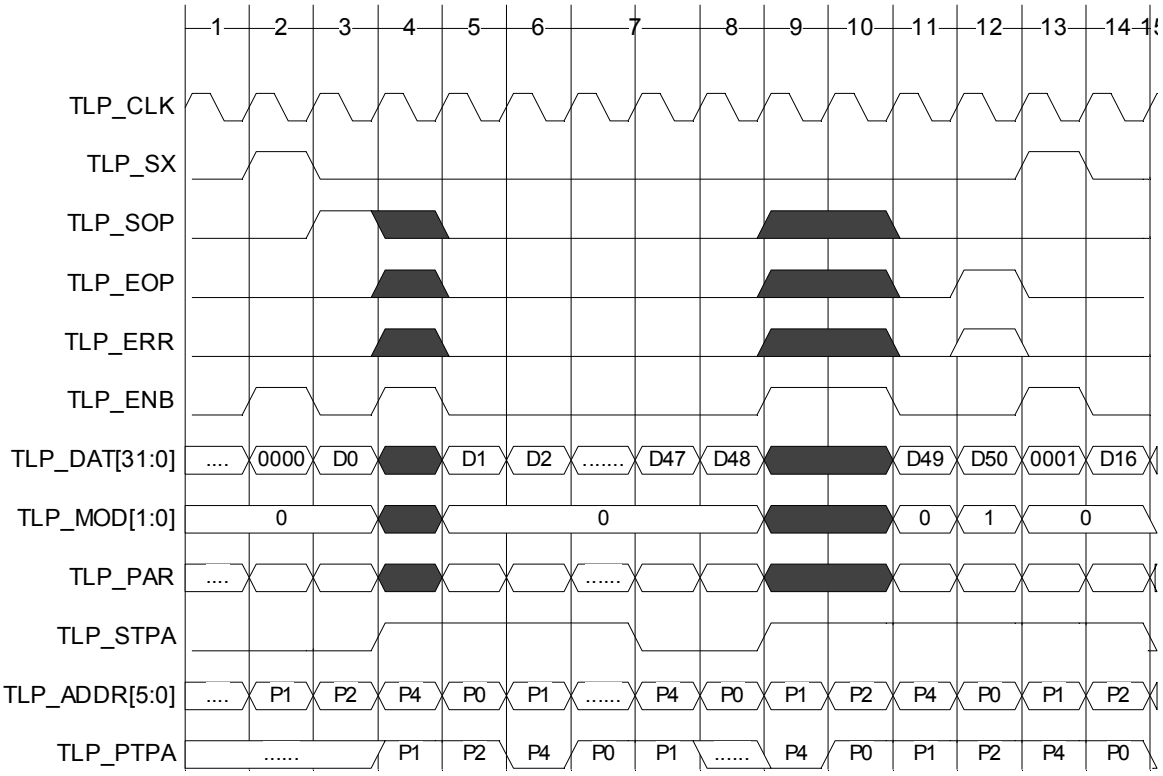
14.1.2 Egress Packet Interface

When the S/UNI-ATLAS-3200 is required to carry a mix of cells and packets, a POS-PHY Level 3 interface is used. In the egress direction, the S/UNI-ATLAS-3200 provides a Tx PHY interface on the input (system) side, and a Tx Link interface on the output (PHY) side. Selection of ingress vs. egress mode and POS vs UL3 signaling must be performed at startup.

The POS-PHY egress transmit interface is controlled by the Link Layer device. Figure 33 is an example of the TxLink block of S/UNI-ATLAS-3200 polling and transmitting to a multi-port PHY device with several channels. The egress input interface (the TxPHY block) works exactly the same way, except that the signals have a TPP (Transmit PHY POS) prefix, and the S/UNI-ATLAS-3200 plays the role of the PHY rather than the Link Layer.

All signals must be updated and sampled using the rising edge of the transmit FIFO clock, TLP_CLK (TPP_CLK on the input side). At the beginning of a transfer, TLP_SX is asserted to indicate that the PHY address is on the data bus TLP_DAT. In the subsequent cycle, TLP_SOP is asserted to show that the first word is present on TLP_DAT, and TLP_ENB is asserted low to indicate valid data. The transfer may be paused at any time by the link layer by deasserting TLP_ENB. S/UNI-ATLAS-3200 will typically move on to another PHY by asserting TLP_SX at this point, but it is not required to. The PHY layer may indicate the that the PHY being transferred to is near-full by deasserting TLP_STPA. The Link Layer must then stop the transfer; it may pause the transfer and resume it once TLP_STPA is reasserted, or it may move on to a different PHY. At the end of a packet, TLP_EOP is asserted. TLP_MOD is valid during the cycle, and indicates how many bytes (between 1 and 4) are valid at the end of the packet. TLP_ERR is also valid during this cycle, and indicates that a packet is errored in some way. S/UNI-ATLAS-3200 will assert TERR if the Traffic Manager indicated the packet was in error, or (configurably) if an interface error such as a parity error was detected.

Figure 33 POS-PHY Level 3 Egress Logical Timing



Transferring cells over this interface is just like transferring packets. The length of the cells is programmed into the TxPHY and TxLink blocks so that they can correctly generate and interpret the packet, but as far as the interface is concerned, ATM cells are simply 52, 56, 60, or 64-byte packets. There exists an option, using the ATM_FIELD and POS_FIELD bits in the TxPHY and TxLink blocks, to insert and check an identifier in the top 8 bits of TDAT during the TLP_SX cycle, which identifies ATM vs packet data. This feature is useful in detecting misconfigurations in the selection of packet vs. ATM PHYs.

TxPhy POS-PHY Logical Timing

The S/UNI-ATLAS-3200 input interface in the egress direction acts as a Tx PHY layer device. This interface is controlled by the attached Link Layer device using the TPP_TENB signal.

Figure 34 is an example of polling and transmission to a multi-port PHY device with several channels. The S/UNI-ATLAS-3200 indicates that a FIFO has at least 16 32-bit words or more of space available by asserting TPP_PTPA when it is polled by the link layer. Polling is accomplished with the TPP_ADDR[5:0] signal. After selection, packet available status is indicated by asserting the selected transmit packet available signal TPP_STPA. TPP_STPA remains asserted while the PHY is selected and until the transmit FIFO is almost full. When TPP_STPA transitions low, it indicates that there are less than 16 32-bit words available in the Transmit FIFO. The latency on this signal is no more than 8 cycles. If STPA is being used, the source must take this latency into account in using STPA to avoid overflow. The use of STPA is optional; the source may safely rely solely on PTPA

Figure 34 TxPhy POS-PHY Packet Transfer

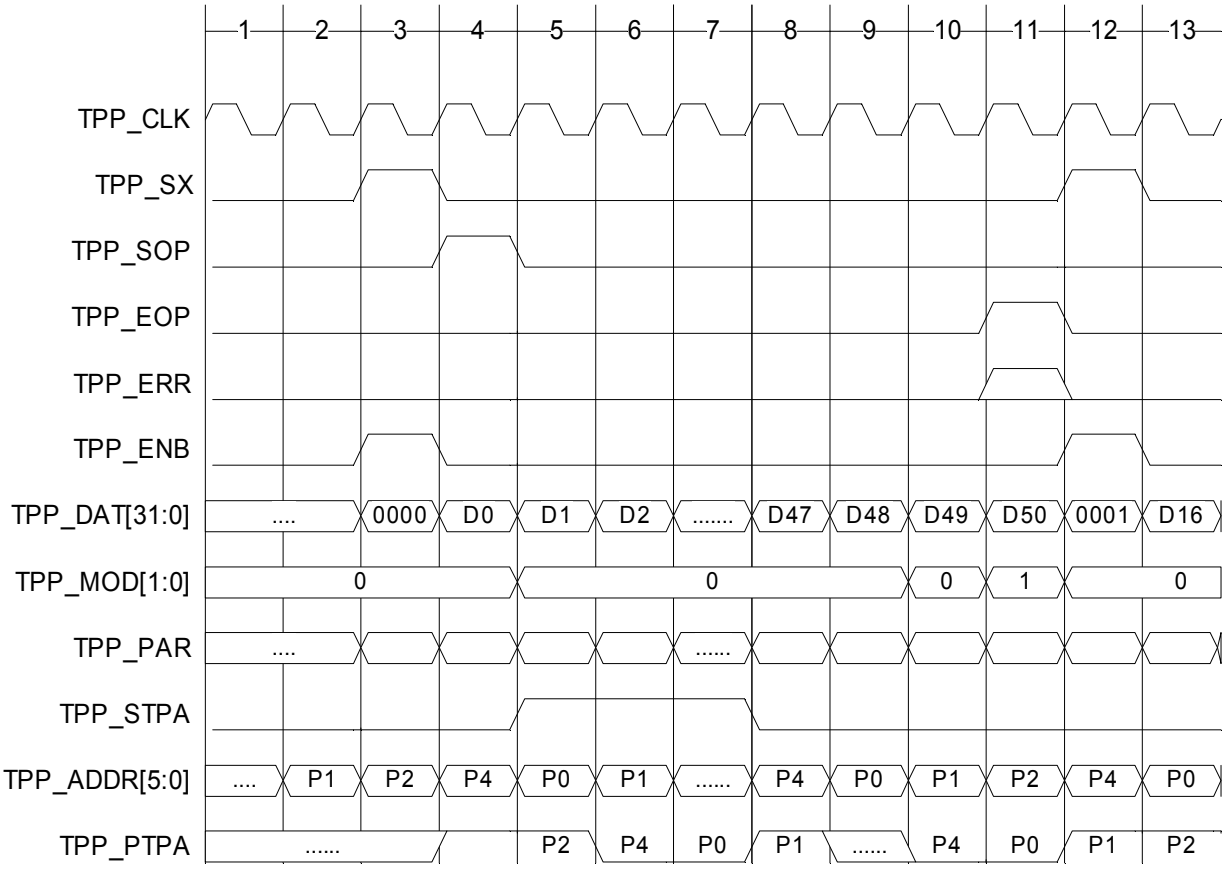
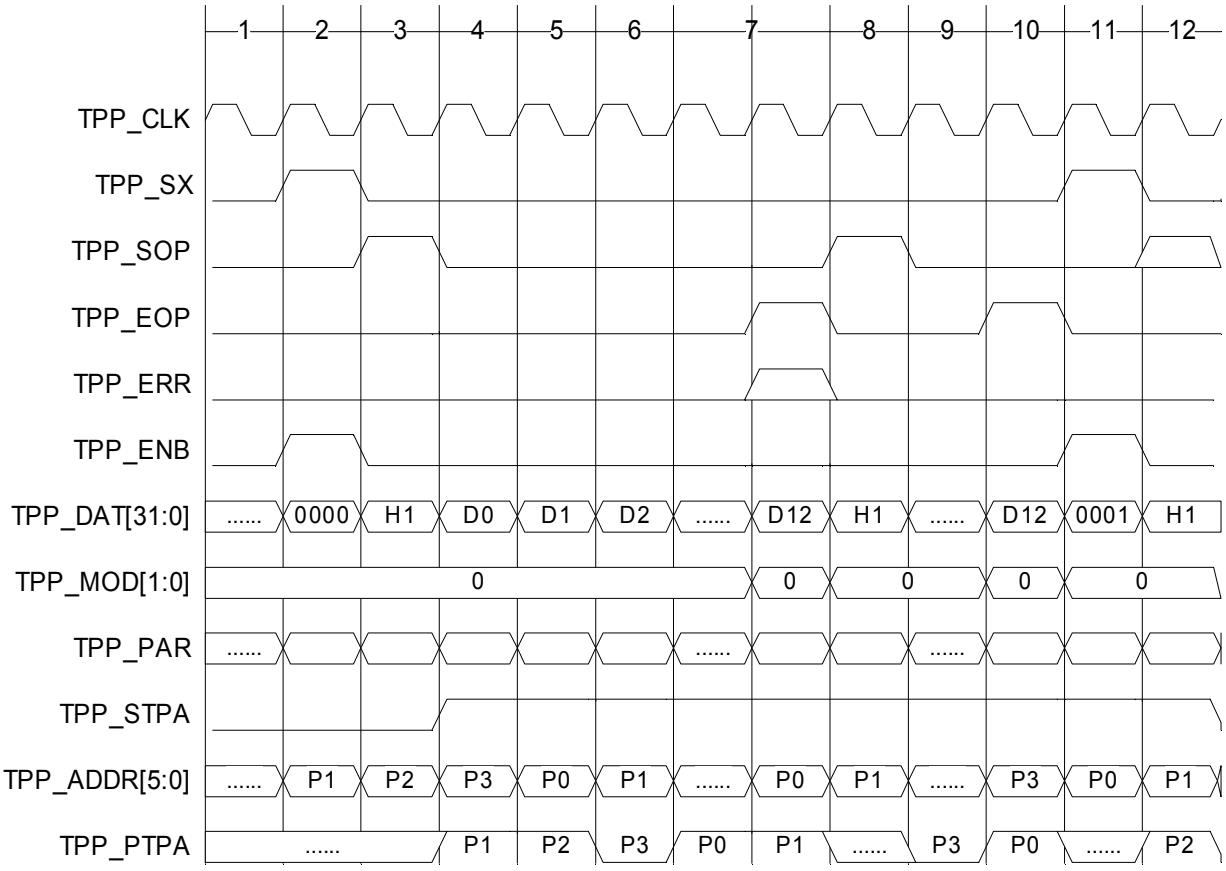


Figure 35 is an example of the Link Layer device polling and sending ATM cells across the POS interface to the S/UNI-ATLAS-3200 Transmit PHY interface. The Link Layer device is not restricted in its polling order. Cells and packets may be interleaved, but they must belong to separate FIFOs.

Figure 35 Transmit POS-PHY ATM Cell Transfer



TxLink POS-PHY Logical Timing

The S/UNI-ATLAS-3200 output interface in the egress direction acts as a Tx Link layer device. This interface controls the attached PHY Layer device using the TLP_ENB signal.

Figure 36 TxLink POS-PHY Logical Timing

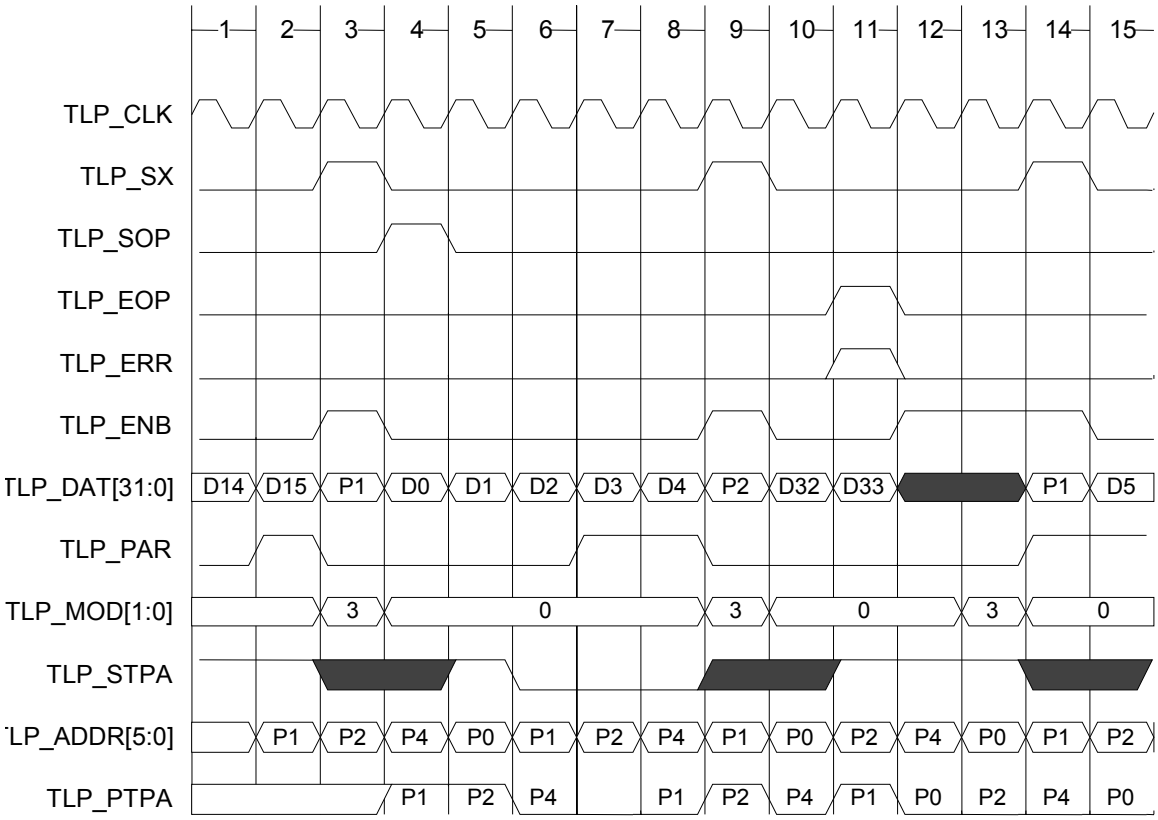


Figure 36 is an example of polling and transmission to a multi-port PHY device with several channels. The PHY layer device indicates that a FIFO is not full by asserting TLP_PTPA when it is polled by the S/UNI-ATLAS-3200. Polling is accomplished with the TLP_ADDR[5:0] signal. After selection, packet available status is indicated by asserting the selected transmit packet available signal TLP_STPA. TLP_STPA remains asserted while the PHY is selected and until the transmit FIFO is almost full. The S/UNI-ATLAS-3200 will halt data transfer three clocks after TLP_STPA is driven low on the bus, if the USE_STPA register bit is logic 1. The S/UNI-ATLAS-3200 will then select the next PHYID in the calendar which has a positive PTPA response and for which data is available in the S/UNI-ATLAS-3200.

The S/UNI-ATLAS-3200 will transmit packets in 16 word bursts. In cycle 1 and 2, a 16 word burst is completing for a packet. In cycle 3, PHY P1 is selected for transfer and the PHY device indicates the selected PHY is nearly full by deasserting TLP_STPA in cycle 6. The ATM Layer device halts data transfer in cycle 9. PHY P1 is again polled in cycle 9, and the PHY device indicates that it has space for additional data. The ATM layer device selects PHY P1 in cycle 14, and continues the packet transfer.

Figure 37 TxLink POS-PHY ATM Cell Transfer Timing

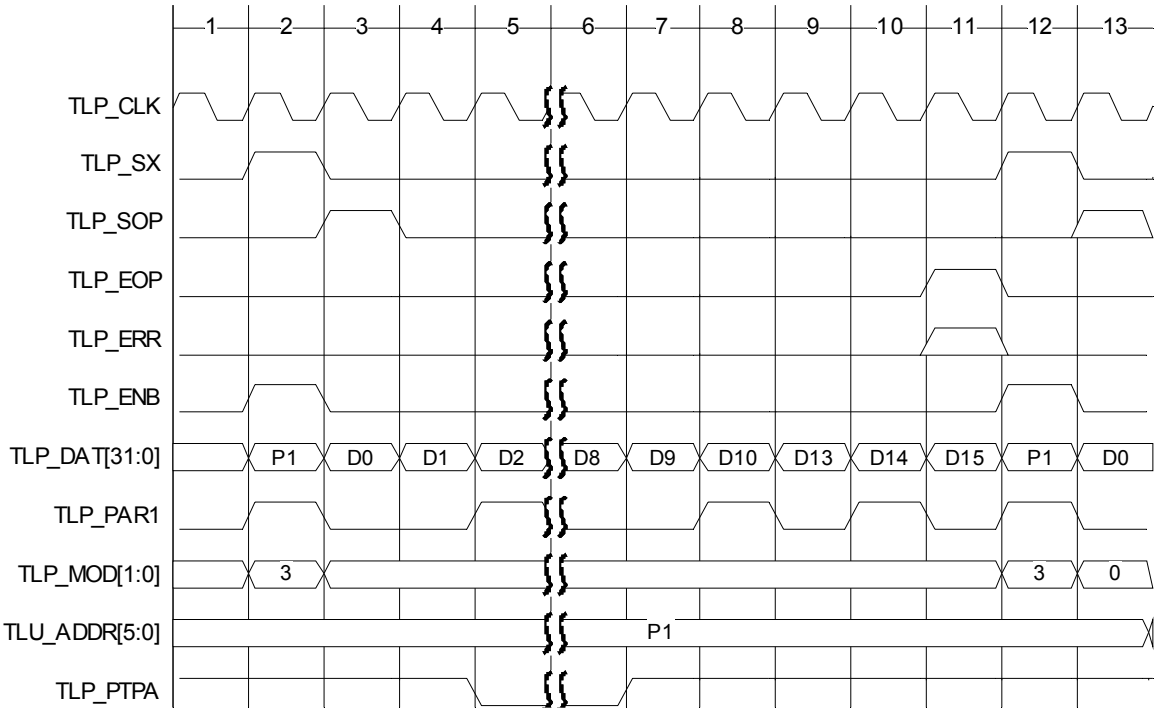


Figure 37 is an example of the Link Layer device sending ATM cells across the POS interface. The status of a given PHY port may be determined by setting the polling address TLU_ADDR bus to the port address. The polled transmit packet available signal TLP_PTPA is updated with the transmit FIFO status in a pipelined manner. The Link Layer device is not restricted in its polling order. The selected transmit packet available TLP_STPA signal allows monitoring the selected PHY status and halting data transfer once the FIFO is full. In this case, PHY P1 is being polled continuously on TLU_ADDR. The PHY device indicates that there is no space for the next burst by driving TLP_PTPA low in cycle 5. Note that the ATM Link Layer device will ignore TLP_PTPA for the selected PHY until 3 clocks after selection. Later on in cycle 6 of the diagram during the transfer of word D8, the PHY indicates that there actually is space in the transmit FIFO for an additional cell. For back to back ATM cells on the POS interface, the PHY device must indicate TLP_PTPA asserted no less then five clocks before the last word of the transfer. Cells and packets may be interleaved, but they will belong to different FIFOs.

14.2 UTOPIA Level 3

The S/UNI-ATLAS-3200 features UTOPIA Level 3 compliant interfaces to the PHY side and the system side. The S/UNI-ATLAS-3200 acts as a master to the PHY side (like any other UL3 ATM layer device), and appears as a 48-PHY device to the system side. To accommodate system side devices which may not support multi-PHY queues in the ingress direction, the Output Cell Interface supports a “self-polled” mode in which it will ignore the presented UTOPIA address and appear as a single PHY.

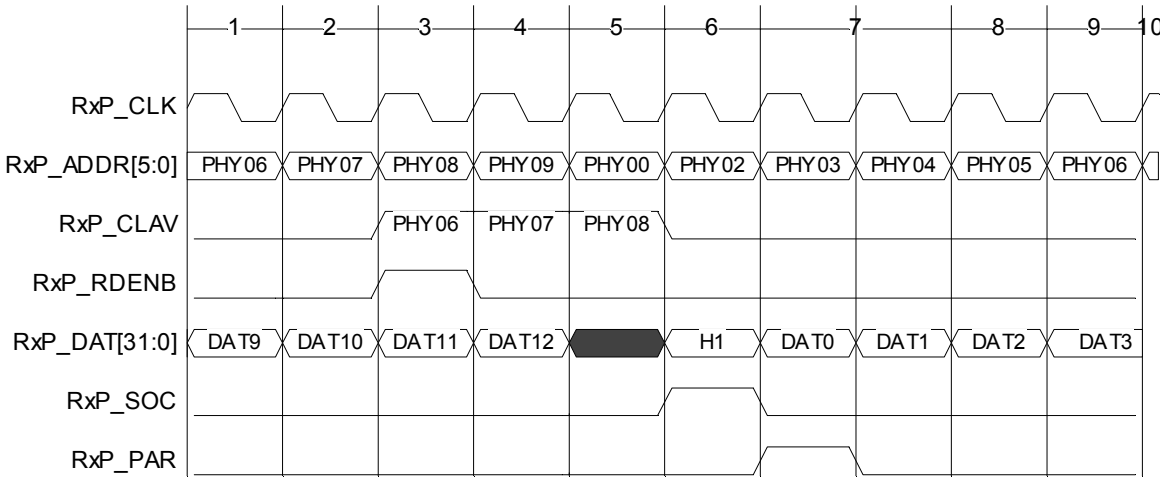
14.2.1 Ingress UL3 Interface

In the Ingress direction, the S/UNI-ATLAS-3200 provides an Rx Link interface on the input (PHY) side, and an Rx PHY interface on the output (system) side. Selection of ingress vs. egress mode and POS vs UL3 signalling must be performed at startup.

Figure 38 shows the format of an Rx UTOPIA transfer. On the input (RxLink) side the 'x' in the signals is a 'L'; on the output (RxPHY) side the 'x' is a 'P'.

The Rx interface in UL3 is controlled by the downstream ATM Layer (aka Link Layer) device, which polls the PHY layer device, and uses RxP_RDENB to select PHYs for transfer, and enable the transfer. Once a transfer has been initiated, it must be completed.

Figure 38 Ingress UTOPIA Logical Timing

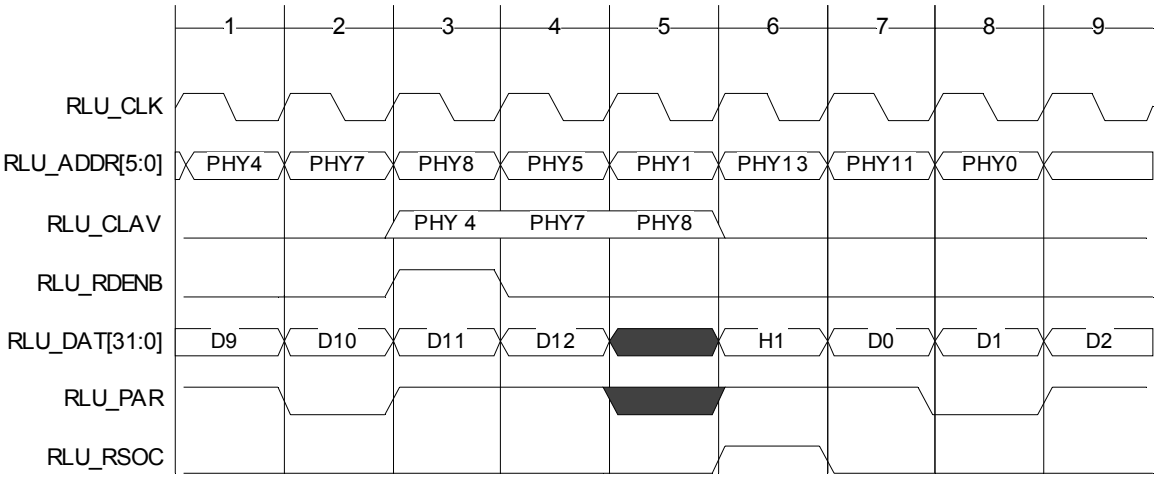


The Receive Link Layer interface is a regular UL3 MPHY interface. The Receive PHY layer interface, however, can operate either as a MPHY interface, or as a single-PHY interface. The single-PHY interface, selected via the Servicing Override bit in the RxP Configuration register, allows the S/UNI-ATLAS-3200 to interface to a MPHY device on its input, and to an non-PHY-aware, single-PHY switch fabric on the other. In this case, cells will be drawn from the internal PHY queues as determined by the RxP Calendar. This operation is transparent to the switch, which sees a single-PHY interface.

RxLink UTOPIA Logical Timing

In the ingress direction, the S/UNI-ATLAS-3200 input cell/packet interface acts as a Receive ATM Layer device, and the upstream device acts as a PHY Layer device, for the purposes of UTOPIA Level 3 cell transfer.

Figure 39 RxLink UTOPIA Cell Transfer



The UTOPIA Receive Interface is controlled by the ATM Layer device. Figure 39 shows the S/UNI-ATLAS-3200 polling the PHY layer device with the address bus in order to gather cell available status. The PHY layer device can send a cell to an ATM port only when PHY port has indicated that it has at least one complete ATM cell available and when the ATM port has indicated to the PHY layer device that it is ready to receive a cell. The S/UNI-ATLAS-3200 will indicate this by asserting the RLU_RDENB in response to a Receive Cell Available (RLU_CLAV) signal from the PHY device. Once the RLU_CLAV signal has been asserted, the PHY layer is committed to a cell transfer. Figure 39 shows that PHY 8 is engaged for transfer with the selection cycle in cycle 4. PHY 8 has two clocks to respond and does so with data in cycle 6.

Figure 40 RxLink Back-to-Back UTOPIA Cell Transfers

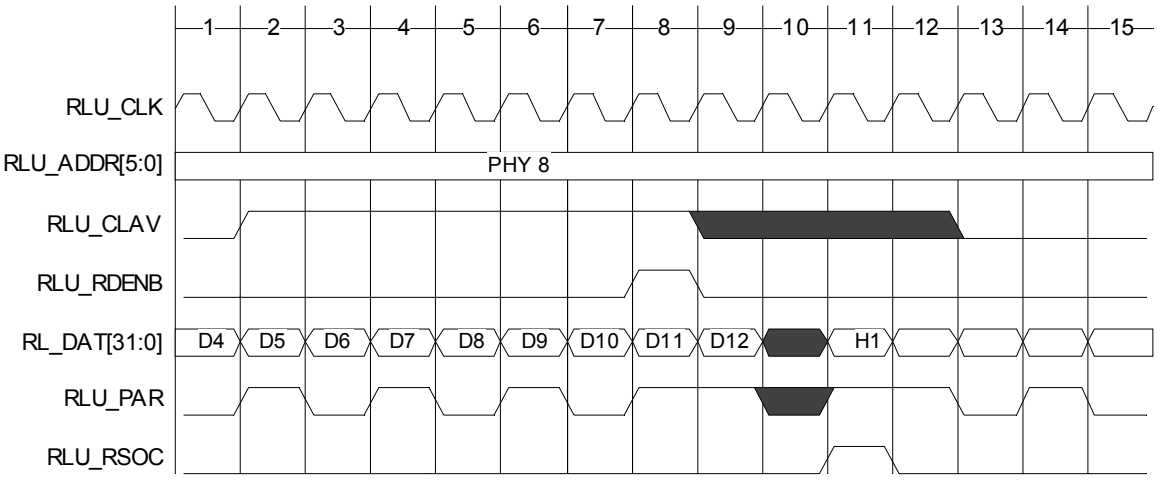


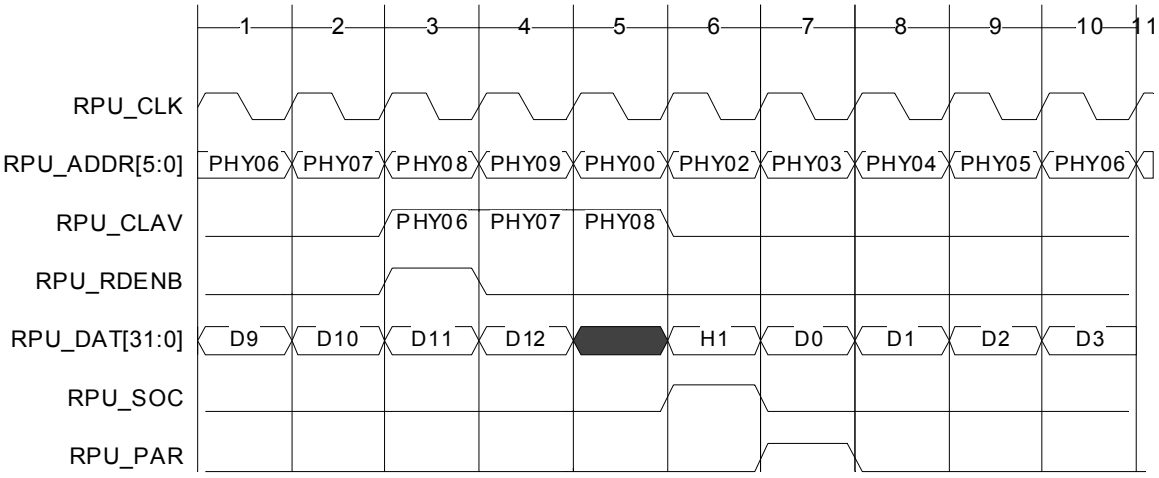
Figure 40 shows the RxLink I/O datapath signals for UTOPIA back to back transfer. Two cells are shown being transferred from the same PHY address (PHY 8) with a dead cycle in between. In order for full bandwidth support, RLU_CLAV must be asserted at least 8 clock cycles before the end of the current transfer. See cycle 2. Note also that the RxLink squelches RLU_CLAV up to RLU_RSOC+1 cycles if the phyid being serviced is identical to the one being polled. This is to guarantee that the RLU_CLAV sent to the RxLink is not for the current cell being serviced, but for the next cell transfer.

S/UNI-ATLAS-3200 always reselects the PHY by temporarily deasserting RLU_RDENB between cell transfers.

RxPhy UTOPIA Timing

In the ingress direction the S/UNI-ATLAS-3200 output cell/packet interface acts as a Receive PHY layer device, and the downstream device acts as an ATM Layer device, for the purposes of UTOPIA Level 3 cell transfer.

Figure 41 RxPhy UTOPIA Cell Transfer



The S/UNI-ATLAS-3200 UTOPIA Receive PHY Interface is controlled by the attached ATM Layer device. Figure 41 shows the ATM layer polling the S/UNI-ATLAS-3200 device with the address bus in order to gather cell available status. The S/UNI-ATLAS-3200 will assert RPU_CLAV only when it can transfer an entire cell. The ATM Layer device will read the cell by asserting the RPU_RDENB in response to a Receive Cell Available (RPU_CLAV) signal from the S/UNI-ATLAS-3200 device. Figure 41 shows that PHY08 is engaged for transfer with the selection cycle in clock number 4. PHY08 has two clocks to respond and does so with data in cycle 6.

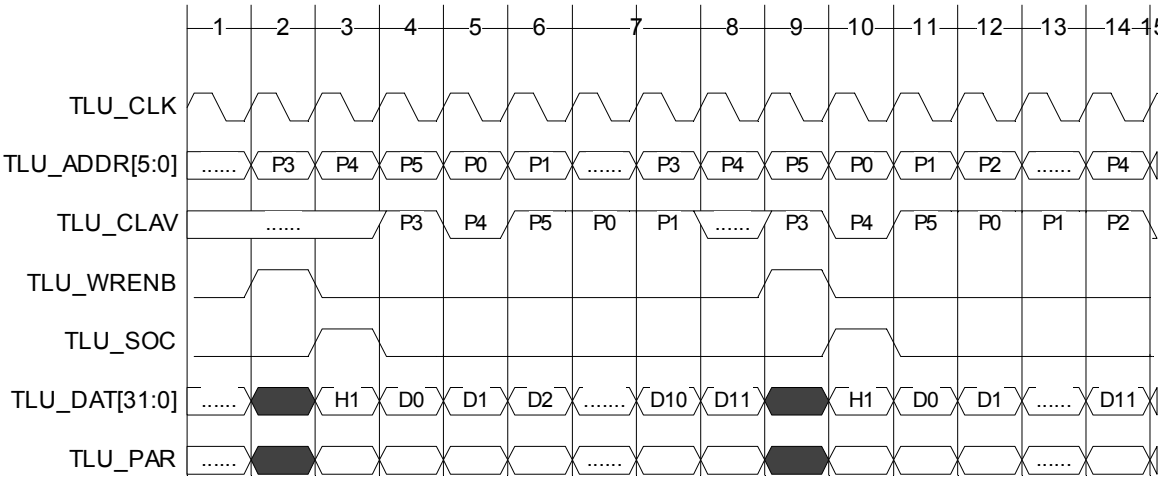
The RxPhy is capable of appearing as a single-PHY device, removing the need for polling. In this case the RxPHY will use an internal calendar to determine the order in which the PHY queues are serviced. Single-PHY operation is controlled via the Servicing Override bit in the RxP Configuration register.

14.2.2 Egress UL3 Interface

In the Egress direction, the S/UNI-ATLAS-3200 provides a Tx PHY interface on the input (system) side, and a Tx Link interface on the output (PHY) side. Selection of ingress vs. egress mode and POS vs UL3 signalling must be performed at startup.

Figure 42 shows the Egress TxLink interface that interfaces to the PHY side; the TxPhy interface operates in the same way, but the signal names start with TPU, and the S/UNI-ATLAS-3200 plays the role of the PHY.

Figure 42 Egress UTOPIA Logical Timing

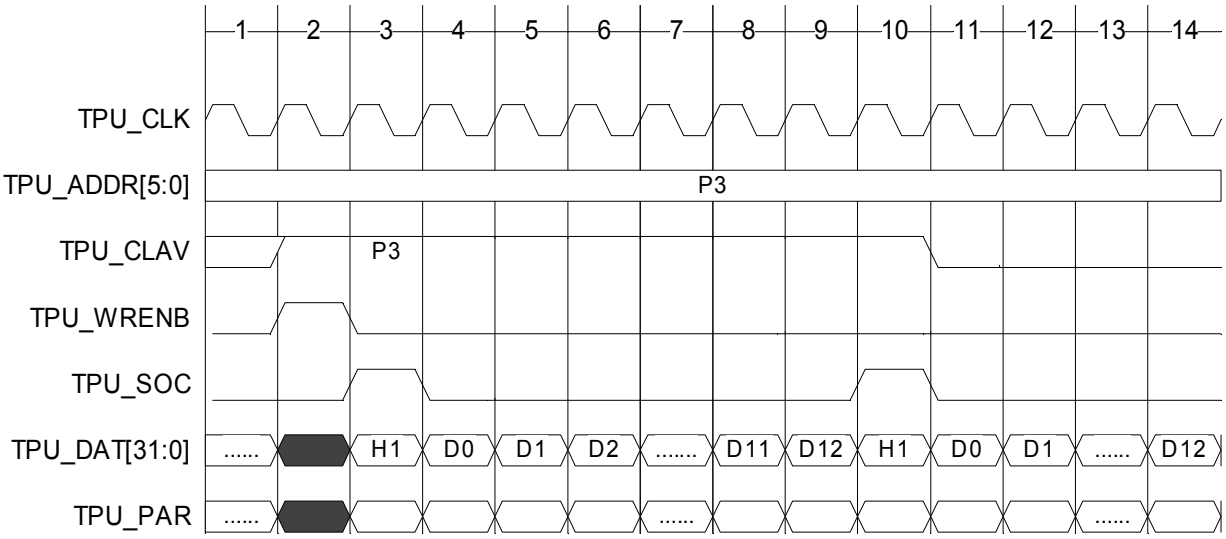


The S/UNI-ATLAS-3200 can send a cell to a PHY port only when the PHY port has indicated to the ATM layer device that it is ready to receive at least one cell. The PHY device will indicate this by asserting the Transmit Cell Available (TLU_CLAV). The PHY device must deassert the TxClav 2 cycles after sampling TLU_SOC high if it cannot accept the immediate transfer of a subsequent cell.

TxPhy UTOPIA Logical Timing

In the egress direction the S/UNI-ATLAS-3200 input cell/packet interface acts as a Transmit PHY layer device, and the upstream device acts as an ATM Layer device, for the purposes of UTOPIA Level 3 cell transfer.

Figure 43 TxPhy UTOPIA Cell Transfer

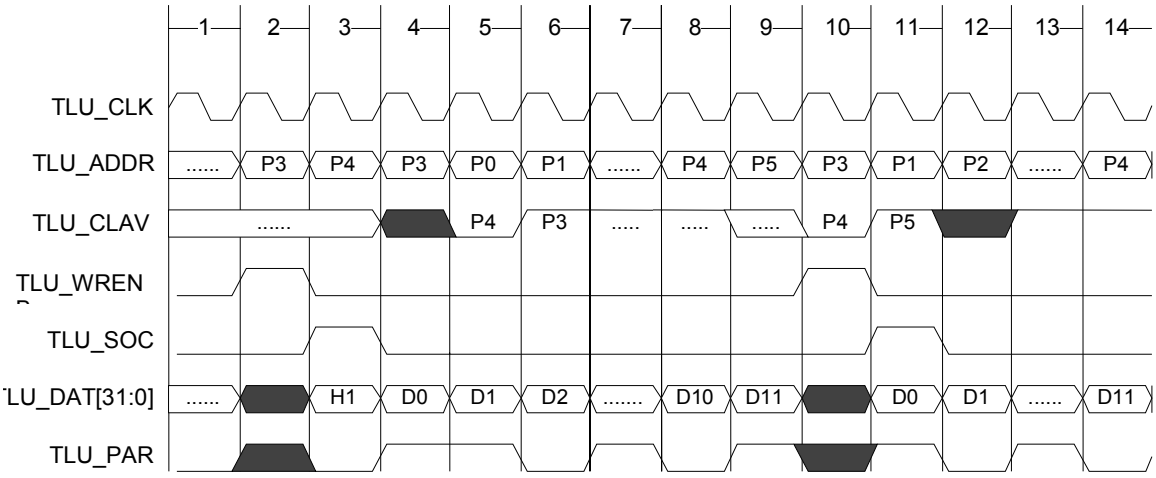


The ATM layer device can send a cell to the S/UNI-ATLAS-3200 transmit PHY port only when the S/UNI-ATLAS-3200 has indicated to the ATM layer device that it is ready to receive at least one cell. The S/UNI-ATLAS-3200 will indicate this by asserting the Transmit Cell Available (TPU_CLAV). In this case, the ATM Layer is only polling a single PHY. The S/UNI-ATLAS-3200 will deassert TPU_CLAV one cycle after TPU_SOC if it cannot accept the immediate transfer of a subsequent cell. Once TPU_CLAV has been asserted, it will have to stay asserted until the clock edge after the Start of Cell (TPU_SOC). Figure 43 shows the case in which cells are transferred back-to-back, utilizing the full bandwidth of the bus. This can be achieved in the case where the S/UNI-ATLAS-3200 indicates 1 cycle after TPU_SOC that it can accept at least one complete cell in addition to the current cell (TPU_CLAV asserted) and the ATM device has a cell ready for transfer.

TxLink UTOPIA Logical Timing

In the egress direction the S/UNI-ATLAS-3200 output cell/packet interface acts as a Transmit ATM Layer device, and the downstream device acts as a PHY Layer device, for the purposes of UTOPIA Level 3 cell transfer.

Figure 44 TxLink UTOPIA Transfer



The UTOPIA Transmit Interface is controlled by the S/UNI-ATLAS-3200. Figure 44 shows the S/UNI-ATLAS-3200 polling the PHY layer device with the address bus (TLU_ADDR) to gather transmit cell available status (TLU_CLAV). The S/UNI-ATLAS-3200 can send a cell to a PHY port only when the PHY port has indicated to the S/UNI-ATLAS-3200 device that it is ready to receive at least one cell. The PHY device will indicate this via TLU_CLAV. The TLU_CLAV in response to the PHY selection (i.e. the value of TLU_CLAV in cycle 4) is ignored by the LINK device. Once TLU_CLAV has been asserted for a particular PHY queue, it will have to stay asserted for that PHY until a cell is transmitted to the PHY layer device on that PHY queue. Figure 44 shows that a cell is engaged for transfer to PHY 3 with the selection cycle in cycle 2.

Figure 45 TxLink Back-to-Back UTOPIA Transfer

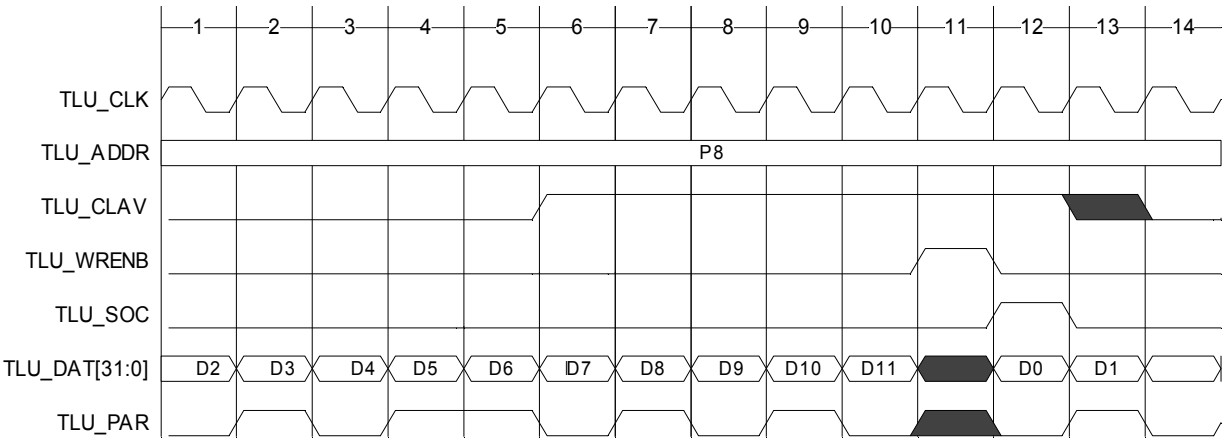


Figure 45 shows the S/UNI-ATLAS-3200 performing a back to back transfer. Two cells are shown being transferred to the same PHY address (PHY 8) with a selection cycle in between. S/UNI-ATLAS-3200 will always perform this selection between cells. In order for full bandwidth support, TLU_CLAV must be asserted at least 5 clock cycles before the end of the current transfer. See cycle 6. Note also that the ATM Layer device ignores TLU_CLAV responses from the PHY up until cycle 14, for the purposes of deciding whether to transfer yet another cell on the same PHY. The cycle after selection, cycle 12, is the first cycle it is valid for the ATM Layer device to poll the selected PHY to determine if it has space for the next cell transfer. This is to guarantee that the TLU_CLAV sent to the ATM Layer is not for the current cell being serviced, but for the next cell transfer.

14.3 SRAM Interface

The S/UNI-ATLAS-3200 stores the search and linkage tables in up to 16M of external SRAM. The SRAM may be in two 256Kx36 or one 256Kx72 units, and must be pipelined ZBT SRAM's rated for at least a 7ns cycle time. Only 8M of external SRAM (e.g. two 128Kx36) is required to support 64K connections. However, up to 16M of RAM may be provisioned if the additional search depth is desired. 18 address bits are provided, to support up to a 256Kx72 external SRAM. If less SRAM is provisioned, the MSB of the RAM address should still be connected to SADDR[17]; SADDR[16] may be left unconnected if only 8M of external SRAM is needed, SADDR[16:15] if only 4M, and so on.

To facilitate timing from S/UNI-ATLAS-3200 to the SRAMs, the device drives the SRAM clock (SRAMCLK_O) along with the address, data, and control signals. To facilitate timing from the SRAM to the S/UNI-ATLAS-3200, a copy of SRAMCLK_O , called SYSCLK_O, must be fed back into the device on the SYSCLK pin. This arrangement is illustrated in Figure 46.

Figure 46 Interface between S/UNI-ATLAS-3200 and External RAM

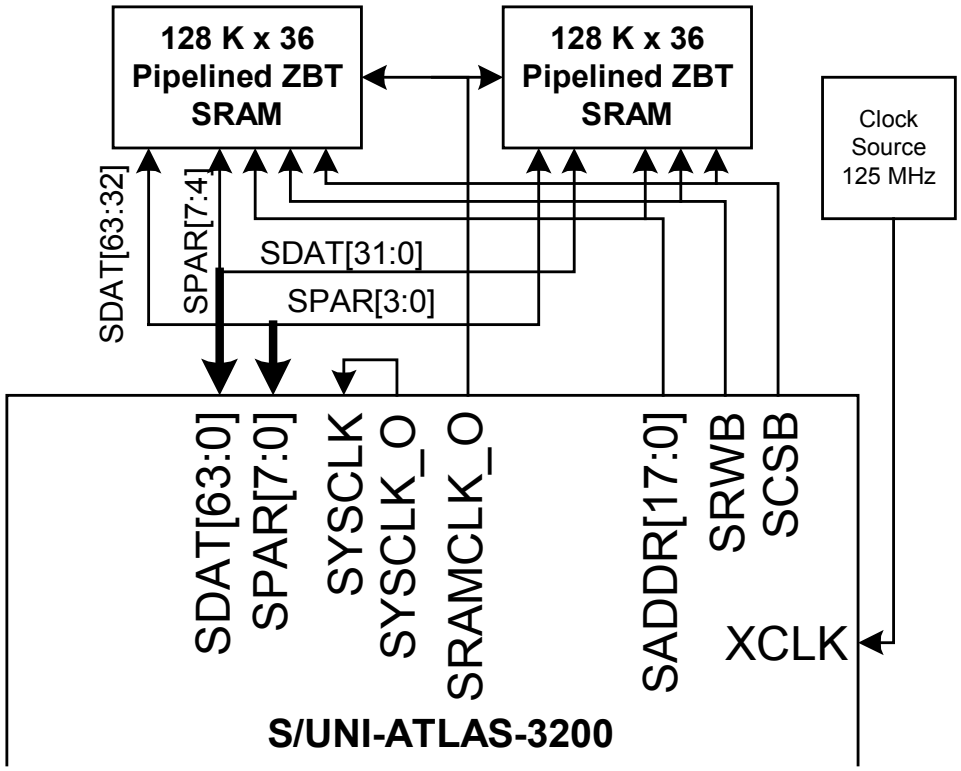
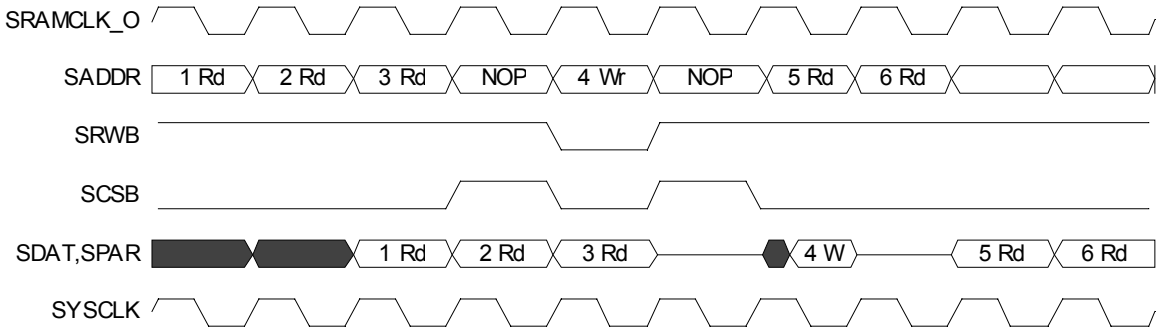


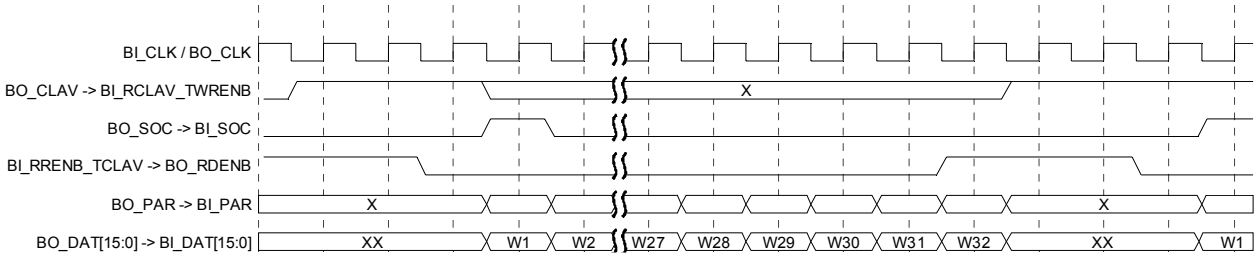
Figure 47 illustrates the operation of the SRAM interface. The majority of accesses to the external SRAMs are reads, with the occasional write initiated by the microprocessor. As as a result, the CSB signal is used to insert dead cycles between reads and writes, to facilitate easy board design.

Figure 47 SRAM Interface Functional Timing



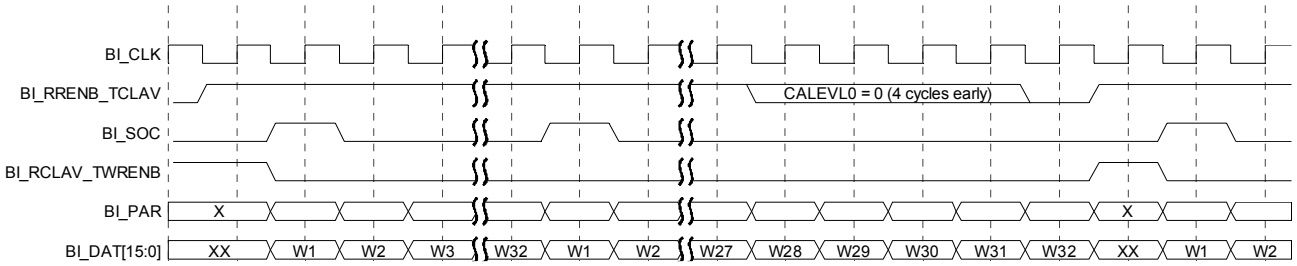
14.4 Backwards Cell Interface

Figure 48 Normal BCIF Functional Timing



In a typical implementation, the BCIFs of two S/UNI-ATLAS-3200 devices are wired directly to each other. In this case, the IBCIF is an Rx Master, and the OBCIF is an Rx Slave. BI_RCLAV_TWRENB is acting as BI_RCLAV. Figure 48 shows a cell transfer, 64 bytes in length, and the start of a second transfer.

Figure 49 IBCIF as Tx Slave Functional Timing



In some implementations, such as when connecting a tester or another device to the interface, it may be desirable to set the IBCIF_TxSlave bit to logic 1. In this case, the BCIF as a whole appears like a PHY device, i.e. with one Tx Slave and one Rx Slave. BI_RCLAV_TWRENB is actiing as BI_TWRENB. In this configuration, back-to-back cells may be transferred.

15 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 52 Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage (VDD33)	-0.3V to +3.9V
Supply Voltage (VDD25, VDDQ25)	-0.3V to 3.5V
Supply Voltage (VDDQ15)	-0.3V to +3.0V
Supply Voltage (VDD15)	-0.3V to +3.0V
Voltage on Any 3.3V I/O Pin	-0.3V to VDD33 + 0.3V
Voltage on Any 2.5V I/O Pin (i.e. the SRAM interface)	-0.3 to VDD25 + 0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±10 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+125°C

16 D.C. Characteristics

TJ = 0°C to TJ=100°C, VDD33 = 3.3 V ±0. 165V, VDDQ25 = 2.5± 0.125V, VDD25 = 2.5± 0.125V, VDDQ15 = 1.5 V ± 0.075V, VDD15 = 1.5 V ± 0.075V

(Typical Conditions: TC = 25°C, VDD = 3.3 V, VDD25 = VDDQ25 = 2.5V, VDDQ15 = VDD15 = 1.5V)

Table 53 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDD33	3.3V Power Supply	3.135	3.3	3.465	Volts	
VDD25	2.5V Power Supply	2.375	2.5	2.625	Volts	
VDDQ25	2.5V Power Supply	2.375	2.5	2.625	Volts	
VDDQ15	1.5V Power Supply	1.425	1.5	1.575	Volts	
VDD15	1.5V Power Supply	1.425	1.5	1.575	Volts	
VIL33	Input Low Voltage (3.3V TTL Only)	-0.3		0.8	Volts	Guaranteed Input LOW Voltage
VIL25	Input Low Voltage (2.5V I/O)	-0.3		0.7		
VIH33	Input High Voltage (3.3V TTL Only)	2.0		VDD33 +0.3	Volts	Guaranteed Input HIGH Voltage
VIH25	Input High Voltage (2.5V I/O)	1.7		VDD25 + 0.3		
VOL	Output or Bidirectional Low Voltage		0.1	0.4	Volts	VDD33 = min, IOL = -2 mA minimum. Note 2
			0.2	0.4	Volts	VDD33 = min, IOL = -8 mA minimum. Note 2
VOH33	Output or Bidirectional High Voltage (3.3V Only)	VDD33 – 0.6V	3.0		Volts	VDD33 = min, IOH = 2 mA minimum. Note 2
		VDD33 – 0.6V			Volts	VDD33=min, IOH = 8mA minimum. Note 2.
VOH25	Output or Bidirectional High Voltage (2.5V Only)	VDD25 – 0.6V				
		VDD25 – 0.6V			Volts	VDD25 = min, IOH = 8mA minimum
VT+	Reset Input High Voltage	2.0			Volts	TTL Schmitt

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VT-	Reset Input Low Voltage			0.8	Volts	TTL Schmitt
VTH	Reset Input Hysteresis Voltage		0.4		Volts	TTL Schmitt
IILPU	Input Low Current	+10		+200	µA	VIL = GND. Notes 1, 2
IIHPU33	Input High Current (3.3V I/O)	-15		+650	µA	VIH = VDD33. Notes 1, 2
IIHPU25	Input High Current (2.5V I/O)	-10		+10	µA	VIH = VDD25. Notes 1, 2
CIN	Input Capacitance		5		PF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance		5		PF	Excluding Package, Package Typically 2 pF
CIO	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
IDDOP unloaded	Operating Current Processing Cells				mA	VDD33 = 3.60 V, VDD15 = 1.575 Outputs Unloaded, SYSCLK = 125 MHz Interface Clocks = 104 MHz BCIF Clock = 52 MHz
IDDOP loaded	Total Operating Current Processing Cells				mA	VDD33 = 3.60 V, VDD15 = 1.575 Outputs Loaded with 50 pf, SYSCLK = 125 MHz Interface Clocks = 104 MHz MHz BCIF Clock = 52 MHz

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

17 A.C. Timing Characteristics

17.1 Conditions

TJ = 0°C to TJ=100°C, VDD33 = 3.3 V ±0.165V, VDD25 = 2.5± 0.125V, VDDQ25 = 2.5± 0.125V, VDDQ15 = 1.5 V ± 0.075V, VDD15 = 1.5 V ± 0.075V

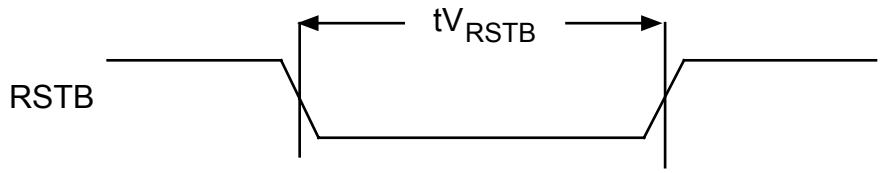
(Typical Conditions: TC = 25°C, VDD = 3.3 V, VDD25 = VDDQ25 = 2.5V, VDDQ15 = VDD15 = 1.5V)

17.2 Reset Timing

Table 54 RTSB AC Timing

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		Ns

Figure 50 RSTB AC Timing

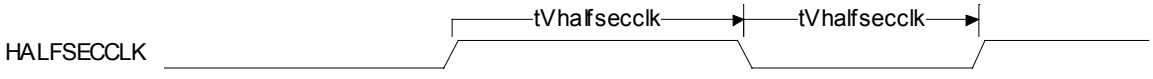


17.3 Half-Second Clock Timing

Table 55 Half-Second Clock AC Timing

Symbol	Description	Min	Max	Units
$tV_{HALFSEC}$	HALFSECCLK pulse width	100		Ns

Figure 51 Half-Second Clock AC Timing



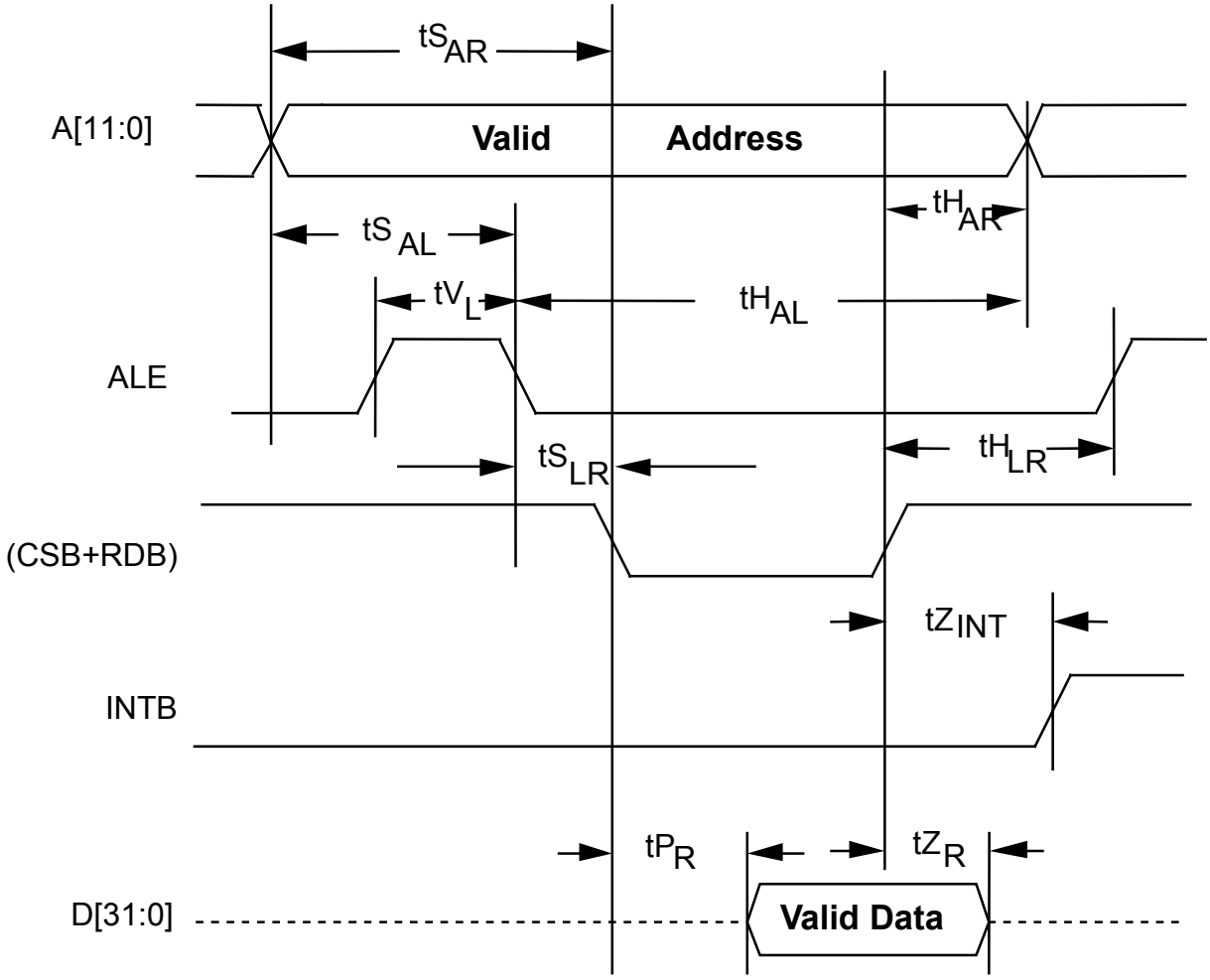
17.4 Microprocessor Interface Read Timing

Table 56 Microprocessor Interface Read Access AC Timing

Symbol	Parameter	Min	Max	Units
TS_{AR}	Address to Valid Read Set-up Time	5		Ns
TH_{AR}	Address to Valid Read Hold Time	2.5		ns

Symbol	Parameter	Min	Max	Units
TS_{ALR}	Address to Latch Set-up Time	5		ns
TH_{ALR}	Address to Latch Hold Time	5		ns
T_{VL}	Valid Latch Pulse Width	10		ns
TS_{LR}	Latch to Read Set-up	0		ns
TH_{LR}	Latch to Read Hold	2.5		ns
TP_{RD}	Valid Read to Valid Data Propagation Delay		30	ns
TZ_{RD}	Valid Read Negated to Output Tri-state		13	ns
TZ_{INTH}	Valid Read Negated to Output Tri-state		20	ns

Figure 52 Microprocessor Interface Read Access AC Timing



Notes on Microprocessor Interface Read Timing:

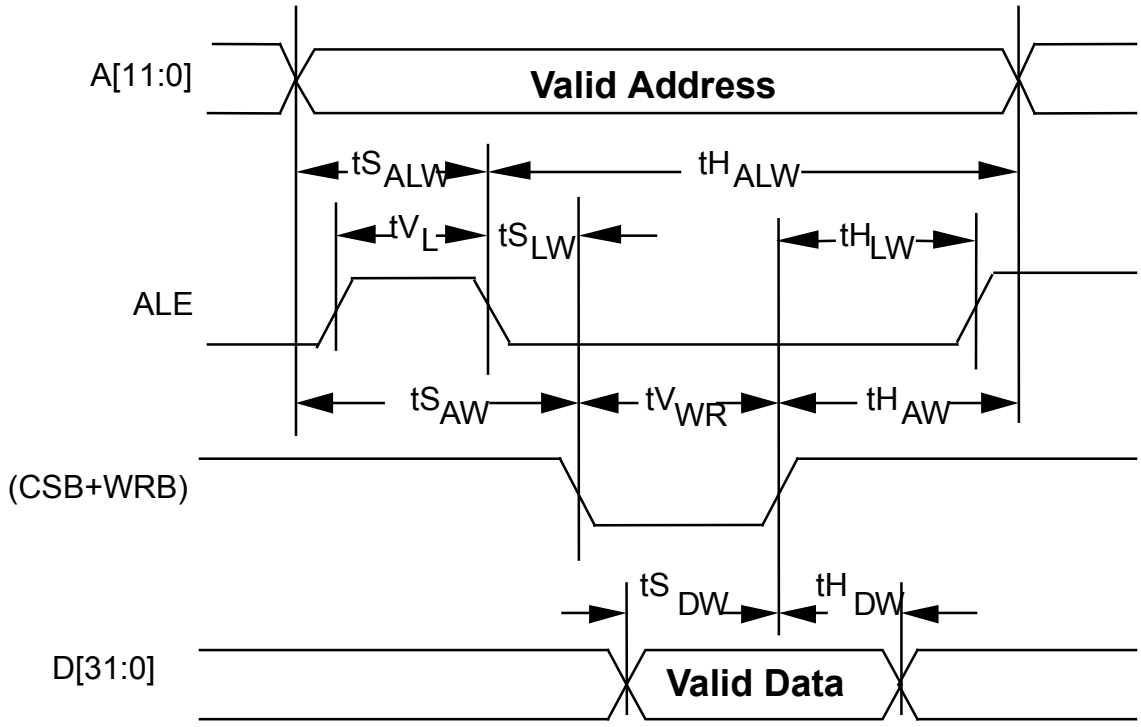
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point o\ the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[31:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable.
5. Parameter tHAR is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17.5 Microprocessor Interface Write Timing

Table 57 Microprocessor Interface Write Access AC Timing

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	5		ns
tS_{DW}	Data to Valid Write Set-up Time	10		ns
tS_{ALW}	Address to Latch Set-up Time	5		ns
tH_{ALW}	Address to Latch Hold Time	5		ns
t_{VL}	Valid Latch Pulse Width	10		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	2.5		ns
tH_{DW}	Data to Valid Write Hold Time	3.0		ns
tH_{AW}	Address to Valid Write Hold Time	2.5		ns

Figure 53 Microprocessor Interface Write AC Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, and tSLW are not applicable.
3. Parameter tHAW is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17.6 UL3/PL3 Interface Timing

Table 58 UTOPIA Level 3 / POS-PHY Level 3 AC Timing

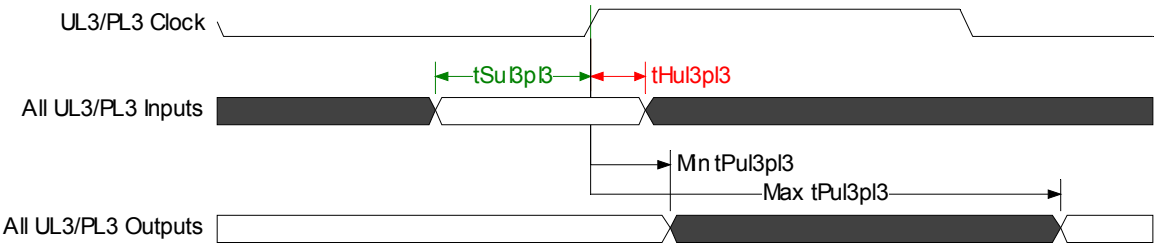
Symbol	Description	Min	Max	Units
$F_{ul3pl3clk}$	UL3/PL3 Clock Frequency (1)	75	104	MHz
$PW_{ul3pl3clk}$	UL3/PL3 Clock pulse Width (high or low)	4.0		ns
tS_{ul3pl3}	UL3/PL3 Input Setup to Clock High	2.0		ns
tH_{ul3pl3}	UL3/PL3 Clock High to Input Hold	0.5		ns

Symbol	Description	Min	Max	Units
TP_{ul3pl3}	UL3/PL3 Clock to Output Propagation Delay (2)	1.5	6.0	ns

Notes:

1. Throughput is not guaranteed below 104 MHz.
2. 30 pf load.

Figure 54 UTOPIA Level 3 / POS-PHY Level 3 AC Timing

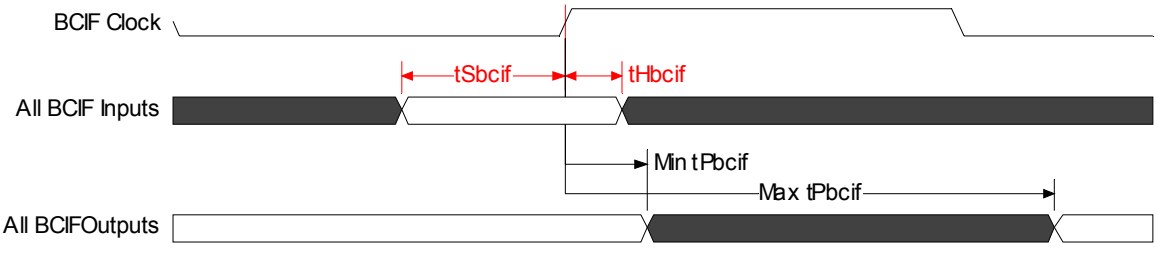


17.7 BCIF Interface Timing

Table 59 BCIF Interface AC Timing

Symbol	Description	Min	Max	Units
$F_{bcifclk}$	BI_CLK or BO_CLK Frequency		52	MHz
$tPW_{bcifclk}$	BI_CLK or BO_CLK High or Low pulse width	7.6		ns
tS_{bcif}	All IBCIF inputs valid to BI_CLK high setup. All OBCIF inputs valid to BO_CLK high setup	4.0		ns
tH_{bcif}	BI_CLK high to IBCIF Input hold. BO_CLK high to OBCIF Input hold	1.0		ns
tP_{bcif}	BI_CLK high to IBCIF Outputs valid BO_CLK high to OBCIF Outputs valid	2.0	12.0	ns

Figure 55 BCIF Interface AC Timing

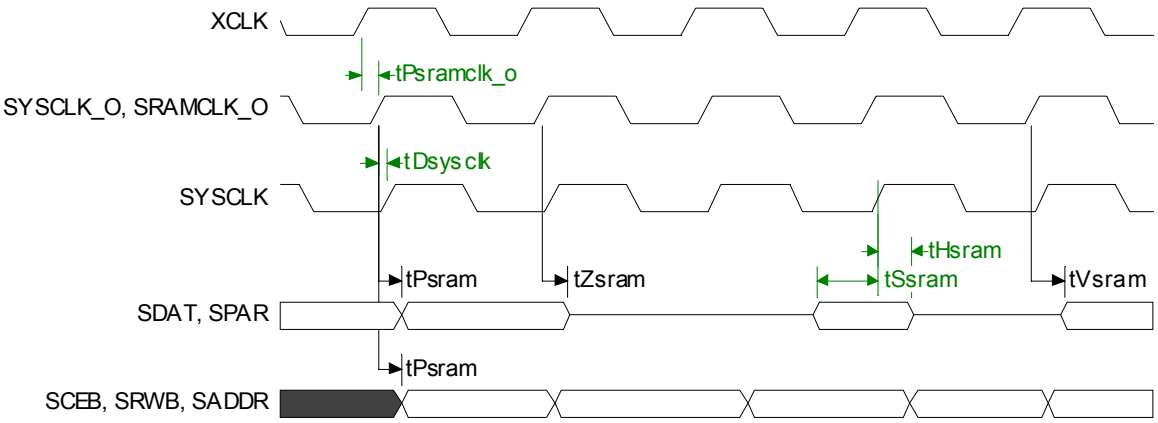


17.8 SRAM Interface Timing

Table 60 SRAM Interface AC Timing

Symbol	Description	Min	Max	Units
F_{xclk}	XCLK Frequency (1)	100	125	MHz
tPW_{xclk}	XCLK High or Low pulse width	3.2		ns
$tP_{sramclk_o}$	XCLK to SRAMCLK_O or SYSCLK_O Delay (unconstrained)	--	--	ns
tD_{sysclk}	Required external Delay from SYSCLK_O to SYSCLK input	0	1.0	ns
tP_{sram}	SRAMCLK_O to SDOUT, SPAR, SCEB, SRWB propagation delay	1.0	5.5	ns
tZ_{sram}	SRAMCLK_O to SDOUT, SPAR high-impedance	1.0	6.0	ns
tV_{sram}	SRAMCLK_O to SDOUT, SPAR low-impedance	1.0	5.5	ns
tS_{sram}	SDAT, SPAR setup to SYSCLK	3.0		
tS_{sram}	SDAT, SPAR hold to SYSCLK	1.0		

Figure 56 SRAM Interface AC Timing



Notes:

1. Min XCLK reflects min frequency for correct operation. Throughput is not guaranteed for frequencies other than 125 MHz.

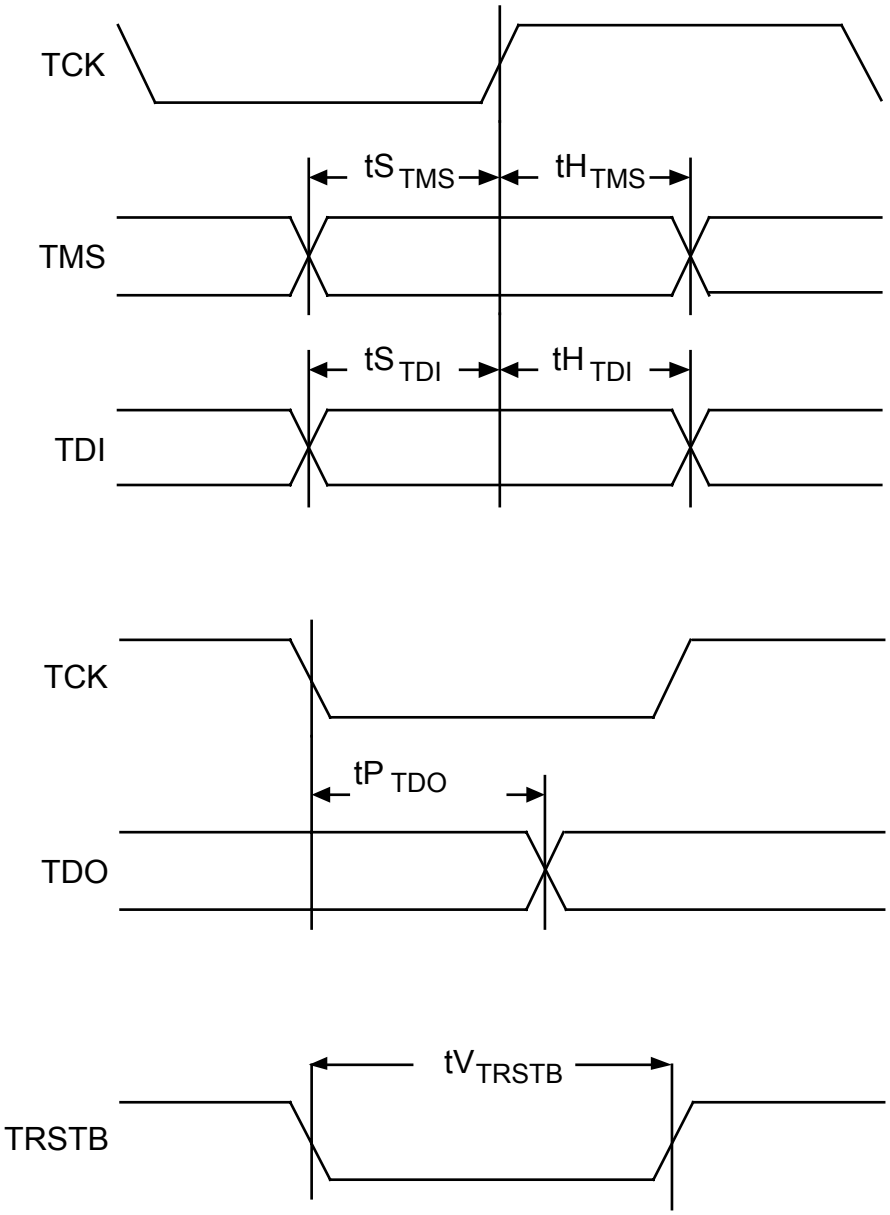
17.9 JTAG Interface Timing

Table 61 JTAG Port Interface Timing

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz

Symbol	Description	Min	Max	Units
	TCK Duty Cycle	40	60	%
$^{TS}_{TMS}$	TMS Set-up time to TCK	50		ns
$^{tH}_{TMS}$	TMS Hold time to TCK	50		ns
$^{tS}_{TDI}$	TDI Set-up time to TCK	50		ns
$^{tH}_{TDI}$	TDI Hold time to TCK	50		ns
$^{tP}_{TDO}$	TCK Low to TDO Valid	2	50	ns
$^{tV}_{TRSTB}$	TRSTB Pulse Width	100		ns

Figure 57 JTAG Port Interface AC Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs.

18 Ordering and Thermal Information

18.1 Ordering Information

Table 62 Ordering Information

Part No.	Description
PM7325-TC	768 TBGA

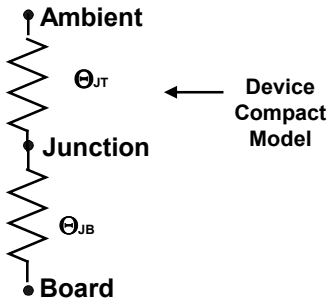
18.2 Thermal Information

This product is designed to operate over a wide temperature range and is suited for commercial applications such as central office equipment.

Maximum long-term operating junction temperature to ensure adequate long-term life	100 ^{0}C
Maximum junction temperature for short-term excursions with guaranteed continued functional performance.[1] This condition will typically be reached when local ambient reaches 70 Deg C.	100 ^{0}C
Minimum ambient temperature	-5 ^{0}C

Thermal Resistance vs Air Flow[2]			
Airflow	Natural Convection	200 LFM	400 LFM
Θ_{JA} (^{0}C/W)	10.7	7.9	6.2

Device Compact Model[3]	
Θ_{JT} (^{0}C/W)	1.2
Θ_{JB} (^{0}C/W)	4.0



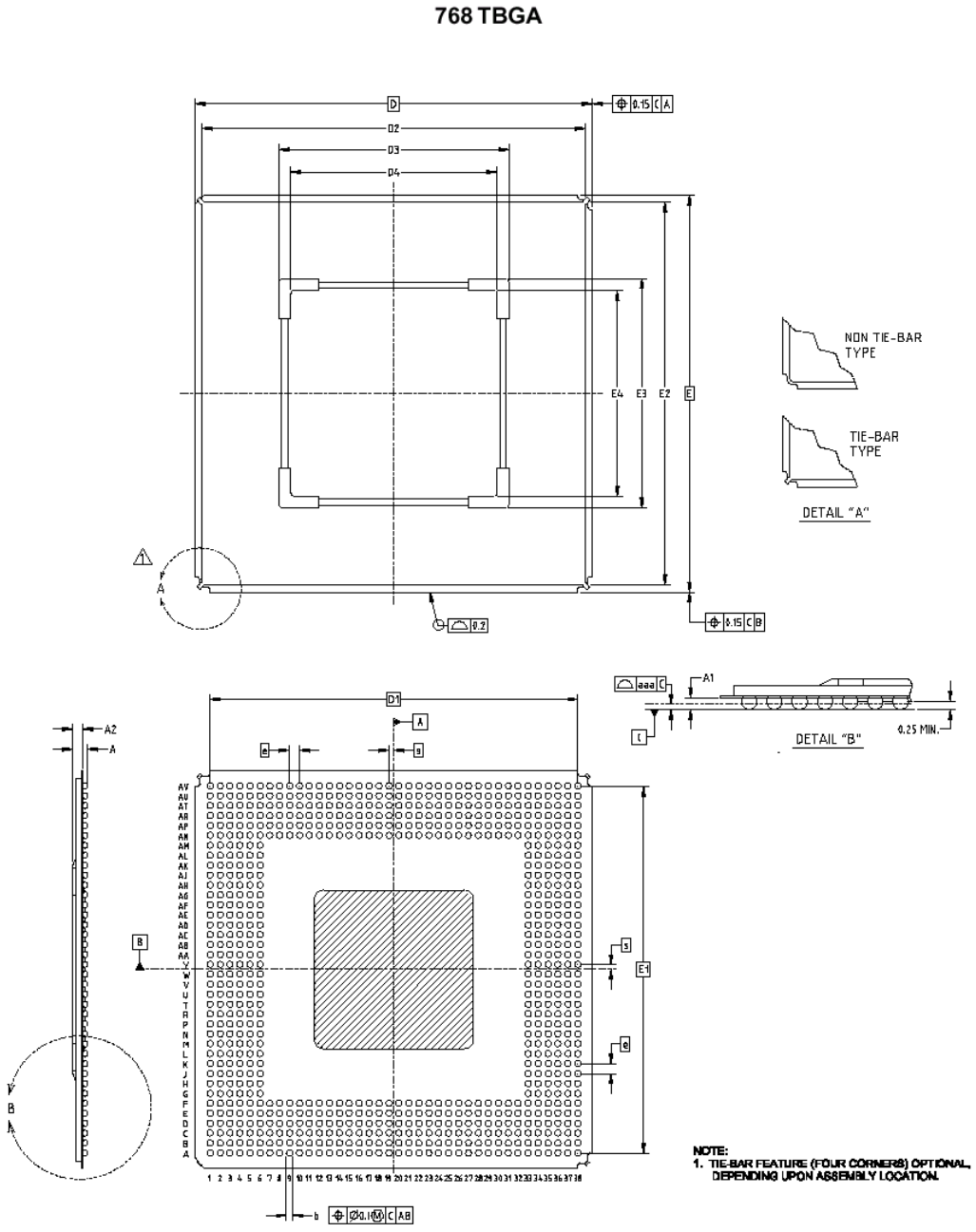
Operating power dissipated in package (watts) at worst case power supply, worst case traffic	
Power (watts)	3.0 W

Notes

1. Short-term is understood as the definition stated in Bellcore Generic Requirements GR-63-Core.
2. Θ_{JA} , the total junction to ambient thermal resistance as measured according to JEDEC Standard JESD51 (2S2P)
3. Θ_{JB}, the junction-to-board thermal resistance and Θ_{JT}, the residual junction to ambient thermal resistance are obtained by simulating conditions described in JEDEC Standard, JESD 15-8.

19 Mechanical Information

Figure 58 768 Tape Ball Grid Array (TBGA)



768 TBGA Dimensions

Package Type (Package Code)	† 768 TBGA (T-BGA768-4040-1.00A6) Non Tie-Bar (T-BGA768-4040-1.00B6) Tie-Bar		
Symbol	Millimeters		
	Min	Nom	Max
A	–	–	1.6
A1	0.4	0.5	0.6
A2	–	–	1.0
b	0.5	0.6	0.7
D		40.0 BSC	
D1		37.0 BSC	
D2	38.4	38.6	38.8
D3	22.9	23.1	23.3
D4	20.5	20.7	20.9
E		40.0 BSC	
E1		37.0 BSC	
E2	38.4	38.6	38.8
E3	22.9	23.1	23.3
E4	20.5	20.7	20.9
e		1.0 BSC	
s		0.5 BSC	
aaa		0.15	

Notes