PMC-Sierra,Inc.

PM8353 QuadPHY™

4-Channel 1.0-1.25 Gbps Transceiver

FEATURES

- Four independent 1.0-1.25 Gbit/s transceivers
- Four secondary channels to support channel redundancy
- Ultra low power operation: 1.25 Watt typical
- Integrated serializer/deserializer, clock synthesis, clock recovery, and 8B/10B encode/decode logic
- Physical Coding Sublayer (PCS) logic for Gigabit Ethernet
- Selectable 8-bit, 10-bit, or IEEE 802.3z GMII parallel interface
- Optional Receive FIFOs which synchronize incoming data to local clock domain
- "Trunking" feature to de-skew and align received parallel data across four channels
- 100-156 MHz Single Data Rate (SDR) parallel transmit interface with clock forwarding
- 100-125 MHz SDR parallel receive interface
- Extensive control of loopback, BIST, and operating modes via 802.3 compliant MDC/MDIO serial interface
- Built-in packet generator/checker
- IEEE 1149.1 JTAG testing support
- IEEE 802.3z Gigabit Ethernet and ANSI X3T11 Fibre Channel support
- High speed outputs which feature programmable output current to directly drive dual-terminated line
- 2.5V, 0.25 micron CMOS technology with 3.3V tolerant I/O
- Direct interface to optical modules, coax, or serial backplanes
- Small footprint 19x19 mm, 289-pin PBGA

APPLICATIONS

- High speed serial backplanes
- Gigabit Ethernet links
- Fibre Channel links
- Intra-system interconnect
- ASIC to PMD link

GENERAL DESCRIPTION

The QuadPHY™ is a Quad PHYsical layer transceiver ideal for systems requiring large numbers of point-to-point gigabit links. It provides four individual serial channels capable of operation at up to 1.25 Gbps each, which may be grouped together to form a single 5.0 Gbps bidirectional link. Each of the four primary channels has a corresponding secondary channel that can be enabled via the MDC/MDIO serial interface.

The QuadPHY includes 8B/10B block coding logic (compliant with 802.3z Gigabit Ethernet and Fibre Channel requirements) which produces run length limited data streams for serial transmission.

A receive FIFO optionally aligns all incoming parallel data to the local clock domain, adding or removing IDLE sequences as required. This simplifies implementation of the upstream ASIC by removing the requirement to deal with multiple clock domains.

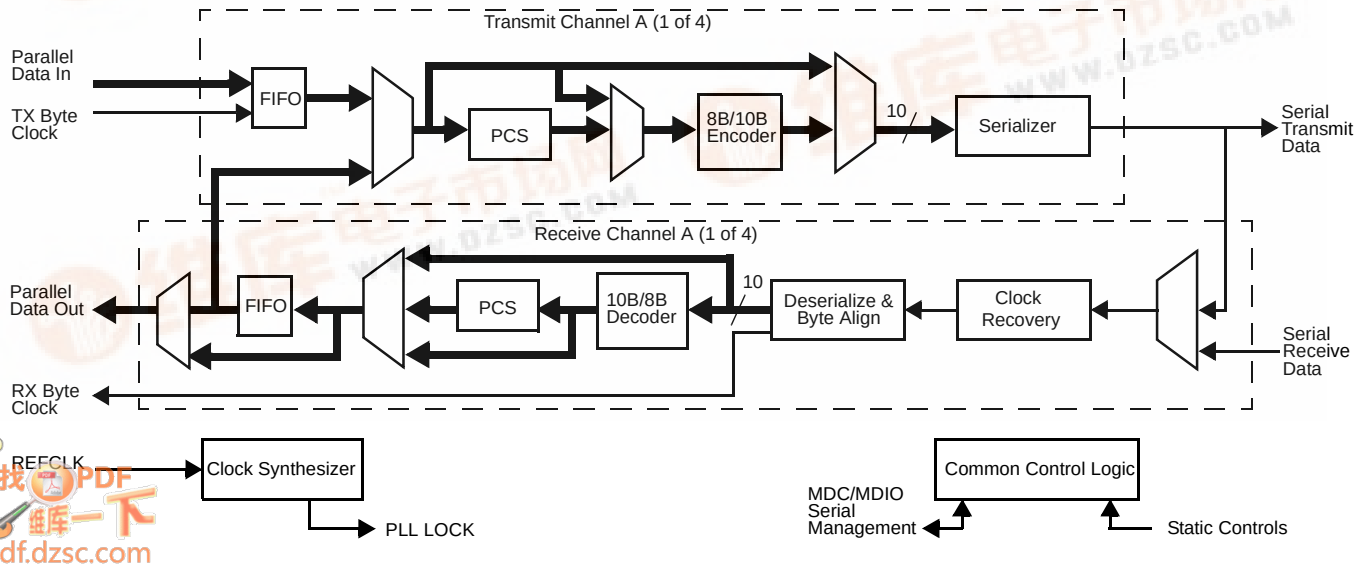
When trunking is enabled, the QuadPHY can remove cable skew differences equivalent to several meters, presenting 4-byte data vectors at the receive interface exactly as they were transmitted.

EXAMPLE ARCHITECTURE

The first figure on the next page shows the QuadPHY in a switch application. This implementation uses four channels of 1.25 Gbaud per linecard, requiring only 16 signal pins per linecard and 64 for the switch card, providing up to 16 Gbps total payload capacity to the switch fabric.

The dotted lines in the figure depict the system clock domains. Note that even though the recovered clock from any or all serial links may be asynchronous to the local clock, the QuadPHY bridges these domains so that the switch fabric and linecards may be designed in only a single clock domain.

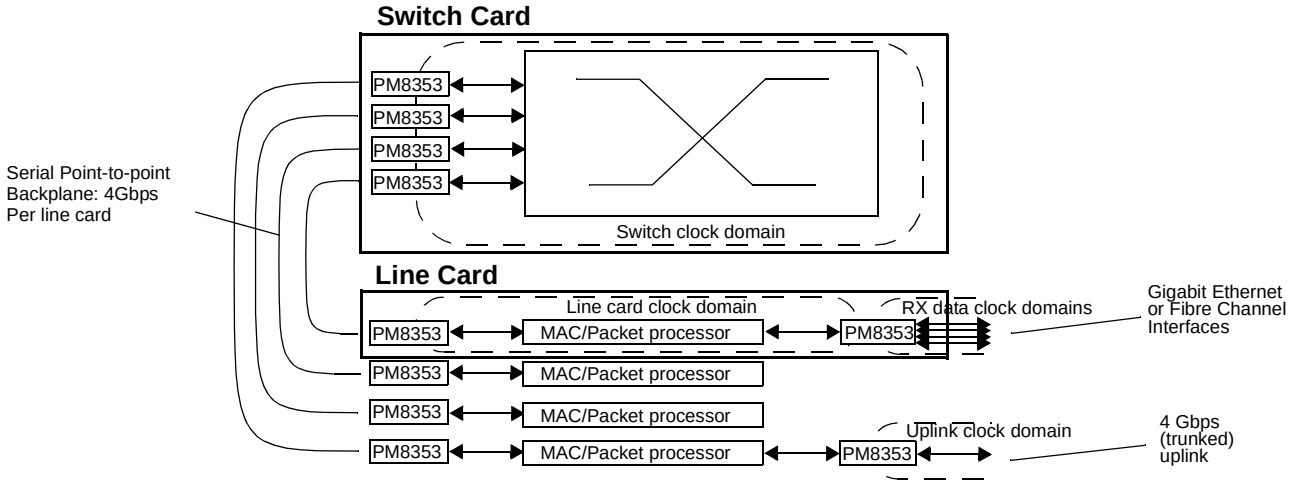
BLOCK DIAGRAM



4-Channel 1.0-1.25 Gbps Transceiver

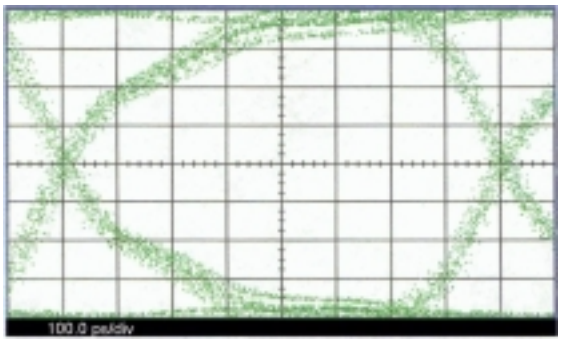
The QuadPHY creates a highly integrated and cost effective physical layer solution for Gigabit Ethernet or Fibre Channel external interfaces.

16 GBPS SWITCH APPLICATION



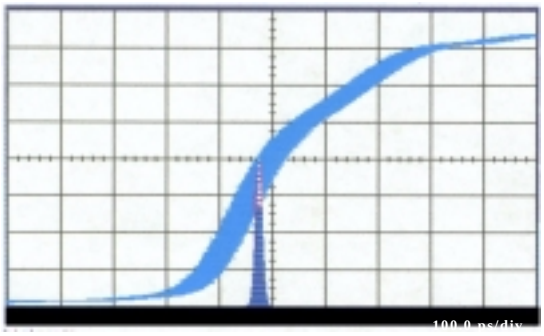
EYE DIAGRAM

Produced by the QuadPHY when driving a 50 Ohm cable, terminated at both near and far ends.



JITTER

Jitter histogram of the QuadPHY showing 6.8 picoseconds, 1 σ jitter with all channels operating.



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