

# PMBFJ620

Dual N-channel field-effect transistor

Rev. 01 — 11 May 2004

Product data sheet

## 1. Product profile

### 1.1 General description

Two N-channel symmetrical junction field-effect transistors in a SOT363 package.

#### CAUTION



This device is sensitive to electrostatic discharge (ESD). Therefore care should be taken during transport and handling.

### 1.2 Features

- Two field effect transistors in a single package
- Low noise
- Interchangeability of drain and source connections
- High gain.

### 1.3 Applications

- AM input stage in car radios
- VHF amplifiers
- Oscillators and mixers.

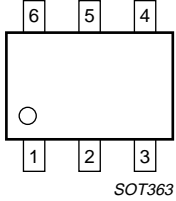
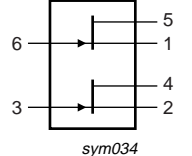
### 1.4 Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per FET</b>						
$V_{DS}$	drain-source voltage		-	-	$\pm 25$	V
$V_{GSoff}$	gate-source cut-off voltage	$V_{DS} = 10\text{ V}; I_D = 1\ \mu\text{A}$	-2	-	-6.5	V
$I_{DSS}$	drain current	$V_{GS} = 0\text{ V}; V_{DS} = 10\text{ V}$	24	-	60	mA
$P_{tot}$	total power dissipation	$T_s \leq 90\text{ }^\circ\text{C}$	-	-	190	mW
$ y_{fs} $	forward transfer admittance	$V_{DS} = 10\text{ V}; I_D = 10\text{ mA}$	10	-	-	mS

## 2. Pinning information

**Table 2: Discrete pinning information**

Pin	Description	Simplified outline	Symbol
1	source (1)	 <p style="text-align: center;">SOT363</p>	 <p style="text-align: center;">sym034</p>
2	source (2)		
3	gate (2)		
4	drain (2)		
5	drain (1)		
6	gate (1)		

## 3. Ordering information

**Table 3: Ordering information**

Type number	Package		
	Name	Description	Version
PMBFJ620	-	plastic surface mounted package; 6 leads	SOT363

## 4. Marking

**Table 4: Marking**

Type number	Marking code <sup>[1]</sup>
PMBFJ620	A8*

[1] \* = p: made in Hong Kong.  
 \* = t: made in Malaysia.  
 \* = W: made in China.

## 5. Limiting values

**Table 5: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

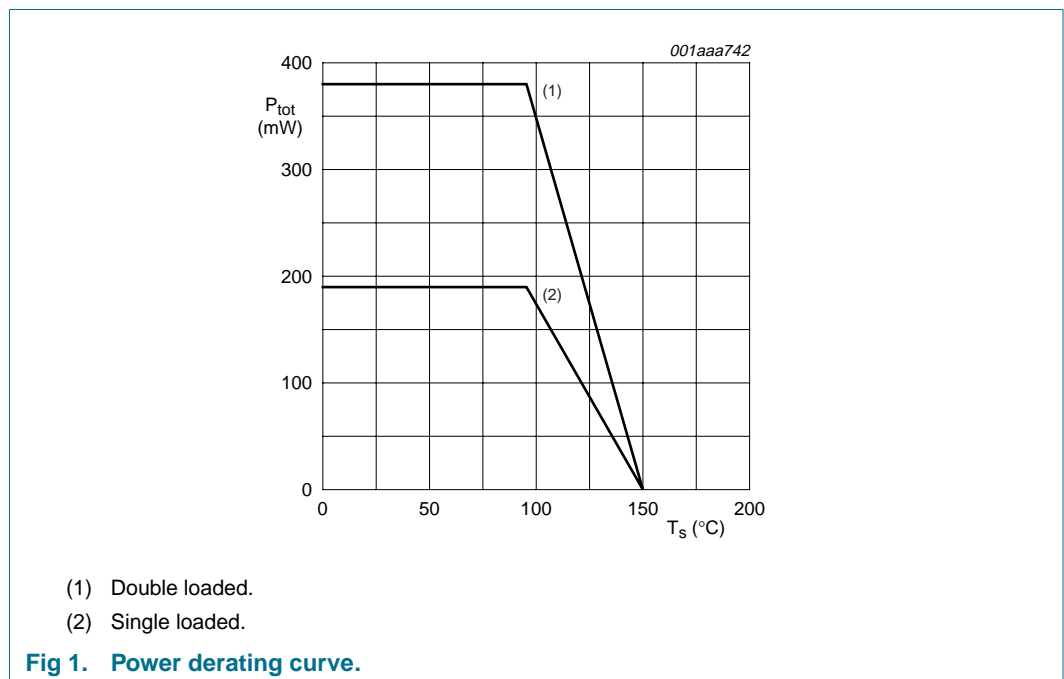
Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per FET</b>					
$V_{DS}$	drain-source voltage		-	$\pm 25$	V
$V_{GSO}$	gate-source voltage	open drain	-	-25	V
$V_{GDO}$	drain-gate voltage	open source	-	-25	V
$I_G$	forward gate current (DC)		-	50	mA
$P_{tot}$	total power dissipation	$T_s \leq 90\text{ }^\circ\text{C}$	-	190	mW
$T_{stg}$	storage temperature		-65	+150	$^\circ\text{C}$
$T_j$	junction temperature		-	150	$^\circ\text{C}$

## 6. Thermal characteristics

**Table 6: Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-s)}$	thermal resistance from junction to soldering points	single loaded	[1] 315	K/W
		double loaded	[1] 160	K/W

[1]  $T_s$  is the temperature at the soldering point of the gate pins, see [Figure 1](#).



## 7. Static characteristics

**Table 7: Characteristics**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

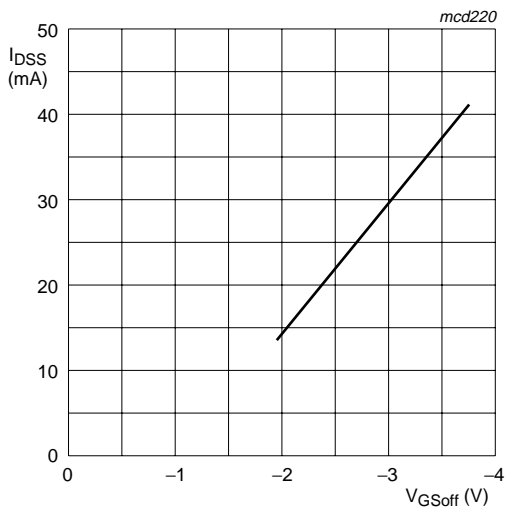
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per FET</b>						
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = -1\text{ }\mu\text{A}$ ; $V_{DS} = 0\text{ V}$	-25	-	-	V
$V_{GSoff}$	gate-source cut-off voltage	$I_D = 1\text{ }\mu\text{A}$ ; $V_{DS} = 10\text{ V}$	-2	-	-6.5	V
$V_{GSS}$	gate-source forward voltage	$I_G = 1\text{ mA}$ ; $V_{DS} = 0\text{ V}$	-	-	1	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 10\text{ V}$ ; $V_{GS} = 0\text{ V}$	24	-	60	mA
$I_{GSS}$	gate-source leakage current	$V_{GS} = -15\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	-1	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 100\text{ mV}$	-	50	-	$\Omega$
$ y_{fs} $	common source forward transfer admittance	$I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$	10	-	-	mS
$ y_{os} $	common source output admittance	$I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$	-	-	250	$\mu\text{S}$

## 8. Dynamic characteristics

**Table 8: Characteristics**

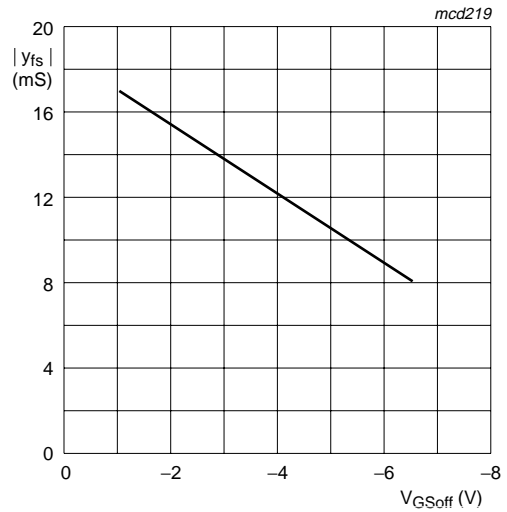
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per FET</b>						
$C_{iss}$	input capacitance	$V_{DS} = 10\text{ V}$ ; $V_{GS} = -10\text{ V}$ ; $f = 1\text{ MHz}$	-	3	5	pF
		$V_{DS} = 10\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	6	-	pF
$C_{rSS}$	reverse transfer capacitance	$V_{DS} = 0\text{ V}$ ; $V_{GS} = -10\text{ V}$ ; $f = 1\text{ MHz}$	-	1.3	2.5	pF
$g_{is}$	common source input conductance	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 100\text{ MHz}$	-	200	-	$\mu\text{S}$
		$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 450\text{ MHz}$	-	3	-	mS
$g_{fs}$	common source transfer conductance	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 100\text{ MHz}$	-	13	-	mS
		$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 450\text{ MHz}$	-	12	-	mS
$g_{rs}$	common source reverse conductance	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 100\text{ MHz}$	-	-30	-	$\mu\text{S}$
		$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 450\text{ MHz}$	-	-450	-	$\mu\text{S}$
$g_{os}$	common source output conductance	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 100\text{ MHz}$	-	150	-	$\mu\text{S}$
		$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 450\text{ MHz}$	-	400	-	$\mu\text{S}$
$V_n$	equivalent input noise voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ mA}$ ; $f = 100\text{ Hz}$	-	6	-	nV/ $\sqrt{\text{Hz}}$



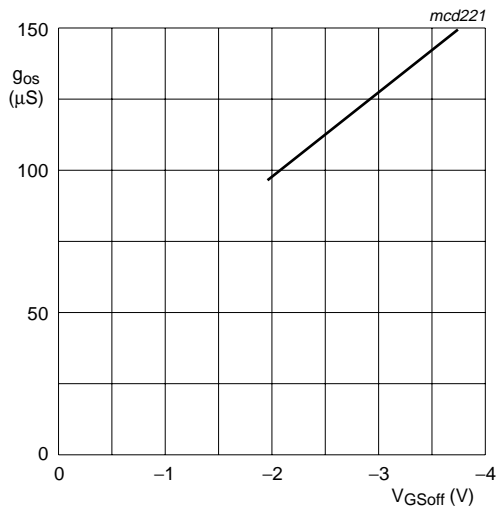
$V_{DS} = 10\text{ V}$ ;  $T_j = 25\text{ }^\circ\text{C}$ .

**Fig. 2.** Drain current as a function of gate-source cut-off voltage; typical values.



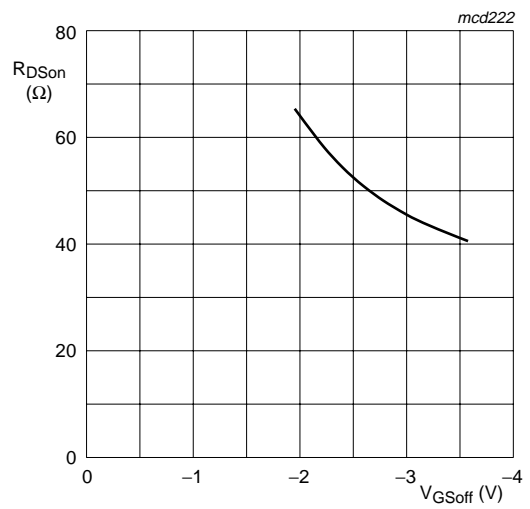
$V_{DS} = 10\text{ V}$ ;  $I_D = 10\text{ mA}$ ;  $T_j = 25\text{ }^\circ\text{C}$ .

**Fig. 3.** Common source forward transfer admittance as a function of gate-source cut-off voltage; typical values.



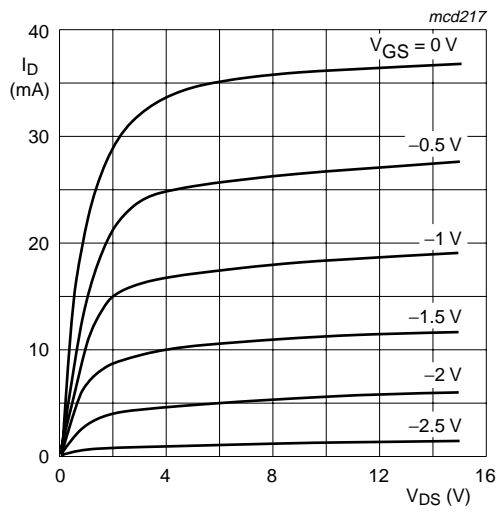
$V_{DS} = 10\text{ V}$ ;  $I_D = 10\text{ mA}$ ;  $T_j = 25\text{ }^\circ\text{C}$ .

**Fig. 4.** Common-source output conductance as a function of gate-source cut-off voltage; typical values.



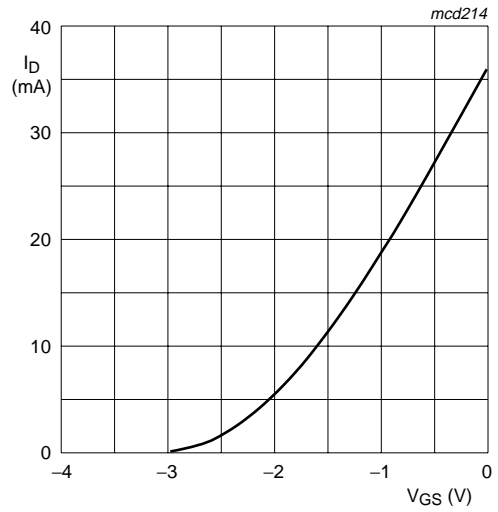
$V_{DS} = 100\text{ mV}$ ;  $V_{GS} = 0\text{ V}$ ;  $T_j = 25\text{ }^\circ\text{C}$ .

**Fig. 5.** Drain-source on-state resistance as a function of gate-source cut-off voltage; typical values.



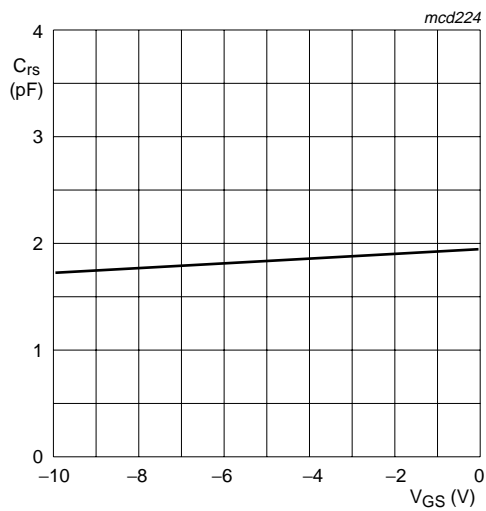
$T_j = 25\text{ }^\circ\text{C}$ .

Fig 6. Typical output characteristics.



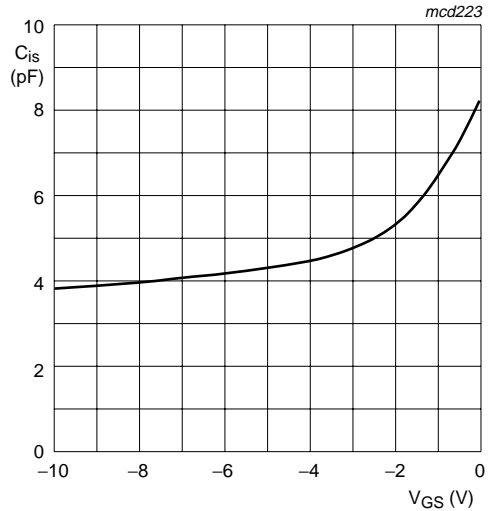
$V_{DS} = 10\text{ V}; T_j = 25\text{ }^\circ\text{C}$ .

Fig 7. Typical transfer characteristics.



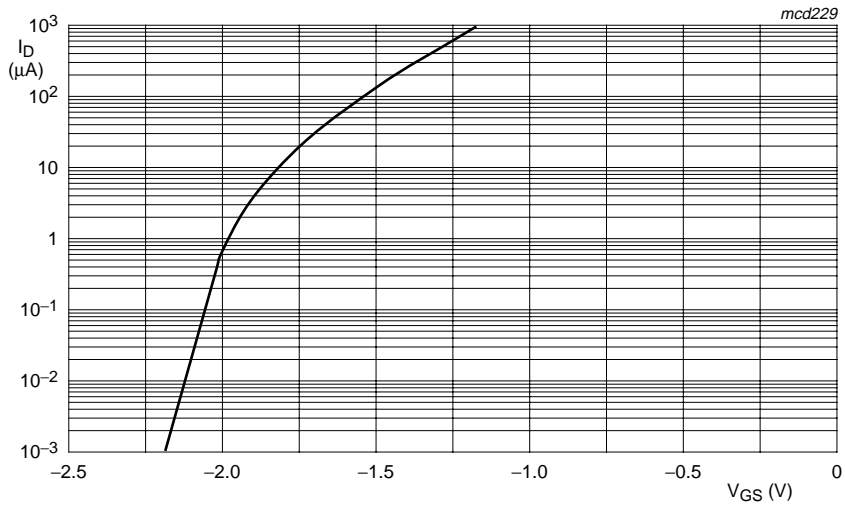
$V_{DS} = 10\text{ V}; T_j = 25\text{ }^\circ\text{C}$ .

Fig 8. Reverse transfer capacitance as a function of gate-source voltage; typical values.



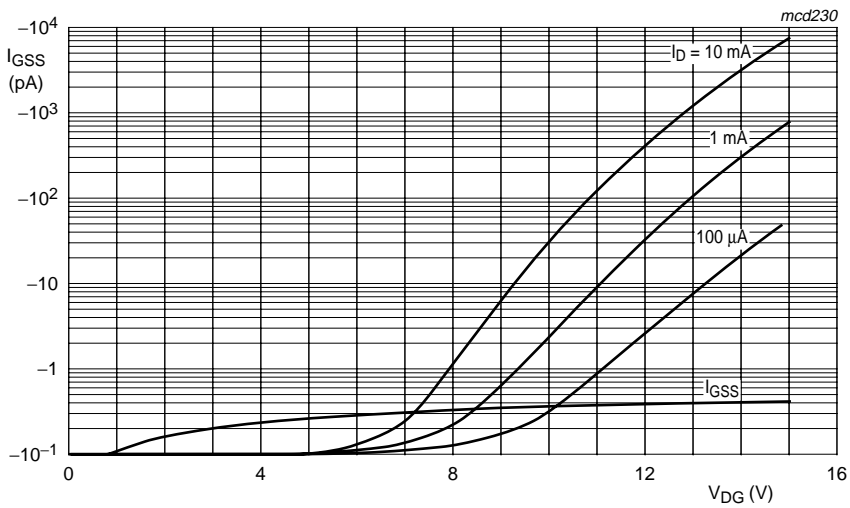
$V_{DS} = 10\text{ V}; T_j = 25\text{ }^\circ\text{C}$ .

Fig 9. Input capacitance as a function of gate-source voltage; typical values.



$V_{DS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}.$

**Fig 10. Drain current as a function of gate-source voltage; typical values.**



$T_j = 25 \text{ }^\circ\text{C}.$

**Fig 11. Gate current as a function of drain-gate voltage; typical values.**

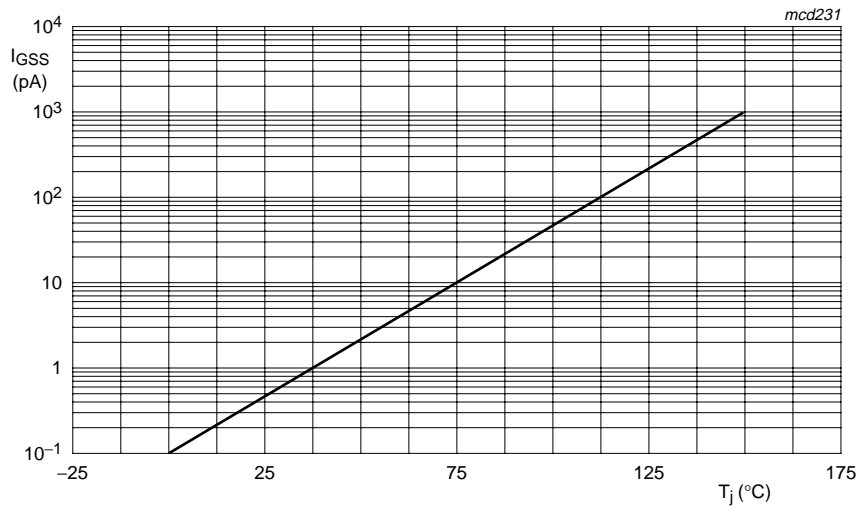
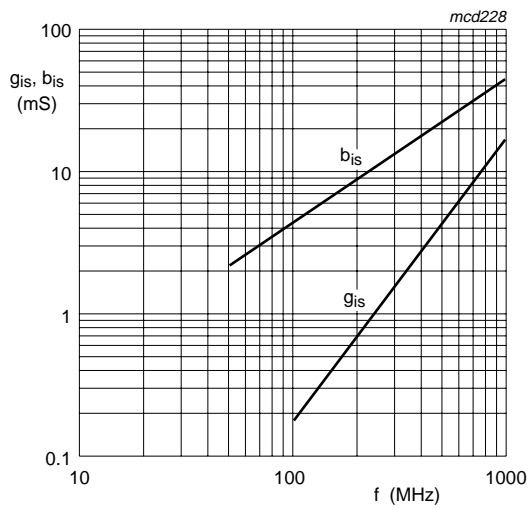


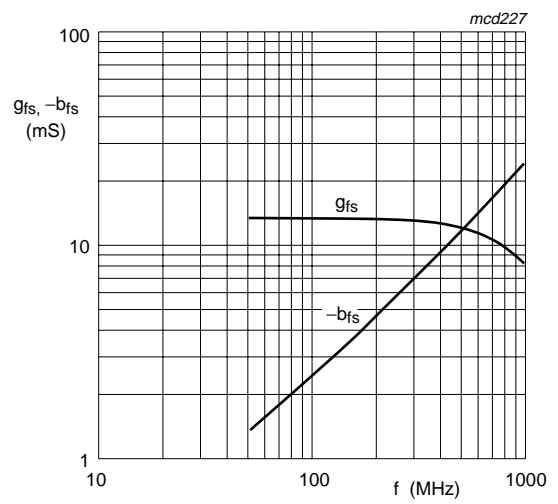
Fig 12. Gate current as a function of junction temperature; typical values.





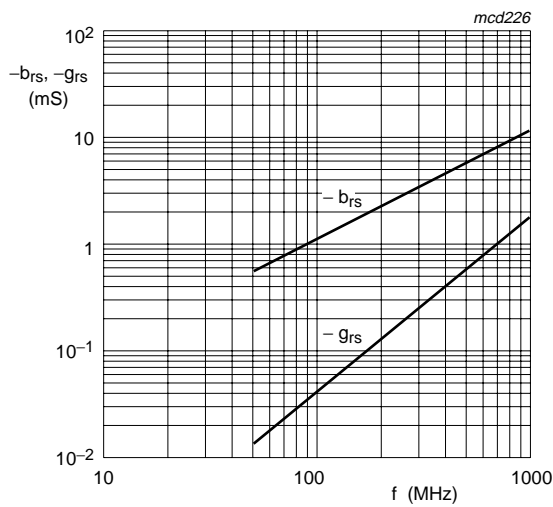
$V_{DS} = 10\text{ V}; I_D = 10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}.$

**Fig 13. Input admittance as a function of frequency; typical values.**



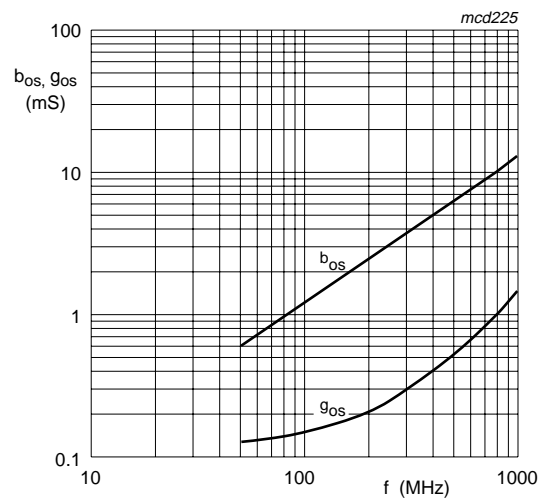
$V_{DS} = 10\text{ V}; I_D = 10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}.$

**Fig 14. Forward transfer admittance as a function of frequency; typical values.**



$V_{DS} = 10\text{ V}; I_D = 10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}.$

**Fig 15. Reverse transfer admittance as a function of frequency; typical values.**



$V_{DS} = 10\text{ V}; I_D = 10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}.$

**Fig 16. Output admittance as a function of frequency; typical values.**

**9. Package outline**

Plastic surface mounted package; 6 leads

SOT363

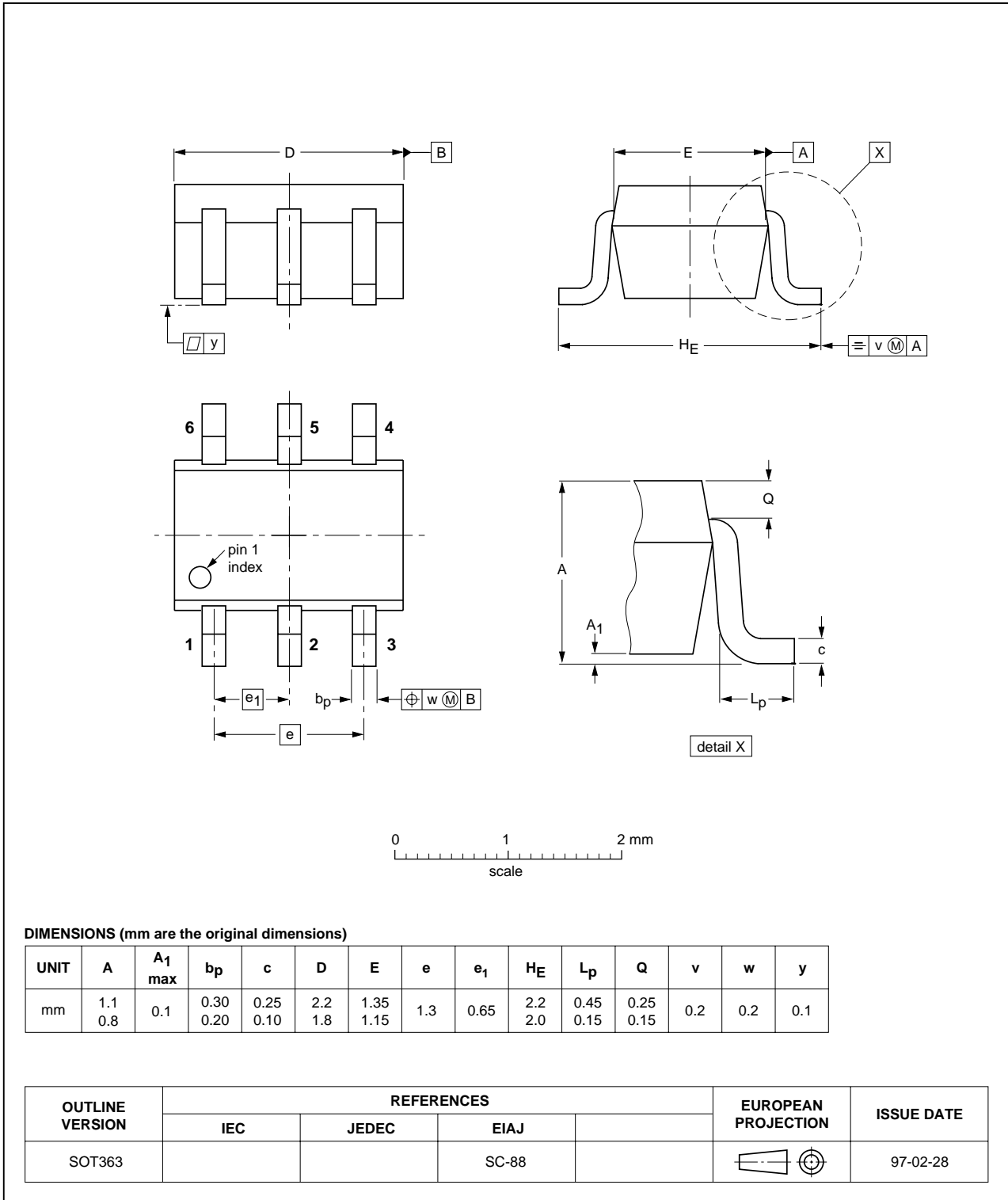


Fig 17. Package outline.



## 10. Revision history

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**Table 9: Revision history**

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
PMBFJ620_1	20040511	Product data	-	9397 750 13006	-

## 11. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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