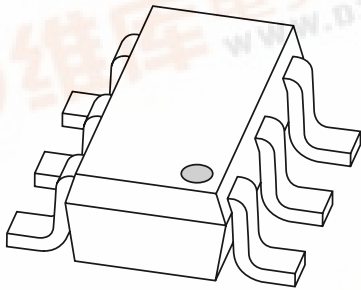


DISCRETE SEMICONDUCTORS

DATA SHEET



PMBT3904D NPN switching double transistor

Product specification

1999 Dec 15

NPN switching double transistor

PMBT3904D

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 40 V)
- Reduces number of components and board space.

APPLICATIONS

- Telephony and professional communication equipment.

DESCRIPTION

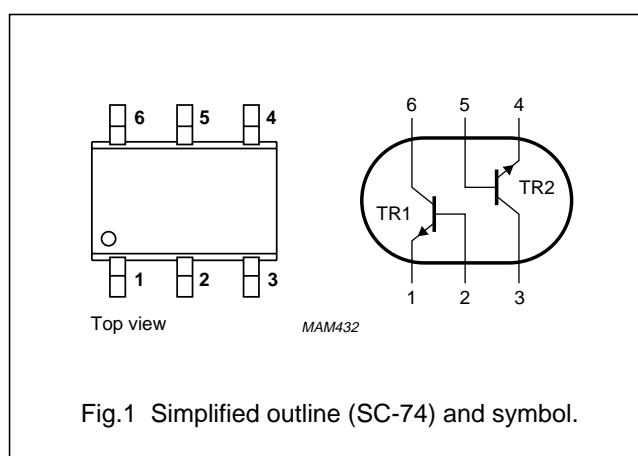
Two independently operating NPN switching transistors in a SC-74, six lead, SMD plastic package.

MARKING

TYPE NUMBER	MARKING CODE
PMBT3904D	D1

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	100	mA
I_{CM}	peak collector current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	600	mW

Note

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	208	K/W

Note

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

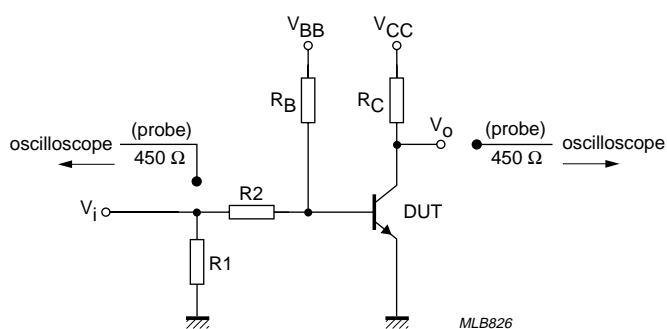
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = 30\text{ V}$	–	50	nA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = 6\text{ V}$	–	50	nA
h_{FE}	DC current gain	$V_{CE} = 1\text{ V}$; note 1; Fig.3 $I_C = 0.1\text{ mA}$ $I_C = 1\text{ mA}$ $I_C = 10\text{ mA}$ $I_C = 50\text{ mA}$ $I_C = 100\text{ mA}$	60 80 100 60 30	– – 300 – –	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 1\text{ mA}$	–	200	mV
		$I_C = 50\text{ mA}; I_B = 5\text{ mA}$	–	200	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 1\text{ mA}$	650	850	mV
		$I_C = 50\text{ mA}; I_B = 5\text{ mA}$	–	950	mV
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = 5\text{ V}; f = 1\text{ MHz}$	–	4	pF
C_e	emitter capacitance	$I_C = i_c = 0; V_{BE} = 500\text{ mV}; f = 1\text{ MHz}$	–	8	pF
f_T	transition frequency	$I_C = 10\text{ mA}; V_{CE} = 20\text{ V}; f = 100\text{ MHz}$	300	–	MHz
F	noise figure	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}; R_S = 1\text{ k}\Omega$; $f = 10\text{ Hz to }15.7\text{ kHz}$	–	5	dB
Switching times (between 10% and 90% levels); (see Fig.2)					
t_{on}	turn-on time	$I_{Con} = 10\text{ mA}; I_{Bon} = 1\text{ mA}; V_{CC} = 3\text{ V};$ $V_{BB} = -1.9\text{ V}$	–	65	ns
t_d	delay time		–	35	ns
t_r	rise time		–	35	ns
t_{off}	turn-off time		–	240	ns
t_s	storage time		–	200	ns
t_f	fall time		–	50	ns

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

NPN switching double transistor

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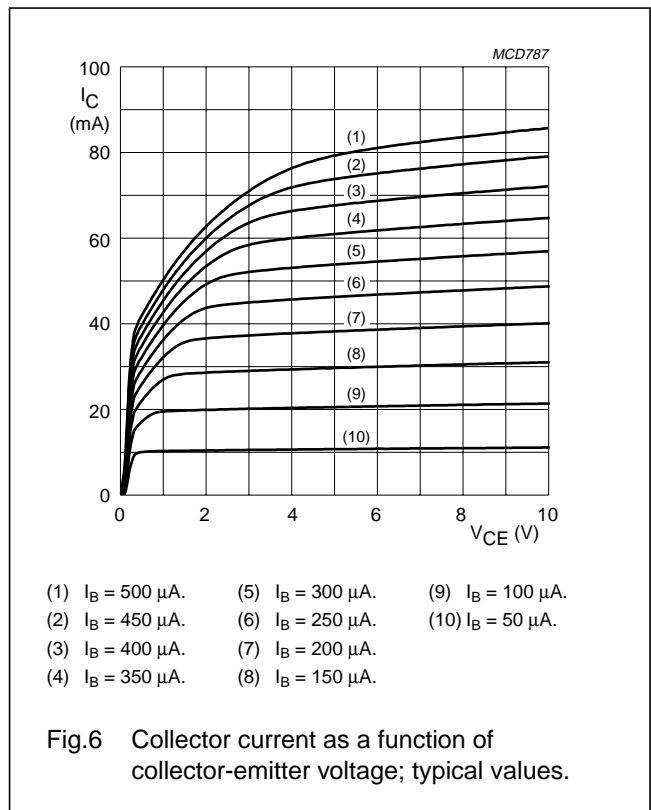
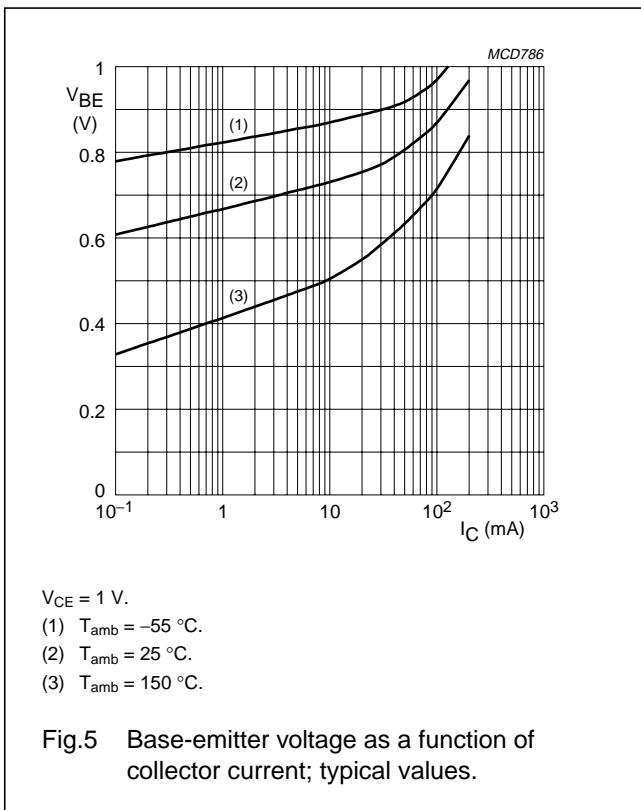
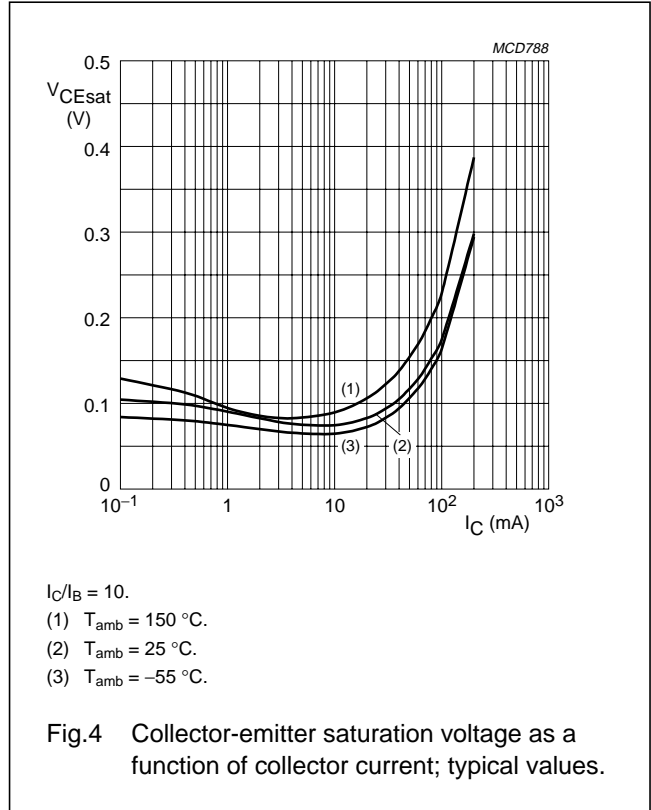
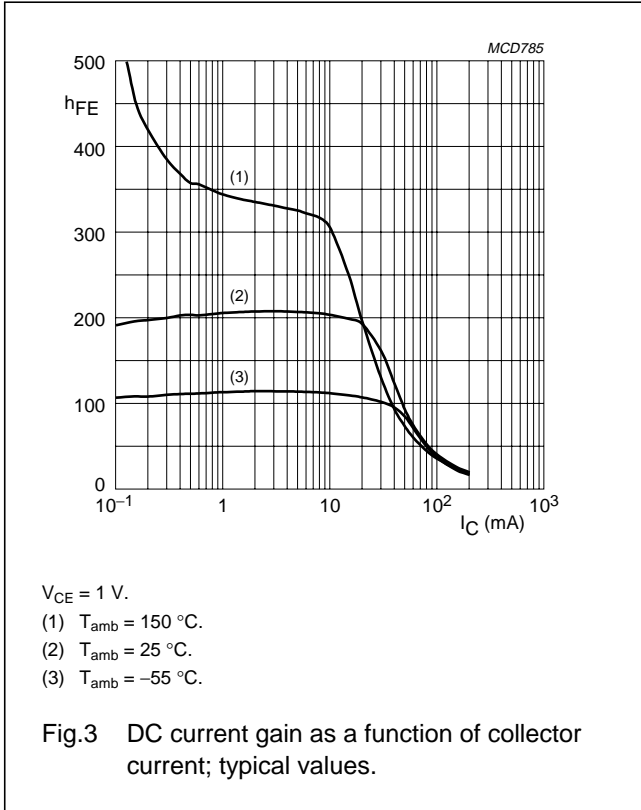


$V_i = 5 \text{ V}$; $T = 600 \mu\text{s}$; $t_p = 10 \mu\text{s}$; $t_r = t_f \leq 3 \text{ ns}$.
 $R_1 = 56 \Omega$; $R_2 = 2.5 \text{ k}\Omega$; $R_B = 3.9 \text{ k}\Omega$; $R_C = 270 \Omega$.
 $V_{BB} = -1.9 \text{ V}$; $V_{CC} = 3 \text{ V}$.
Oscilloscope: input impedance $Z_i = 50 \Omega$.

Fig.2 Test circuit for switching times.

NPN switching double transistor

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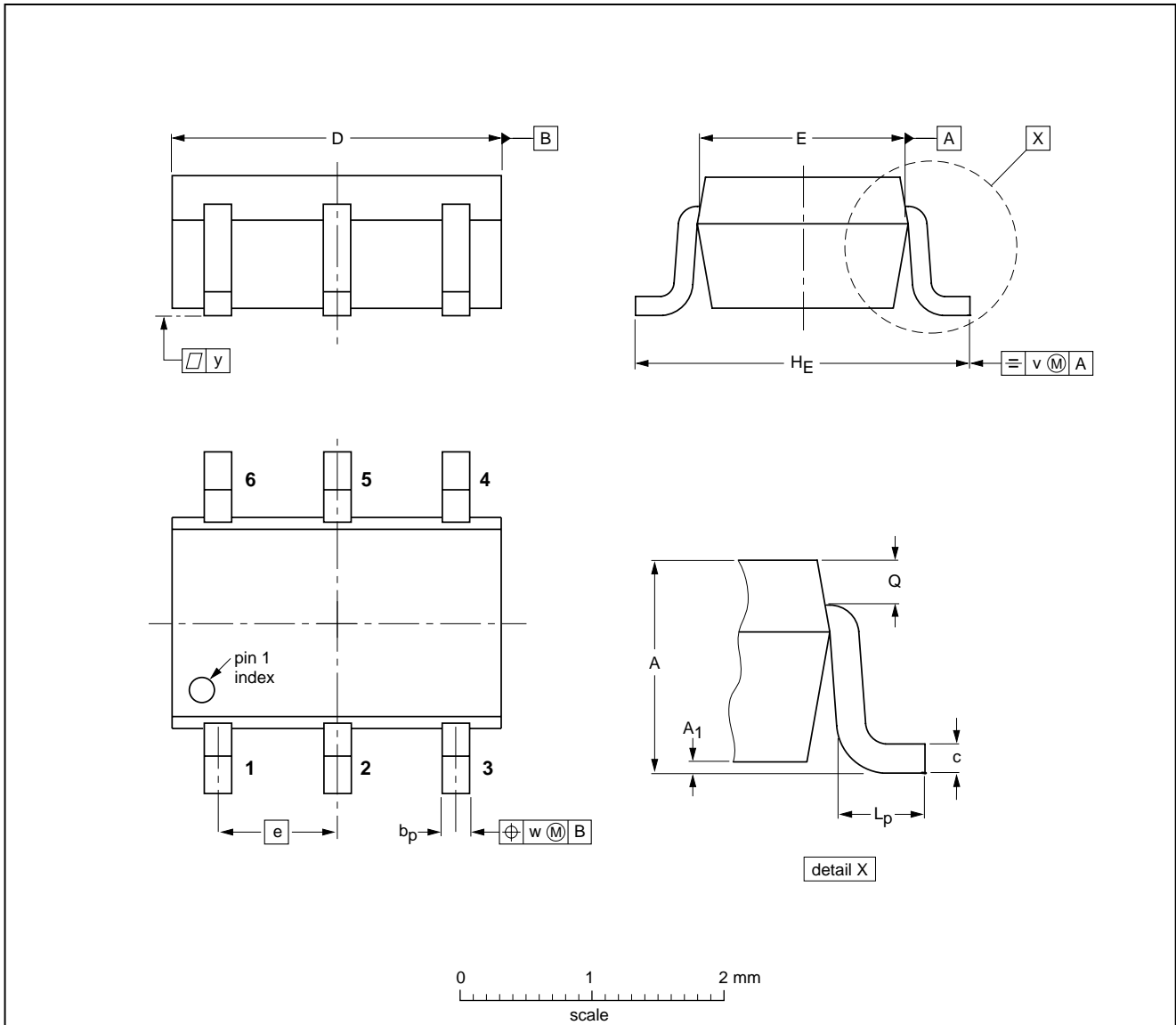
NPN switching double transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	bp	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			97-02-28

NPN switching double transistor

PMBT3904D

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

115002/01/pp8

Date of release: 1999 Dec 15

Document order number: 9397 750 06428

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