MITSUBISHI SEMICONDUCTOR <Application Specific Intelligent Power Module>

PS11012

FLAT-BASE TYPE
INSULATED TYPE

PS11012

INTEGRATED FUNCTIONS AND FEATURES

- Converter bridge for 3 phase AC-to-DC power conversion.
- Circuit for dynamic braking of motor regenerative energy.
- 3-phase IGBT inverter bridge configured by the latest 3rd. generation IGBT and diode technology.
- Inverter output current capability Io (Note 1):

Type Name	100% load	150% over load
PS11012	1.5A (rms)	2.25A (rms), 1min

(Note 1) : The inverter output current is assumed to be sinu-soidal and the peak current value of each of the above loading cases is defined as : $I_{OP} = I_O \times \sqrt{2}$
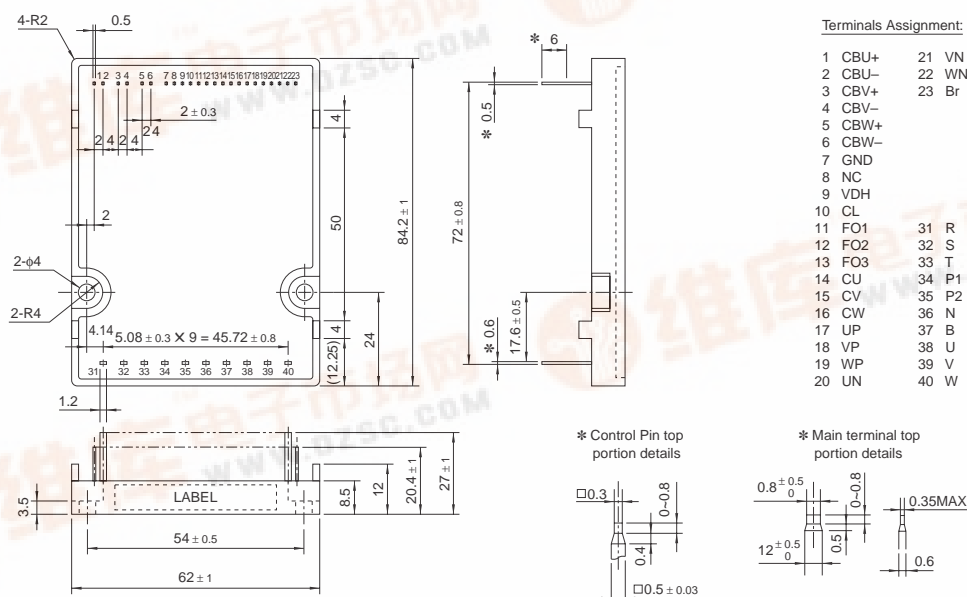
INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS:

- For inverter side upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Short circuit protection (SC).
  Bootstrap circuit supply scheme (single drive power supply) and Under voltage protection (UV).
- For inverter side lower-leg IGBTs : Drive circuit, Short circuit protection (SC).
  Control supply circuit under- & over- voltage protection (OV/UV).
  System over temperature protection (OT). Fault output signaling circuit (FO) and Current limit warning signal output (CL).
- For Brake circuit IGBT : Drive circuit
- Warning and Fault signaling :
  FO1 : Short circuit protection for lower-leg IGBTs and Input interlocking against spurious arm shoot-through.
  FO2 : N-side control supply abnormality locking (OV/UV).
  FO3 : System over-temperature protection (OT).
  CL : Warning for inverter current overload condition
- For system feedback control : Analogue signal feedback reproducing actual inverter output phase currents (3φ).
- Input Interface : 5V CMOS/TTL compatible, Schmitt trigger input, and Arm-Shoot-Through interlock protection.

APPLICATION

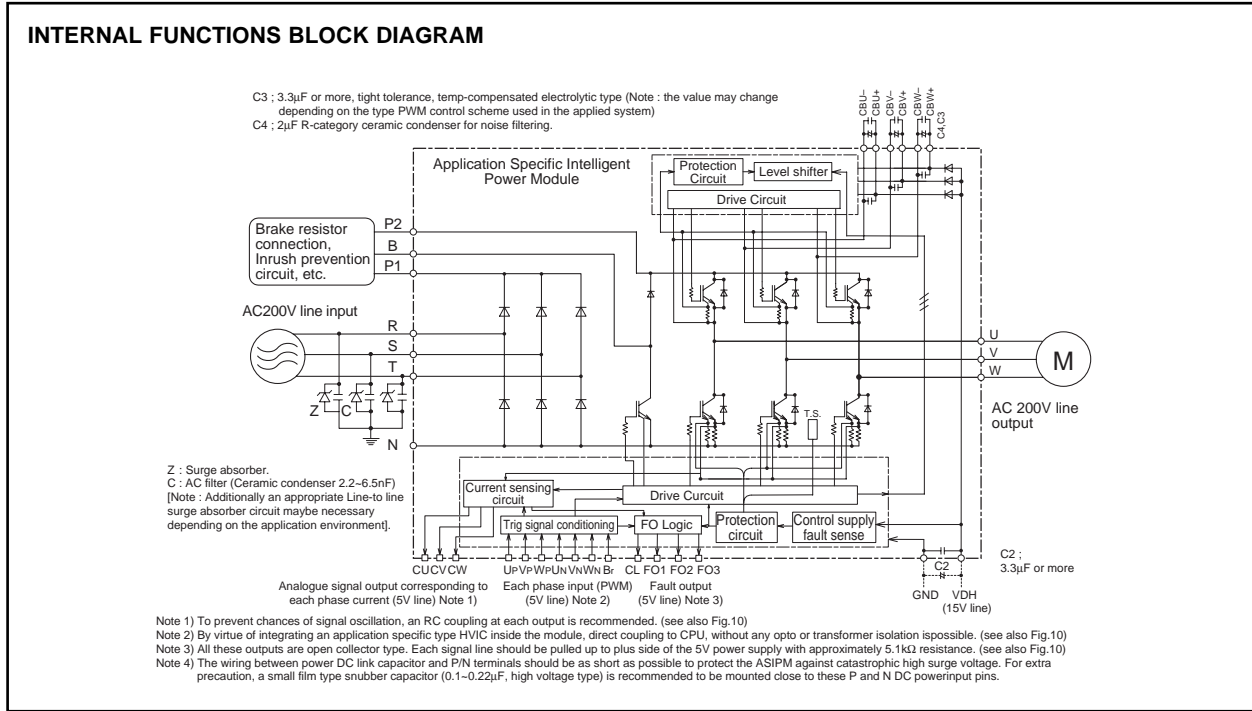Acoustic noise-less 0.2kW/AC200V class 3 phase inverter and other motor control applications

PACKAGE OUTLINES

Terminals Assignment:

1	CBU+	21	VN
2	CBU–	22	WN
3	CBV+	23	Br
4	CBV–		
5	CBW+		
6	CBW–		
7	GND		
8	NC		
9	VDH		
10	CL		
11	FO1	31	R
12	FO2	32	S
13	FO3	33	T
14	CU	34	P1
15	CV	35	P2
16	CW	36	N
17	UP	37	B
18	VP	38	U
19	WP	39	V
20	UN	40	W

✳ Control Pin top portion details

✳ Main terminal top portion details

(Fig. 1)

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INTERNAL FUNCTIONS BLOCK DIAGRAM

C3 ; 3.3μF or more, tight tolerance, temp-compensated electrolytic type (Note : the value may change depending on the type PWM control scheme used in the applied system)
C4 ; 2μF R-category ceramic condenser for noise filtering.

Application Specific Intelligent Power Module

Protection Circuit → Level shifter
Drive Circuit

Brake resistor connection, Inrush prevention circuit, etc.   P2 / B / P1

AC200V line input   R / S / T

U / V / W → M   AC 200V line output

Z : Surge absorber.
C : AC filter (Ceramic condenser 2.2~6.5nF)
[Note : Additionally an appropriate Line-to line surge absorber circuit maybe necessary depending on the application environment].

Current sensing circuit
Drive Cicruit
Trig signal conditioning — FO Logic — Protection circuit — Control supply fault sense

C2 ; 3.3μF or more

GND VDH (15V line)

CU CV CW
Analogue signal output corresponding to each phase current (5V line) Note 1)

UP VP WP UN VN WN Br
Each phase input (PWM) (5V line) Note 2)

CL FO1 FO2 FO3
Fault output (5V line) Note 3)

Note 1) To prevent chances of signal oscillation, an RC coupling at each output is recommended. (see also Fig.10)
Note 2) By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU, without any opto or transformer isolation ispossible. (see also Fig.10)
Note 3) All these outputs are open collector type. Each signal line should be pulled up to plus side of the 5V power supply with approximately 5.1kΩ resistance. (see also Fig.10)
Note 4) The wiring between power DC link capacitor and P/N terminals should be as short as possible to protect the ASIPM against catastrophic high surge voltage. For extra precaution, a small film type snubber capacitor (0.1~0.22μF, high voltage type) is recommended to be mounted close to these P and N DC powerinput pins.

(Fig. 2)

MAXIMUM RATINGS (Tj = 25°C)
INVERTER PART (Including Brake Part)

Symbol	Item	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P2-N	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P2-N, Surge-value	500	V
V_P or V_N	Each output IGBT collector-emitter static voltage	Applied between P-U, V, W, Br or U, V, W, Br-N	600	V
$V_{P(S)}$ or $V_{N(S)}$	Each output IGBT collector-emitter switching surge voltage	Applied between P-U, V, W, Br or U, V, W, Br-N	600	V
$\pm I_C (\pm I_{CP})$	Each output IGBT collector current	$T_C = 25°C$	$\pm 4 (\pm 8)$	A
$I_C (I_{CP})$	Brake IGBT collector current		2 (4)	A
$I_F (I_{FP})$	Brake diode anode current	Note: "( )" means I_C peak value	2 (4)	A

CONVERTER PART

Symbol	Item	Condition	Ratings	Unit
V_{RRM}	Repetitive peak reverse voltage		800	V
Ea	Recommended AC input voltage		220	V
I_O	DC output current	3φ rectifying circuit	25	A
I_{FSM}	Surge (non-repetitive) forward current	1 cycle at 60Hz, peak value non-repetitive	138	A
I^2t	I^2t for fusing	Value for one cycle of surge current	80	A^2s

CONTROL PART

Symbol	Item	Condition	Ratings	Unit
V_{DH}, V_{DB}	Supply voltage	Applied between V_{DH}-GND, C_{BU+}-C_{BU-}, C_{BV+}-C_{BV-}, C_{BW+}-C_{BW-}	20	V
V_{CIN}	Input signal voltage	Applied between $U_P \cdot V_P \cdot W_P \cdot U_N \cdot V_N \cdot W_N \cdot Br$-GND	$-0.5 \sim 7.5$	V
V_{FO}	Fault output supply voltage	Applied between $F_{O1} \cdot F_{O2} \cdot F_{O3}$-GND	$-0.5 \sim 7$	V
I_{FO}	Fault output current	Sink current of $F_{O1} \cdot F_{O2} \cdot F_{O3}$	15	mA
V_{CL}	Current-limit warning (CL) output voltage	Applied between CL-GND	$-0.5 \sim 7$	V
I_{CL}	CL output current	Sink current of CL	15	mA
I_{CO}	Analogue current signal output current	Sink current of $CU \cdot CV \cdot CW$	± 1	mA

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FLAT-BASE TYPE
INSULATED TYPE

TOTAL SYSTEM

Symbol	Item	Condition		Ratings	Unit
Tj	Junction temperature		(Note 2)	−20 ~ +125	°C
Tstg	Storage temperature	—		−40 ~ +125	°C
TC	Module case operating temperature		(Fig. 3)	−20 ~ +100	°C
Viso	Isolation voltage	60 Hz sinusoidal AC applied between all terminals and the base plate for 1 minute.		2500	Vrms
—	Mounting torque	Mounting screw: M3.5		0.78 ~ 1.27	kg·cm

Note 2) The item defines the maximum junction temperature for the power elements (IGBT/Diode) of the ASIPM to ensure safe operation. However, these power elements can endure junction temperature as high as 150°C instantaneously . To make use of this additional temperature allowance, a detailed study of the exact application conditions is required and, accordingly, necessary information is requested to be provided before use.

CASE TEMPERATURE MEASUREMENT POINT (3mm from the base surface)
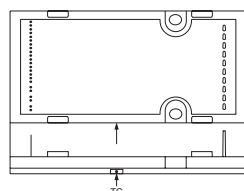
(Fig. 3)

THERMAL RESISTANCE

Symbol	Item	Condition	Ratings			Unit
			Min.	Typ.	Max.	
Rth(j-c)Q	Junction to case Thermal Resistance	Inverter IGBT (1/6)	—	—	6.1	°C/W
Rth(j-c)F		Inverter FWDi (1/6)	—	—	6.1	°C/W
Rth(j-c)QB		Brake IGBT	—	—	7.3	°C/W
Rth(j-c)FB		Brake FWDi	—	—	6.1	°C/W
Rth(j-c)FR		Converter Di (1/6)	—	—	4.8	°C/W
Rth(c-f)	Contact Thermal Resistance	Case to fin, thermal grease applied (1 Module)	—	—	0.053	°C/W

ELECTRICAL CHARACTERISTICS (Tj = 25°C, VDH = 15V, VDB = 15V unless otherwise noted)

Symbol	Item	Condition	Ratings			Unit
			Min.	Typ.	Max.	
VCE(sat)	Collector-emitter saturation voltage	VDH = VDB = 15V, Input = ON, Tj = 25°C, IC = 4A	—	—	2.9	V
VEC	FWDi forward voltage	Tj = 25°C, IC = −4A, Input = OFF	—	—	2.9	V
VCE(sat)Br	Brake IGBT Collector-emitter saturation voltage	VDH = 15V, Input = ON, Tj = 25°C, IC = 2A	—	—	3.5	V
VFBr	Brake diode forward voltage	Tj = 25°C, IF = 2A, Input = OFF	—	—	2.9	V
IRRM	Converter diode reverse current	VR = VRRM, Tj = 125°C	—	—	8	mA
VFR	Converter diode voltage	Tj = 25°C, IF = 5A	—	—	1.5	V
ton	Switching times	1/2 Bridge inductive load, Input = ON	0.3	0.6	1.5	μs
tc(on)		VCC = 300V, IC = 4A, Tj = 125°C	—	0.2	0.6	μs
toff		VDH = 15V, VDB = 15V	—	1.1	1.8	μs
tc(off)		Note : ton, toff include delay time of the internal control circuit	—	0.35	1.0	μs
trr	FWD reverse recovery time		—	0.1	—	μs
	Short circuit endurance (Output, Arm, and Load, Short Circuit Modes)	VCC ≤ 400V, Input = ON (one-shot) Tj = 125°C start 13.5V ≤ VDH = VDB ≤ 16.5V	• No destruction • FO output by protection operation			
	Switching SOA	VCC ≤ 400V, Tj ≤ 125°C, IC < IOL(CL) operation level, Input = ON 13.5V ≤ VDH = VDB ≤ 16.5V	• No destruction • No protecting operation • No FO output			

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ELECTRICAL CHARACTERISTICS (TJ = 25°C, VDH = 15V, VDB = 15V UNLESS OTHERWISE NOTED)

Symbol	Item	Condition		Min.	Typ.	Max.	Unit
IDH	Circuit current	VDH = 15V, VCIN = 5V		—	—	150	mA
Vth(on)	Input on threshold voltage			0.8	1.4	2.0	V
Vth(off)	Input off threshold voltage			2.5	3.0	4.0	V
Ri	Input pull-up resistor	Integrated between input terminal-VDH		—	150	—	kΩ
fPWM	PWM input frequency	Tc ≤ 100°C, Tj ≤ 125°C		2	—	20	kHz
txx	Allowable input on-pulse width	VDH = 15V, TC = −20°C ~ +100°C (Note 3)		1	—	500	µs
tdead	Allowable input signal dead time for blocking arm shoot-through	Relates to corresponding input (Except brake part) TC = −20°C ~ +100°C		2.2	—	—	µs
tint	Input inter-lock sensing	Relates to corresponding input (Except brake part)		—	65	100	ns
VCO	Analogue signal linearity with output current	Ic = 0A	VDH = 15V	1.87	2.27	2.57	V
VC+(200%)		Ic = IOP(200%)	TC = −20°C ~ +100°C	0.77	1.17	1.47	V
VC−(200%)		Ic = −IOP(200%)	(Fig. 4)	2.97	3.37	3.67	V
|ΔVCO|	Offset change area vs temperature	VDH = 15V, TC = −20°C ~ +100°C		—	15	—	mV
VC+	Analogue signal output voltage limit	Ic > IOP(200%), VDH = 15V		—	—	0.7	V
VC−		(Fig. 4)		4.0	—	—	V
ΔVC(200%)	Analogue signal over all linear variation	|VCO-VC±(200%)|		—	1.1	—	V
rCH	Analogue signal data hold accuracy	Correspond to max. 500µs data hold period only, Ic = IOP(200%) (Fig. 5)		−5	—	5	%
td(read)	Analogue signal reading time	After input signal trigger point (Fig. 8)		—	3	—	µs
±IOL	Current limit warning (CL) operation level	VDH =15V, TC = −20°C ~ +100°C (Note 4)		4.77	5.80	6.90	A
ICL(H)	Signal output current of CL operation	Idle	Open collector output	—	—	1	µA
ICL(L)		Active		—	1	—	mA
SC	Short circuit over current trip level	Tj = 25°C (Fig. 7) (Note 5)		6.95	12.0	19.2	A
OT	Over temperature protection	Trip level	VDH =15V	100	110	120	°C
OTr		Reset level		—	90	—	°C
UVDH	Supply circuit under & over voltage protection	Trip level	TC = −20°C ~ +100°C Tj ≤ 125°C	11.05	12.00	12.75	V
UVDHr		Reset level		11.55	12.50	13.25	V
OVDH		Trip level		18.00	19.20	20.15	V
OVDHr		Reset level		16.50	17.50	18.65	V
UVDB		Trip level		10.0	11.0	12.0	V
UVDBr		Reset level		10.5	11.5	12.5	V
tdV		Filter time		—	10	—	µs
IFO(H)	Fault output current	Idle	Open collector output	—	—	1	µA
IFO(L)		Active		—	1	—	mA

(Note 3) : (a) Allowable minimum input on-pulse width : This item applies to P-side circuit only.
(b) Allowable maximum input on-pulse width : This item applies to both P-side and N-side circuits excluding the brake circuit.

(Note4) : CL output : The "current limit warning (CL) operation circuit outputs warning signal whenever the arm current exceeds this limit. The circuit is reset automatically by the next input signal and thus, it operates on a pulse-by-pulse scheme.

(Note5) : The short circuit protection works instantaneously when a high short circuit current flows through an internal IGBT rising up momentarily. The protection function is, thus meant primarily to protect the ASIPM against short circuit distraction. Therefore, this function is not recommended to be used for any system load current regulation or any over load control as this might, cause a failure due to excessive temperature rise. Instead, the analogue current output feature or the over load warning feature (CL) should be appropriately used for such current regulation or over load control operation. In other words, the PWM signals to the ASIPM should be shut down, in principle, and not to be restarted before the junction temperature would recover to normal, as soon as a fault is feed back from its FO1 pin of the ASIPM indicating a short circuit situation.

RECOMMENDED CONDITIONS

Symbol	Item	Condition	Ratings	Unit
VCC	Supply voltage	Applied across P2-N terminals	400 (max.)	V
VDH, VDB	Control supply voltage	Applied between VDH-GND, CBU+-CBU−, CBV+-CBV−, CBW+-CBW−	15±1.5	V
ΔVDH, ΔVDB	Supply voltage ripple		±1 (max.)	V/µs
VCIN(on)	Input on voltage		0 ~ 0.3	V
VCIN(off)	Input off voltage		4.8 ~ 5.0	V
fPWM	PWM Input frequency	Using application circuit	2 ~ 20	kHz
tdead	Arm shoot-through blocking time	Using application circuit	2.2 (min.)	µs

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Fig. 4 OUTPUT CURRENT ANALOGUE SIGNALING LINEARITY

(Fig. 4)
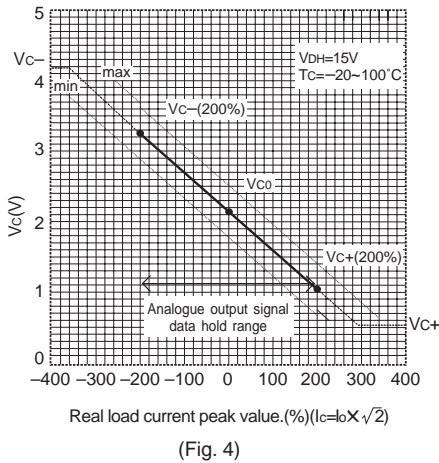
Fig. 5 OUTPUT CURRENT ANALOGUE SIGNALING "DATA HOLD" DEFINITION

$$r_{CH}= \frac{V_{CH}(505\mu s)-V_{CH}(5\mu s)}{V_{CH}(5\mu s)}$$
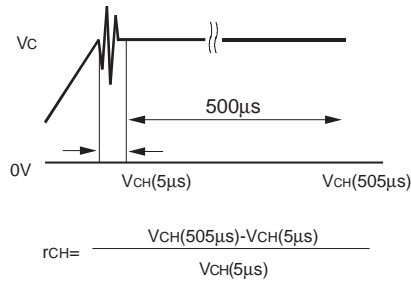
Note ; Ringing happens around the point where the signal output voltage changes state from "analogue" to "data hold" due to test circuit arrangement and instrumentational trouble. Therefore, the rate of change is measured at a 5 μs delayed point.

Fig. 6 INPUT INTERLOCK OPERATION TIMING CHART
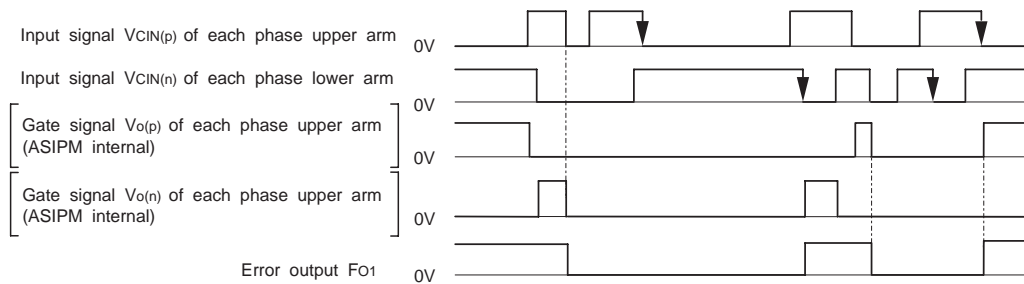
Note : Input interlock protection circuit ; It is operated when the input signals for any upper-arm / lower-arm pair of a phase are simultaneously in "LOW" level.

By this interlocking, both upper and lower IGBTs of this mal-triggered phase are cut off, and "Fo" signal is outputted. After an "input interlock" operation the circuit is latched. The "Fo" is reset by the high-to-low going edge of either an upper-leg, or a lower-leg input, whichever comes in later.

Fig. 7 TIMING CHART AND SHORT CIRCUIT PROTECTION OPERATION
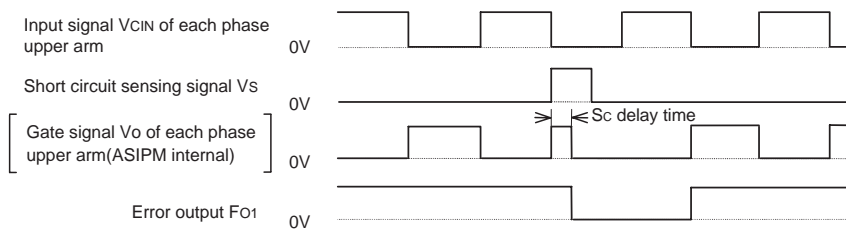
Note : Short circuit protection operation. The protection operates with "Fo" flag and reset on a pulse-by-pulse scheme. The protection by gate shutdown is given only to the IGBT that senses an overload (excluding the IGBT for the "Brake").

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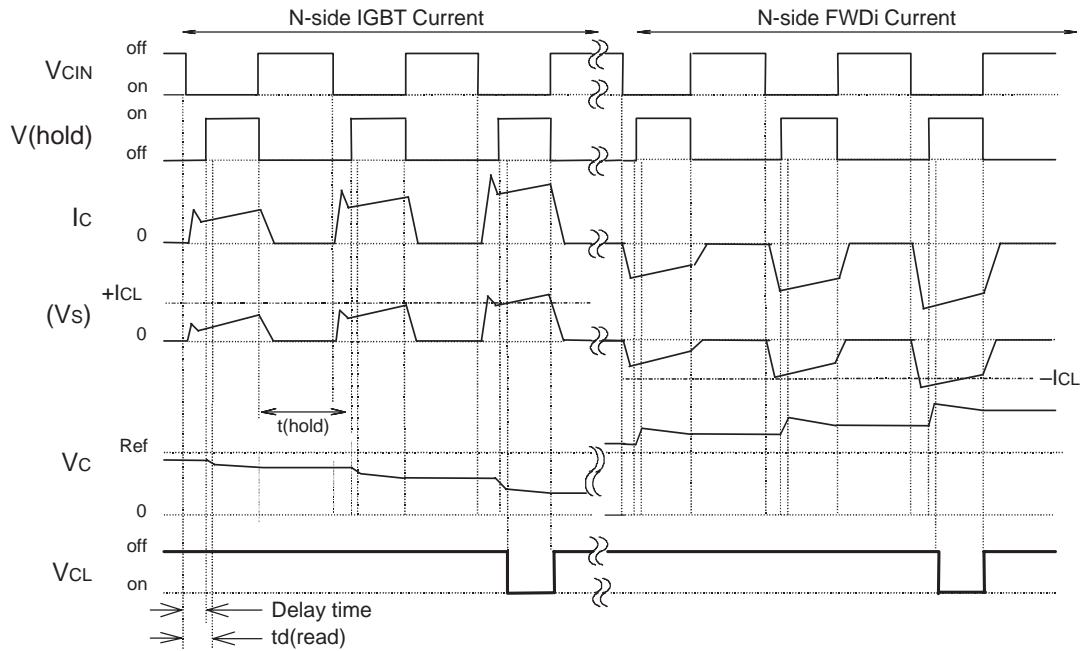## Fig. 8 INVERTER OUTPUT ANALOGUE CURRENT SENSING AND SIGNALING CHART

Fig. 9 START-UP SEQUENCE

Normally at start-up, Fo and CL output signals will be pulled-up High to Supply voltage (OFF level); however, F$_{O1}$ output may fall to Low (ON) level at the instant of the first ON input pulse to an N-Side IGBT. This can happen particularly when the boot-strap capacitor is of large size. F$_{O1}$ resetting sequence (together with the boot-strap charging sequence) is explained in the following graph

Fig. 10 RECOMMENDED I/O INTERFACE CIRCUIT
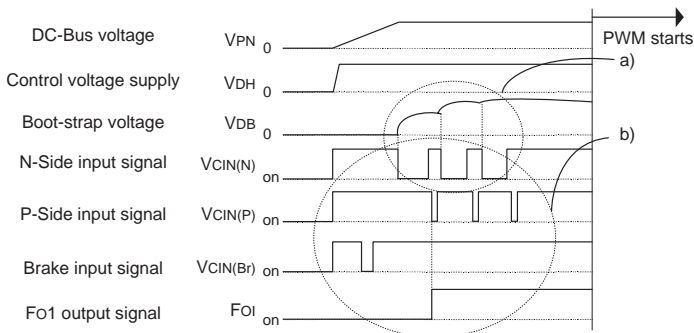
a) Boot-strap charging scheme :
Apply a train of short ON pulses at all N-IGBT input pins for adequate charging (pulse width = approx. 20µs number of pulses =10 ~ 500 depending on the boot-strap capacitor size)

b) F$_{O1}$ resetting sequence:
Apply ON signals to the following input pins : Br → Un/Vn/Wn → Up/Vp/Wp in that order.

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