SIEMENS

ICs for Communications

Analog Line Interface Solution
ALIS

PSB 4595 Version 2.1

PSB 4596 Version 2.1

Data Sheet 06.98

DS 1

ALIS **Revision History:**		**Current Version: 06.98**
Previous Version:		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

Edition 06.98

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
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1 Overview

The PSB 4595 and PSB 4596 two-chip solution forms the complete front end of a modem or fax machine. This Analog Line Interface Solution (ALIS) consists of a DAA, a codec and a hybrid circuit, and bridges the gap between the phone line and the data pump. The analog PSB 4595 is manufactured in low-power BiCMOS technology and the digital PSB 4596 in CMOS technology. The ALIS concept is a fully programmable modem front end which allows a single design for the worldwide market:

- Adaptation to specific countries and applications is achieved by downloading appropriate coefficient sets.
- Isolation is achieved by a digital capacitor interface, without a transformer; making the ALIS particularly suitable for designing PCMCIA modems.
- Thanks to an advanced digital-filter concept in combination with the programmable electronic DAA, ALIS provides both excellent transmission performance and high adaptability. This second-generation digital filter concept also allows maximum autonomy between the various filter blocks. This performance makes ALIS suitable for V.34+ and V.90 modem applications.

A minimum number of external components is required to complete the functional range of ALIS. Its internal precision is based on a very accurate band-gap reference. The frequency behavior is determined largely by digital filters which exhibit no fluctuations. As a result of the ADC and DAC concepts, its linearity is limited only by second-order parasitic effects.

The ALIS chip set can be easily adapted and connected to various modem data pumps or to host-based modem solutions. The flexible digital interface of ALIS allows easy programming via the modem data pump or a controller.

Siemens offers a range of reference and evaluation tools for the ALIS chip set. For appropriate tools, please contact your nearest Siemens representative.

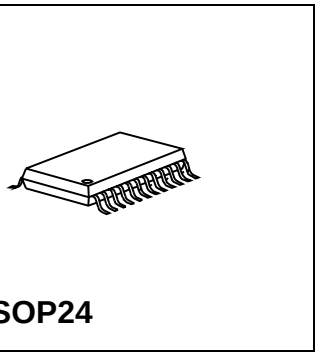
SIEMENS

Analog Line Interface Solution
ALIS

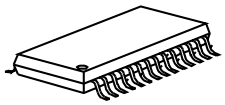
PSB 4595
PSB 4596

CMOS

1.1 Features



P-TSSOP24



P-SSOP28

- ALIS substitutes data access arrangement (DAA), codec and hybrid
- Ring detection: level, frequency and cadence
- Caller ID: detection, decoding and storage
- Programmable to different country requirements
- Programmable DC characteristics
- ALIS supports V.34+ and V.90
- ALIS complies with ETS 300 001 and FCC requirements
- Isolation by digital capacitor interface
- Analog part powered from the tip/ring line by an integrated voltage regulator
- High performance analog-to-digital and digital-to-analog conversion
- DSP-based solution for adapting the transmission behavior, especially for

- AC impedance matching
- trans-hybrid balancing
- frequency response
- gain

- Advanced test capabilities:

- digital loops
- analog loops

- High-pass filter in receive path to suppress line interference (50/60 Hz)
- Isolated control pins for general purpose use
- Advanced low-power 0.8µm analog BICMOS technology for ALIS analog and 0.8µm CMOS technology for ALIS digital
- Two-chip solution: the P-TSSOP24 and P-SSOP28 packages are PCMCIA-compliant

Type	Ordering Code	Package
PSB 4595 V2.1		P-TSSOP24
PSB 4596 V2.1		P-SSOP28

1.2 Logic Symbol

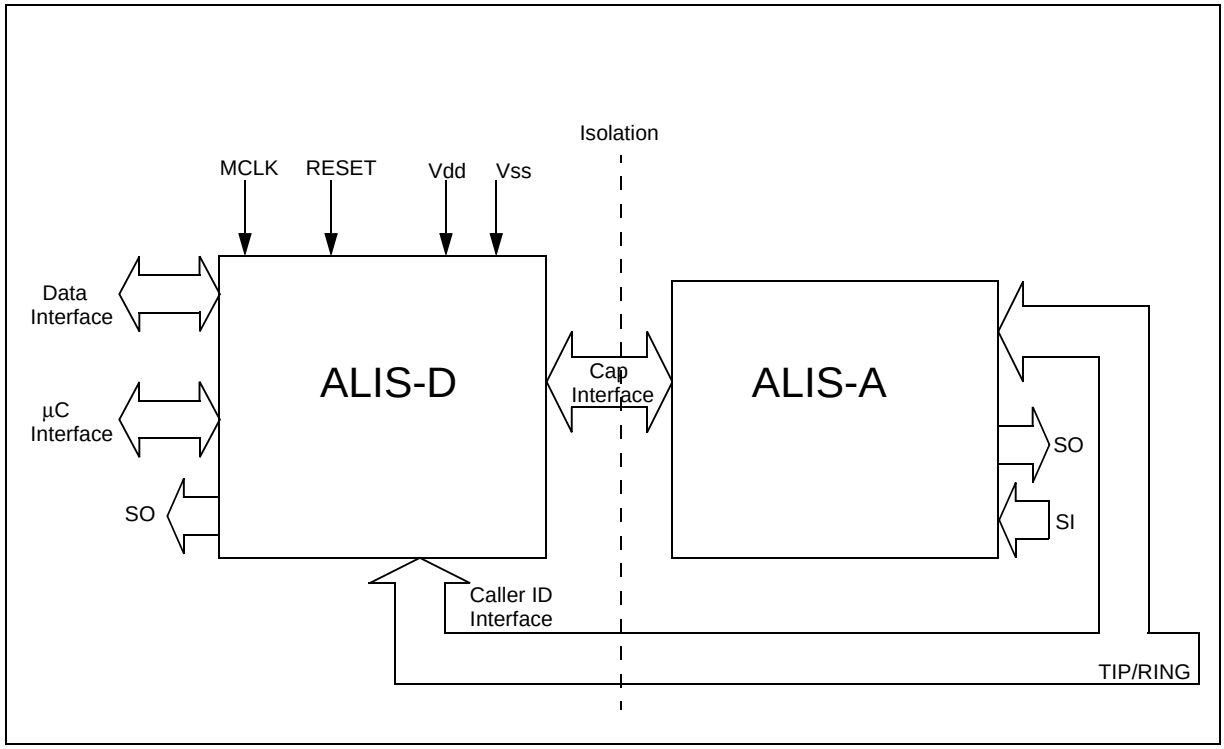


Figure 1 Logic Symbol of the ALIS Chipset

2 Pin Definition and Functions

2.1 Pin Configuration

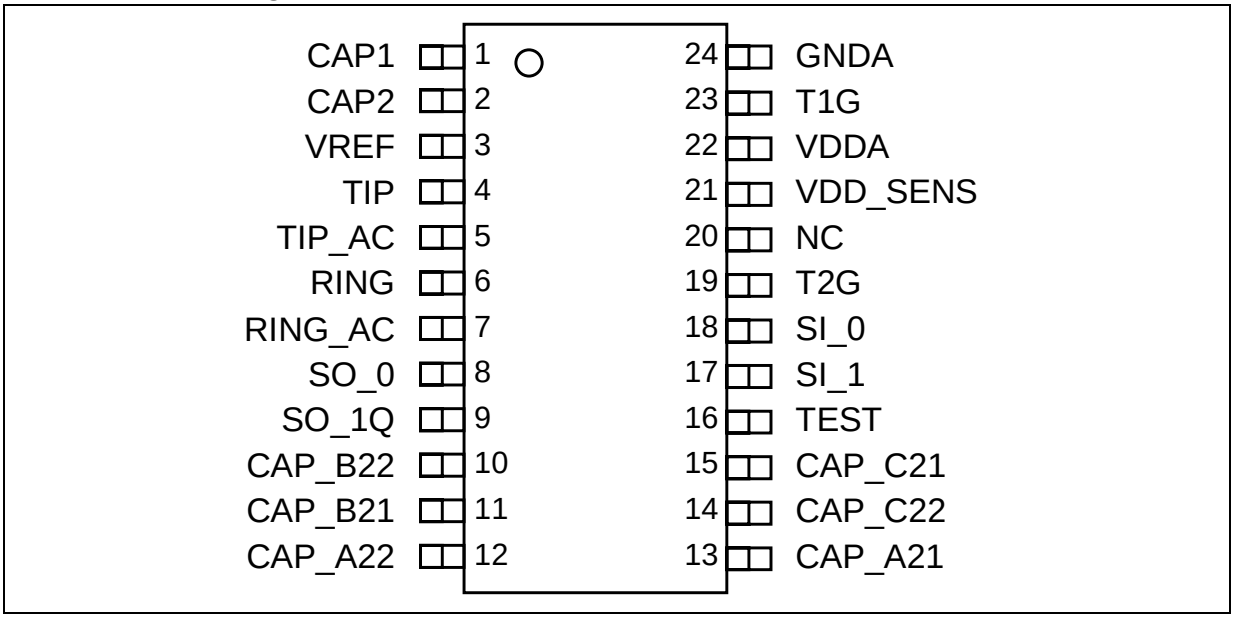


Figure 2 Pin Configuration of ALIS-A (Top View)

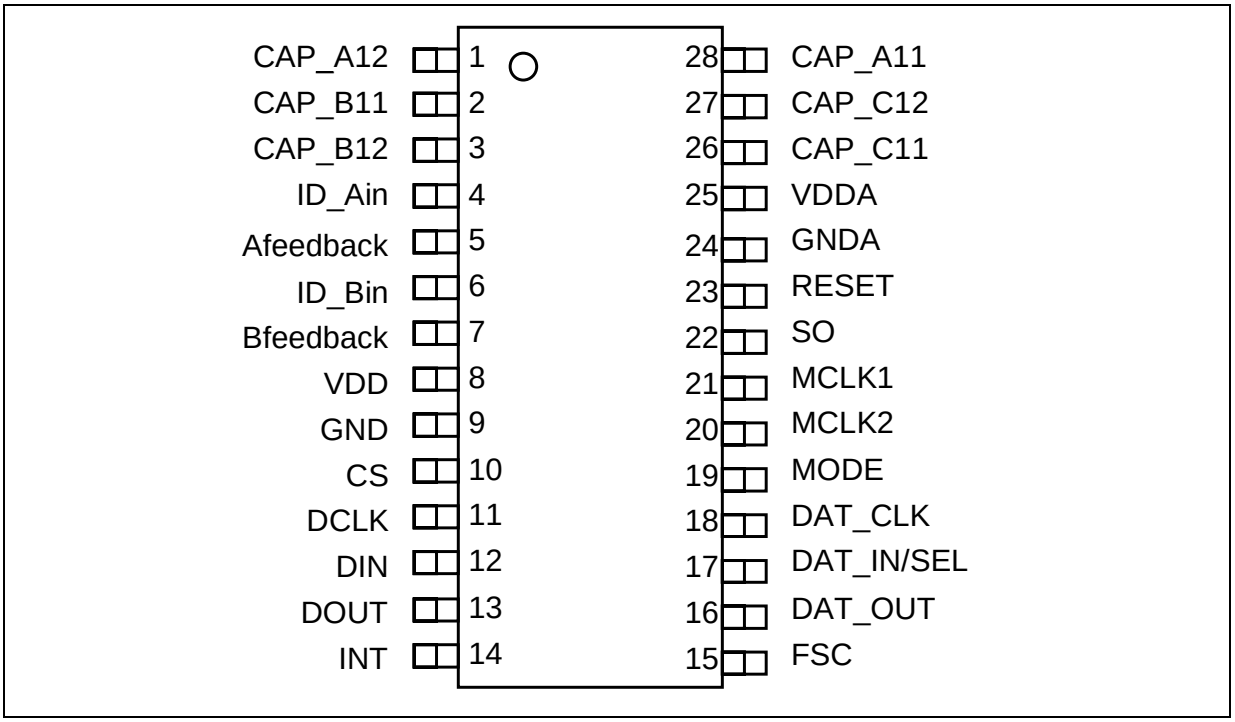


Figure 3 Pin Configuration of ALIS-D (Top View)

2.2 Pin Definition of ALIS-A PSB 4595

Pin No.	Symbol	Function	Descriptions
22	VDDA	Power	Programmable supply for the circuitry
24	GNDA	Power	Analog ground: All signals are referred to this pin
4	TIP	I	TIP AC+DC sense input
5	TIP_AC	I	TIP AC sense input
6	RING	I	RING AC+DC sense input
7	RING_AC	I	RING AC sense input
23	T1G	O	Gate for external transistor T1 (AC/DC control)
19	T2G	O	Gate for external transistor T2 (VDDA control)
21	VDD_SENS	I	VDDA sense input
3	VREF	I/O	Reference voltage: Must be connected to GNDA via an external capacitor of more than 10 nF (typ. 15 nF)
1	CAP1	I/O	Pin for external capacitor of more than 1 µF for DC filtering to pin Cap2
2	CAP2	I/O	See Cap1
18	SI_0	I	Auxiliary input pin 0
17	SI_1	I	Auxiliary input pin 1
8	SO_0	O	Auxiliary output pin 0
9	SO_1Q	O	Auxiliary output pin 1
16	TEST	I	Must be connected permanently to GNDA
13	CAP_A21	I	Must be connected via a capacitor of more than 5pF to CAP_A11.
12	CAP_A22	I	Must be connected via a capacitor of more than 5pF to CAP_A12.
11	CAP_B21	O	Must be connected via a capacitor of more than 5pF to CAP_B11.
10	CAP_B22	O	Must be connected via a capacitor of more than 5pF to CAP_B12.

Pin No.	Symbol	Function	Descriptions
15	CAP_C21	I	Must be connected via a capacitor of more than 5pF to CAP_C11.
14	CAP_C22	I	Must be connected via a capacitor of more than 5pF to CAP_C12.

Table 1: ALIS-A Pin Definition

2.3 Pin Definition of ALIS-D PSB 4596

Pin No.	Symbol	Function	Description
8	VDD	Power	+5 Volt supply for the digital circuitry
9	GND	Power	Ground digital: All signals are referred to this pin
25	VDDA	Power	+5 Volt supply for the analog circuitry
24	GNDA	Power	Ground analog: All analog signals are referred to this pin
21	MCLK1	I	Master clock1: One pin of a crystal or ceramic resonator is connected. This pin can also be driven from an external clocking source of 16.384 MHz, synchronous to FSC (MCLK=FSC*2048)
20	MCLK2	O	Master clock2: The other pin of a crystal or ceramic resonator is connected. When MCLK1 is driven by an external clock, this pin should be left open
23	RESET	I	Reset input: Forces the device to default mode (low active)
15	FSC	BI	As input: Frame synchronisation clock, 8kHz, identifies the beginning of the frame. FSC must be synchronous to MCLK (MCLK=FSC*2048) As Output: Indicates the beginning of a new frame
17	DAT_IN / SEL	I	Data interface: Receive data from the DSP. The data is received in 16-bit bursts every 125 ms. Interface selection pin in MUX mode.
16	DAT_OUT	O	Data interface: Transmit data to the DSP. The data is transmitted in 16-bit bursts every 125 ms
18	DAT_CLK	I	Data clock 128 to 1024 kHz: Determines the rate at which data is shifted into or out of the data interface
10	CS	I	µ-controller interface: Chip select enable to read or write data. Active low

Pin No.	Symbol	Function	Description
11	DCLK	I	µ-controller interface: Clock. Maximum clock rate 1024 kHz
12	DIN	I	µ-controller interface: Input data
13	DOUT	TRI	µ-controller interface: DOUT is high 'Z' if no data is transmitted
14	INT	O	µ-controller interface: Interrupt output pin
19	MODE	I	Interface mode pin (parallel or MUX mode)
4	ID_Ain	I	Input for caller ID comparator (connection to TIP)
6	ID_Bin	I	Input for caller ID comparator (connection to RING)
5	A feedback	O	Feedback for caller ID comparator
7	B feedback	O	Feedback for caller ID comparator
28	CAP_A11	O	Must be connected via a capacitor of more than 5pF to CAP_A21.
1	CAP_A12	O	Must be connected via a capacitor of more than 5pF to CAP_A22.
2	CAP_B11	I	Must be connected via a capacitor of more than 5pF to CAP_B21.
3	CAP_B12	I	Must be connected via a capacitor of more than 5pF to CAP_B22.
26	CAP_C11	O	Must be connected via a capacitor of more than 5pF to CAP_C21.
27	CAP_C12	O	Must be connected via a capacitor of more than 5pF to CAP_C22.
22	SO	O	Auxiliary output pin

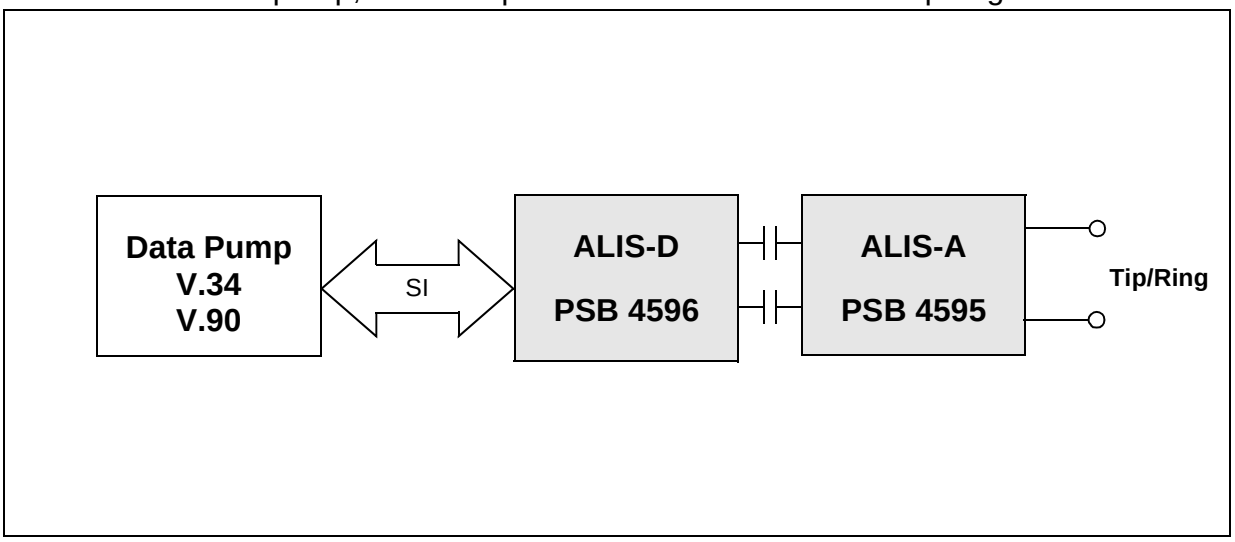
Table 2: ALIS-D Pin Definition

3 System Integration

ALIS can be used in different modem applications to connect the data pump to the TIP/ RING wire.

3.1 ALIS with DSP-based Modem

For a modem data pump, the ALIS provides the front-end to the tip/ring.



Note: SI: Serial Interface

Figure 4 DSP-based Modem Application

Isolation is provided by a capacitor interface, without transformer. This allows very flat frequency response over the entire voice band, even at low frequencies.

In V.90 Modem applications, the 50/60 Hz high-pass filter can be turned off.

3.2 ALIS with Software Modem

ALIS also supports software modems where V.34 runs on the host computer (e.g. in combination with a USB controller).

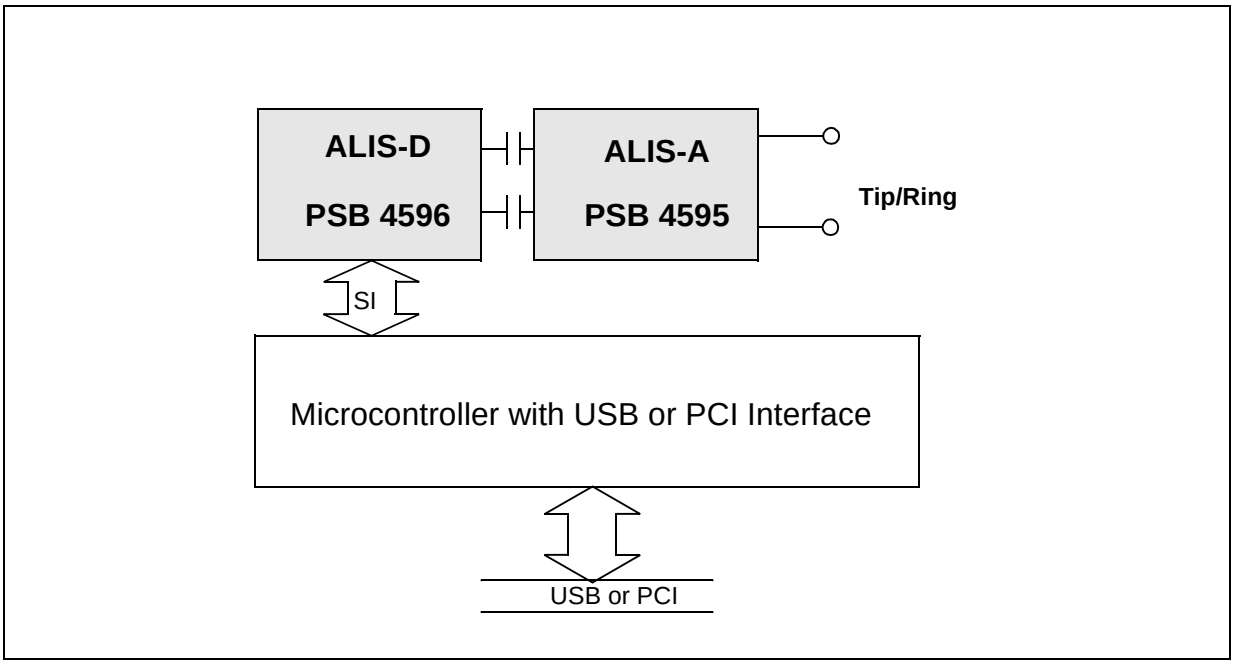


Figure 5 Software Modem Application

3.3 Hybrid Modem (ISDN plus Analog)

In combination with the SIEMENS ISDN chip set, ALIS supports hybrid modems, , allowing connection to either the TIP/RING line or to an S or U-interface for ISDN applications.

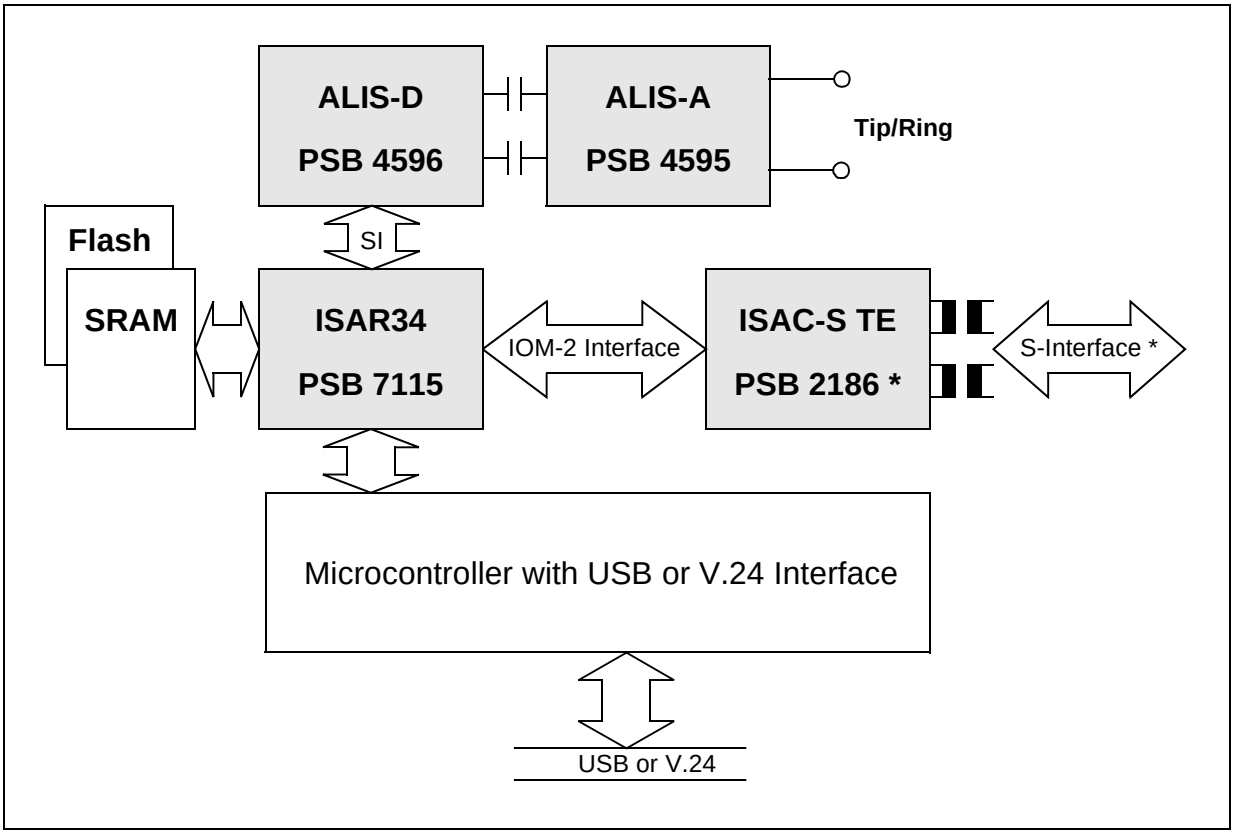


Figure 6 Hybrid Modem Application, with S-interface: ISAR34 Enhanced Data Access Controller (PSB 7115) and ISDN Access Controller for S-Bus ISAC-S TE (PSB 2186)

* Figure 4 shows a hybrid modem with the ISDN S-interface. To meet the ISDN U-interface, the ISAC-S TE PSB 2186 is replaced by the IEC-Q TE PSB 21911.

3.4 Modem with Speakerphone

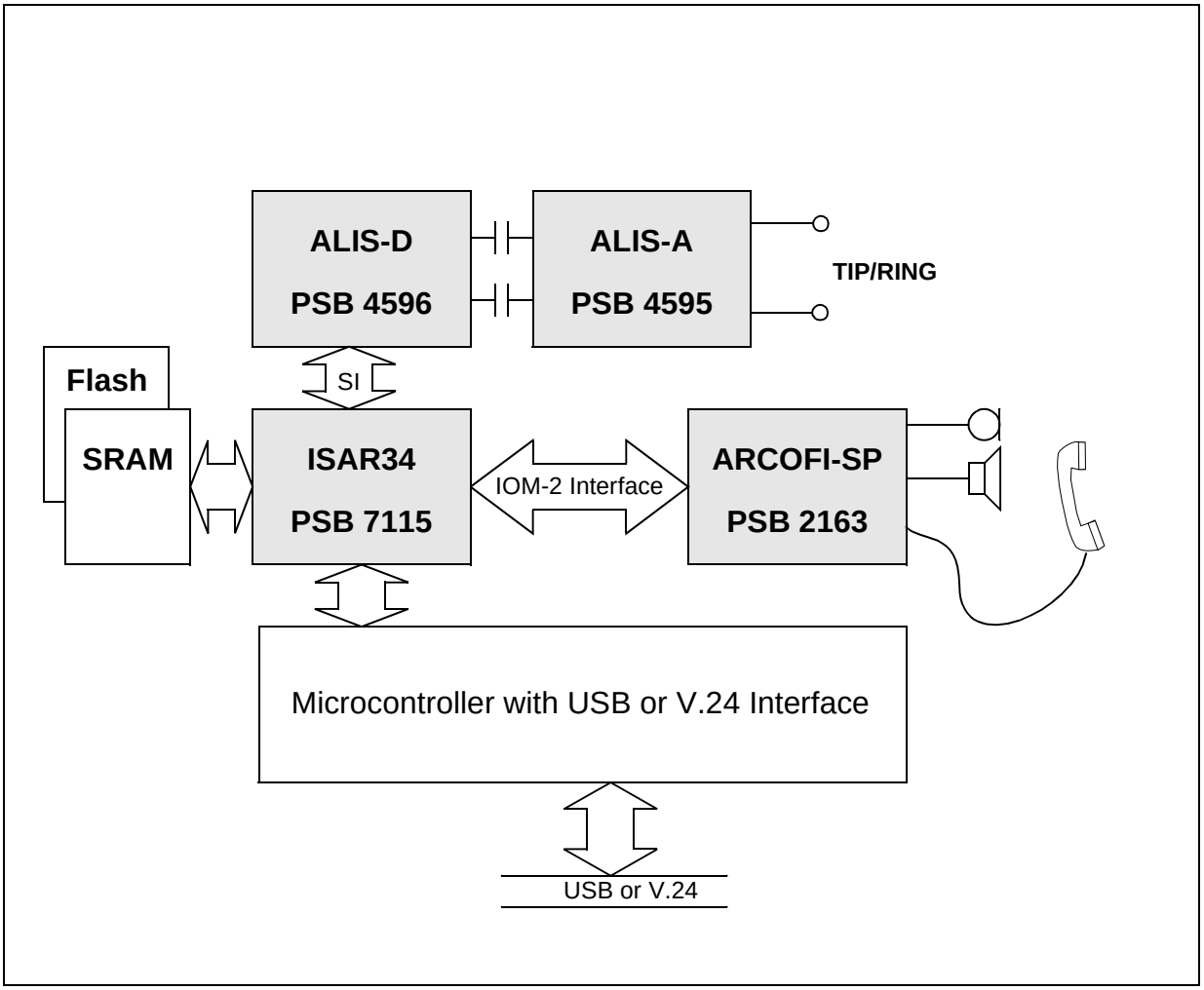


Figure 7 Application with Speakerphone: ARCOFI-SP Audio Ringing Codec (PSB 2160, PSB 2163, PSB 2165, PSB 2168) and ISAR34 Enhanced Data Access Controller (PSB 7115)

3.5 Analog Videophone

The diagram below shows a system solution for an analog videophone application using a SIEMENS chip set.

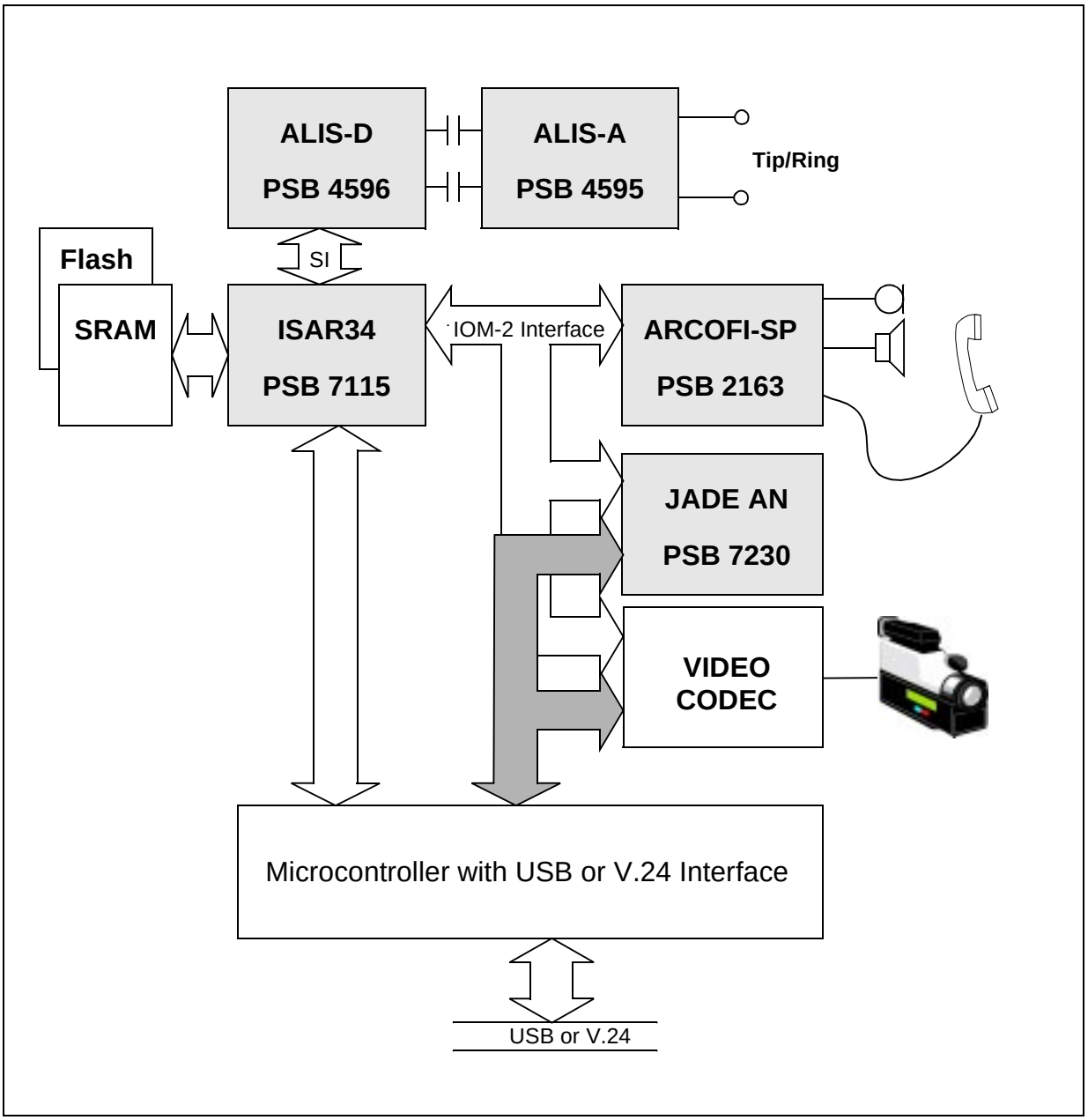


Figure 8 ARCOFI-(SP) Audio Ringing Codec (PSB 2160, PSB 2163, PSB 2165, PSB 2168) ; ISAR34 Enhanced Data Access Controller (PSB 7115); JADE Joint Audio Decoder Encoder (PSB 7230, PSB 7238)

4 ALIS Implementation

The ALIS chip set replaces all the major parts of a conventional front end for modem solutions. The circuit consists of two major parts, a DSP-based codec and an electronic DAA. Advanced features such as ring detection, pulse dialing and caller ID are integrated on-chip. Additional operating modes such as sleep mode or ringing mode are implemented to minimize power consumption.

4.1 ALIS Block Diagram

The tip/ring telephone line interface is connected mainly with the ALIS-A. It is also connected with the ALIS-D for Caller ID functions..

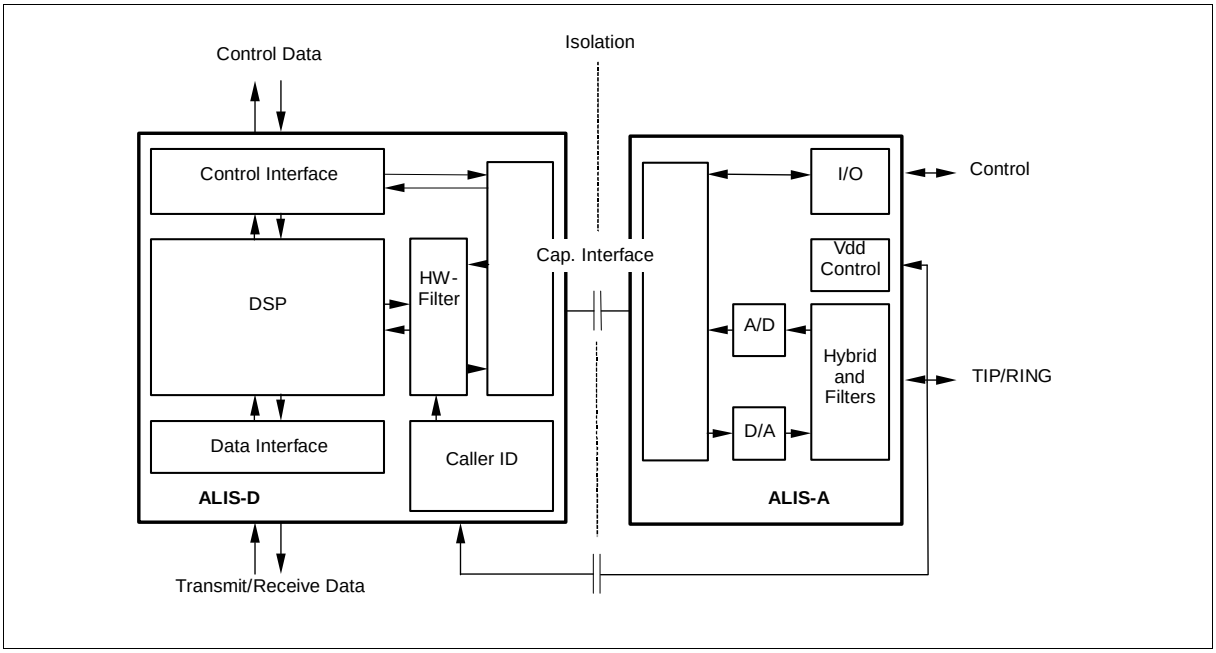


Figure 9 ALIS Block Diagram

The analog front end (ALIS-A) is connected to the line via TIP/RING. The programmable supply voltage for ALIS-A is generated from the line by the Vdd control. Two/four wire conversion is implemented in the hybrid circuit. Analog anti-aliasing pre-filters (PREFI) and smoothing post-filters (POFI) are included for signal conditioning. High-performance over-sampling analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) assure the required conversion accuracy. The ADCs and DACs are connected to the digital signal processor (DSP) on the digital part (ALIS-D) via a dedicated capacitor interface which also provides the required isolation to the line. Special hardware filters perform filtering functions such as interpolation and decimation. The DSP handles all the necessary algorithms. These include bandpass filtering, sample rate conversion, ringing detection, and caller ID decoding. All programmable filters and functions are also controlled and processed by the DSP. The control interface allows external control of the ALIS features and provides transparent access to ALIS commands and signaling pins. Thus pre-calculated sets of coefficients can be downloaded from the system to the on-

chip coefficient RAM (CRAM) in order to program the filters. Transmit and receive data is transferred to and from the data pump via the data interface.

4.2 ALIS AC Signal Flow Graph

ALIS architecture is based on digital filters. The data path through these filters is shown in the next few diagrams. The filter concept also allows maximum autonomy between the different filter blocks. Each filter block has a one-to-one correspondence with a specific network element. Marked filters (grey) can be programmed by the user.

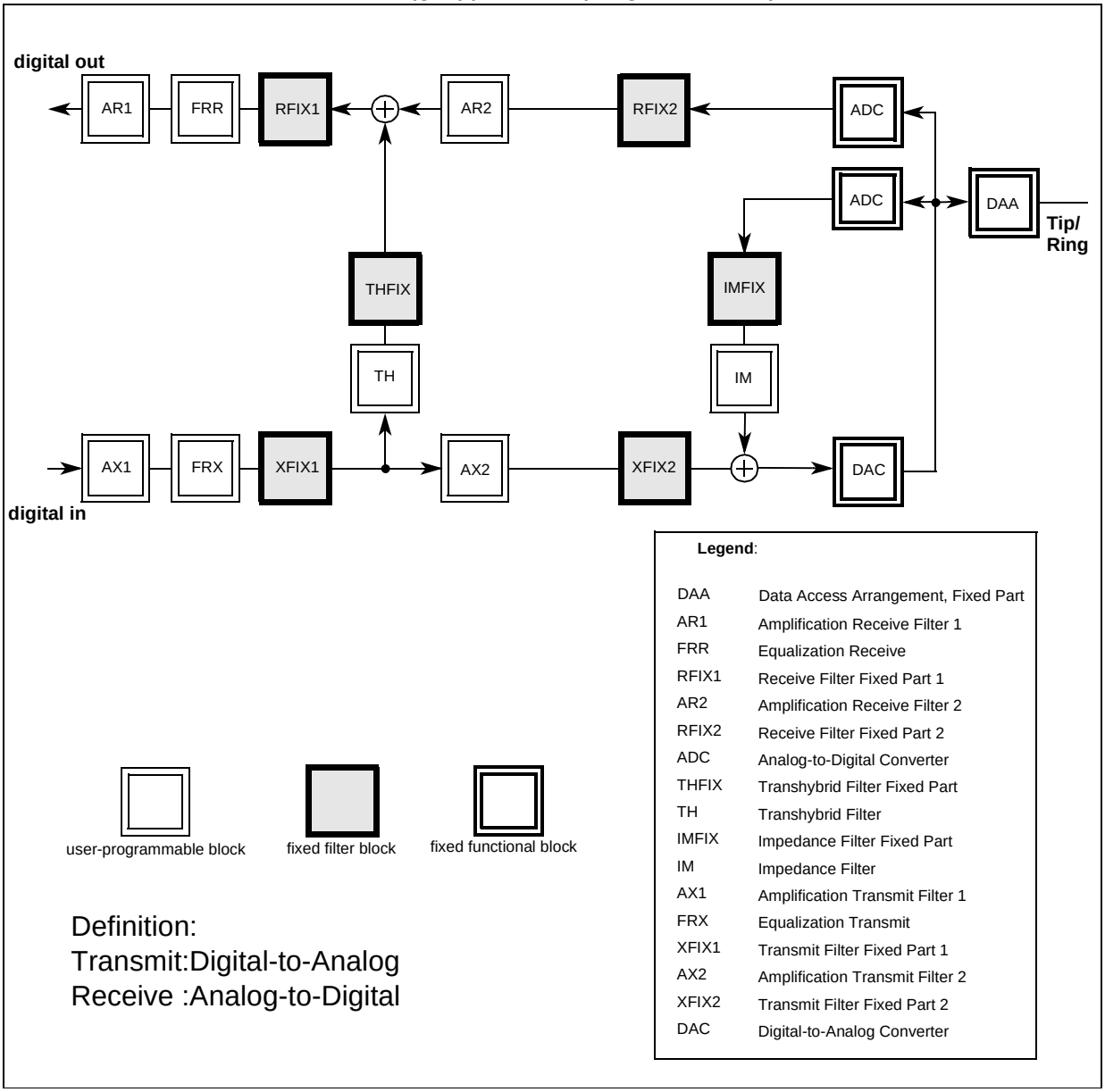


Figure 10 AC Signal Flow Graph

4.2.1 Receive Path

After passing the DAA and a simple anti-aliasing pre-filter with an analog gain stage, the voice signal is converted to a 1-bit digital data stream in the sigma-delta converter. The first down-sampling steps are performed in fast digital hardware filters. Subsequent processing is implemented in the digital structure which allows easy and flexible programming of parameters. Finally, the fully processed signal is transferred to the data interface.

Subsequent processing is done by microcode in the digital filter structure to allow adaptability. Gain adjustment is provided in two stages, AR1 and AR2. The total gain adjustment is programmable in two ranges: from 14 to 24 dB, in steps of 0.5 dB; and from -3 to 14 dB, with steps between 0.02 and 0.05 dB.

Located inbetween is a decimation stage to reduce the sampling rate to the 8 kHz PCM rate, and a low-pass filter to band-limit the signal in accordance with ITU-T G.714 and ETSI (NET33) recommendations (in RFIX1); also an equalization stage (in FRR).

Finally, the signal is passed out to the Serial Data Interface (SDI).

ALIS meets or exceeds all ITU and ETSI (NET33) recommendations on attenuation distortion and group delay.

4.2.2 Transmit Path

The digital input signal is received via the data interface. Low-pass filtering, gain correction and frequency-response correction are implemented in the digital filter structure. The up-sampling interpolation is then performed by fast hardware structures to reduce the DSP load. The up-sampled 1-bit data stream is converted to an analog equivalent which is smoothed by a post-filter (POFI) and converted to a 2-wire signal in the DAA.

There are also two independent tone generators which can insert tones into the Transmit path. They have adjustable frequencies, default 2 kHz, and a programmable bandpass-filter to adapt the output for DTMF. When either tone generator is on, the data signal transmission is suppressed.

4.2.3 Loops

ALIS implementation includes two loops. One is used to generate the AC-termination impedance (IM) and the other is used to perform proper hybrid balancing (TH). A simple additional path IM (from the receive to the transmit path) supports the impedance-matching function.

4.2.4 Test Features

Several analog and digital test loops are implemented in ALIS. The receive and transmit paths may be short-circuited at two different points for test purposes.

4.3 ALIS Ring and Caller ID Signal Flow Graph

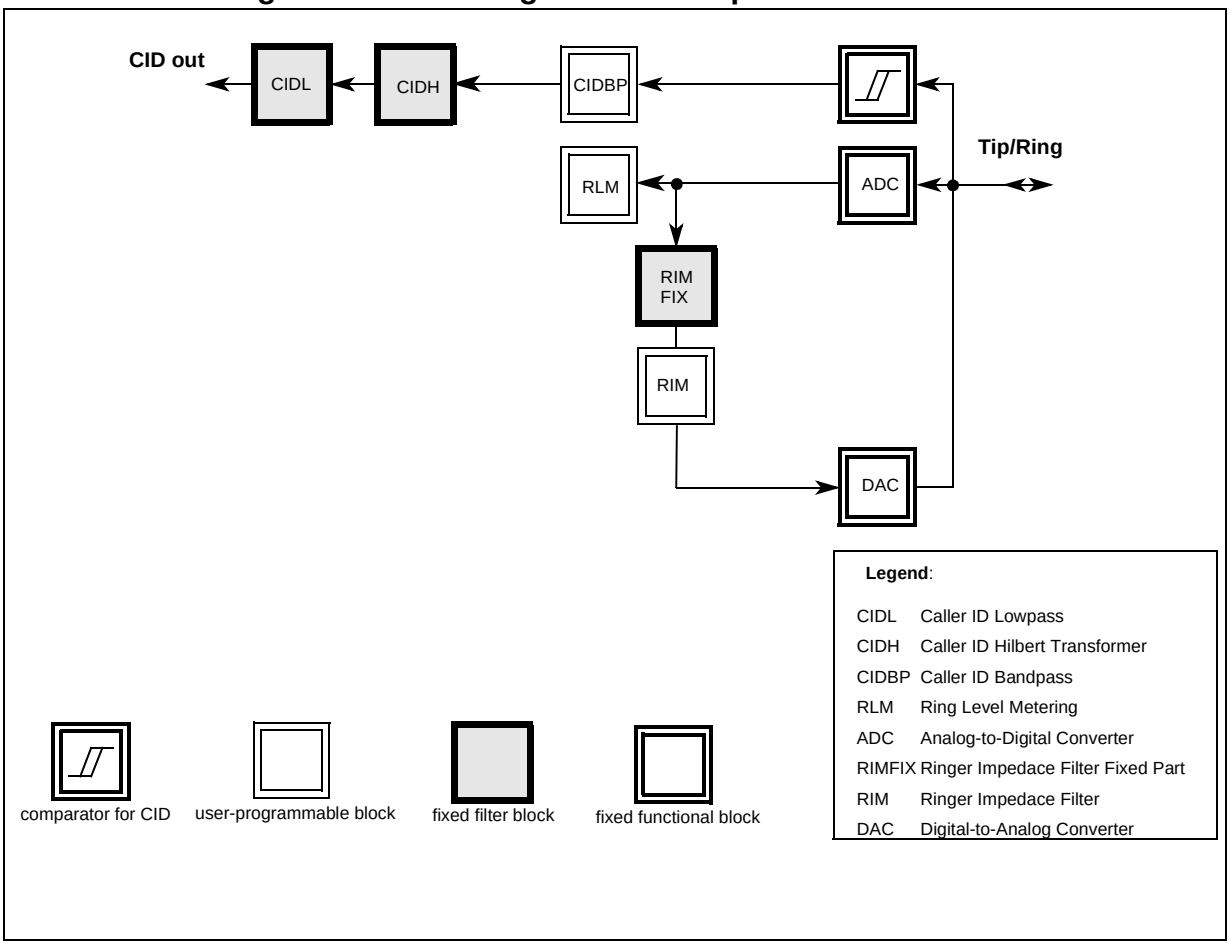


Figure 11 Ring Signal Flow Graph

These data paths operate only when the ALIS is in Ringing state.

4.3.1 Caller ID (CID) Path

The Caller ID receiver meets Bellcore specifications TR-NWT-000030 and SR-TSV-002476 for Caller ID. In this service, the calling party's information (Calling Line Identification Presentation (CLIP)) is transmitted in the silent interval between the first and second ring. ALIS receives and stores up to 4096 bits of the 1200 baud FSK (Frequency Shift Keying) signal. The decoding scheme meets the Bell 202 and ITU-T V.23 specifications.

The FSK signal which contains the caller information is converted to a 1-bit data stream by a comparator in order to minimize power consumption. Down-sampling steps are performed in fast digital hardware filters. To decode the caller ID, bandpass filtering, Hilbert transformation and other functions are implemented. The output CID-out is sampled at 1200 baud, and stored in the CID-RAM.

4.3.2 Ring-Level Metering (RLM) Path

The analog signal is converted to a 1-bit data stream in the ADC. After decimation in hardware filters, the remaining processing is done in the digital filter structure (in RLM): bandpass filtering to select the ringing frequency, and integration to determine if the amount of energy in-band has exceeded the threshold for a valid ring signal. The bandpass parameters and threshold are programmable.

Ringing is detected in this path. The digital input is bandpass filtered, integrated and compared to a threshold to determine if a ringing signal has occurred. The threshold and bandpass filters are programmable. The result of this operation can be monitored by reading the RMR bit (see “CR1 Configuration Register 1 (Dialing)” on page 40).

4.3.3 Loops

A loop is available to generate the Ring-termination impedance (RIM).

4.3.3.1 Test Features

There are three loopbacks on ALIS-D to test interfaces:

- Host interface: loopback from the PCM interface (just inside ALIS-D)
- Caller ID interface: loopback from Caller ID input to capacitor interface
- Capacitor interface: loopback through different parts of the capacitor interface

There are two loopbacks on ALIS-A:

- Tip/ring interface: loopback from the tip/ring, before the ADC
- Codec: loopback from the tip/ring, after the codec

5 Configuration Overview

5.1 Connection to the Telephone Line

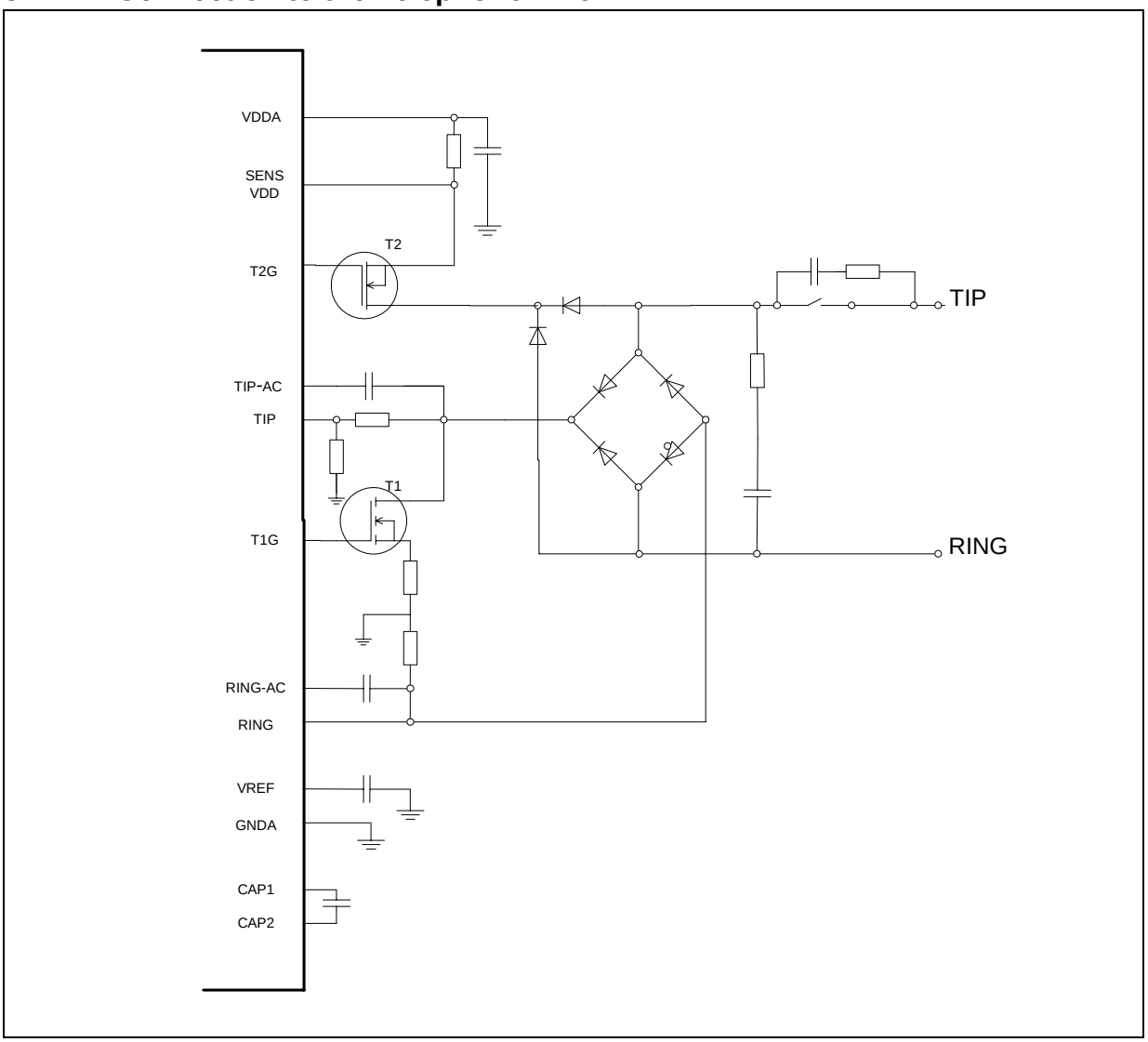


Figure 12 Connection of ALIS-A to the Telephone Line

As shown in the figure, ALIS-A requires a minimum of components to complete the DAA:

- Protection circuit: not shown.

- Bridge: using Schottky diodes will improve the performance at low feeding conditions. Recommended: Dual Schottky diode SIEMENS BAT 240A.

- Resistors for current sensing.

- Capacitors for AC coupling and VDD buffering.

- Two transistors (T1, T2) to handle the line current. T2 must be of depletion type, in order to deal with start-up. Recommended transistors: T1: SIEMENS BSP 88; T2: SIEMENS BSP 129.

- Components for EMC protection: not shown, as they depend on the board layout.

ALIS-D can optionally be connected to the tip/ring to provide Caller ID functions. The CID circuit requires two capacitors and four resistors.

5.2 Host Interface

The host interface consists of a serial µ-controller interface and a 16-bit linear data interface. They are used to connect ALIS either to a µ-controller and or to a data pump. The two serial interfaces can be accessed on two separate serial ports or in time-multiplex (MUX) mode on a single serial port.

5.2.1 The µ-Controller Interface

The ALIS internal configuration registers, the auxiliary ports, and the Coefficient RAM (CRAM) are programmable via the serial µ-controller interface. This interface consists of four pins:

CS:	Chip select, to enable interface (active low)
DCLK:	Clock, 1 kHz to 1024 kHz
DIN:	Data input
DOUT:	Data output

CS is used to start serial access to the ALIS registers and the Coefficient RAM. Following a CS falling edge, the first eight bits received at DIN specify the command. Subsequent data bytes (the number depends on the command) are stored in the selected configuration registers or the selected part of the CRAM.
Serial interface specification: 8 bit, no parity, no start/stop bit. Every command must begin with a CS falling edge.

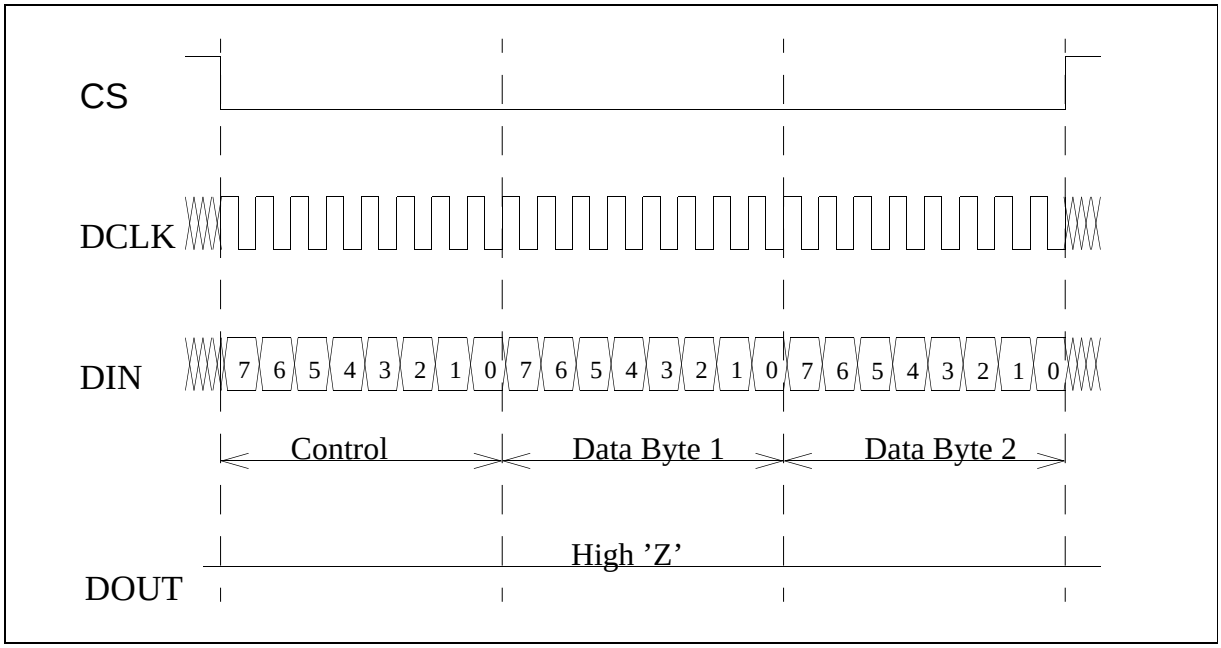


Figure 13 Example of a Write Access, two Data Bytes transferred

If the first eight bits received via DIN specify a read command, ALIS will start to respond via DOUT with its specific identification byte. The number of specified data bytes within the command (contents of configuration registers or contents of the CRAM) will follow on DOUT.

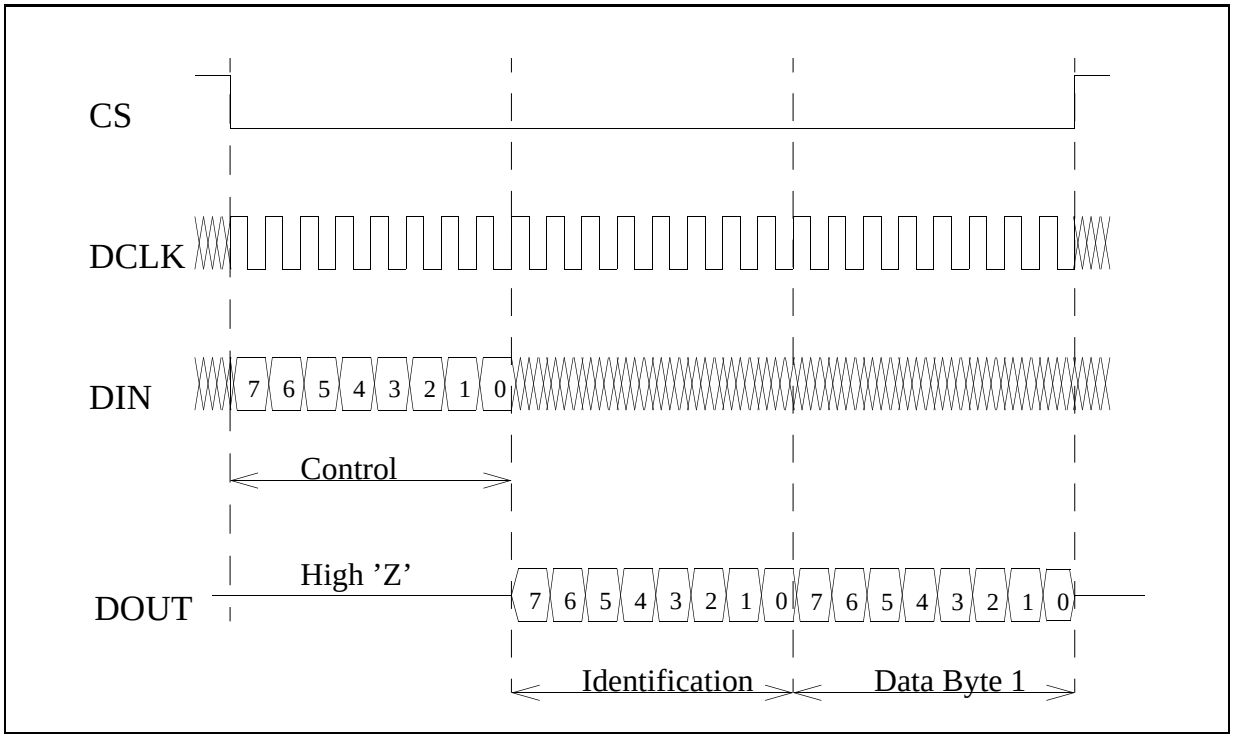


Figure 14 Example of a Read Access, one Data Byte transferred via DOUT

The data transfer is synchronized by DCLK. DIN is latched at the falling edge of DCLK, while DOUT changes with the rising edge of DCLK. During the execution of a command which is followed by output data (read command), the device will not accept any new command via DIN. The data transfer sequence can be interrupted by setting CS to '1'.

To reduce the number of connections to the µ-processor, DIN and DOUT may be strapped together to form a bi-directional data pin.

5.2.2 The Data Interface

A serial data interface is used for transferring voice data. The interface consists of five pins:

DAT_CLK: Clock, 128 kHz to 1024 kHz

FSC: Frame synchronization clock, 8 kHz

DAT_IN: Transmit data input

DAT_OUT: Receive data output

The Frame Sync (FSC) pulse identifies the beginning of a receive and a transmit frame. DAT_CLK synchronizes the data transfer on DAT_IN and DAT_OUT. The data bytes are first serialized to 16-bit width and MSB. The rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data.

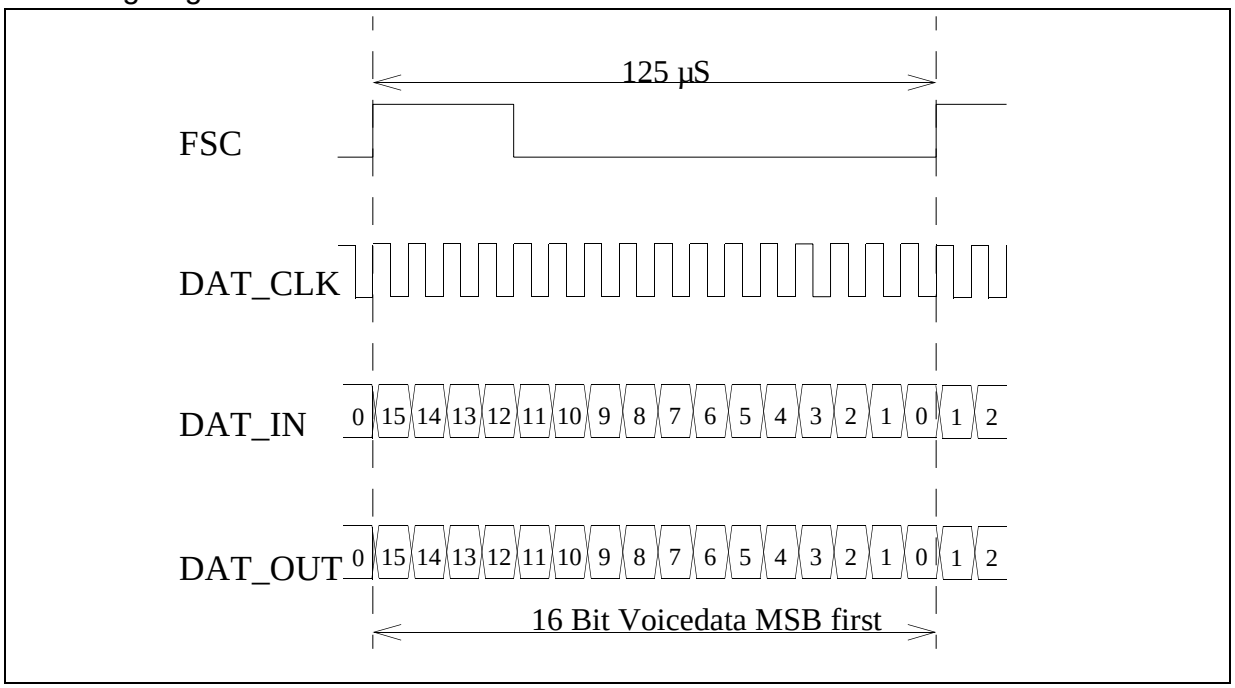


Figure 15 Example of a Clock Rate of 128 kb/s

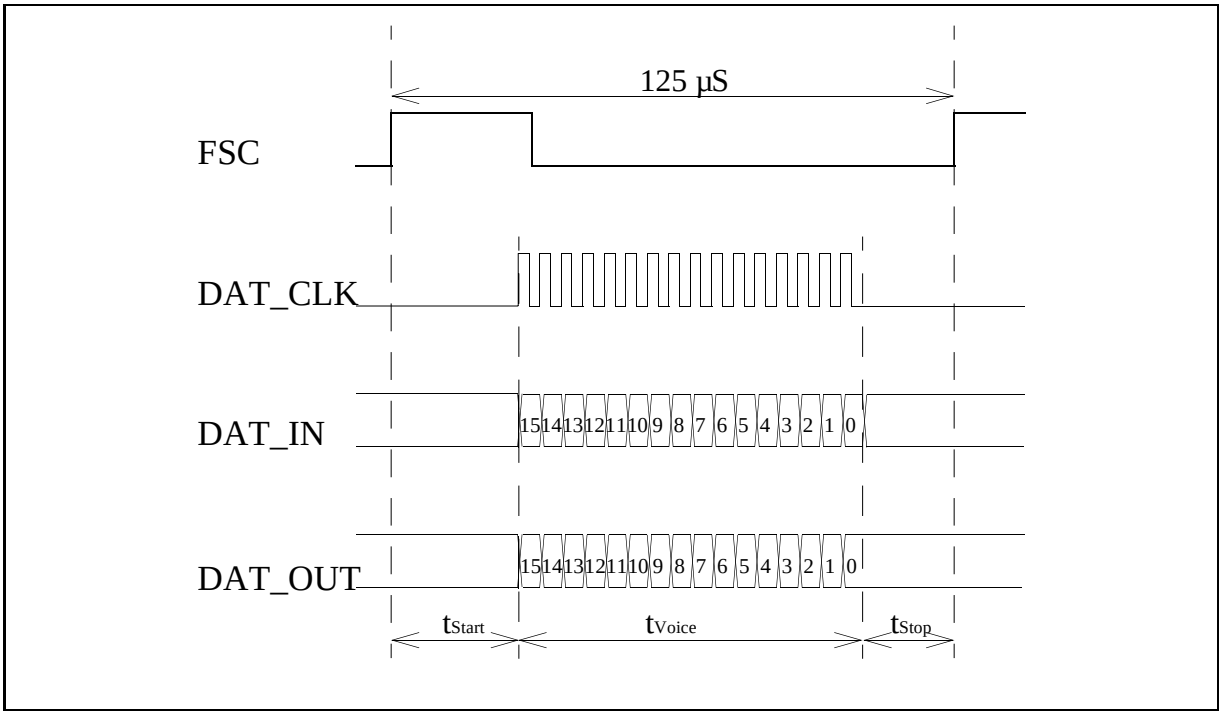


Figure 16 Example of a Clock Rate higher than 128 kb/s

The data package must stay within the frame, $t_{Start} > 0$ and $t_{Stop} > 0$.

The FSC signal can be generated externally by the host or by ALIS.

5.2.3 Interface Modes

5.2.3.1 Demux Mode

Connection of the MODE pin to GND allows the µC and the data interface to be accessed via two serial ports.

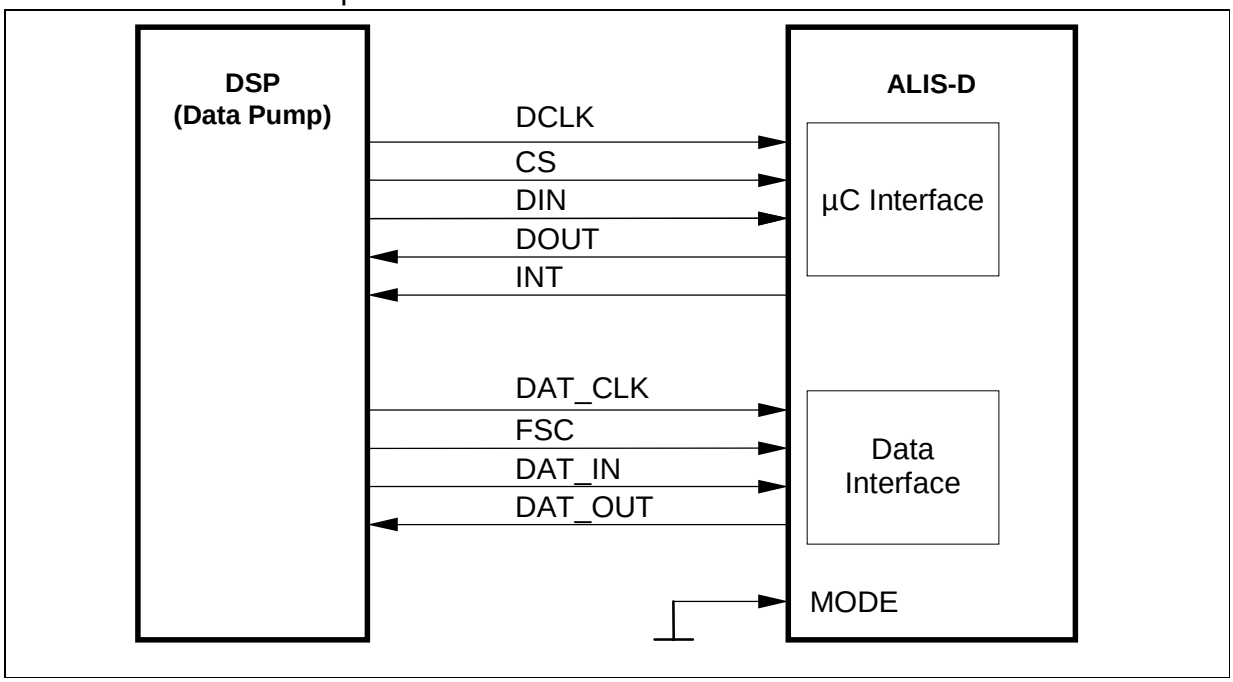


Figure 17 Host Interface in Demux Mode, FSC as Input

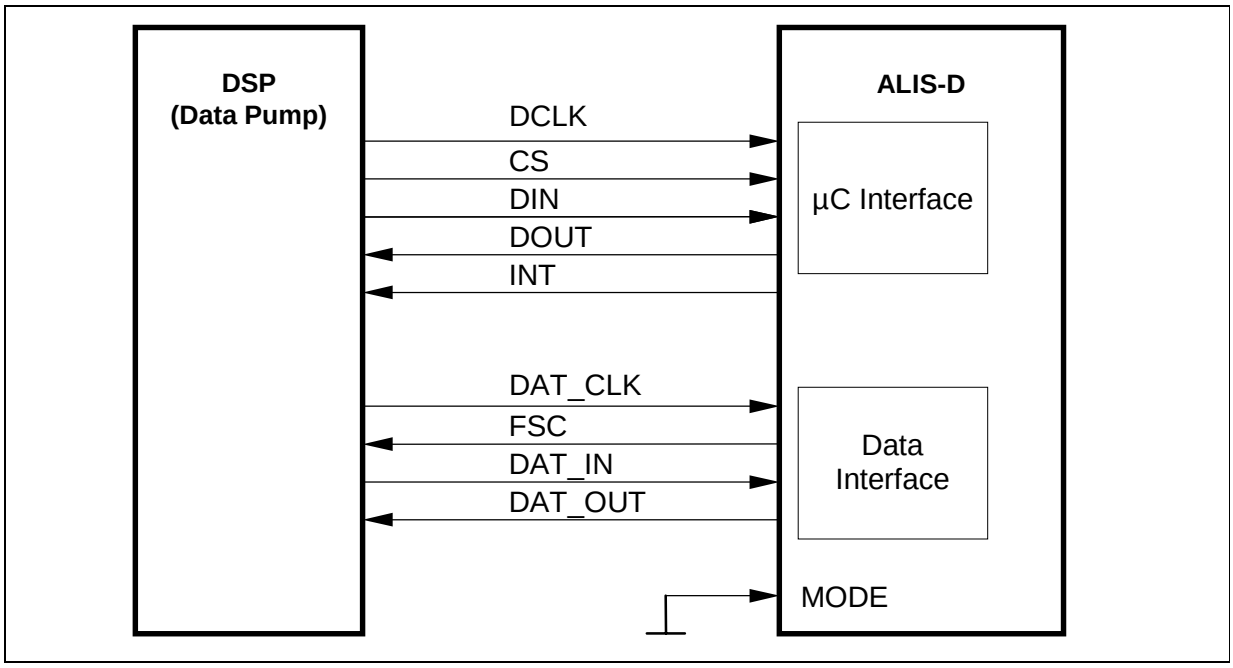


Figure 18 Host Interface in Demux Mode, FSC as Output

5.2.3.2 Multiplex Mode

Connection of the MODE pin to VDD allows the two interfaces to be time-multiplexed on a single port. The interfaces are selected by the DAT_IN/SEL pin.

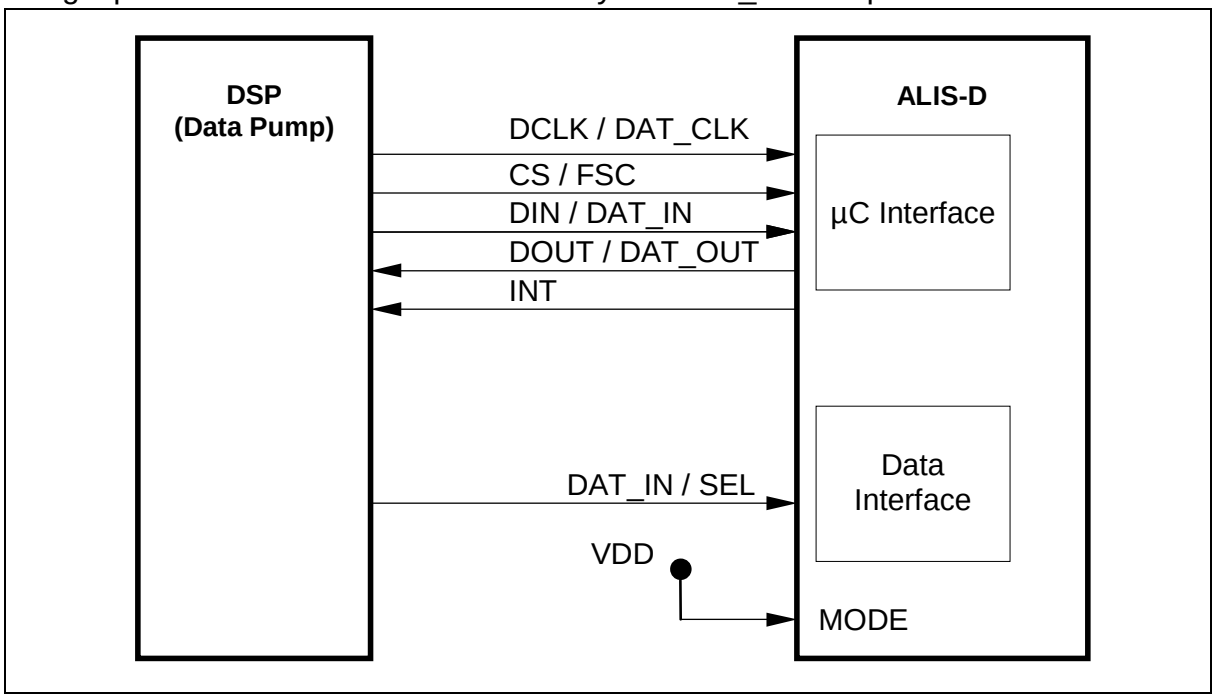


Figure 19 Host Interface in MUX Mode, FSC as Input

DAT_IN / SEL = 0	
PIN No	**Function**
11	DCLK
10	CS
12	DIN
13	DOUT

DAT_IN / SEL = 1	
PIN No	**Function**
11	DAT_CLK
10	FSC
12	DAT_IN
13	DAT_OUT

Table 3: Pin Definition in MUX mode, FSC as Input

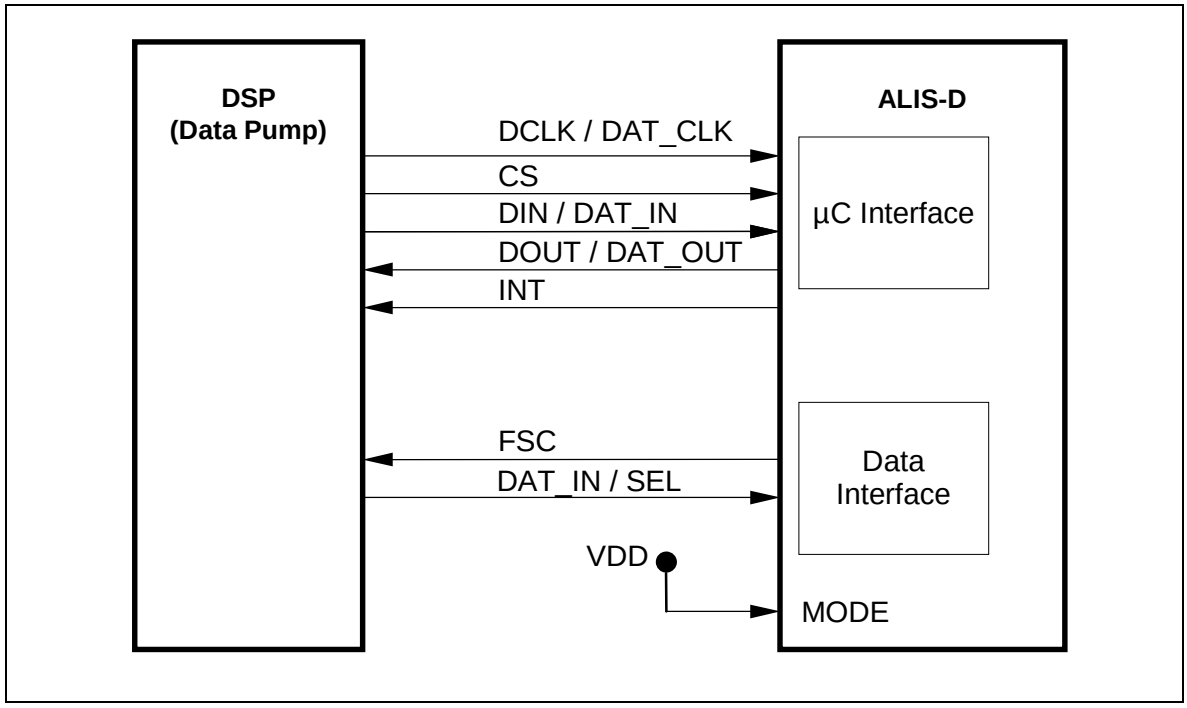


Figure 20 Host Interface in MUX mode, FSC as Output

DAT_IN / SEL = 0	
PIN No	**Function**
11	DCLK
10	CS
12	DIN
13	DOUT
15	FSC (output)

DAT_IN / SEL = 1	
PIN No	**Function**
11	DAT_CLK
10	VDD / GND[1)]
12	DAT_IN
13	DAT_OUT
15	FSC (output)

1) must be connected to a fixed potential

Table 4: Pin Definition in MUX Mode, FSC as Output

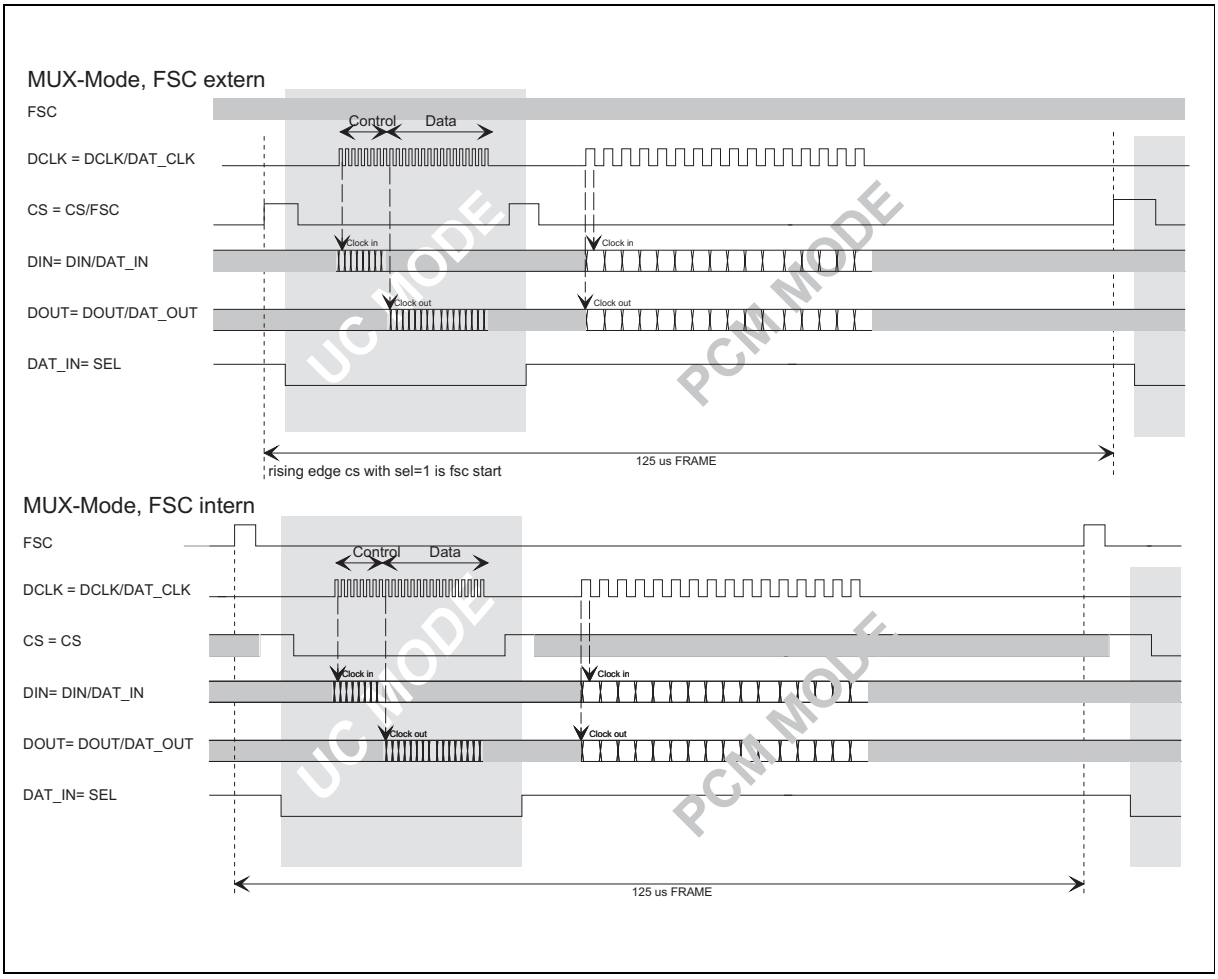


Figure 21 Protocol for Transmission of µC- and PCM Data in MUX Mode

5.3 Clocking

ALIS operates with a typical master clock frequency of 16.384 MHz. This clock can either be supplied from an external source or generated with a crystal by ALIS-D.

It is essential that the ratio of the master clock frequency to the FSC frequency is exactly 2048. This is of course guaranteed if the FSC signal is generated internally.

5.3.1 External clock

When providing the master clock externally, an external clock signal must be connected to pin MCLK1. The MCLK2 pin must remain unconnected and the CLK_EXT bit in CR0 must be programmed to a logic ’1’. (see the section “CR0 Configuration Register 0 (Filters)” on page 39).

5.3.2 Crystal clock

Because ALIS includes an on-chip oscillator circuit, an external crystal may be used. This crystal is connected across the MCLK1 and MCLK2 pins with two capacitors (see Figure 22 ”External Crystal Connections”) . The CLK_EXT bit in CR0 must be programmed to a logic '0' (= default value after reset). The capacitor values depend on the crystal type and are specified by the crystal manufacturer. A microprocessor-grade crystal with a parallel-resonant fundamental frequency is recommended.

To ensure that the ratio between the master clock and the FSC signal is correct, ALIS can be programmed to internal FSC generation (set Fsc_en bit in CR4 to a logic '1'). See Figure 18 “Host Interface in Demux Mode, FSC as Output” on page 30 and Figure 20 “Host Interface in MUX mode, FSC as Output” on page 32.

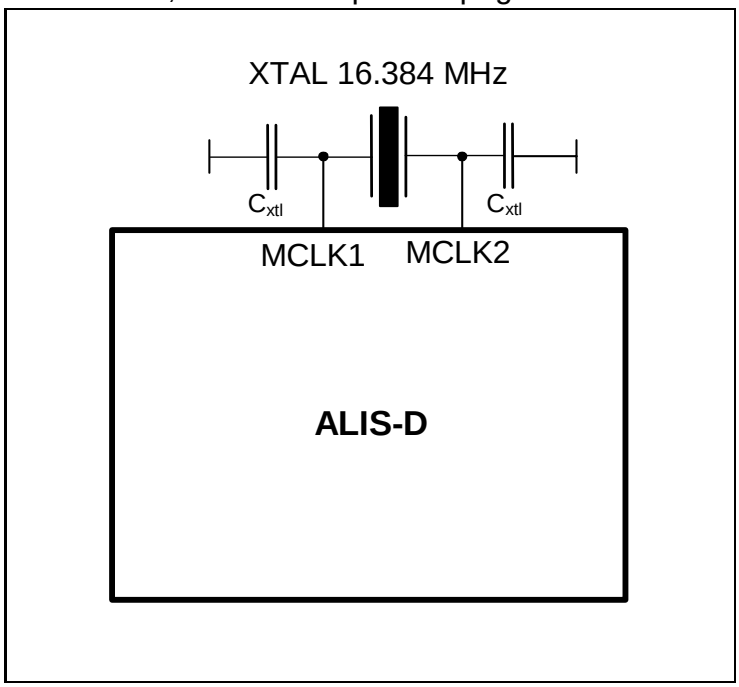


Figure 22 External Crystal Connections

5.4 Capacitor Interface

A capacitor interface is used to decouple ALIS-A from ALIS-D. It is a bi-directional serial interface and is used for exchanging control and data information between ALIS-A and ALIS-D. The transmission format is digital to avoid distortion and for performance reasons. For the size and tolerance of the capacitors, see the section “ALIS Cap Interface” on page 86.

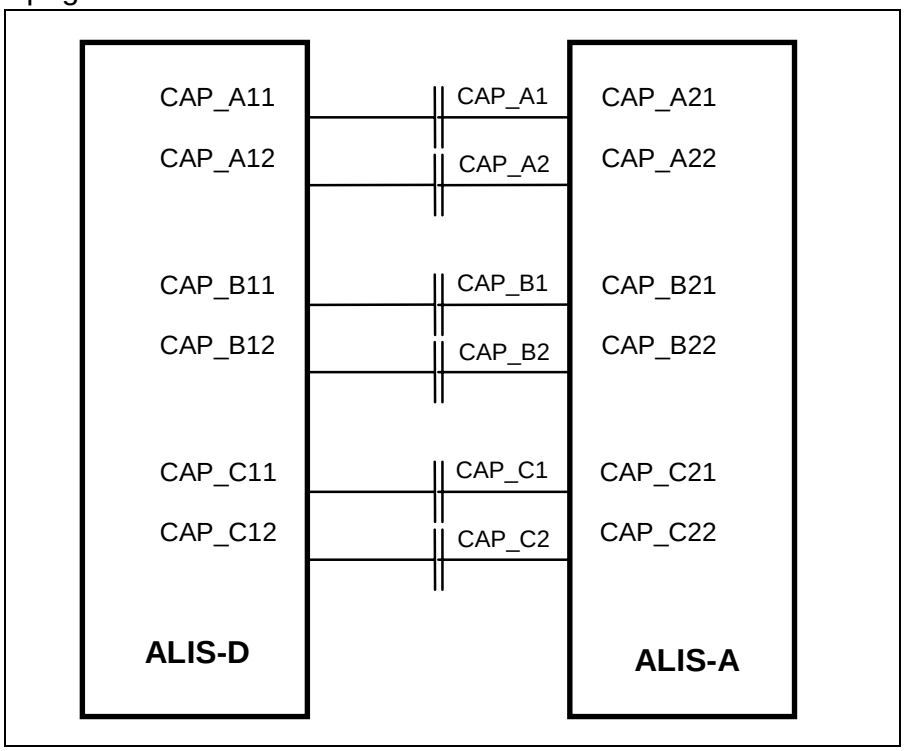


Figure 23 Connection of Capacitor Interface between ALIS-A and ALIS-D

5.5 Caller ID Interface

To receive the caller ID, ALIS-D must be connected to the line via an RC network. See the section “ALIS Caller ID Interface” on page 86".

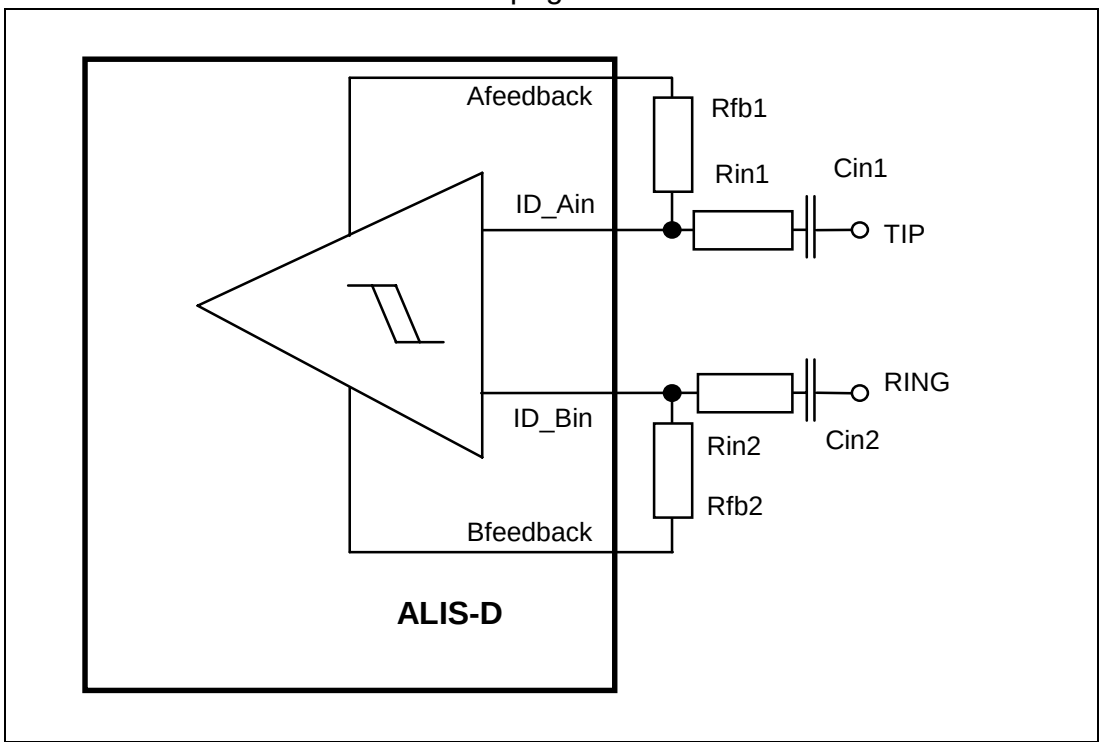


Figure 24 Caller ID Interface Connection of ALIS-D to Tip/Ring

6 Programming ALIS

Appropriate commands via the serial µ-controller interface enable very flexible programming and verification of ALIS.

Four different commands are used to access the various control registers and RAMs: SOP (see page 38), XOP (see page 44), COP (see page 50) and CAO (see page 51). The first byte received via DIN selects the command type. Each command can be used as a write or read command. Thanks to the extended ALIS control facilities, the SOP, XOP and COP commands contain additional information for programming (writing) and verifying (reading) the ALIS status (e.g. number of subsequent bytes, software reset, operating mode).

Up to 8 bytes of data can be read or written with an SOP, XOP or COP command. The CAO command allows all 512 bytes of the caller ID RAM to be read or written. Any read command causes ALIS to respond with its specific identification byte before sending the requested information.

6.1 Types of Commands and Data Bytes

The ALIS commands are selected by bit 3, 4 and 6 of the command byte as shown below.

SOP command

Bit	7	6	5	4	3	2	1	0
	PU 1	PU 0	RW	1	0	LSEL2	LSEL1	LSEL0

XOP command

Bit	7	6	5	4	3	2	1	0
	RST	0	RW	1	1	LSEL2	LSEL1	LSEL0

COP command

Bit	7	6	5	4	3	2	1	0
	0	0	RW	0	CODE 3	CODE 2	CODE 1	CODE 0

CAO command

Bit	7	6	5	4	3	2	1	0
	0	1	RW	1	1	0	0	0

6.1.1 Storage of Programming Information:

- 6 Configuration registers: CR0, CR1, etc. CR5 accessed by SOP commands
- 8 Extended registers: XR0, XR1, etc. XR7 accessed by XOP commands
- 1 Coefficient RAM: CRAM accessed by COP commands
- 1 Caller ID RAM: RAM accessed by CAO commands

6.2 SOP Command

The SOP (status operation) command allows the ALIS status registers to be written or read via the µ-controller interface.

Bit	7	6	5	4	3	2	1	0
	PU 1	PU 0	RW	1	0	LSEL2	LSEL1	LSEL0

PU Power-up operation command (only with SOP write command)

PU = 0 0: ALIS is set to sleep mode

PU = 0 1: ALIS is set to ringing mode

PU = 1 0: ALIS is set to conversation mode

PU = 1 1: ALIS is set to pulse dialing mode

RW Read/Write: Enables reading from ALIS or writing information to ALIS

RW = 0: Write to ALIS

RW = 1: Read from ALIS

LSEL Length select information (see also programming procedure)
This field identifies the number of subsequent data bytes

LSEL = 000:1 byte of data follows (CR0)

LSEL = 001:2 bytes of data follow (CR1, CR0)

LSEL = 010:3 bytes of data follow (CR2. CR1, CR0)

LSEL = 011:4 bytes of data follow (CR3, CR2. CR1, CR0)

LSEL = 100:5 bytes of data follow (CR4, CR3, CR2, CR1, CR0)

LSEL = 101:6 bytes of data follow (CR5, ..., CR1, CR0)

Note: If only one configuration register requires modification, for example CR3, this can be accomplished by setting LSEL=011 and releasing pin CS after CR3 is written, to.

6.2.1 CR0 Configuration Register 0 (Filters)

Default value: 00H

Configuration register CR0 defines the basic ALIS settings, which are: enabling/ disabling the programmable digital filters and tone generators.

Bit	7	6	5	4	3	2	1	0
	TH	IM	FRX	FRR	AX	AR	RIP	CLK_ EXT

TH Enable Trans-Hybrid Balancing (TH)-Filter

TH = 0: TH-filter disabled

TH = 1: TH-filter enabled

IM Enable Impedance Matching (IM)-Filter

IM = 0: IM-filter disabled

IM = 1: IM-filter enabled

FRX Enable Frequency Response Transmit (FRX)-Filter

FRX = 0: FRX-filter disabled

FRX = 1: FRX-filter enabled

FRR Enable Frequency Response Receive (FRR)-Filter

FRR = 0: FRR-filter disabled

FRR = 1: FRR-filter enabled

AX Enable Amplification/Attenuation Transmit (AX)-Filter

AX = 0: AX-filter disabled

AX = 1: AX-filter enabled

AR Enable Amplification/Attenuation Receive (AR)-Filter

AR = 0: AR-filter disabled

AR = 1: AR-filter enabled

RIP Enable Ringer Impedance (RIP)-Filter

RIP = 0: RIP-filter disabled

RIP = 1: RIP-filter enabled

CLK_EXT External clock signal

CLK_EXT = 0: Crystal Oscillator is enabled, clock will be generated by crystal

CLK_EXT = 1: Crystal Oscillator is disabled, clock must be supplied by external source

6.2.2 CR1 Configuration Register 1 (Dialing)

Default value: 00H
Configuration register CR01 selects tone generator modes and other operating modes

Bit	7	6	5	4	3	2	1	0
	E_ Tone2	E_ Tone1	P_ Tone2	P_ Tone1	Pulse	No_ auto_ ring	RMR	RM

E_Tone2 Enable programmable tone generator 2

E_Tone2= 0: Programmable tone generator 2 disabled

E_Tone2= 1: Programmable tone generator 2 enabled

E_Tone1 Enable programmable tone generator 1

E_Tone1= 0: Programmable tone generator 1 disabled

E_Tone1= 1: Programmable tone generator 1 enabled

P_Tone2 User-programmed frequency or fixed frequency selected

P_Tone2= 0: Fixed frequency for tone generator 2 selected

P_Tone2= 1: Programmed frequency for tone generator 2 selected

P_Tone1 User programmed frequency or fixed frequency selected

P_Tone1= 0: Fixed frequency for tone generator 1 selected

P_Tone1= 1: Programmed frequency for tone generator 1 selected

Pulse Pulse dialing

Pulse = 1: Make for pulse dialing

Pulse = 0: Break for pulse dialing

No_auto_ring

No_auto_ring= 1:Test mode to disable automatic switching from sleep mode to ringing mode after valid ring.

No_auto_ring= 0:Normal operating mode, ALIS switches automatically to ringing mode after ringing detection

RMR Result of ringing metering function (this bit cannot be written)

RMR = 0: Detected level was lower than the programmed[1)] reference

RMR = 1: Detected level was higher than the programmed reference. See “Flow of Ring Sequence and Detection” on page 65.

RM Ringing metering function[2)]

1 The threshold can be programmed in the CRAM. Coefficients see “Ring Detect” on page 81.

RM = 0: Ringing metering function disabled

RM = 1: Ringing metering function enabled

6.2.3 CR2 Configuration Register 2 (Caller ID)

Bit	7	6	5	4	3	2	1	0
	COT/R			IDR	Call_ pon	Call_ en	Call_I	Call_II

Default value: 00H

COT/R Select cut-off transmit/receive paths

0 0 0: Normal operation

0 0 1: COR16 Cut-off receive path at 16 kHz (input of TH filter)

0 1 0: COR8 Cut-off receive path at 8 kHz

1 0 1: COT2M Cut-off transmit path at 2 MHz (POFI output)

1 1 0: COT64 Cut-off transmit path at 64 KHz (IM filter input)

IDR Initialize data RAM

IDR = 0: Normal operation selected

IDR = 1: Contents of data RAM set to 0 (for test purposes)

Call_pon Enable the caller ID Path

Call_pon = 0: Caller ID Path disabled

Call_pon = 1: Caller ID Path enabled
(see Call_pctl in “CR3 Configuration Register 3 (Test Loops)” on page 42)

Call_en Enable the caller ID

Call_en = 1: Caller ID decoding enabled

Call_en = 0: Caller ID decoding disabled

Call_I Result of caller ID decoding (this bit cannot be written, for test purposes only)

Call_I = 1: 1st tone of caller ID detected

Call_I = 0: 1st tone of caller ID not detected

Call_II Result of caller ID decoding (this bit can not be written, for test purpose only)

Call_II = 1: 2nd tone of caller ID detected

[2] Explanation of the ringing metering function: The ring signal is rectified, and the voltage is measured. If the voltage exceeds a certain value, the bit RMR is set to ’1’.

Call_II = 0: 2nd tone of caller ID not detected

6.2.4 CR3 Configuration Register 3 (Test Loops)

Bit	7	6	5	4	3	2	1	0
	Test Loops				SEL	Call_ pctl	DHP-R	DHP-X

Default value: 00H

Test Loops Four-bit field for selection of analog and digital loopbacks

- 0101 ALB_CIF: Cap. interface loop of the signal from the input circuit (CAP_B11/12 is connected to the output drivers (CAP_A11/12, CAP_C11/12)
- 1000 ALB-CID: Caller ID loop; the output signal from the caller ID comparator is connected to the output drivers of the capacitor interface (CAP_A11/12, CAP_C11/12);
- 1001 DLB-2M: Loop via HW filters;
- 1100 DLB-128k: Loop inside DSP;
- 1101 DLB-64k: Loop inside DSP;
- 1111 DLB-PCM: Loop via PCM interface; the received data is sent back in the next frame;

SEL Test loop selection

- SEL = 0: Test loops via impedance path selected
- SEL = 1: Test loops via receive path selected

Call_pctl Caller ID path control

- Call_pctl = 0: Caller ID interface enabled during ringing mode
- Call_pctl = 1: Caller ID interface will be selected by the Call_pon bit in CR2

Note: The path can be controlled manually for test purposes. Must be ’0’ for normal operation.

DHP-X Disable high-pass in transmit direction

- DHP-X = 0: Transmit high-pass enabled
- DHP-X = 1: Transmit high-pass disabled

DHP-R Disable high-pass in receive direction

- DHP-R = 0: Receive high-pass enabled
- DHP-R = 1: Receive high-pass disabled

6.2.5 CR4 Configuration Register 4 (Analog Gain)

Bit	7	6	5	4	3	2	1	0
	AGR_ Z 1	AGR_ Z 0	AGR_ R 1	AGR_ R 0	AGX 1	AGX 0	Int_en	Fsc_ en

Default value: 00H

AGR_Z Analog gain in impedance loop (can be used as AGC)

AGR_Z = 00: Analog gain A disabled (0 dB amplification)

AGR_Z = 11: Analog gain A enabled (2.5 dB amplification)

AGR_Z = 10: Analog gain A enabled (6 dB amplification)

AGR_Z = 01: Analog gain A enabled (-3.5 dB amplification)[1)]

AGR_R Analog gain in receive direction (can be used as AGC)

AGR_R = 00: Analog gain B disabled (0 dB amplification)

AGR_R = 01: Analog gain B enabled (3.5 dB amplification)

AGR_R = 11: Analog gain B enabled (6 dB amplification)

AGX Analog gain in transmit direction (can be used as AGC)

AGX = 00: Analog gain A disabled (0 dB amplification)

AGX = 01: Analog gain A enabled (-6 dB amplification)

AGX = 10: Analog gain A enabled (3.5 dB amplification)

AGX = 11: Analog gain A enabled (-2.5 dB amplification)

Int_en Interrupt enable

Int_en = 1: Enable interrupts

Int_en = 0: Disable interrupts

Fsc_en FSC signal-source selection

Fsc_en = 0: FSC must be generated externally

Fsc_en = 1 FSC generated internally

[1] Note: the sum of AGR_Z and AGX should be zero for stability reasons.

6.2.6 CR5 Configuration Register 5 (Version)

Bit	7	6	5	4	3	2	1	0
	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

V The current version of ALIS (this byte cannot be written)
02H for ALIS V2.1

6.3 XOP Command

The ALIS digital command/indication interface to the line and external equipment is configured and evaluated by the Extended Operation (XOP) command. Other common functions are also assigned by this command.

Bit	7	6	5	4	3	2	1	0
	RST	0	RW	1	1	LSEL2	LSEL1	LSEL0

RST Software reset (same as RESET pin)
RST = 0: No reset
RST = 1: ALIS is reset to the default settings

RW Read / Write: Enables reading from or writing to ALIS
RW = 0: Write to ALIS
RW = 1: Read from ALIS

LSEL Length select information. Specifies the number of subsequent data bytes
LSEL = 000 1 byte of data follows (XR0)
LSEL = 001 2 bytes of data follow (XR1, XR0)
:
LSEL= 111 8 bytes of data follow (XR7, ..., XR1, XR0)

6.3.1 XR0 Extended Register 0 (Interrupt Register)

Any interrupt indications can be monitored in the interrupt register. Interrupts can be signaled via a logic ’1’ on the INT line. After an indication has occurred, further loading of the interrupt register is locked until its contents are read via the µ-controller interface. Reading the interrupt register XR0 releases the lock and the INT line is set to low again. See “Interrupt Controller” on page 60 for more details.

For XOP Read Commands

Bit	7	6	5	4	3	2	1	0
	0	Wake_ up	Ca- dence	RING	Caller _ID	VDD_ OK	SI_1	SI_0

Default value: 00H

Wake_up Wake_up Interrupt

Wake_up = 0: No Wake_up Interrupt

Wake_up = 1: If CLK_OFF bit is set (see “XR6 Extended Register 6 (Power State)” on page 49) and a ringing signal occurs[1)], then a Wake_up Interrupt is generated. To clear this interrupt, the CLK_OFF bit must be reset and ALIS-D must be supplied with a clock.

Cadence Cadence Interrupt

Cadence = 0: No cadence Interrupt
(time between two ring bursts is available from XR4)

Cadence = 1: Time between two ring bursts exceeds the programmed time
(see “XR2 Extended Register 2 (Cadence Time Out)” on page 47).

RING Ring Interrupt

RING = 0: No ring burst

RING = 1: No_auto_ring=0: this bit is set after the second valid ring burst
No_auto_ring=1: ALIS stays in sleep mode and waits for a command. This bit represents the ring detection signal from ALIS-A. See“CR1 Configuration Register 1 (Dialing)” on page 40.

Note: In this case, a command is mandatory to avoid a deadlock.

Caller_ID Caller ID Interrupt

Caller_ID = 0: No caller ID preamble detected

Caller_ID = 1: Caller ID preamble detected

VDD_OK Vdd at ALIS-A Interrupt

VDD_OK = 1: Power supply for ALIS-A is available and the connection between ALIS-A and ALIS-D is working

VDD_OK = 0: No power supply for ALIS-A or no connection between ALIS-A and ALIS-D

1 Any signal at the line with a voltage of more than 18 V. To decode a valid ring signal, ALIS must be switched to the Ringing Mode.

SI_0 Status of pin SI_0 at ALIS-A is transferred to this register

SI_1 Status of pin SI_1 at ALIS-A is transferred to this register

Note: The auxiliary pins (SO_0, SO_1, SI_0, SI_1) are isolated via the capacitor interface.

With XOP-Write Commands to Control the SO Output Pins

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	SO_2	SO_1	SO_0

SO_0 Pin SO_0 at ALIS-A is set to the assigned value if ALIS is not in sleep mode

SO_1 Pin SO_1Q at ALIS-A is set to the inverted assigned value if ALIS is not in sleep mode

SO_2 Pin SO at ALIS-D is set to the assigned value

6.3.2 XR1 Extended Register 1 (Interrupt Enable Register)

Bit	7	6	5	4	3	2	1	0
	0	M_Wake_up	M_ Cadence	M_ RING	M_ Caller_ ID	M_ VDD_ OK	M_ SI_1	M_ SI_0

Default value: 00H

M_Wake_up

M_Wake_up = 0:Disable Wake_up Interrupt

M_Wake_up = 1:Enable Wake_up Interrupt

M_Cadence

M_Cadence = 0:Disable Cadence Interrupt

M_Cadence = 1:Enable Cadence Interrupt

M_RING

M_RING = 0**:** Disable RING Interrupts

M_RING = 1: Enable RING Interrupts

M_Caller_ID

M_Caller_ID = 0:Disable Caller_ID Interrupt

M_Caller_ID = 1:Enable Caller_ID Interrupt

M_VDD_OK

M_VDD_OK = 0:Disable VDD Interrupt

M_VDD_OK = 1:Enable VDD Interrupt

M_SI_1

M_SI_1 = 0**:** Disable SI_1 Interrupts

M_SI_1 = 1: Enable SI_1 Interrupts

M_SI_0

M_SI_0 = 0: Disable SI_0 Interrupts

M_SI_0 = 1: Enable SI_0 Interrupts

6.3.3 XR2 Extended Register 2 (Cadence Time Out)

Bit	7	6	5	4	3	2	1	0
	CTO 7	CTO 6	CTO 5	CTO 4	CTO 3	CTO 2	CTO 1	CTO 0

Default value: 7DH

CTO ms Programmable Cadence Time Out:

If the time between the first two ring bursts exceeds the time progammed in this register, a cadence interrupt is generated. The time-out is programmable in steps of 64 ms up to 16 seconds.

Note: 00 means no cadence time-out programmed - no interrupt will be generated.

6.3.4 XR3 Extended Register 3 (DC Characteristic)

Bit	7	6	5	4	3	2	1	0
	AGB1	AGB0	B_off	DCU 1	DCU 0	DCI	DCR 1	DCR 0

AGB Analog gain for analog trans-hybrid filter

AGB = 00: Gain for analog trans-hybrid filter = 1.9 dB

AGB = 01: Gain for analog trans-hybrid filter = 0 dB

AGB = 10: Gain for analog trans-hybrid filter = -2.1 dB

AGB = 11: Gain for analog trans-hybrid filter = -3.4 dB

B_off Enable analog trans-hybrid filter

B_off = 0: Analog trans-hybrid filter on

B_off = 1: Analog trans-hybrid filter off

Note: The analog trans-hybrid filter is an analog pre-filter optimized for long loops with a trans-hybrid loss of about 10 dB.

DCU = 00: U0 for DC characteristic is 0 V

DCU = 01: U0 for DC characteristic is 1.5 V

DCU = 10: U0 for DC characteristic is 3.5 V

DCU = 11: U0 for DC characteristic is 7.2 V

Note: These values do not include the voltage drop at the external diodes. See also "DC Characteristics" on page 88.

DCI Limit current for the DC characteristic

DCI = 0: Limit current is 100 mA

DCI = 1: Limit current is 50 mA

DCR Resistance of the DC characteristic

DCR = 00: R for DC characteristic is 280 Ω

DCR = 01: R for DC characteristic is 240 Ω

DCR = 10: R for DC characteristic is 200 Ω

DCR = 11: R for DC characteristic is 100 Ω

Note: If DCU is programmed to 7.2V (DCU = 11), then R for the DC characteristic is always 70 Ω irrespective of the contents of DCR. See "DC Termination" on page 84.

6.3.5 XR4 Extended Register 4 (Cadence)

Bit	7	6	5	4	3	2	1	0
	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

C ms (read only)

Contains the measured time between the two first ring bursts (time step 64 ms) if the time is below the cadence time-out as programmed in XR2.

6.3.6 XR5 Extended Register 5 (Ring Timer)

Bit	7	6	5	4	3	2	1	0
	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0

Default value: 22H

T ms Ring latency timer, programmable in steps of 2 ms

ALIS-A decodes any signal of more than 18 V at TIP/RING. This signal will be transferred over to ALIS-D for further processing. This timer bridges the time when the sine wave of the ring signal is below the 18 V mark to ensure that ALIS does not fall back into sleep mode.

6.3.7 XR6 Extended Register 6 (Power State)

Bit	7	6	5	4	3	2	1	0
	0	0	0	CKL_ OFF	0	0	CPS1	CPS0

Default value: 00H

CPS Current Power State (read only)

CPS = 00 Power state is sleep

CPS = 01 Power state is ringing

CPS = 10 Power state is conversation

CPS = 11 Power state is pulse dialing

Note: The power mode can be programmed by the SOP command. The current power state will be indicated in this register.

CLK_OFF Turn off master clock (ALIS is programmed to deep-sleep mode)

CLK_OFF = 0 Master clock is not turned off internally

CLK_OFF = 1 Master clock is turned off internally

Note: The external clock can be turned off after setting the CLK_OFF bit. The clock must be switched on for programming ALIS.

Note: When a crystal is used, it will be turned off automatically when the CLK_OFF bit is set. It will be switched on when the CS signal goes low. However, the user must wait until the crystal is working before initiating a command.

6.3.8 XR7 Extended Register 7 (Vdd)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	Vdd1	Vdd0	0

Default value: 00H

Vdd Current Power State

Vdd = 00 Vdd of ALIS-A is 4.25 V

Vdd = 01 Vdd of ALIS-A is 4.38 V (test purpose only)

Vdd = 10 Vdd of ALIS-A is 3.90 V (test purpose only)

Vdd = 11 Vdd of ALIS-A is 4 V

6.4 COP Command

A Coefficient Operation (COP) command allows the coefficients for the programmable filters to be written to the ALIS coefficient RAM or read from this RAM via the µ-controller interface for verification.

Bit	7	6	5	4	3	2	1	0
	0	0	RW	0	CODE 3	CODE 2	CODE 1	CODE 0

RW Read/Write

RW = 0 Subsequent data is written to ALIS

RW = 1 Read data from ALIS

CODE includes the number of following bytes and the filter address

0	0	0	0	TH filter coefficients (part 1)	(followed by 8 bytes of data)
0	0	0	1	TH filter coefficients (part 2)	(followed by 8 bytes of data)
0	0	1	0	TH filter coefficients (part 3)	(followed by 8 bytes of data)
0	0	1	1	Ringer impedance (part 1)	(followed by 8 bytes of data)
0	1	0	0	IM filter coefficients (part 1)	(followed by 8 bytes of data)

0	1	0	1	IM filter coefficients (part 2)	(followed by 8 bytes of data)
0	1	1	0	Ringer impedance (part 2)	(followed by 8 bytes of data)
0	1	1	1	FRR filter coefficients	(followed by 8 bytes of data)
1	0	0	0	FRX filter coefficients	(followed by 8 bytes of data)
1	0	0	1	AR filter coefficients	(followed by 4 bytes of data)
1	0	1	0	AX filter coefficients	(followed by 4 bytes of data)
1	0	1	1	Tone1 coefficients	(followed by 4 bytes of data)
1	1	0	0	Tone2 coefficients	(followed by 4 bytes of data)
1	1	0	1	Level metering ringing	(followed by 4 bytes of data)
1	1	1	0	Caller ID 1st tone	(followed by 8 bytes of data)
1	1	1	1	Caller ID 2nd tone	(followed by 8 bytes of data)

6.5 CAO Command

A CAO (caller ID operation) command allows the decoded caller ID to be read. A CAO command is always followed by 512 bytes of data.

Bit	7	6	5	4	3	2	1	0
	0	1	RW	1	1	0	0	0

RW Read/Write

RW = 0 Subsequent data is written to ALIS (test purposes only)

RW = 1 Read data from ALIS

6.6 Register Summary

6.6.1 CR Registers:

Bit	7	6	5	4	3	2	1	0
CR0	TH	IM	FRX	FRR	AX	AR	RIP	CLK_EXT
CR1	E_ Tone2	E_ Tone1	P_ Tone2	P_ Tone1	Pulse	No_ auto	RMR	RM
CR2	COT/R			IDR	Call_p on	Call_e n	Call_I	Call_II
CR3	TestLoops				SEL	Cal _pctl	DHP-R	DHP-X
CR4	AGR_ Z 1	AGR_ Z 0	AGR_ R1	AGR_ R 0	AGX 1	AGX 0	Int_en	Fsc_ en
CR5	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

Table 5: Summary of CR Registers

6.6.2 XR Registers:

Bit	7	6	5	4	3	2	1	0
XR0/ R	0	Wake_ up	Caden ce	RING	Caller_ ID	VDD_ OK	SI_1	SI_0
XR0/ W	0	0	0	0	0	SO_2	SO_1	SO_0
XR1	0	M_Wa ke_up	M_Cad ence	M_ RING	M_Call er_ID	M_VD D_OK	M_ SI_1	M_ SI_0
XR2	CTO 7	CTO 6	CTO 5	CTO 4	CTO 3	CTO 2	CTO 1	CTO 0
XR3	AGB1	AGB0	B_off	DCU 1	DCU 0	DCI	DCR 1	DCR0
XR4	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
XR5	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0
XR6	0	0	0	CLK_O FF	0	0	CPS1	CPS0
XR7	0	0	0	0	0	Vdd1	Vdd0	0

Table 6: Summary of CR Registers

7 ALIS Command Structure

The sections below show the structure of the SOP, XOP, COP and CAO write and read commands. Section 7.5 shows an example of a mixed command.

7.1 SOP Commands

7.1.1 SOP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP write 1 byte	x	x	0	1	0	0	0	0		Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP write 2 bytes	x	x	0	1	0	0	0	1		Idle								
CR1	Data									Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP write 3 bytes	x	x	0	1	0	0	1	0		Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP write 4 bytes	x	x	0	1	0	0	1	1		Idle								
CR3	Data									Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								

7.1.2 SOP - Read Commands

DIN	7	6	5	4	3	2	1	0	Bit
SOP read 1 byte	x	x	1	1	0	0	0	0	
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DOUT
Idle								
1	0	0	0	0	0	0	1	ID
Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit
SOP read 2 bytes	x	x	1	1	0	0	0	1	
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DOUT
Idle								
1	0	0	0	0	0	0	1	ID
Data								CR1
Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit
SOP read 3 bytes	x	x	1	1	0	0	1	0	
	Idle								
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DOUT
Idle								
1	0	0	0	0	0	0	1	ID
Data								CR2
Data								CR1
Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit
SOP read 4 bytes	x	x	1	1	0	0	1	1	
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DOUT
Idle								
1	0	0	0	0	0	0	1	ID
Data								CR3
Data								CR2
Data								CR1
Data								CR0

Note: x: in accordance with the description of the power-up operation command. See “SOP Command” on page 38.

7.2 XOP Commands

7.2.1 XOP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP write 2 bytes	0	0	0	1	1	0	0	1		Idle								
XR1	Data									Idle								
XR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP write 3 bytes	0	0	0	1	1	0	1	0		Idle								
XR2	Data									Idle								
XR1	Data									Idle								
XR0	Data									Idle								

7.2.2 XOP - Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP read 1 byte	0	0	1	1	1	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								XR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP read 2 bytes	0	0	1	1	1	0	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								XR1
	Idle									Data								XR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP read 3 bytes	0	0	1	1	1	0	1	0		Idle								

Idle	
Idle	
Idle	
Idle	

1	0	0	0	0	0	0	1	ID
Data								XR2
Data								XR1
Data								XR0

7.3 COP Command

7.3.1 COP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP write 4 bytes	0	0	0	0	b	b	b	b		Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP write 8 bytes	0	0	0	0	b	b	b	b		Idle								
Coeff. 7	Data									Idle								
Coeff. 6	Data									Idle								
Coeff. 5	Data									Idle								
Coeff. 4	Data									Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								

7.3.2 COP - Read Commands

DIN	7	6	5	4	3	2	1	0	Bit
COP read 4 bytes	0	0	1	0	b	b	b	b	
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DOUT
Idle								
1	0	0	0	0	0	0	1	ID
Data								Coeff.3
Data								Coeff.2
Data								Coeff.1
Data								Coeff.0

DIN	7	6	5	4	3	2	1	0	Bit
COP read 8 bytes	0	0	1	0	b	b	b	b	
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DOUT
Idle								
1	0	0	0	0	0	0	1	ID
Data								Coeff.7
Data								Coeff.6
Data								Coeff.5
Data								Coeff.4
Data								Coeff.3
Data								Coeff.2
Data								Coeff.1
Data								Coeff.0

Note: b: in accordance with the description of the COP command. See “COP Command” on page 50.

7.4 CAO Command

7.4.1 CAO - Write Commands

DIN	7 6 5 4 3 2 1 0 Bit	7 6 5 4 3 2 1 0
CAO write	0 1 0 1 1 0 0 0	Idle
	Caller ID 512	Idle
	Caller ID 511	Idle
	Caller ID 510	Idle
	...	Idle
	Caller ID 1	Idle

7.4.2 CAO - Read Commands

DIN	7 6 5 4 3 2 1 0 Bit	7 6 5 4 3 2 1 0	DOUT
CAO read	0 1 1 1 1 0 0 0		
	Idle	1 0 0 0 0 0 0 1	ID
	Idle	Data	Caller ID 512
	Idle	Data	Caller ID 511
	Idle		...
	Idle	Data	Caller ID 1

7.5 Example of a Mixed Command

Every single command must begin with a falling edge of CS.

DIN	7 6 5 4 3 2 1 0	Bit	7 6 5 4 3 2 1 0	DOUT
SOP write 4 bytes	x x 0 1 0 0 1 1		Idle	
CR3	Data		Idle	
CR2	Data		Idle	
CR1	Data		Idle	
CR0	Data		Idle	
XOP write 2 bytes	0 0 0 1 1 0 0 1		Idle	
XR1	Data		Idle	
XR0	Data		Idle	
COP write 4 bytes	0 0 0 0 b b b b		Idle	
Coeff. 3	Data		Idle	
Coeff. 2	Data		Idle	
Coeff. 1	Data		Idle	
Coeff. 0	Data		Idle	
SOP read 3 bytes	x x 1 1 0 0 1 0		Idle	
	Idle		1 0 0 0 0 0 0 1	ID
	Idle		Data	CR2
	Idle		Data	CR1
	Idle		Data	CR0
COP read 4 bytes	0 0 1 0 b b b b		Idle	
	Idle		1 0 0 0 0 0 0 1	ID
	Idle		Data	Coeff.3
	Idle		Data	Coeff.2
	Idle		Data	Coeff.1
	Idle		Data	Coeff.0
XOP read 1 byte	0 0 1 1 1 0 0 0		Idle	
	Idle		1 0 0 0 0 0 0 1	ID
	Idle		Data	XR0

8 Interrupt Controller

There are seven different sources that can cause interrupts in ALIS. The status of these sources are read from interrupt register XR0. Every interrupt source can be enabled individually in interrupt-enable register XR1.

To monitor an interrupt source, the corresponding bit must be set in XR1. If an enabled interrupt indication occurs, the interrupt register XR0 is locked. The lock is released when the interrupt register XR0 is read. Any interrupt indication occurring during a locked period will be detected after the lock has been released.

NOTE: An interrupt is only acknowledged when the appropriate bit has been set in the interrupt-enable register XR1.

The INT pin can be used as an indication to allow external hardware to read the interrupt register. If the Int_en bit (CR4) is set, the INT pin goes to ’1’ whenever the interrupt register is locked.

The host must analyze the bits in the interrupt register to determine the cause of the pending interrupt. All interrupt sources that are not enabled must be ignored by the host in its analysis. It is possible for several sources together to cause only one interrupt! (i.e. breakdown of serial connection to ALIS-A: VDD_OK, SI_0, SI_1; if more interrupts occur during the locked period). If the interrupt was caused by a CADENCE, RING, CALLER_ID or WAKE_UP interrupt, the indication that caused the pending interrupt is reset by reading interrupt register XR0.

As only one interrupt can be stored internally, the host must respond immediately to avoid loss of interrupts.

8.1 Nature and Sources of Interrupts:

There are three different kinds of interrupt indications depending on their source as shown in the sections below.

8.1.1 Interrupt Indication at Signal Change:

Interrupts:	SI_0, SI_1, VDD_OK;
Sources:	Signaling pins at ALIS-A (SI_0, SI_1); VDD_OK indicates that ALIS-A has a power supply and that the serial connection via the cap. interface is working;
Interrupt indication:	Any change in the signals will generate an interrupt. The host must store the previous state of these bits to check which signal caused an interrupt.
Note:	These bits will go to ‘0’ when there is no connection to ALIS-A via the cap. interface. This will cause interrupts!
Lock behaviour:	At *lock-release time,* the current signal is compared to the signal stored at *lock time*. Any difference will cause another interrupt.

8.1.2 Interrupt Indication at Event:

Interrupts:	CALLER_ID, RING, CADENCE;
Sources:	CALLER_ID: Complete marker sequence of caller ID detected; RING: Depending on automatic mode switching: - detection of more than 18 V at TIP/RING (No_auto_ring ’1’); - 2nd valid ringing (No_auto_ring ’0’); CADENCE: Time-out for 2nd ring burst; the time can be programmed in XR2 (No_auto_ring ’0’);
Interrupt indication:	These interrupts indicate that a certain event has occurred. The bits are set from their source and can be reset from the host only by reading the interrupt register. Whenever one of these bits is set, this is an indication that this event has occurred.
Lock behaviour:	If one of these events occurs while the register is locked, another interrupt will be generated as soon as the lock is released.

8.1.3 Interrupt Indication at High Level:

If ALIS-D is set to deep-sleep mode (XR6, CLK_OFF = ’1’), this interrupt indicates that there is a signal greater than 18 V at TIP/RING.

Interrupts:	WAKE_UP;
Source:	ring_detect signal from ALIS-A;
Interrupt indication:	More than 18 V at TIP/RING. It is cleared after the interrupt register has been read. Another interrupt is generated if the signal remains higher than 18 V.
Lock behaviour:	The interrupt will lock the register as soon as clock is turned on again! (If no clock signal is applied to ALIS-D, the other interrupts cannot occur anyway.)

9 Operating Modes

9.1 Reset (Basic Settings Mode)

Condition: RESET low, MCLK can be down

ALIS-D:

After initial application of VDD (power-on reset), reset of the setting pin to ’0’ during operation or a software reset (see XOP command), ALIS-D enters the basic settings mode. Basic settings means that the ALIS-D configuration registers CR0... CR5 and XR0... XR7 are initialized to the default value (sleep mode). All programmable filters are disabled.

If any voltage is applied to any input pin before the initial application of VDD, ALIS may be unable to enter the basic settings mode. In this case, it is necessary to reset ALIS or to initialize its configuration registers to the default value.

ALIS-A:

When the plug is connected to TIP/RING and the hook switch is closed, ALIS-A generates its supply voltage from the line current and performs a power-on reset.

9.2 Deep Sleep Mode

Condition: RESET ’1’, if used the external master clock can be deactivated.

It can be entered from any mode by programming the CLK_OFF bit in XR6. During deep sleep mode, the serial control interface is ready to receive and register commands only when MCLK is switched on (see “XR6 Extended Register 6 (Power State)” on page 49). Incoming rings will be indicated by the Wake_up interrupt.

9.3 Sleep Mode

Condition: RESET ’1’, if used the external master clock must be activated.

When the RESET pin (RESET state) is released, ALIS enters sleep mode. ALIS is forced to sleep mode when the PU (power up) bits are set to '00' in the SOP command. During sleep mode, the serial control interface is ready to receive commands and transmit data. Voice data received on the DAT_IN pin will be ignored. The ALIS configuration registers the caller ID RAM, and the coefficient RAM can be loaded and read back in this mode.

9.4 Ringing Mode

Condition: RESET ’1’, if used the external master clock must be activated.

This mode is entered automatically when bit No_auto_ring is set to 0 from sleep mode after the first ringing pulse or when the PU bits are set to '01' in the SOP command. In this mode, ALIS will measure the level, frequency and cadence of the ringing signal. The cadence between the first two ring bursts is stored in XR4. If the Caller_en bit is enabled, an incoming caller ID will be decoded and stored (see CAO command).

9.5 Conversation Mode

Condition: RESET ’1’, if used the external master clock must be activated.

The operating mode is entered upon recognition of the PU bits set to '10' in a SOP command.

In conversation mode, the AC impedance loops and the DC loops are switched on. The programmed AC and DC characteristics are implemented by these loops. The receive and transmit paths are on. The tone generators are available.

9.6 Pulse Dialing Mode

Condition: RESET ’1’, if used the external master clock must be activated.

The pulse dialing mode is entered by setting the PU bits to '11' in a SOP command.

In pulse dialing mode, the external transistor T1 is switched on and off in accordance with the PULSE bit in CR1. The pulse timing must be controlled by the host.

9.7 Operating Flowchart

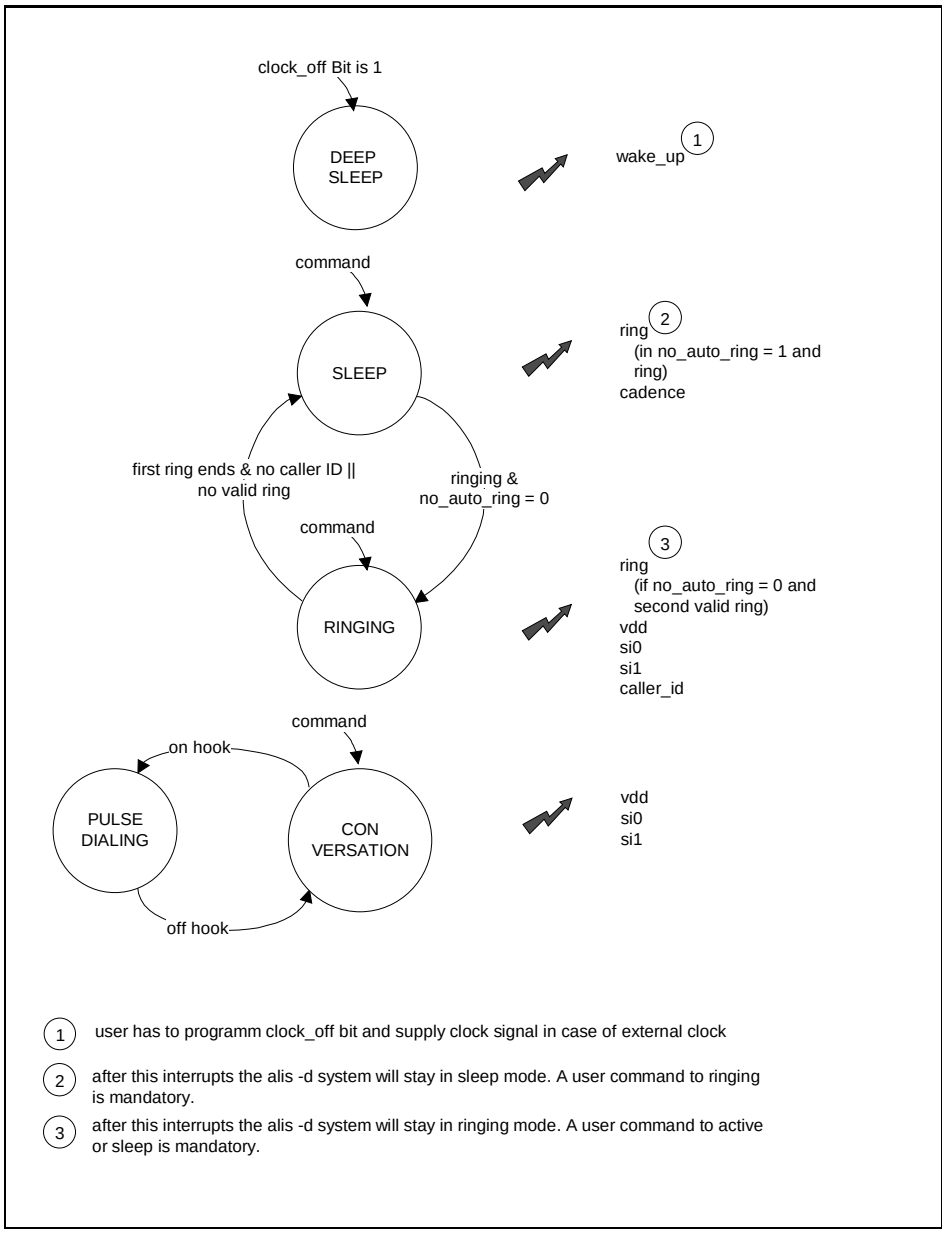


Figure 25 Operating Mode Transitions and Interrupts

9.8 Flow of Ring Sequence and Detection

Ring detection works in ALIS as a two step procedure.

In a first step, ALIS-A will detect any AC signal at TIP and RING with a peak value of more than 18 V and will generate the Ring_detect signal. This signal can either generate an interrupt or switch ALIS to ringing mode depending on the No_auto_ring bit in CR1 (see “CR1 Configuration Register 1 (Dialing)” on page 40). The current power mode can

be read from the register XR6 (see “XR6 Extended Register 6 (Power State)” on page 49).

As a second step, only if enabled by RM (see “CR1 Configuration Register 1 (Dialing)” on page 40) in ringing mode, the TIP/RING signal will be band-filtered and compared to a programmable threshold. If the result is higher than this threshold, the RMR-bit signal is set to one. The ring threshold can be polled as the RMR bit in CR1. The following flow charts show these sequences in more detail.

Note: The initial connection to TIP RING looks like a ring voltage to ALIS-A. The reaction of ALIS-D depends on the auto_ring bit:
a) auto_ring: ALIS-D goes to ringing, since the spike is not a valid ringing signal. ALIS-D then goes to sleep mode.
b) No_auto_ring: ALIS-D generates a ring interrupt, stays in sleep mode and waits for a command. The user has to switch ALIS-D to ringing and poll the RMR bit. If ringing is not valid (RMR bit = 0), the chip can be set back to sleep mode.

To detect a valid ring signal and caller ID, ALIS must be programmed to the following setting:

- set RM to ’1’ (see “CR1 Configuration Register 1 (Dialing)” on page 40)
- cadence time-out must be programmed to PTT requirements (see “XR2 Extended Register 2 (Cadence Time Out)” on page 47)
- ring latency timer must be programmed to a value higher than four times the ring period (see “XR5 Extended Register 5 (Ring Timer)” on page 49)
- valid ring coefficients
- set No_auto_ring to ’0’ (see “CR1 Configuration Register 1 (Dialing)” on page 40)
- enable Call_en (see “CR2 Configuration Register 2 (Caller ID)” on page 41)
- enable corresponding interrupts

9.8.1 Successful Ring Sequence, Auto Ring Enabled, no Caller ID

The following chart and diagram show the successful flow of a ring-event detection with automatic power-mode change (No_auto_ring = 0, Caller_en = 0, RM = 1). In this operating mode, ALIS will not decode a caller ID.

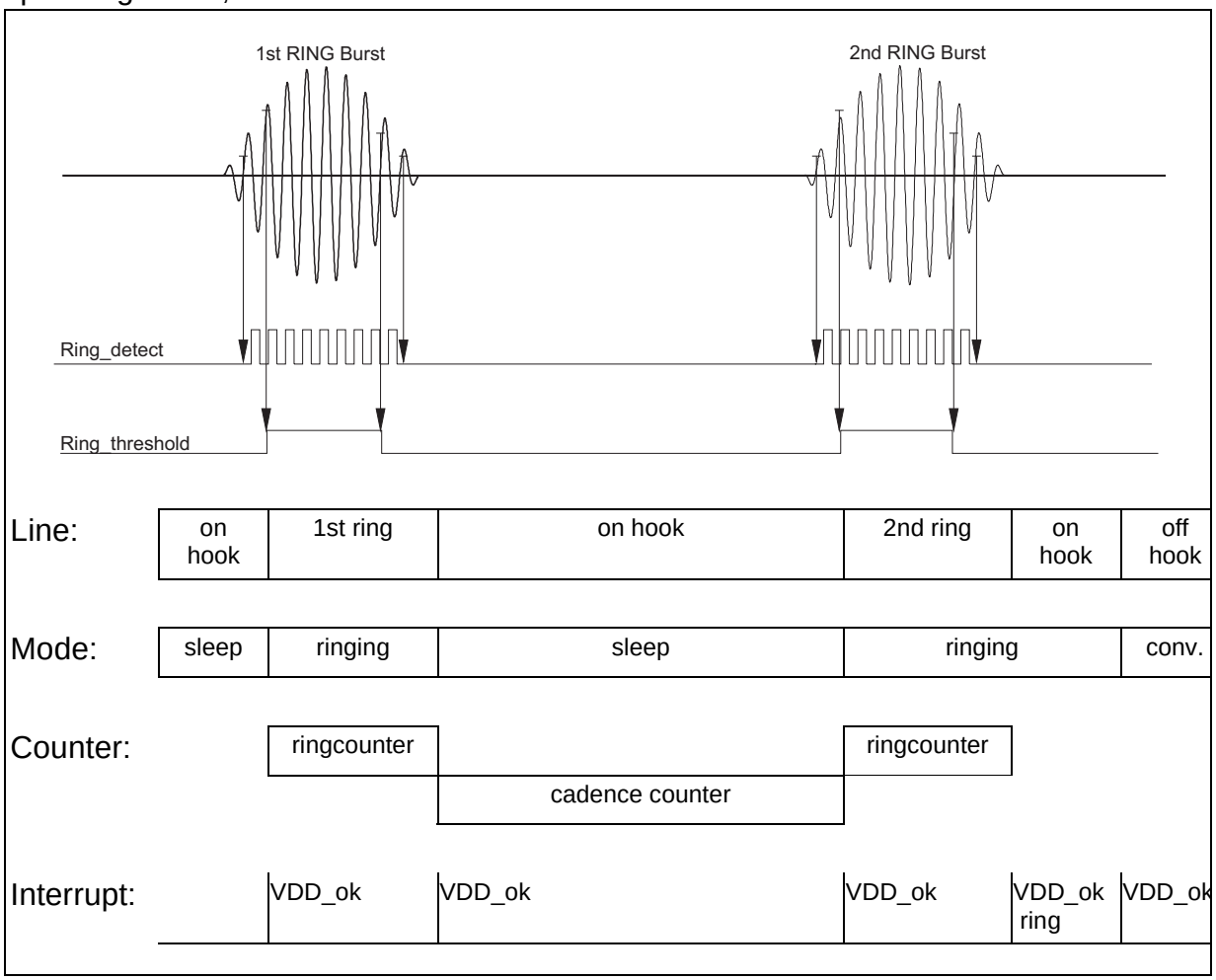


Figure 26 Successful Ring Sequence, No_auto_ring = 0; Caller_en = 0

9.8.2 Successful Ring Sequence, Auto Ring Enabled, Caller ID

The following chart and diagram show the successful flow of a ring-event detection with automatic power-mode change (No_auto_ring = 0, Caller_en = 1, RM = 1). In this operating mode, ALIS will decode and store a caller ID.

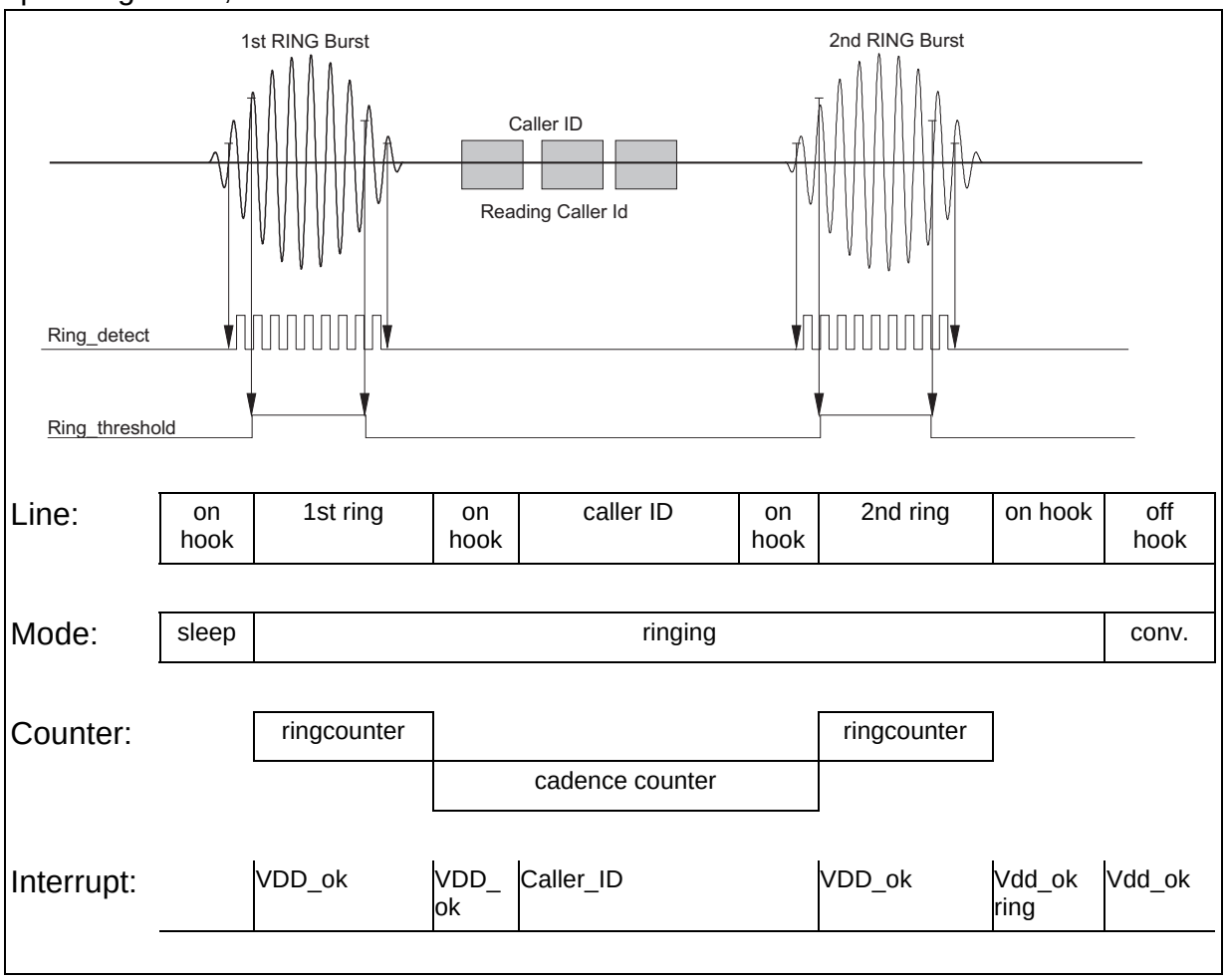


Figure 27 Successful Ring Sequence, No_auto_ring = 0; Caller_en = 1

9.8.3 Unsuccessful Ring Sequence, Auto Ring Enabled, no Caller ID

The following chart and diagram show the unsuccessful flow of a ring-event detection because of no 2nd ring with automatic power-mode change (No_auto_ring = 0, Caller_en = 0, RM = 1).

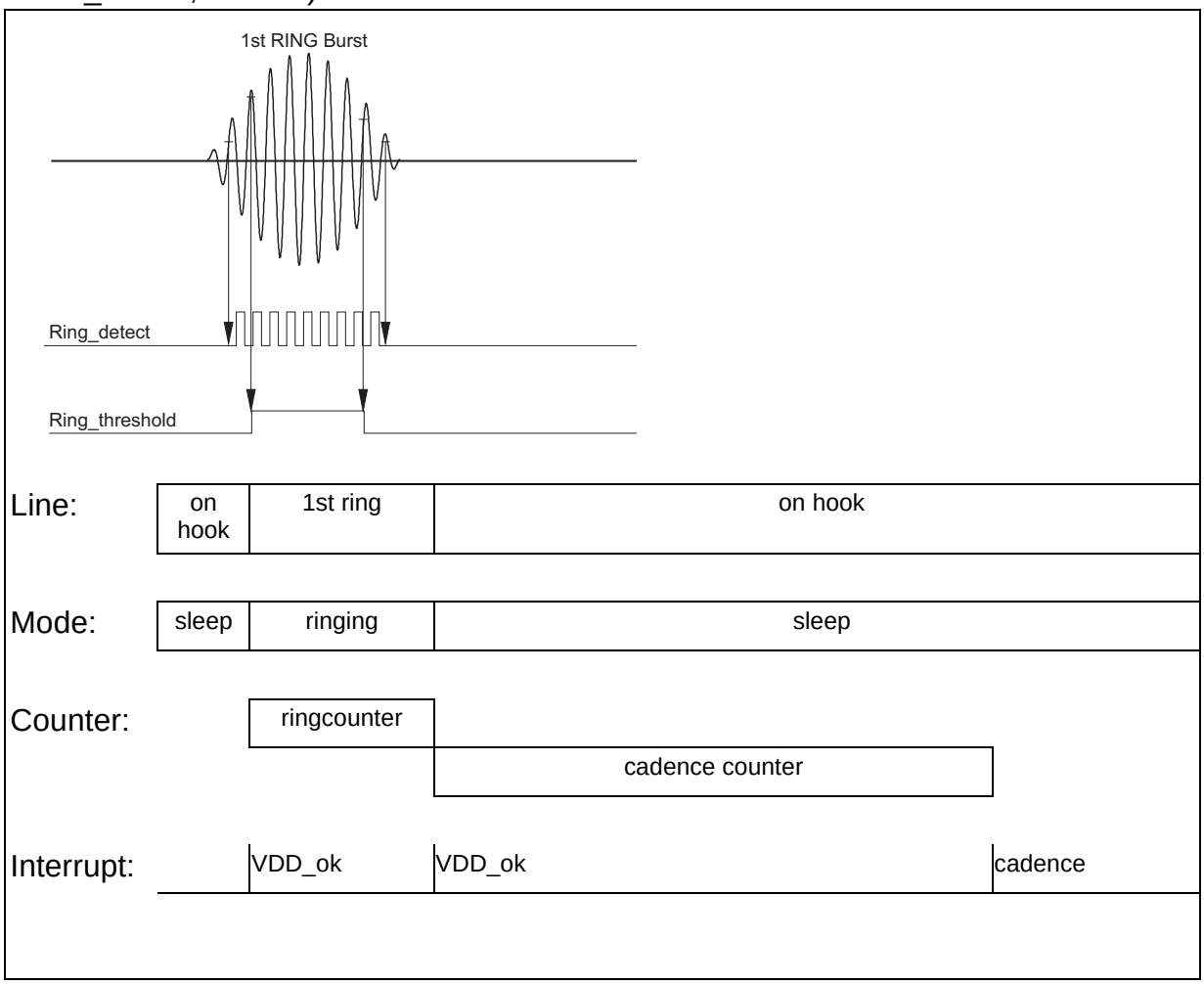


Figure 28 Unsuccessful Ring Sequence, No_auto_ring = 0; Caller_en = 0

9.8.4 Unsuccessful Ring Sequence, Auto Ring Enabled, Caller ID

The following chart and diagram show the unsuccessful flow of a ring-event detection because of no 2nd ring with automatic power-mode change (No_auto_ring = 0, Caller_en = 1, RM = 1).

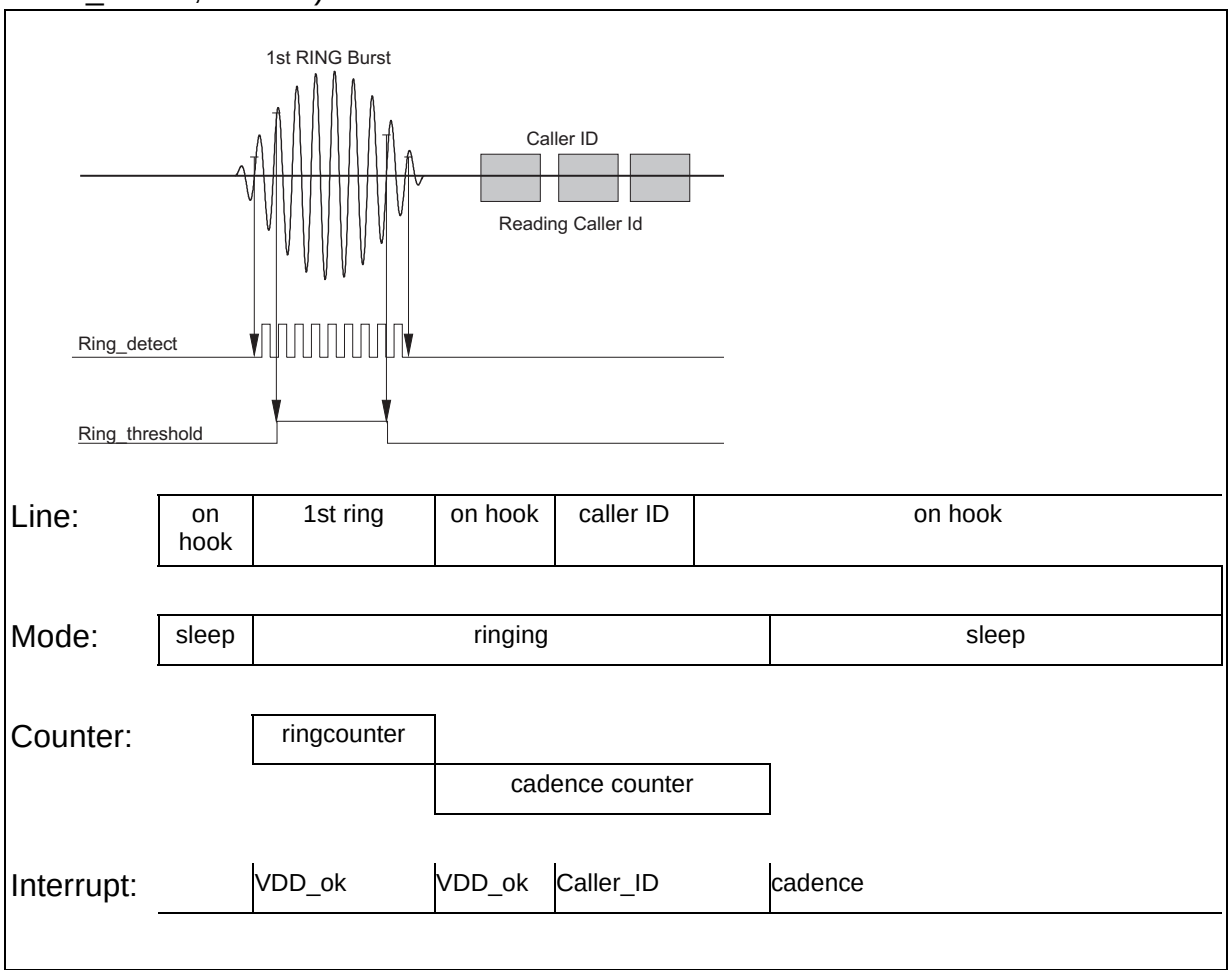


Figure 29 Unsuccessful Ring Sequence, No_auto_ring = 0; Caller_en = 1

9.8.5 Successful Ring Sequence, Auto Ring Disabled, No Caller ID

The following chart and diagram show the successful flow of a ring-event detection with no automatic power-mode change (No_auto_ring = 1, Caller_en = 0, RM = 1). In this operating mode, ALIS will not decode the caller ID.

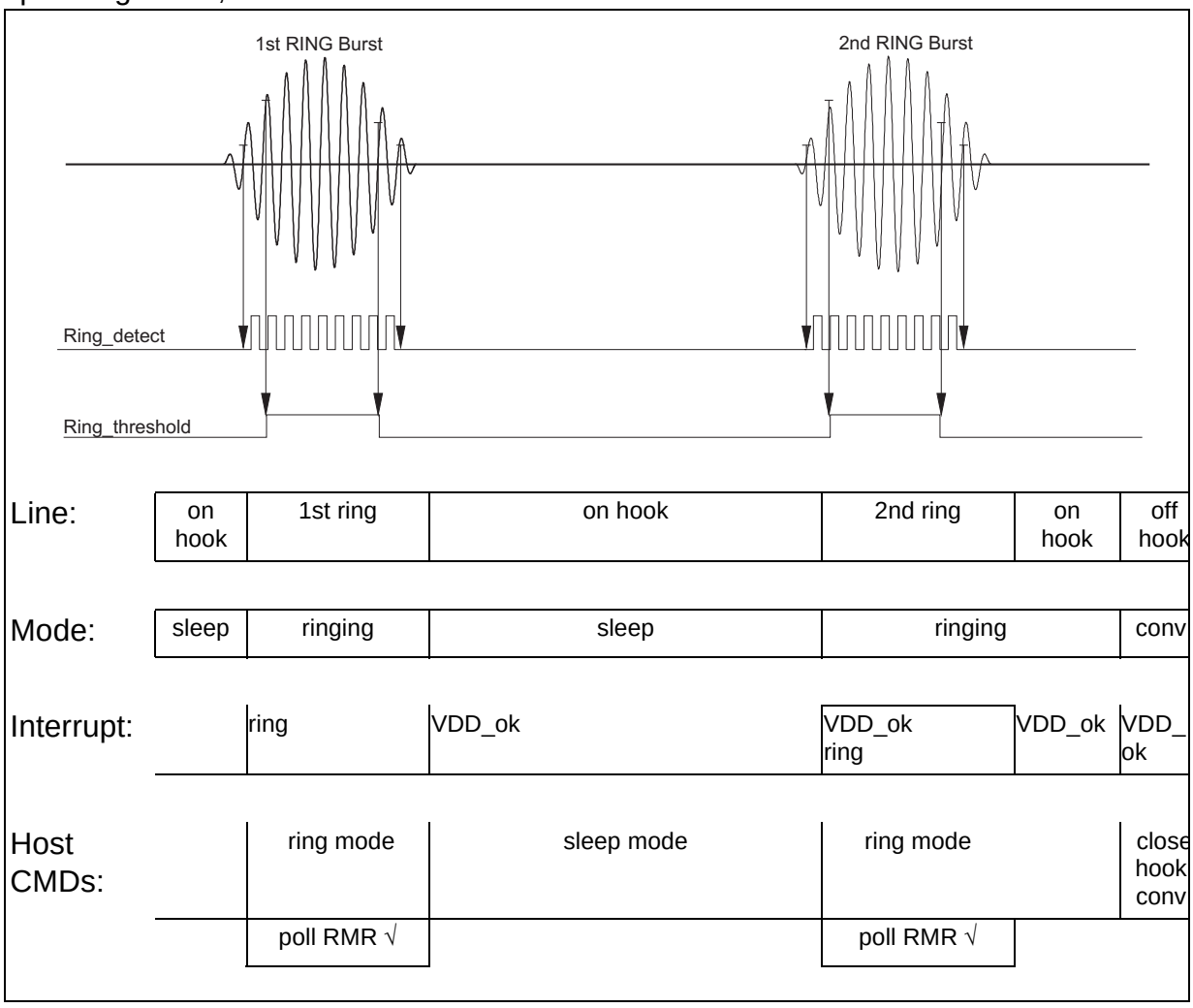


Figure 30 Successful Ring Sequence, No_auto_ring = 0; Caller_en = 0

Note: The RMR bit must be polled by the host to verify that the ringing signal is above the programmed threshold level and check the VDD interrupts.

9.8.6 Successful Ring Sequence, Auto Ring Disabled, Caller ID

The following chart and diagram show the successful flow of a ring-event detection with no automatic power-mode change (No_auto_ring = 1, Caller_en = 1, RM = 1). In this operating mode, ALIS will decode and store the caller ID.

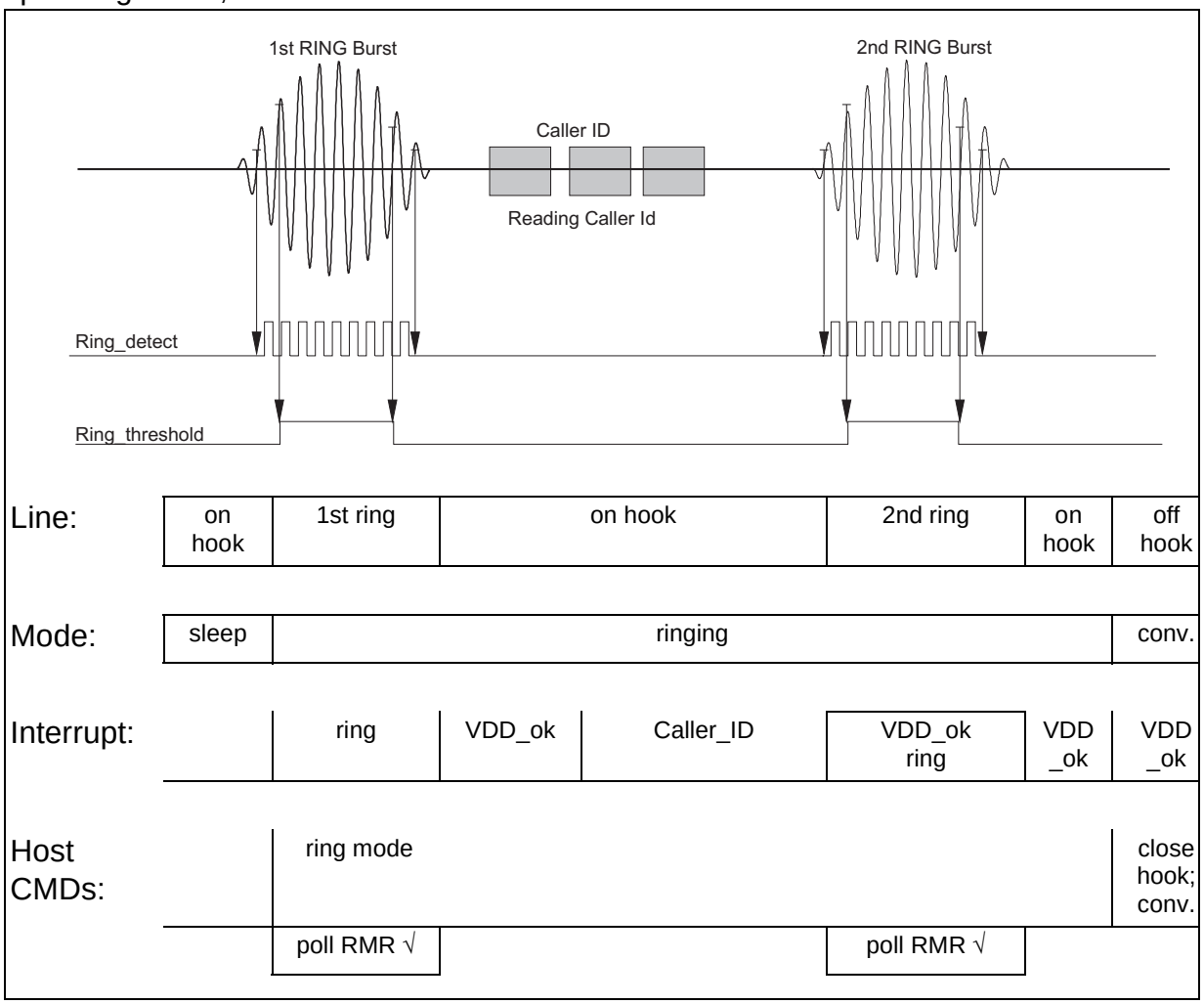


Figure 31 Successful Ring Sequence, No_auto_ring = 1; Caller_en = 1

Note: The RMR bit must be polled by the host to verify that the ringing signal is above the programmed threshold level.
By leaving ALIS in ringing mode after the first ring, the caller ID can be detected and stored.

9.8.7 Unsuccessful Ring Sequence, Auto Ring Disabled, no Caller ID

The following chart and diagram show the unsuccessful flow of a ring-event detection because of no 2nd ring with no automatic power-mode change (No_auto_ring = 1, Caller_en = 0, RM = 1).

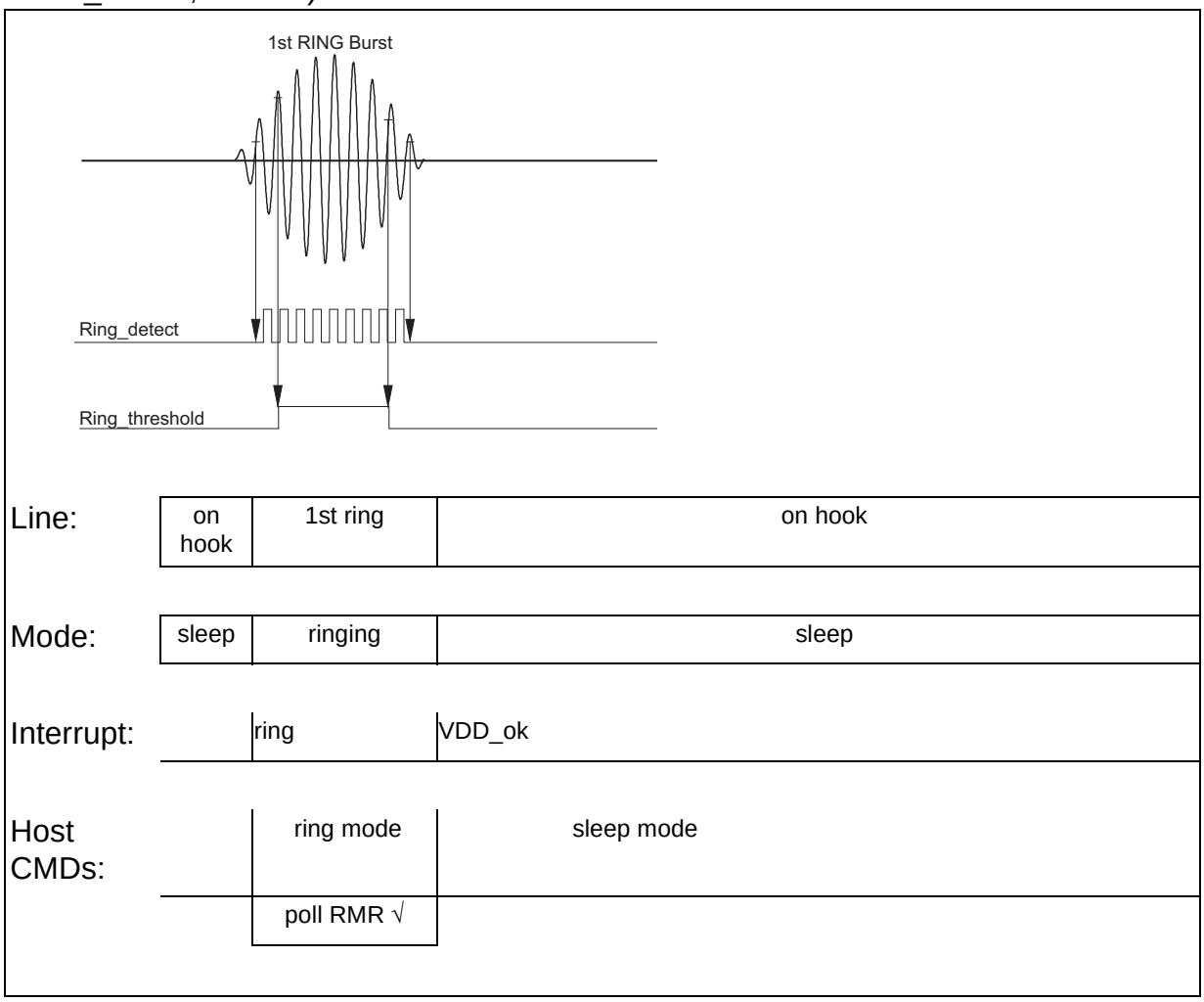


Figure 32 Unsuccessful Ring Sequence, No_auto_ring = 1; Caller_en = 0

Note: The RMR bit must be polled by the host to verify that the ringing signal is above the programmed threshold level.
The cadence time and number of rings must be calculated by the host.

9.8.8 Unsuccessful Ring Sequence, Auto Ring Disabled, Caller ID

The following chart and diagram show the unsuccessful flow of a ring-event detection because of no 2nd ring with no automatic power-mode change (No_auto_ring = 0, Caller_en = 1, RM = 1). .

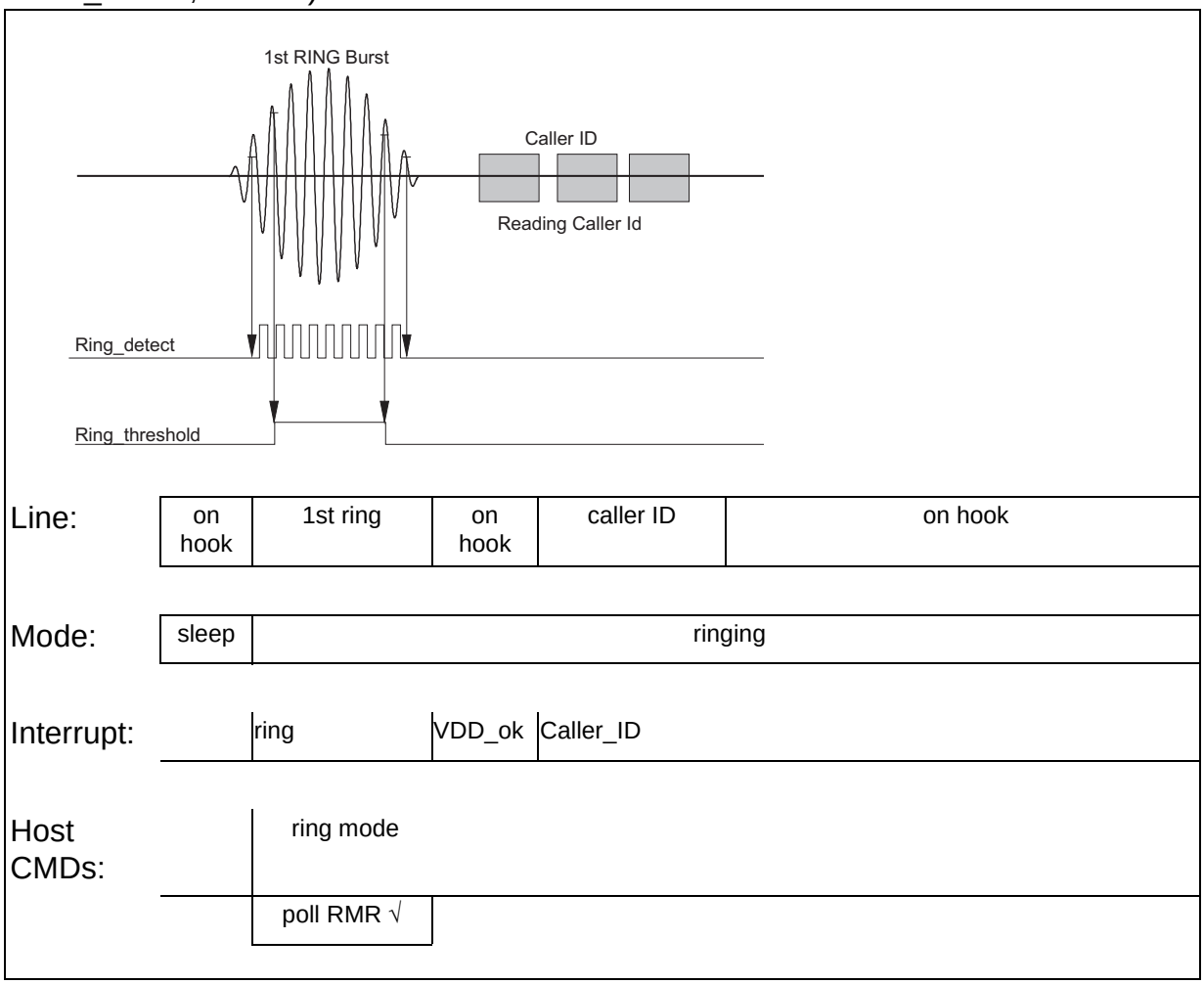


Figure 33 Unsuccessful Ring Sequence, No_auto_ring = 1; Caller_en = 1

Note: The cadence time and the number of rings must be calculated by the host.

9.8.9 Unsuccessful Ring Sequence, Auto Ring Enabled

The following chart and diagram shows an unsuccessful flow of a ring-event detection because ringing is below the ring threshold level with an automatic power-mode change (No_auto_ring = 0, RM = 1).

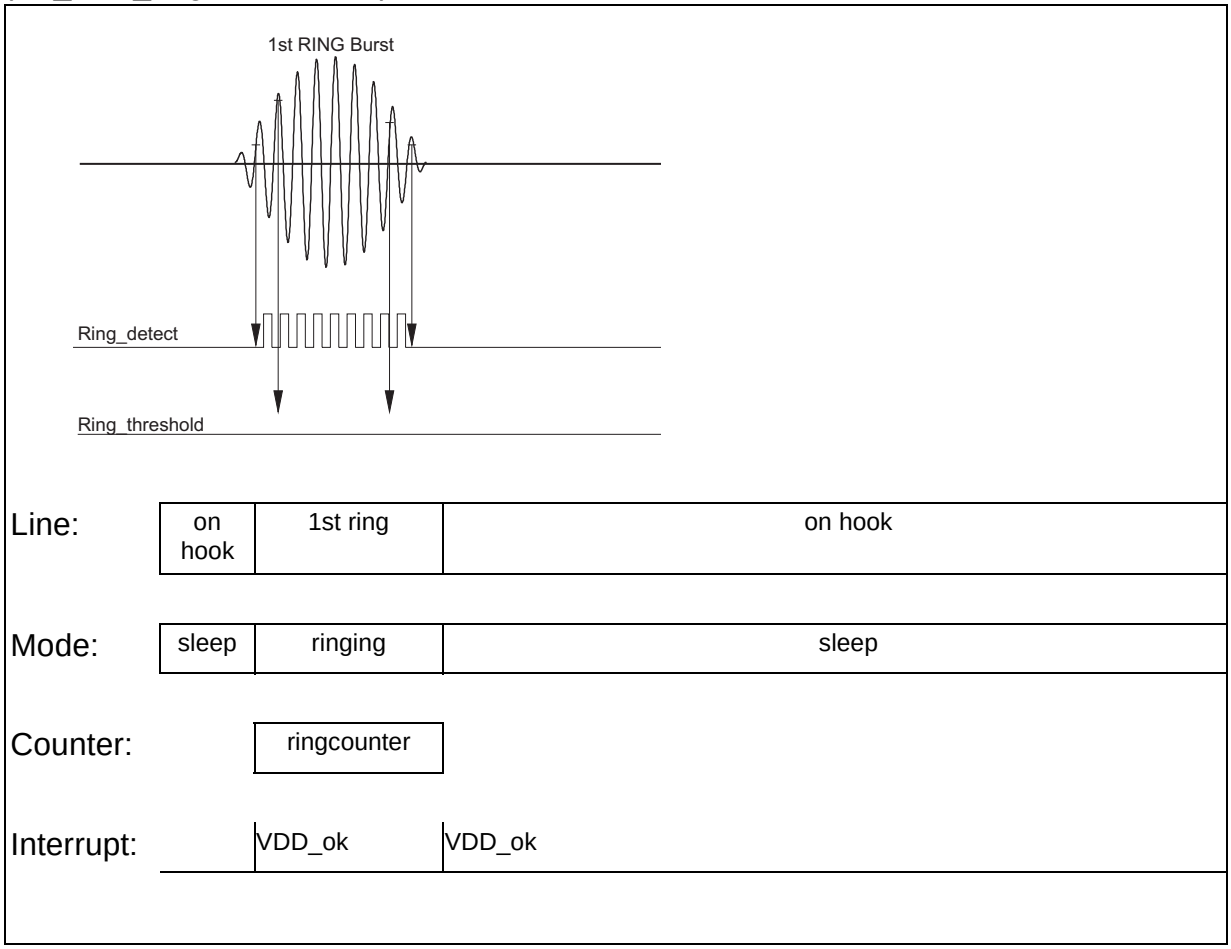


Figure 34 Unsuccessful Ring Sequence, No_auto_ring = 0

9.8.10 Unsuccessful Ring Sequence, Auto Ring Disabled

The following chart and diagram show an unsuccessful flow of a ring-event detection because ringing is below the ring threshold level with no automatic power-mode change (No_auto_ring = 1, RM = 1).

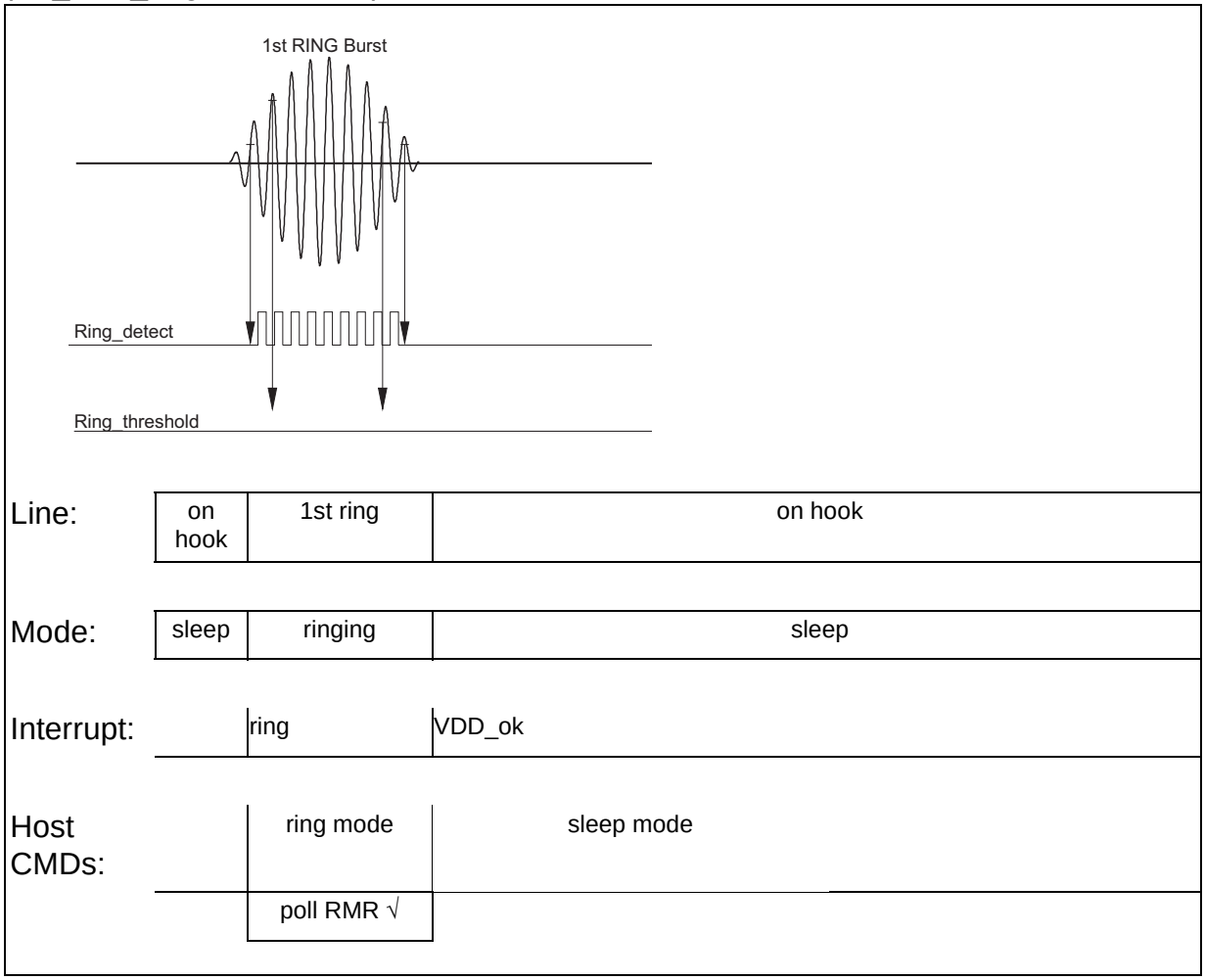


Figure 35 Unsuccessful Ring Sequence, No_auto_ring = 0

Note: RMR will not be '1'

9.8.11 Start from Deep Sleep Mode

The following chart and diagram show a start-up procedure from deep sleep mode.

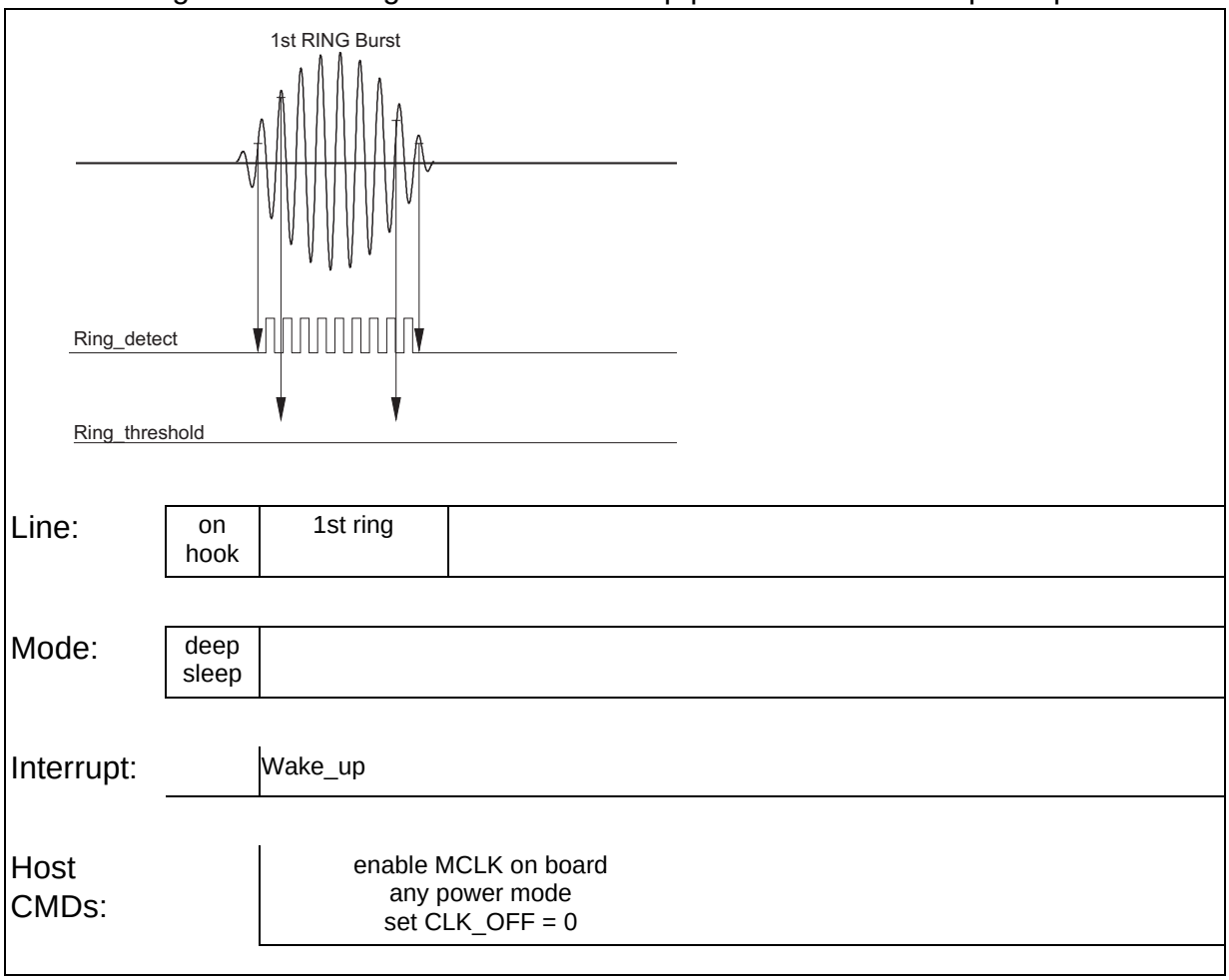


Figure 36 Deep Sleep Start

Note: After the wake_up interrupt, any power mode and operation flow can be programmed as described in the previous sections .

10 Modem Functions

10.1 Pulse Dialing

Pulse dialing will be implemented by shortening the line with external transistor T1. Pulse timing must be controlled by the host. Pulse shaping is implemented in ALIS-A and complies with ETS 300 001

10.2 DTMF Dialing

DTMF Dialing is implemented by two internal tone generators (see “Programming the ALIS DTMF Tone Generators” on page 78). Since the level of tone generator 2 is 3 dB higher than that of tone generator 1, the former should be used for the high frequency group. The frequency accuracy of the tone generators is better than ±1%. The absolute transmission level can be programmed using the AX filter. Software for computing the coefficients is available.
The tone generators can also be used to generate any in-band sine wave for test or measurement purposes.

10.2.1 Programming the ALIS DTMF Tone Generators

Two independent tone generators are available. When one or both of them are turned on, the voice signal is switched off automatically. A programmable bandpass filter is included to make the generated signal suitable for DTMF. The default frequency for both tone generators is 2000 Hz. Coefficients for other frequencies are generated by a software tool.

Byte sequences for programming both tone generators and bandpass filters:

Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
697 Hz	0B *)	11	B3	5A	2C
770 Hz	0B *)	12	33	5A	C3
852 Hz	0B *)	13	3C	5B	32
941 Hz	0B *)	1D	1B	5C	CC
1209 Hz	0C *)	32	32	52	B3
1336 Hz	0C *)	EC	1D	52	22
1477 Hz	0C *)	AA	AC	51	D2
1633 Hz	0C *)	9B	3B	51	25

*) 0B is used for programming tone generator 1
0C is used for programming tone generator 2

Table 7: Programming the tone generators

The sine wave is filtered by a bandpass, the Q factor of this band filter can be altered in the range from 0 to 7 and can be programmed by setting the first nibble of byte 3 to the corresponding value (always 5 in this table). The resulting signal amplitude can be set by programming the filters AR1 and AR2.

10.3 Caller ID

The caller ID interface is compatible with Bellcore TR-NWT-000030 and SR-TSV-002476 as regards generic requirements for transmitting asynchronous voice-band data to customer premises equipment (CPE) from a serving stored-control switching system (SPCS) or a central office (CO). In this service, the information about the calling party is embedded in the silent interval between the first and the second ring. During this period, ALIS receives and stores up to 4096 bits of the1200-baud FSK signal. The decoding also complies with BELL 202 and CCITT V.23 specifications. (see “Programming the ALIS Caller ID Coefficients” on page 81)

10.3.1 Characteristics for Caller ID

Parameter	Sym-bol	Limit Values			Unit	Reference
		min	typ	max		
Input detection level	Vin	-36 12.3		-9 275	dBm mV	
Detect frequencies Bell 202 1 (mark) Bell 202 0 (space) CCITT V.23 1 (mark) CCITT V.23 0 (space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	 Bell 202 CCITT V.23
Input noise tolerance	SNR	20			dB	
Input baud rate		1188	1200	1212	Hz	

Table 8: Characteristics of Caller ID

10.3.2 Storage and Reading of Caller ID

The storage of the decoded caller ID is enabled after the first space following the mark state. This event will be indicated by the caller ID interrupt. The maximum storage size is 4096 bits. Start, stop-bit and check-sum decoding must be performed by the host.

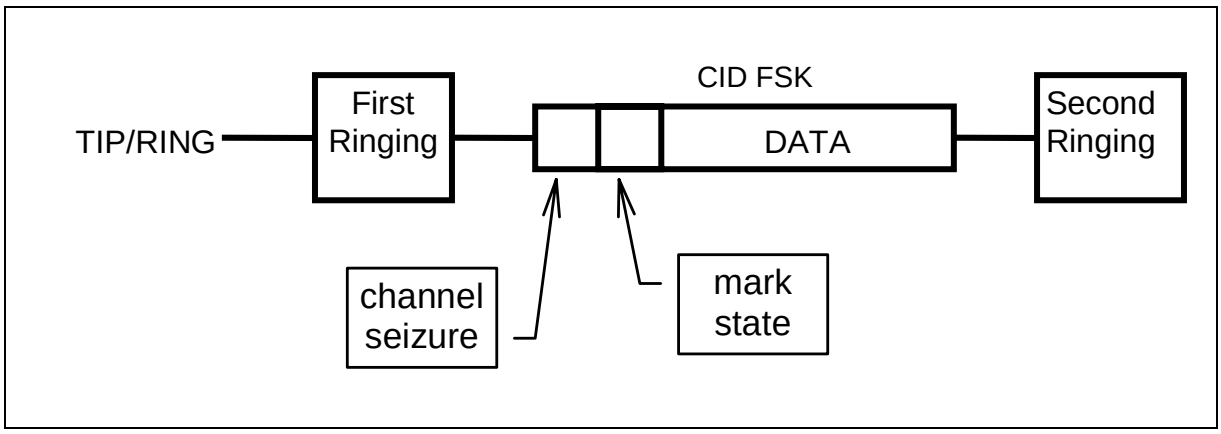
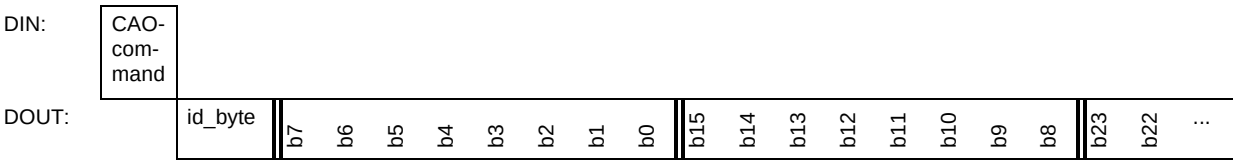


Figure 37 CID Input Timing

When the RAM is read with the CAO command, the received bits will be sent from ALIS in the following order:



b0 is the first caller ID data bit after the ’0’ which ends the marker sequence, b1 the second, b2 the third etc. ...

The host can read the caller ID RAM at any time. Note that the read data may be erroneous when caller ID data is received at the same time, as old and new data might be mixed. However, the received caller ID bits are stored correctly in the RAM!

-> Try not to read the RAM while the caller ID is being received!

10.3.3 Programming the ALIS Caller ID Coefficients

Frequency	Command	Byte 1,2	Byte 3,4	Byte 5,6	Byte 7,8
BELL 202 / CCITT V.23	0E (CID1)	CA 0E	CA 09	99 99	99 99
	0F (CID2)	FD B5	BA 07	DA XX	XX XX

Table 9: Programming the ALIS Caller ID Coefficients

10.4 Billing Pulse

Billing pulse frequencies of 12 and 16 kHz are filtered out by the digital part of ALIS. No external components are necessary for blocking.

10.5 Ring Detect

10.5.1 Functional Description

In sleep mode, any signal greater than a typical value of 18 volts will be detected. Depending on the No_auto_ring bit, either an interrupt will occur or ALIS will be switched automatically to ringing mode. In this mode, the ringing signal will be passed to ALIS-D and decoded. If the ring burst does not meet the programmed requirements within a programmable time, ALIS will return to sleep mode. After a latency time, ALIS will decode the caller ID. When the second valid ring burst occurs, a ring interrupt is generated, signalling the incoming call to the host (see “Flow of Ring Sequence and Detection” on page 65)

10.5.2 Programming the ALIS Ring Detect Coefficients

Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
25 Hz 70Vrms 10 kΩ 1.0 µF	0D	AA	05	0F	8E
	Command	**Byte 1,2**	**Byte 3,4**	**Byte 5,6**	**Byte 7,8**
	03	1C B3	AB AB	54 2D	62 2D
	06	2D 62	A6 BB	2A 7D	0A D4

Table 10: Programming ALIS Ring Detect Coefficients

Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
50 Hz 50Vrms 10kΩ 0.6 µF	0D	22	15	B5	84
	Command	**Byte 1,2**	**Byte 3,4**	**Byte 5,6**	**Byte 7,8**
	03	1C A4	AA AB	BD 2B	A2 2D
	06	2B A2	A6 BB	2C 63	3A D4

Table 11: Programming ALIS Ring Detect Coefficients

10.5.3 Ring Threshold in Sleep Mode

Parameter	Symbol	Limit Values			Unit	Reference
		min	typ	max		
Ring Threshold			12	18	Vrms	

Table 12: Ring Threshold in Sleep Mode

11 Electrical Characteristics

11.1 Programmable Filters

A set of programmable filters is used to adapt the whole system to:

- country standards
- board designs (EMI capacitors etc.)
- data pumps
- telephone lines

Note: All these coefficients will be computed by a coefficient program. Any change in these computed values may cause a loss of performance or instability.

In detail, the following filters are programmable:

- Trans-hybrid balancing (TH) filter
- Trans-hybrid pre-balancing filter
- Impedance matching (IM) filter
- Frequency response receive (FRR) filter
- Frequency response transmit (FRX) filter
- Ringer impedance

Amplification/attenuation transmit (AX) filter

Gain for AX filter

range 3.. -14 dB: step size 0.02 .. 0.05 dB

range -14 .. -24 dB: step size 0.5 dB

Gain for AGX

range 3.5, 0 -2.5, -6

Amplification/attenuation receive (AR) filter

Gain for AR filter

range -3 .. 14 dB: step size 0.02 .. 0.05 dB

range 14 .. 24 dB: step size 0.5 dB

Gain for AGR_R:

range 0, 3.5, 6 dB

Gain for AGR_Z:

range -3.5, 0, 2.5, 6 dB

11.2 DC Characteristics

The filter coefficients are generated by a software tool including a high-level model of ALIS and additional user-defined or application-specific system components.

11.2.1 DC Termination

The DC termination is enabled in conversation mode and is disabled during ringing mode, puls dialing mode and sleep mode. The DC termination can be programmed according to the formula:

for i < Imax

$$i(u) = \frac{(u - Uo)}{R}$$

for i > Imax

$$i(u) = Imax$$

Note: U_0 is the sum of the U value listed in table 14 and the flow voltage of the diodes in the external bridge (typ. 2 x 0.4 V)

11.2.2 Programming Ranges for DC Termination

Imax
50 mA
100 mA

Table 13: Programming Range for Imax

U (DCU)
0 V
1.5 V
3.5 V
7.2 V

Table 14: Programming Range for U

R (DCR)
70 Ω
100 Ω
200 Ω
240 Ω
280 Ω

Table 15: Programming Range for R

Note: For programming details, see "XR3 Extended Register 3 (DC Characteristic)" on page 47

11.2.3 Input Current in Puls Dialing Mode

Uab = 30 V DC

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Input current at break	Iin			500	µA

Table 16: Input Current in Puls Dialing Mode

11.3 AC Termination

11.3.1 Ringer Impedance

Programming of the ringer impedance is supported by a software tool. The following table shows typical values.

Uab = 70 Vrms

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Ringer impedance (20 Hz < f <60 Hz)[1)]	Rin	5	10	25	kΩ
Typical capacitors	Cin	0.6		1	µF
Ringer impedance in other modes[2)]					

1) The frequency range can be changed

2) Ringer impedance is generated only in ring mode

Table 17: Ringer Impedance

11.4 ALIS Caller ID Interface

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Capacitance	Cin		50		nF
Rin	Rin		50		kΩ
Rfb	Rfb		200		kΩ

Table 18: ALIS Caller ID Interface

11.4.1 Ring Detect Levels and Frequencies

.

Parameter	Symbol	Limit Values			Unit	Tolerance
		min	typ	max		
Range of programs for ring-level detection	Vring	30		100	V	±10%
Ring-level detection step size	Δ Vring			10	V	±10%
Range of programs for frequency detection	Fring	20		60	Hz	±10%

Table 19: Ring Detect Levels and Frequencies

11.5 ALIS Cap Interface

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Capacitance	Cin	5	10	1000	pF
Tolerance between CAP_x1 and CAP_x2				5	%
Inductance				10	nH
Isolation		2	4		kV

Table 20: ALIS Cap Interface

12 Electrical Performance Characteristic

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		min	max	
Digital supply voltage	VDD	-0.3	7.0	V
Analog supply voltage	VDDA	-0.3	7.0	V
Analog input and output voltage	Vin, Vout	-0.3	VDDA + 0.3	V
Digital input voltages	VDin	-0.3	VDD + 0.3	V
DC input and output current	Iin, Iout	-10	10	mA
Storage temperature	TST	-60	125	°C
Ambient temperature under bias	TA	-10	80	°C
Max. power dissipation	PDmax		1	W

Note: Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at maximum levels may degrade performance and affect reliability.

Table 21: Absolute Maximum Ratings

12.2 Recommended Operating Conditions

Parameter	Symbol	Conditions			Unit
		min	typ	max	
Digital supply voltage	VDD	4.75	5.0	5.25	V
Analog supply voltage ALIS-A (programmed to 4.25 V)	VDDA	4.00	4.25		V
Analog supply voltage ALIS-D	VDDA	4.75	5.0	5.25	V
Ambient temperature under bias	TA	0		70	°C
Operating frequency	fclk		16.384	20**	MHz
Clock duty cycle		45	50	55	%
Signal rise and fall time	tr, tf			20	ns

Note: Extended operation outside the recommended limits may degrade performance and affect reliability.

*Note: **This value is guaranteed by design. Characterization and periodically samples will be applied to production devices at this test conditions.*

Table 22: Recommended Operating Conditions

12.3 DC Characteristics

12.3.1 ALIS-A

VDDA= 4.25V progr.; TA=0 - 70°C

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min	typ	max	
Power-up time	tPU				100	ms
VDDA supply current[1)]						
Ringing mode[2)]	IDDA1	Vring=60V DC + 90Vrms, fring=25 - 50Hz		2.5	3	mA
Conversation mode[3)]	IDDA2	fclk=16.384MHz		7	10	mA
Pulse dialing mode	IDDA3	Vab=30 V DC			500	µA
Digital interface						

Low-level input voltage	VIL[4)]				0.8	V
High-level input voltage	VIH[4)]		2.0			V
Low-level output voltage	VOL[5)]	IOL=5mA			0.5	V
High-level output voltage	VOH[5)]	IOH=-5mA	3.25			V
Input current low	IIL	VIL=GNDA			±1	µA
Input current high	IIH	VIH=VDDA			±1	µA
Input resistance						
Sleep mode	Rin	note[6)]				MΩ
Conversation mode	Rin	see 10.2.3				Ω
Pulse dialing mode	Rin	Inter-pulsing period (make)			200	Ω
Ring threshold	VRThresh	VDDA=4.25V ext.			15	VRMS
Power supply rejection	PSRR	Ripple: 0-150kHz; 70mVrms				
either supply/direction		300Hz - 3.4kHz	40			dB
either supply/direction		3.4kHz - 150kHz	25			dB

1) Will be taken from TIP/RING when the hook switch is open

2) In ringing mode the ringer impedance will be synthesized. Therefore a current according to this impedance will flow from TIP/RING. This current is taken out of the ring burst as an AC current.

3) In conversation mode the DC characteristic will be synthesized and a current according to this characteristic will flow from TIP/RING.

4) Digital Inputs: Test, SI_0, SI_1

5) Digital Outputs: SO_0, SO_1Q

6) Within this mode the hook switch must be open and the input resistance is infinite.

Table 23: DC Characteristics ALIS-A

12.3.2 ALIS-D

VDD = VDDA= 5V± 5%; TA=0 - 70°C

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min	typ	max	
Supply current		VDD=5V, no loads				
Deep sleep mode	IDD0			<10	50	µA
Sleep mode	IDD1	fclk = 16.384 MHz		3.5	10	mA
Ringing mode	IDD2			8.0	15	mA
Conversation mode	IDD3			13	25	mA
Pulse dialing mode	IDD4			8.0	15	mA
Low-level input voltage	VIL1[1)] VIL2[2)] VIL3[3)]				0.8 1.5 0.5	V
High-level input voltage	VIH1[1)] VIH2[2)] VIH3[3)]		2.0 3.5 3.5			V
Low-level output voltage	VOL[4)]	IOL=5mA			0.5	V
High-level output voltage	VOH[4)]	IOH=-5mA	VDD-0.5			V
Input current low	IIL[1,2)]	VIL=GND			±1	µA
Input current high	IIH[1,2)]	VIH=VDD			±1	µA
Tri-state current low	IOZL[5)]	VIL=GND			±1	µA
Tri-state current high	IOZH[5)]	VIH=VDD			±1	µA

1) TTL Inputs: DCLK, CS, DIN, DAT_CLK, DAT_IN, MODE, FSC

2) CMOS Input: RESET

3) Clock Input: MCLK1

4) Outputs: DOUT, INT, DAT_OUT, FSC

5) Tristates, Bidirectionals: DOUT, FSC

Table 24: DC Characteristics ALIS-D

12.4 AC Transmission Characteristics

Unless otherwise stated, the transmission characteristics are guaranteed within the following test conditions:

TA=0 °C to 70 °C

VDD=5V ±5%

VDDA=4.25V (generated from ALIS-A)

Line impedance ZL = 600 ± 0.1% Ohms

Termination impedance ZM = 600 Ohms

digital: 0dBm0 = -3 dB FS

analog: 0 dBm is equal to the voltage of 0.775 Vrms when loaded with 600 Ohms

0 dBm = 0dBm0

f=1004Hz.

2 V_{RMS} metering at 12 or 16 kHZ

VDDA programmed to 4,25 V: $V_{TIP/RING}$>=6,8 V

VDDA programmed to 4 V: $V_{TIP/RING}$>=6,5 V

12.4.1 Absolute Gain Error

AGX=AGR=0 dB

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
Absolute gain error receive	AE_R					-10 dBm
TA=25 °C; VDDA=4.25V		-1	±0.5	+1	dB	
TA=0-70 °C; VDDA=4.25V		-1.2	±0.7	+1.2	dB	
Absolute gain error transmit	AE_X					-10 dBm0
TA=25 °C; VDDA=4.25V		-1	±0.5	+1	dB	
TA=0-70 °C; VDDA=4.25V		-1.2	±0.7	+1.2	dB	

Table 25: Absolute gain error

12.4.2 Gain Tracking

AGX=AGR=0dB

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
Gain tracking receive	GT_R	-0.15	±0.01	0.15		0 to -10 dBm
		-0.15	±0.01	0.15		-30 to -40 dBm
		-0.3	±0.07	0.3		-40 to -50 0.dBm
Gain tracking transmit	GT_X	-0.5	±0.05	0.5		0 to -10 dBm0
		-0.1	±0.07	0.1		-10 to -40 dBm0
		-0.5	±0.3	0.5		-40 to -50 dBm0

Table 26: Gain Tracking

12.4.3 Harmonic Distortion plus Noise

-10 dBm0; ZL= 600 Ω; f=1004 Hz

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
HDN receive	THDN_R_c	74	77		dBFS	C-weighted
HDN transmit	THDN_T_c	74	77		dBFS	
HDN receive	THDN_R_l	72	75		dBFS	linear-weighted[1)]
HDN transmit	THDN_T_l	72	75		dBFS	

1) Linear weighted values are guaranteed by design, characterization, and periodically samples and testing production devices at this test conditions

Table 27: Harmonic Distortion plus Noise

12.4.4 Harmonic Distortion

-10 dBm0; ZL= 600 Ω; f=100 to 2000 Hz, 2nd and 3rd harmonic

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
HD receive	HDN_R	80			dB	
HD transmit	HDN_T	80			dB	
HD of echo signals via TIP/RING	HDN_E_l	80			dB	

Table 28: Harmonic Distortion for Echo Signals

12.4.5 Return Loss

The return loss at a level of 0 dBm0 will be better than 16 dB in a 300-3600 Hz bandwidth using the following set of defined impedances

600 Ohms

220 Ohms + (820 Ohms in parallel with 115 nF)

120 Ohms + (820 Ohms in parallel with 110 nF)

370 Ohms + (620 Ohms in parallel with 310 nF)

12.4.6 Frequency Response

12.4.6.1 Receive

Reference frequency 1kHz, input signal level 0dBm0

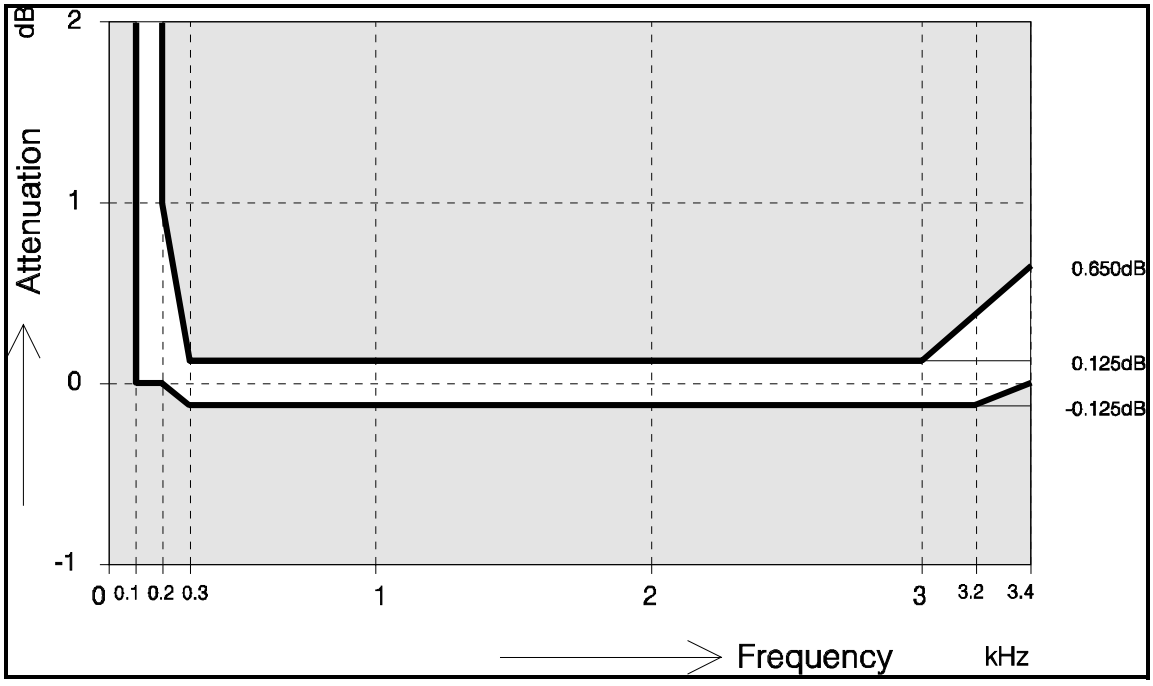


Figure 38 Frequency Response Receive

12.4.6.2 Transmit

Reference frequency 1kHz, input signal level 0dBm0

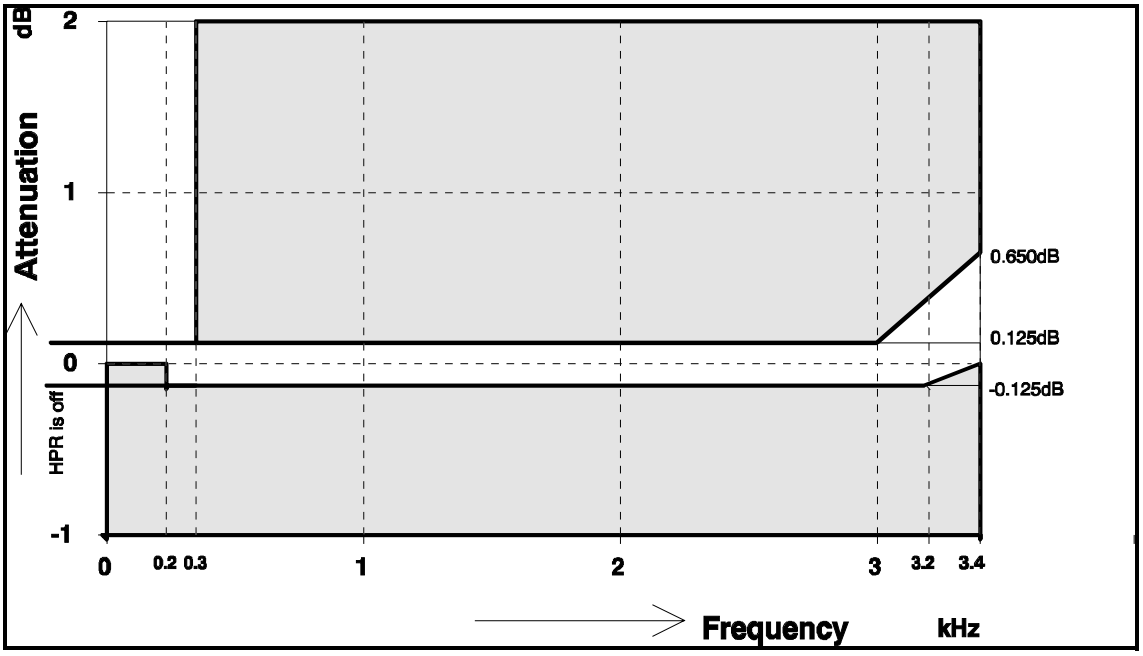


Figure 39 Frequency Response Transmit

12.4.7 Group Delay

Maximum delays when ALIS is operating with H(TH)=H(IM)=0 and H(FRR)=H(FRX)=1 including the delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group Delay deviations remain within the limits in the figures below.

12.4.7.1 Group Delay Absolute Values

Parameter	Symbol	Limit Values			Unit	Reference
		min	typ	max		
Receive delay	DRA			340	µs	Input signal level 0 dBm0
Transmit delay	DXA			400	µs	

Table 29: Group Delay

12.4.7.2 Group Delay Distortion Receive

Input signal level 0dBm0

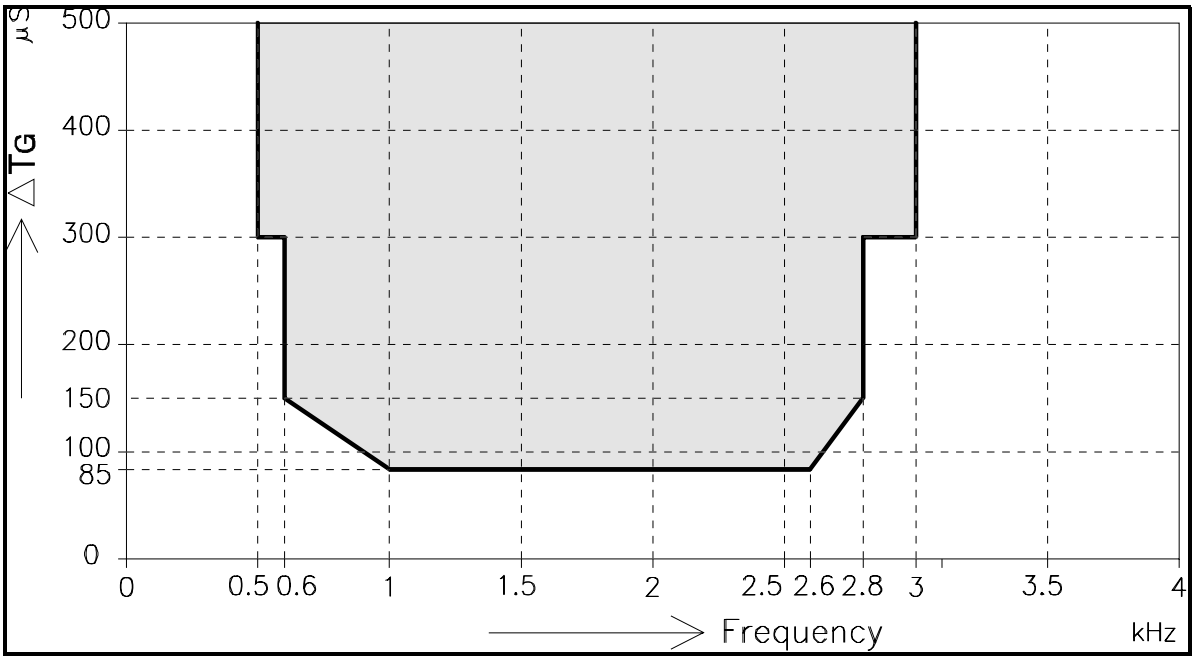


Figure 40 Group Delay Distortion Receive

12.4.7.3 Group Delay Distortion Transmit

Input signal level 0dBm0 [1])

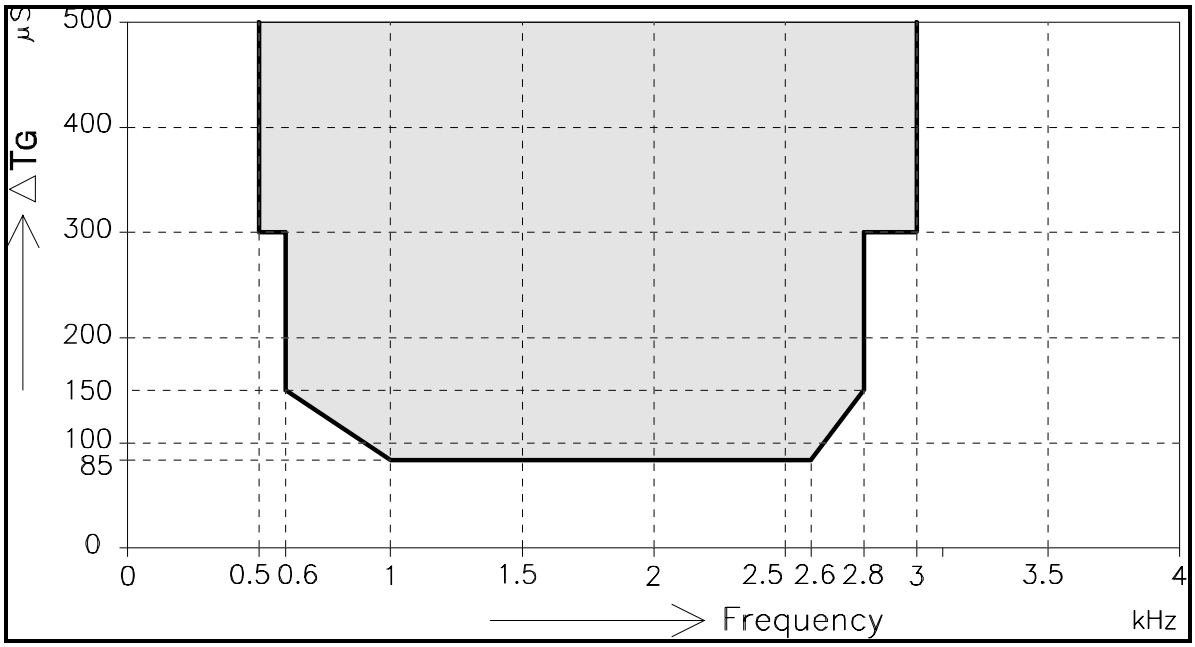


Figure 41 Group Delay Distortion Transmit

[1] R is switched on: reference point is at TGmin
HPR is switched off: reference point is at 1.5 kHz

12.4.8 Out-of-Band Signals at TIP/RING Receive

When an 0dBm0 out-of-band sine-wave signal with a frequency of (<<100Hz or 3.4kHz to 100kHz) is applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0dBm0, 1kHz sine wave reference signal at the analog input.[1)])

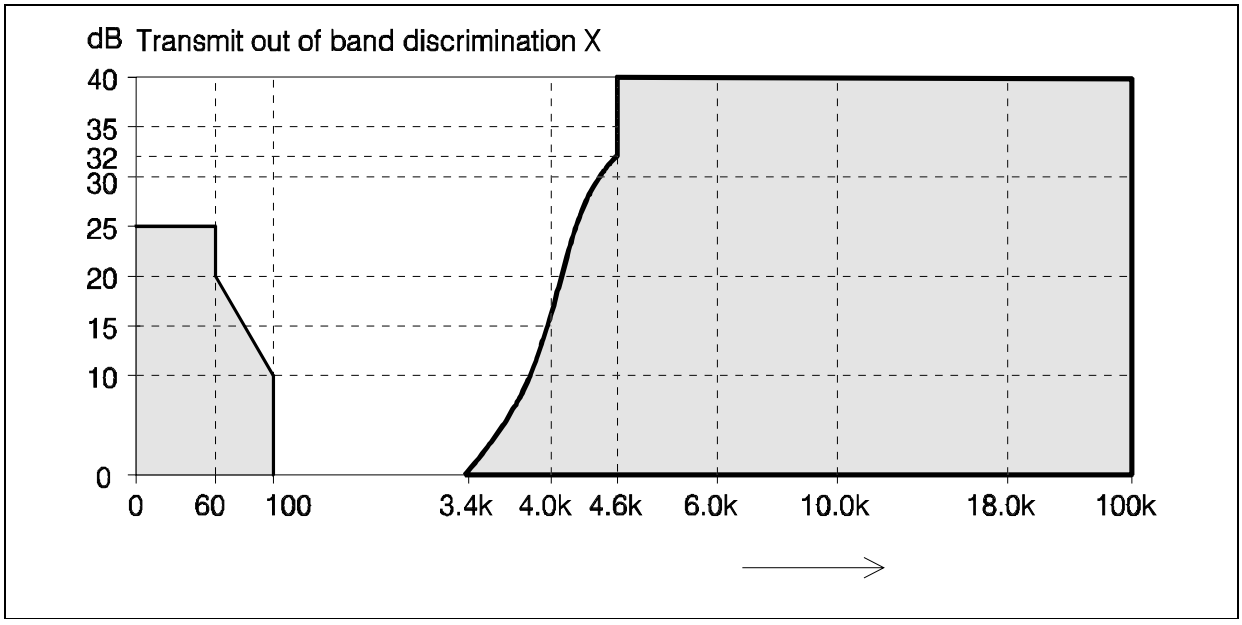


Figure 42 Out of Band Receive

1 Poles at 12 kHz ± 150 Hz and 16 kHz ± 150 Hz will be provided

12.4.9 Out-of-Band Signals at TIP/RING Transmit

When a 0 dBm0 sine wave with a frequency of (300Hz to 3.99kHz) is applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0 1 kHz sine-wave reference signal at the analog output.

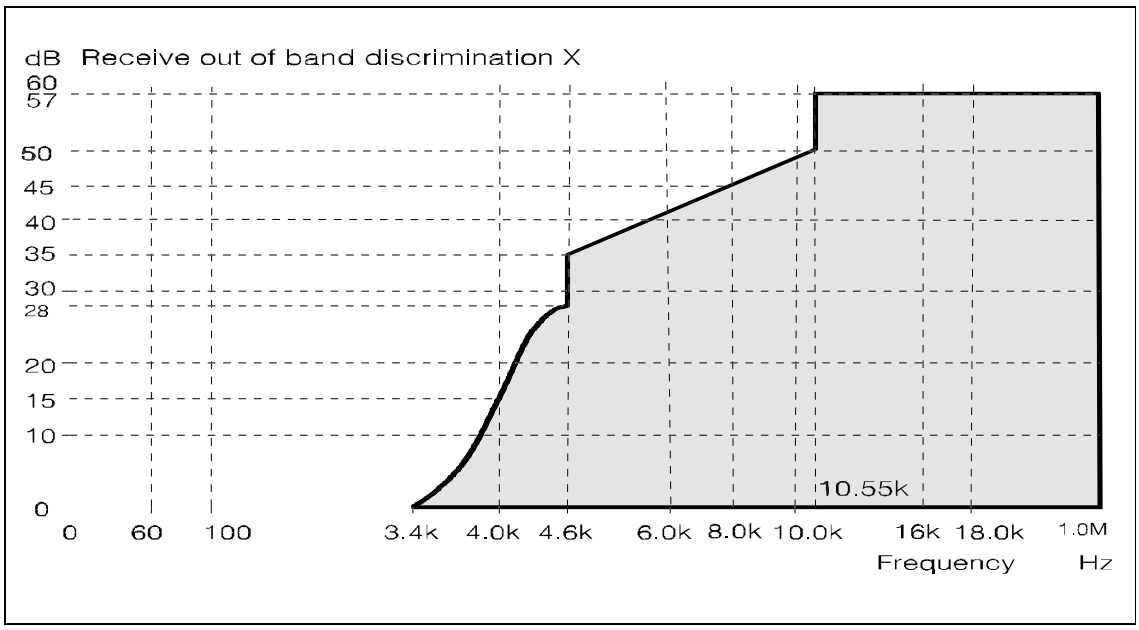


Figure 43 Out of Band Transmit

12.4.10 Trans-hybrid Loss

The quality of trans-hybrid balancing is very sensitive to deviations in gain and group delay. These deviations are inherent in ALIS A/D and D/A converters as well as in all the external components used.

Measurement of ALIS trans-hybrid loss: A 0dBm0 sine wave signal and a frequency in the range between 300 - 3400 Hz is applied to the digital input. The resulting analog output signal VOUT at TIP RING is received and canceled by the TH filter. The programmable filters FRR, AR, FRX, AX and IM and the balancing filter TH are enabled with optimized coefficients.

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below. (Filter coefficients will be provided.)

Parameter	Symbol	Limit Values		Unit	Test condition
Trans-hybrid loss at		min	typ		
300 Hz	THL 300	27	40	dB	TA=25° C; VDDA=4.25V;
500 Hz	THL 500	33	45	dB	
2500 Hz	THL2500	29	40	dB	
3000 Hz	THL3000	27	35	dB	
3400 Hz	THL3400	27	35	dB	

Table 30: Trans-hybrid Loss

The listed values for THL correspond to a typical variation of the signal amplitude and delay in the analog blocks.

Amplitude =typ. ±0.8 dB

Delay =typ. ±0.5 µs

12.5 AC Timing Characteristics

12.5.1 Input/ Output Waveform for AC Tests

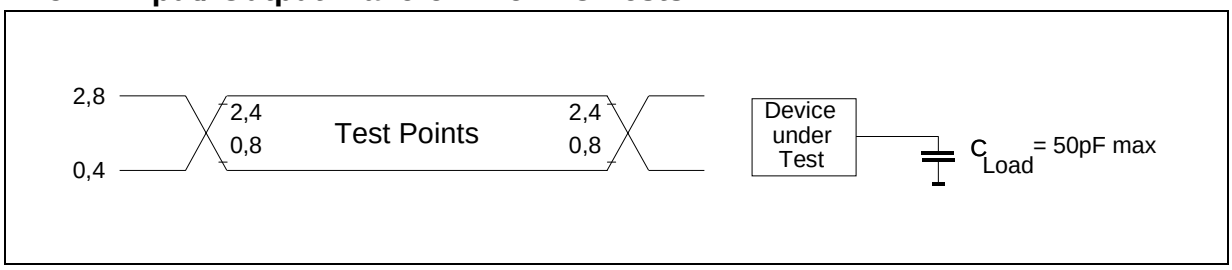


Figure 44 Waveform for AC Tests

12.5.2 Reset Timing

For resetting ALIS to its basic settings mode, negative pulses applied to the RESET pin have to be lower than 1.5 volts (CMOS Schmitt trigger input) and longer than 180 ns. Signals shorter than 40 ns are ignored.

12.5.3 Control Interface Timing

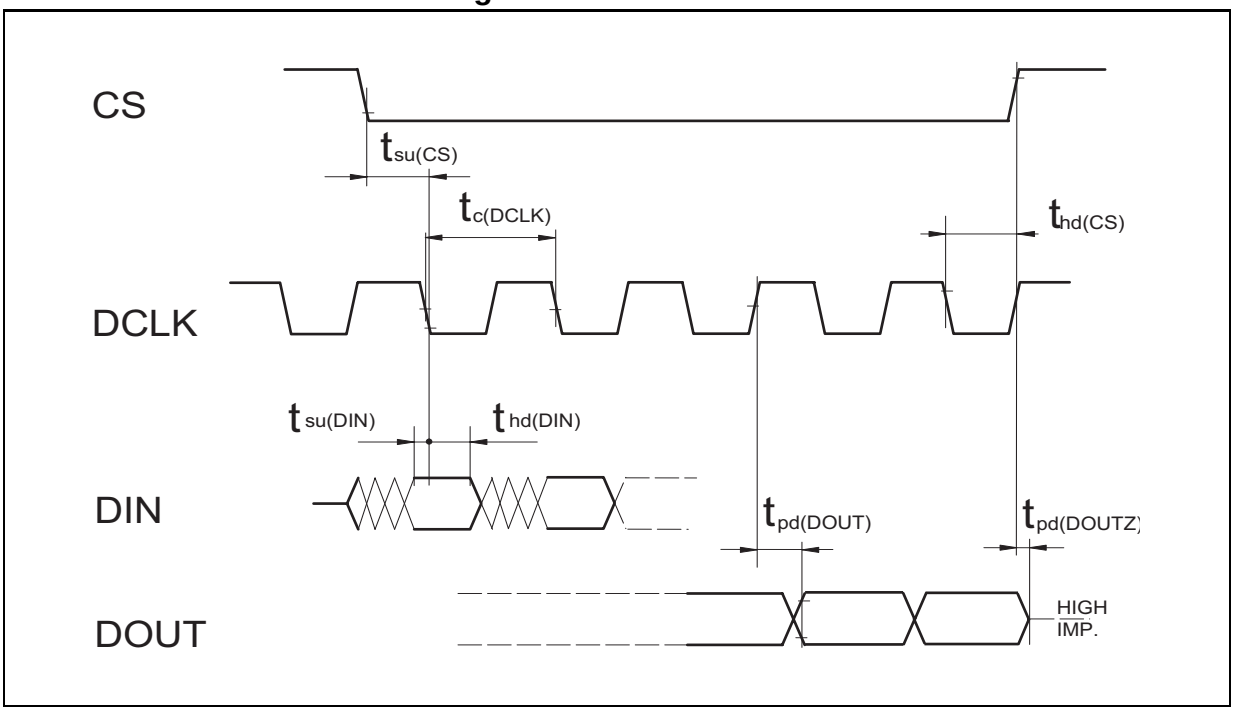


Figure 45 Control Interface Timing

VDD=VDDA= 5V± 5%; TA= 0 - 70°C

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Clock cycle time	tc(DCLK)	1/1024		1	ms
Clock duty cycle		45	50	55	%
Setup time, CS↓ before DCLK↓	tsu(CS)	50 2*tclk[1)]			ns
Hold time, CS↑ after DCLK↓	thd(CS)	120			ns
Setup time, DIN before DCLK↓	tsu(DIN)	60			ns
Hold time, DIN after DCLK↓	thd(DIN)	120			ns
Delay time, DCLK↑, to DOUT	tpd(DOUT)			100	ns
Delay time, CS↑ to DOUTZ	tpd(DOUTZ)			100	ns

1) tclk=1/fclk

Table 31: Control Interface Switching Characteristics

12.5.4 Data Interface Timing

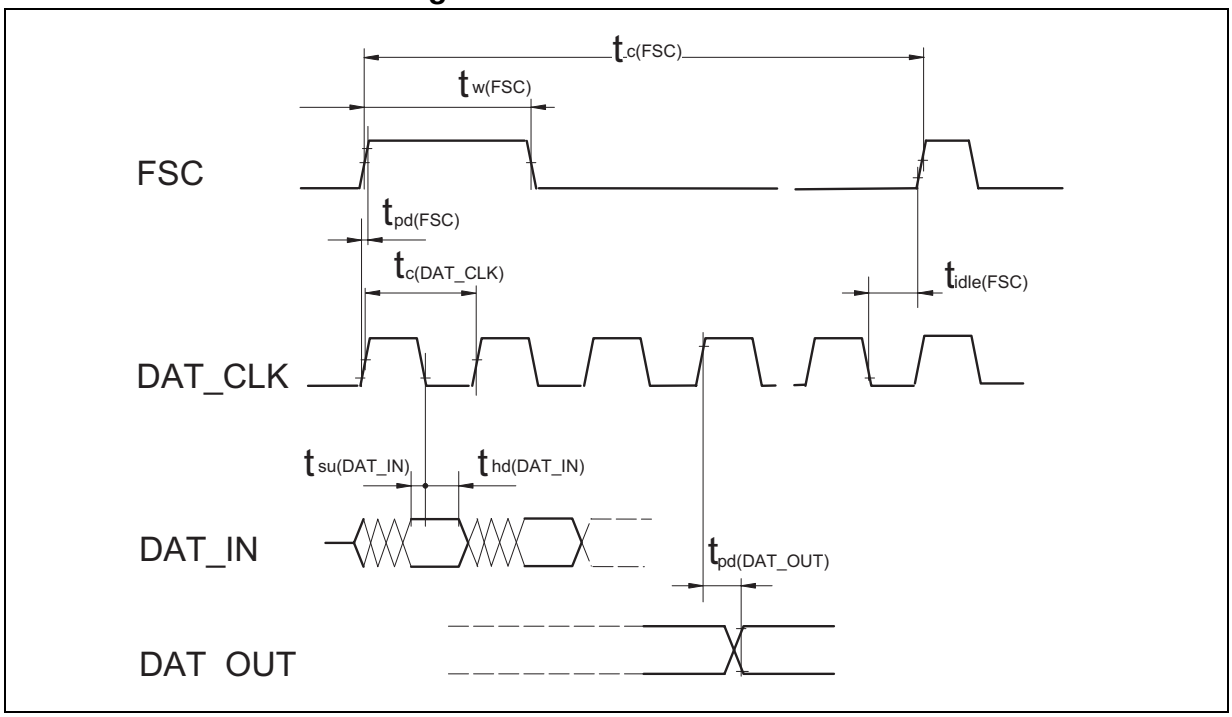


Figure 46 Data Interface Timing

VDD=VDDA= 5V± 5%; TA=0 - 70°C

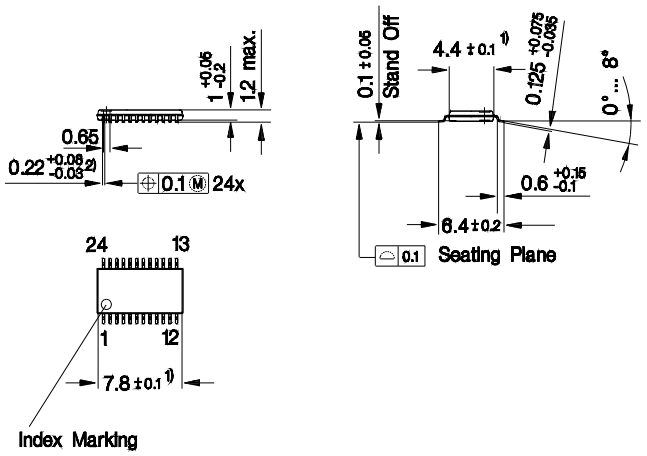
Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Data clock cycle time	tc(DAT_CLK)	1/ 1024		1/ 128	ms
Data clock duty cycle		45	50	55	%
Frame synch clock cycle time	tc(FSC)		125		µs
FSC pulse width (as input)	tw(FSC)	488			ns
FSC pulse width (as output)[1)]	tw(FSC)		tclk*20		µs
Setup time, DAT_IN before DAT_CLK↓	tsu(DAT_IN)	50			ns
Hold time, DAT_IN after DAT_CLK↓	thd(DAT_IN)	100		180	ns
Delay time, DAT_CLK↑ to DAT_OUT	tpd(DAT_OUT)			100	ns
Idle time, DAT_CLK↓ to FSC↑	tidle(FSC)	488			ns
Delay time, DAT_CLK↑ to FSC↑	tpd(FSC)		0		ns
Setup time, FSC↑ to DAT_CLK↓	tsu(FSC)	tclk+60			ns

1) Guaranteed by design

Table 32: Data Interface Switching Characteristics

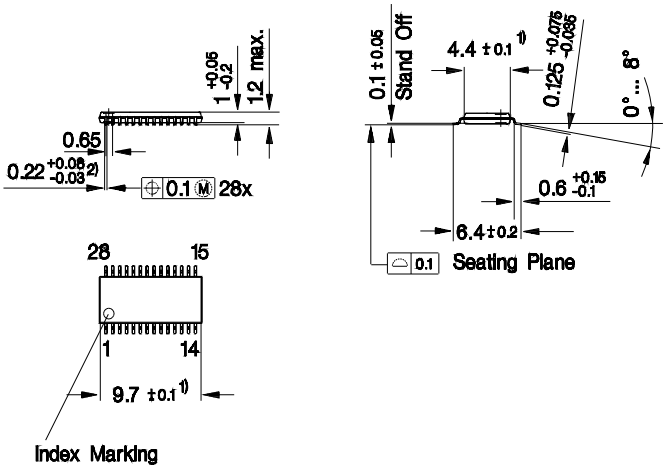
12.5.5 Package Outlines

P-SSOP28
(Plastic Shrink
Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

P-TSSOP24
(Plastic Thin Shrink
Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm