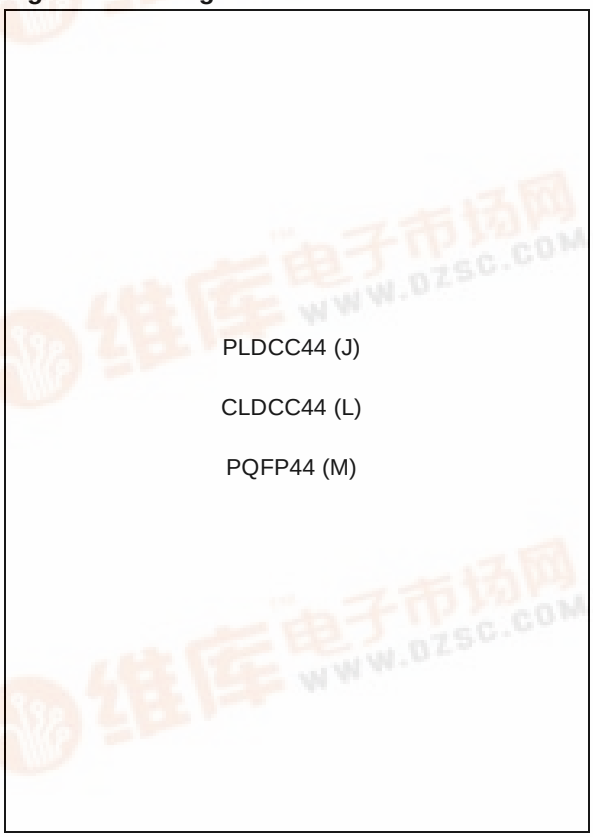
PSD211R
ZPSD211R, ZPSD211RV

Low Cost Field Programmable Microcontroller Peripherals

FEATURES SUMMARY

- Single Supply Voltage:
  - 5 V±10% for PSD211R and ZPSD211R
  - 2.7 to 5.5 V for ZPSD211RV
- Up to 256 Kbit of EPROM
- Input Latches
- Programmable I/O ports
- Programmable Security

Figure 1. Packages



PSD211R Family

PSD211R ZPSD211R ZPSD211RV

Low Cost Microcontroller Peripherals

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Programmable Peripheral

PSD211R

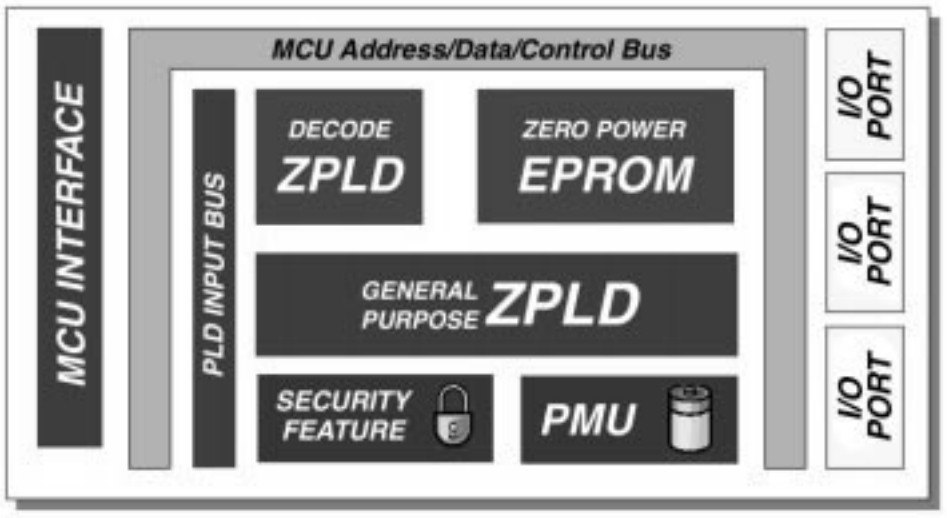
Field-Programmable Microcontroller Peripheral

1.0 Introduction

The low cost PSD211R family integrates high-performance and user-configurable blocks of EPROM and programmable logic into one part. The PSD211R products also provide a powerful microcontroller interface that eliminates the need for external “glue logic”. The part’s integration, small form factor, low power consumption, and ease of use make it the ideal part for interfacing to virtually any microcontroller.

The major functional blocks of the PSD211R include:

- Two programmable logic arrays
- 256 Kb of EPROM
- Input latches
- Programmable I/O ports
- Programmable security



The PSD211R family architecture (Figure 1) can efficiently interface with, and enhance, almost any 8-bit multiplexed microcontroller system. This solution provides microcontrollers the following:

- Chip-select logic, control logic, and latched address signals that are otherwise implemented discretely
- Port expansion (reconstructs lost microcontroller I/O)
- An EPROM (with security)
- Compatible with 8031-type architectures that use separate Program and Data Space.

Updated March 1, 1999. See page 47.

1.0 Introduction (Cont.)

The PSD211R I/O ports can be used for:

- Standard I/O ports
- Programmable chip select outputs
- Address inputs
- Demultiplexed address outputs.

Implementing your design has never been easier than with PSDsoft—WSI's software development suite. Using PSDsoft, you can do the following:

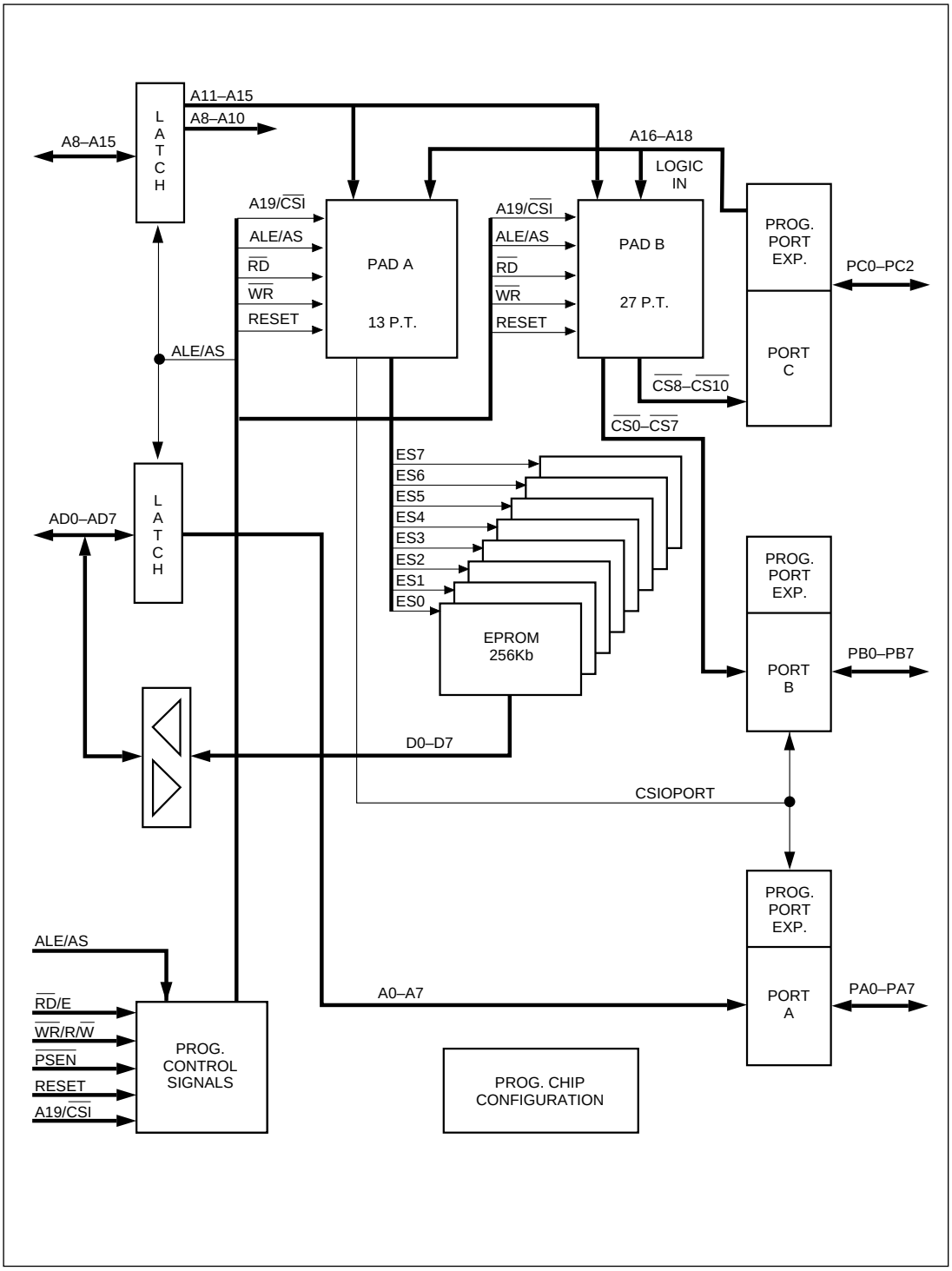
- Configure your PSD211R to work with virtually any 8-bit microcontroller
- Specify what you want implemented in the programmable logic using a high-level Hardware Description Language (HDL)
- Simulate your design
- Download your design to the part using a programmer.

2.0 Notation

Throughout this data sheet, references are made to the PSD211R. In most cases, these references also cover the ZPSD211R and ZPSD211RV products. Exceptions will be noted. Also, references to the ZPSD211R will also cover the low-voltage ZPSD211RV. (Again, exceptions will be noted.) Use the following table to determine what references cover which product versions:

Reference	*PSD211R*	*ZPSD211R*	*ZPSD211RV*
PSD211R or PSD	X	X	X
PSD211R only	X		
Non-ZPSD	X		
ZPSD versions only		X	X
Non-V versions	X	X	
V versions only or 3 V part only or ZPSD211RV only			X

Figure 1. PSD211R Family Architecture



3.0 Key Features

- ❑ Low cost programmable microcontroller peripheral
- ❑ 256Kb of UV EPROM with the following features:
  - Configurable as 32 K x 8
  - Divided into eight equally-sized mappable blocks for optimized address mapping
  - As fast as 70 ns access time, which includes address decoding
- ❑ 19 I/O pins that can be individually configured for :
  - Microcontroller I/O port expansion
  - Programmable Address decoder (PAD) I/O
  - Latched address output
- ❑ Two Programmable Arrays (PAD A and PAD B) replace your discrete PLD or decoder and have the following features:
  - Up to 13 Inputs and 24 outputs
  - 36 Product terms (9 for PAD A and 27 for PAD B)
  - Ability to decode up to 1 MB of address
- ❑ Microcontroller logic that eliminates the need for external “glue logic” has the following features:
  - Ability to interface to multiplexed buses
  - Built-in address latches for multiplexed address/data bus
  - ALE and Reset polarity are programmable (Reset polarity not programmable on V-versions)
  - Multiple configurations are possible for interface to many different microcontrollers
- ❑ Programmable power management with standby current as low as 1µA (V versions only)
  - CMiser bit—programmable option to reduce AC power consumption in memory
  - Turbo Bit (ZPSD only)—programmable bit to reduce AC and DC power consumption in the PADs
- ❑ Built-in security locks the device and PAD decoding configuration
- ❑ Wide Operating Voltage Range
  - V-versions: 2.7 to 5.5 volts
  - Others: 4.5 to 5.5 volts
- ❑ Available in a variety of packaging (44-pin PLDCC, CLDCC, and PQFP)
- ❑ Simple, menu-driven software (PSDsoft) allows configuration and design entry on a PC.

4.0 PSD211R Family Feature Summary

Use the following table to determine which PSD product will fit your needs. Refer back to this page whenever there is confusion as to which part has what features.

Table 1. PSD211R Product Summary

Part	# PLD Inputs	EPROM Size	Voltage	Turbo Bit	Typical Standby Current
PSD211R	13	256 Kb	5 V		50 µA
ZPSD211R	13	256 Kb	5 V	X	10 µA
ZPSD211RV	13	256 Kb	3 V/5 V	X	1 µA

NOTE: The low power version of the ZPSD211R (the ZPSD211RV) can only accept an active-low level Reset input.

5.0 Partial Listing of Microcontrollers Supported

- **Motorola family:** 68HC11, 68HC05C0
- **Intel family**: 80C31, 80C51, 80C188, 80C198
- **Philips family:** 80C31 and 80C51 based MCUs
- **Zilog:** Z8

6.0 Applications

- **Telecommunications:**
  - Cellular phone
  - Digital PBX
  - Digital speech
  - FAX
  - Digital Signal Processing (DSP)
- **Portable Industrial Equipment**:
  - Industrial Control
  - Measurement meters
  - Data recorders
  - Security and access control
- **Medical Instrumentation:**
  - Hearing aids
  - Monitoring equipment
  - Diagnostic tools

7.0 ZPSD Background

Portable and battery-powered systems have recently become major embedded control application segments. As a result, the demand for electronic components having extremely low power consumption has increased dramatically. Recognizing this trend, WSI, Inc. developed a new lower power PSD part, denoted ZPSD211R. The Z stands for Zero-power because ZPSD products virtually eliminate the DC component of power consumption, reducing it to standby levels. Virtual elimination of the DC component is the basis for the words “Zero-power” in the ZPSD name. ZPSD products also minimize the AC power component when the chip is changing states. The result is a programmable microcontroller peripheral family that replaces discrete circuit components, while drawing less power.

7.0 ZPSD Background (Cont.)

7.1 Integrated Power Management™ Operation

Upon each address or logic input change to the ZPSD, the device powers up from low power standby for a short time. Then the ZPSD consumes only the necessary power to deliver new logic or memory data to its outputs as a response to the input change. After the new outputs are stable, the ZPSD latches them and automatically reverts back to standby mode. The I_{CC} current flowing during standby mode and during DC operation is identical and is only a few microamperes.

The ZPSD automatically reduces its DC current drain to these low levels and does not require controlling by the CSI (Chip Select Input). Disabling the CSI pin unconditionally forces the ZPSD to standby mode independent of other input transitions. The only significant power consumption in the ZPSD occurs during AC operation. The ZPSD contains the first architecture to apply Zero-power techniques to memory and logic blocks.

Figure 2 compares ZPSD zero power operation to the operation of a discrete solution. A standard microcontroller (MCU) bus cycle usually starts with an ALE (or AS) pulse and the generation of an address. The ZPSD detects the address transition and powers up for a short time. The ZPSD then latches the outputs of the PAD and EPROM to the new values. After finishing these operations, the ZPSD shuts off its internal power, entering standby mode. The time taken for the entire cycle is less than the ZPSD's "access time."

The ZPSD will stay in standby mode while its inputs are not changing between bus cycles. In an alternate system implementation using discrete EPROM, and other discrete components, the system will consume operating power during the entire bus cycle. This is because the chip select inputs on the memory devices are usually active throughout the entire cycle. The AC power consumption of the ZPSD may be calculated using the composite frequency of the MCU address and control signals, as well as any other logic inputs to the ZPSD.

Figure 2. ZPSD Power Operation vs. Discrete Implementation

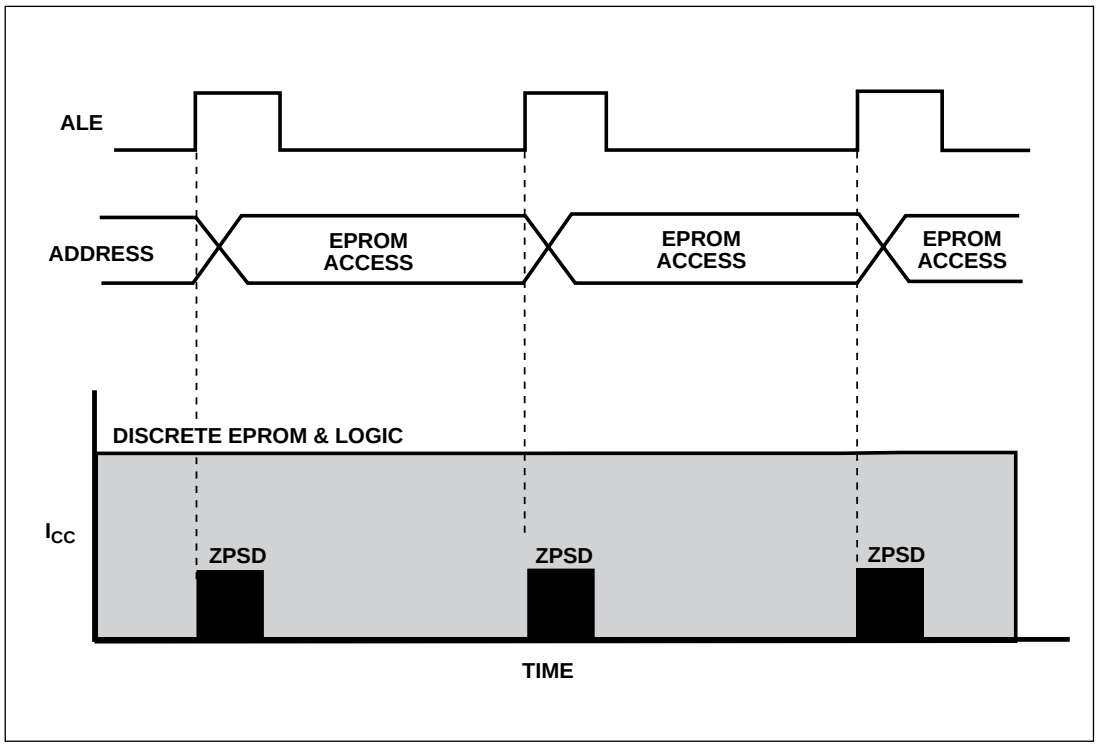


Table 2. PSD211R Pin Descriptions

Name	Type	Description
$\overline{PSEN}$	I	This pin is for 8031 or compatible MCUs that use $\overline{PSEN}$ to separate program space from data space. In this case, $\overline{PSEN}$ is used for reads from the EPROM. **Notes:** 1) If your MCU does not output a $\overline{PSEN}$ signal, pull up this pin to V_{CC}. 2) In programming mode, this pin is pulsed between V_{PP} and 0 V.
$\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$	I	The following control signals can be connected to this port, based on your MCU (and the way you configure the PSD in PSDsoft): 1. $\overline{WR}$—active-low write pulse. 2. $R/\overline{W}$—active-high read/active-low write input. **Note:** in programming mode, this pin **must** be tied to V_{PP}.
$\overline{RD}$/E	I	The following control signals can be connected to this port, based on your MCU (and the way you configure the PSD in PSDsoft): 1. $\overline{RD}$—active-low read input. 2. E—E clock input.
A19/$\overline{CSI}$	I	The following control signals can be connected to this port: 1. $\overline{CSI}$-Active-low chip select input. If your MCU supports a chip select output, and you want the PSD to save power when not selected, use this pin as a chip select input. 2. If you don't wish to use the $\overline{CSI}$ feature, you may use this pin as an additional input (logic or address) to the PAD. A19 can be latched with ALE/AS, or be a transparent logic input.
Reset	I	**PSD211R/ZPSD211R:** This pin is user-programmable and can be configured to reset on a high- or low-level input. Reset must be applied for at least 100 ns. **ZPSD211RV:** This pin is not configurable, and the chip will only reset on an active-low level input. Reset must be applied for at least 500 ns, and no operations may take place for an additional 500 ns minimum. (See Figure 8.)
ALE/AS	I	Connect ALE or AS to this pin. The polarity of this pin is configurable. The trailing edge of ALE/AS latches all multiplexed address inputs.
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	I/O	These pins make up Port A. These port pins are configurable, and can have the following functions: (see Figure 5) 1. MCU I/O—in this mode, the direction of the pin is defined by its direction bit, which resides in the direction register. 2. Latched address output.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	I/O	These pins make up Port B. These port pins are configurable, and can have the following functions: (see Figure 6) 1. MCU I/O—in this mode, the direction of the pin is defined by its direction bit, which resides in the direction register. 2. Chip select output—each of PB0-3 has four product terms available per pin, while PB4-7 have 2 product terms each. See Figure 4.

Legend: The Type column abbreviations are: I = input only; I/O = input/output; P = power.

Table 1. PSD211R Pin Descriptions (cont.)

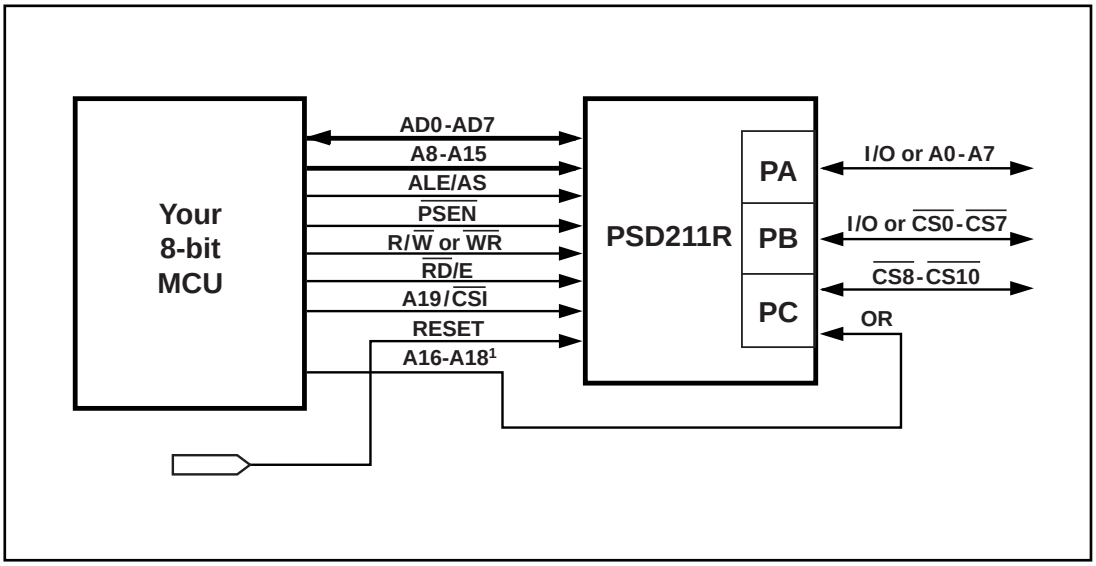
Name	Type	Description
PC0 PC1 PC2	I/O	These pins make up Port C. These port pins are configurable, and can have the following functions (see Figure 7): 1. PAD input—when configured as an input, a bit individually becomes an address or a logic input, depending on your PSDsoft design file. When declared as an address, the bits are latched with ALE/AS. 2. PAD output—when configured as an output (i.e. there is an equation written for it in your PSDsoft design file), there is one product term available to it.
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	These pins are the multiplexed, low-order address/data byte (AD0-AD7). As inputs, address information is latched by the ALE/AS signal and used internally by the PSD. The pins also serve as MCU data bus inputs or outputs, depending on the MCU control signals ($\overline{RD}$, $\overline{WR}$, etc.).
A8 A9 A10 A11 A12 A13 A14 A15	I/O	These pins are the high-order address inputs (A8-A15).
GND	P	Ground Pin
V_{CC}	P	Supply voltage input.

Legend: The Type column abbreviations are: I = input only; I/O = input/output; P = power.

8.0 Operating Mode

The PSD211R operates in 8-bit address/data mode, enabling it to interface directly to a variety of 8-bit multiplexed microcontrollers. It works as follows: the address/data bus (AD0-AD7) is bi-directional and permits the latching of the address when the ALE/AS signal is active. On the same pins, the data is read from or written to the device, depending on the state of the control signals ($\overline{WR}$, $\overline{RD}$, etc.). You should connect your MCU according to the following figure. Ports A through C can be configured according to Table 3, below.

Figure 3. Connecting a PSD211R to an 8-Bit Multiplexed-Bus MCU



NOTE: 1. Connect A16-A18 to Port C if your MCU outputs more than 16 bits of address.

Table 3. Bus and Port Configuration Options

Port	*Configurations*
A	I/O or low-order (latched) address lines
B	I/O and/or $\overline{CS0}$–$\overline{CS7}$
C	A16-A18 or $\overline{CS8}$-$\overline{CS10}$

9.0 Programmable Address Decoder (PAD)

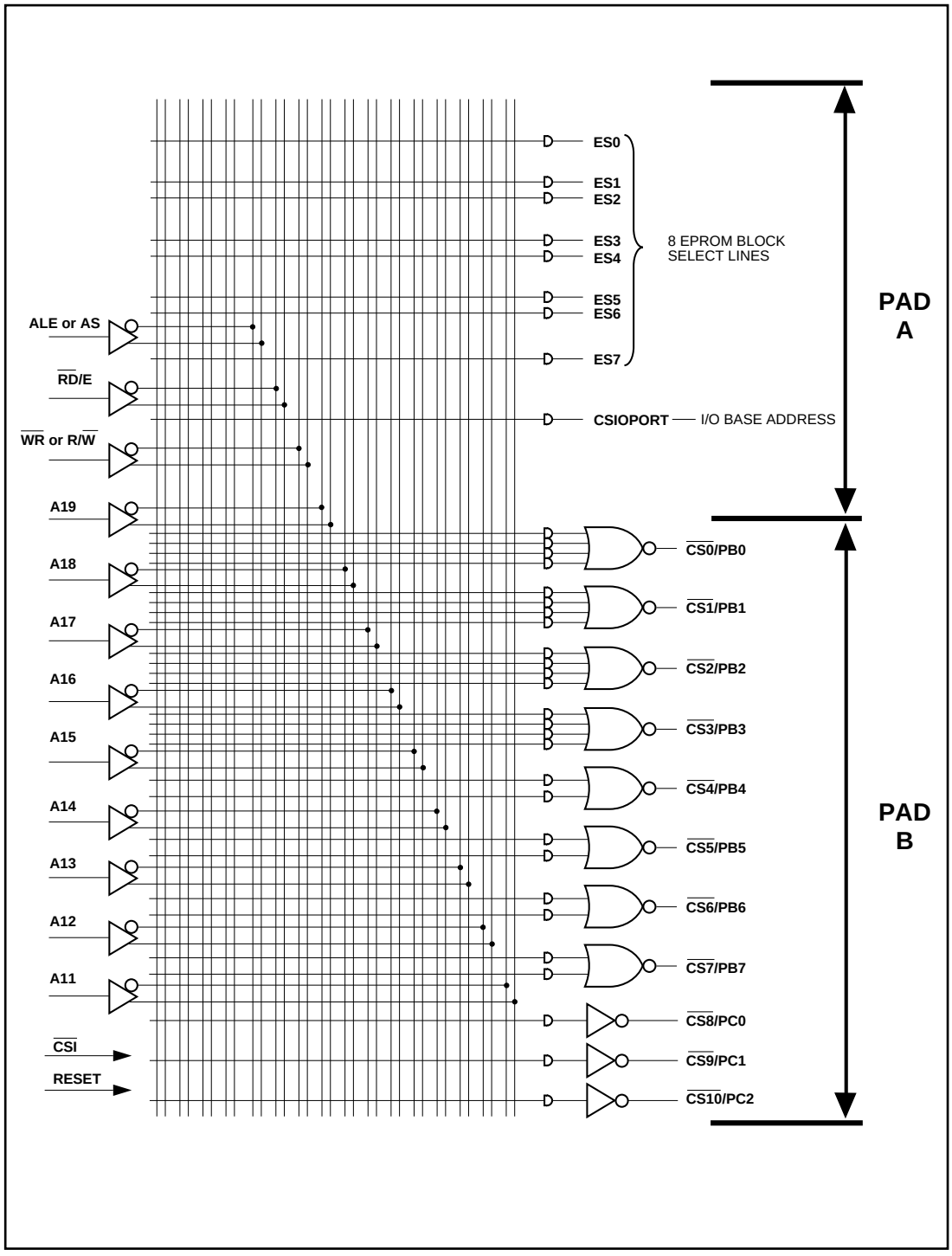
The PSD211R contains two programmable arrays, referred to as PAD A and PAD B (Figure 4). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks and I/O ports.

PAD B outputs to Ports B and C for off-chip usage. PAD B can also be used to extend the decoding to select external devices or as a random logic replacement.

PAD A and PAD B receive the same inputs. The PAD logic is configured by PSDsoft based on the designer's input. The PAD's non-volatile configuration is stored in a re-programmable CMOS EPROM. Windowed packages are available for erasure by the user. See Table 4 for a list of PAD A and PAD B functions.

Programmable Address Decoder (PAD)

Figure 4. PAD Description



NOTES: 1. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 7A and 7B.
2. RESET deselects all PAD output signals. See Tables 8A and 8B.
3. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.

Programmable Address Decoder (PAD) (cont.)

Table 4. PSD211R PAD A and PAD B Functions

Function	
PAD A and PAD B Inputs	
A19/$\overline{CSI}$	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 7A and 7B). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 4, Note 3.
A11–A15	These are address inputs.
$\overline{RD}$/E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE/AS	This is the ALE or AS input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 8A and 8B.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Table 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 4, Note 3. Each of them is a function of one product term of the PAD inputs.

10.0 I/O Port Functions

The PSD211R has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The next section describes the control registers for the ports. Following that are sections that describe each port. Figures 5 through 7 show the structure of Ports A through C, respectively.

Note: any unused inputs should be connected directly to ground or pulled up to V_{CC} (using a 10KΩ to 100KΩ resistor).

10.1 CSIOPORT Registers

Control of the ports is primarily handled through the CSIOPORT registers. There are 24 bytes in the address space, starting at the base address labeled CSIOPORT. Since the PSD211R uses internal address lines A15-A11 for decoding, the CSIOPORT space will occupy 2 Kbytes of memory, on a 2 Kbyte boundary. This resolution can be improved to reduce wasted address space by connecting lower order address lines (A10 and below) to Port C. Using this method, resolution down to 256 Kbytes may be achieved. The CSIOPORT space **must be defined in your PSDsoft design file**. The following tables list the registers located in the CSIOPORT space.

Table 5. CSIOPORT Registers for 8-Bit Data Busses

Register Name	Offset (in hex) from CSIOPORT Base Address	Type of Access Allowed
Port A Pin Register	+2	Read
Port A Direction Register	+4	Read/Write
Port A Data Register	+6	Read/Write
Port B Pin Register	+3	Read
Port B Direction Register	+5	Read/Write
Port B Data Register	+7	Read/Write
Power Management Register (Note 1)	+10	Read/Write

NOTE: 1. ZPSD only.

10.2 Port A (PA0-PA7)

MCU I/O Mode

The default configuration of Port A is MCU I/O. In this mode, every pin can be set (at run-time) as an input or output by writing to the respective pin's direction flip-flop (DIR FF, Figure 5). As an output, the pin level can be controlled by writing to the respective pin's data flip-flop (DFF, Figure 5A). The Pin Register can be read to determine logic level of the pin. The contents of the pin register indicate the true state of the PSD driving the pin through the DFF or an external source driving the pin.

10.0 I/O Port Functions (Cont.)

10.2 Port A (PA0-PA7) (Cont.)

Latched Address Output Mode

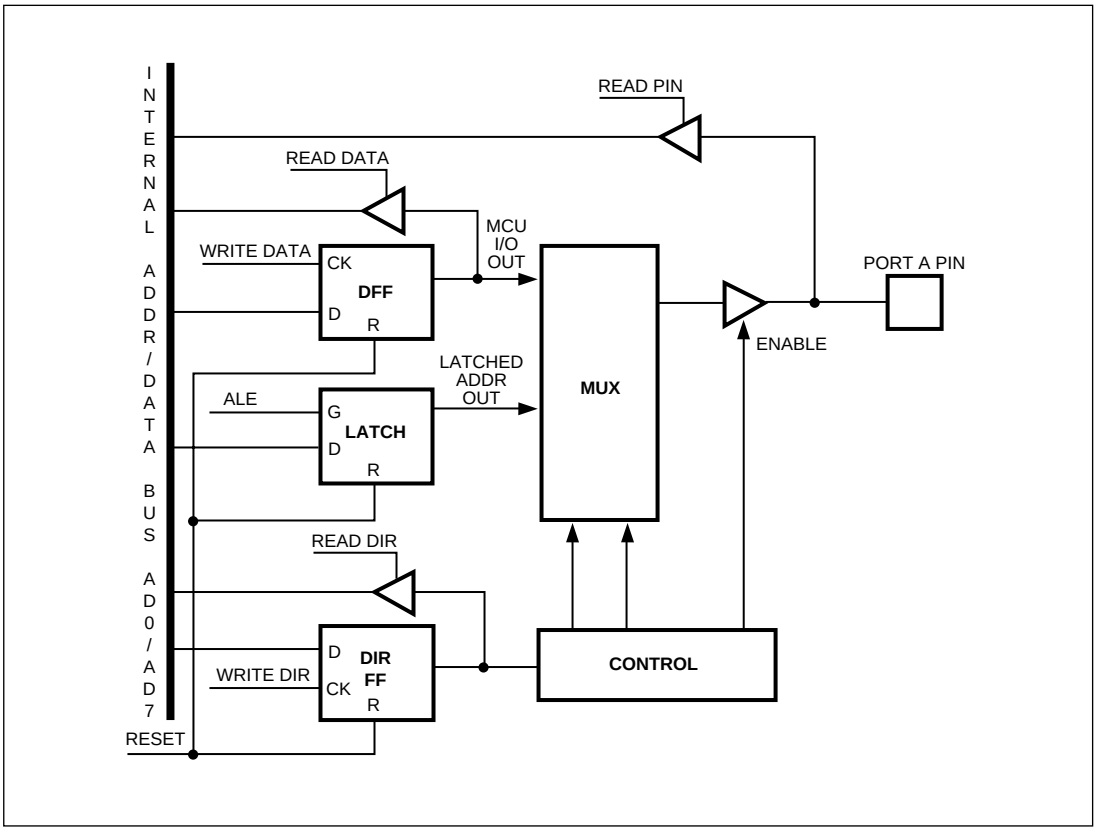
Alternatively, any bit(s) of Port A can be configured to output a low-order demultiplexed address bus bit. The address is provided by the internal PSD address latch, which latches the address on the trailing edge of ALE/AS. Port A then outputs the desired demultiplexed address bits. This feature can eliminate the need for an external latch (for example: 74LS373) if you have devices that require low-order latched address bits. Although any pin of Port A may output an address signal, the pin is position-dependent. In other words, pin PA0 of Port A may only pass A0, PA1 only A1, and so on.

The control registers of Port A are located in CSIOPORT space; see Table 5. Each pin of Port A can be individually configured. The following table summarizes what the control registers (in CSIOPORT space) for Port A do:

Register Name	*0 Value*	*1 Value*	*Default Value* (Note 1)
Port A Pin Register	Sampled logic level at pin = '0'	Sampled logic level at pin = '1'	X
Port A Direction Register	Pin is configured as input	Pin is configured as output	0
Port A Data Register	Data in DFF = '0'	Data in DFF = '1'	0

NOTE: 1. Default value is the value after reset.

Figure 5. Port A Pin Structure



10.0 I/O Port Functions (Cont.)

10.3 Port B (PB0-PB7)

MCU I/O Mode

The default configuration of Port B is MCU I/O. In this mode, every pin can be set (at run-time) as an input or output by writing to the respective pin's direction flip-flop (DIR FF, Figure 6). As an output, the pin level can be controlled by writing to the respective pin's data flip-flop (DFF, Figure 6). The Pin Register can be read to determine logic level of the pin. The contents of the Pin Register indicate the true state of the PSD driving the pin through the DFF or an external source driving the pin.

Chip Select Output

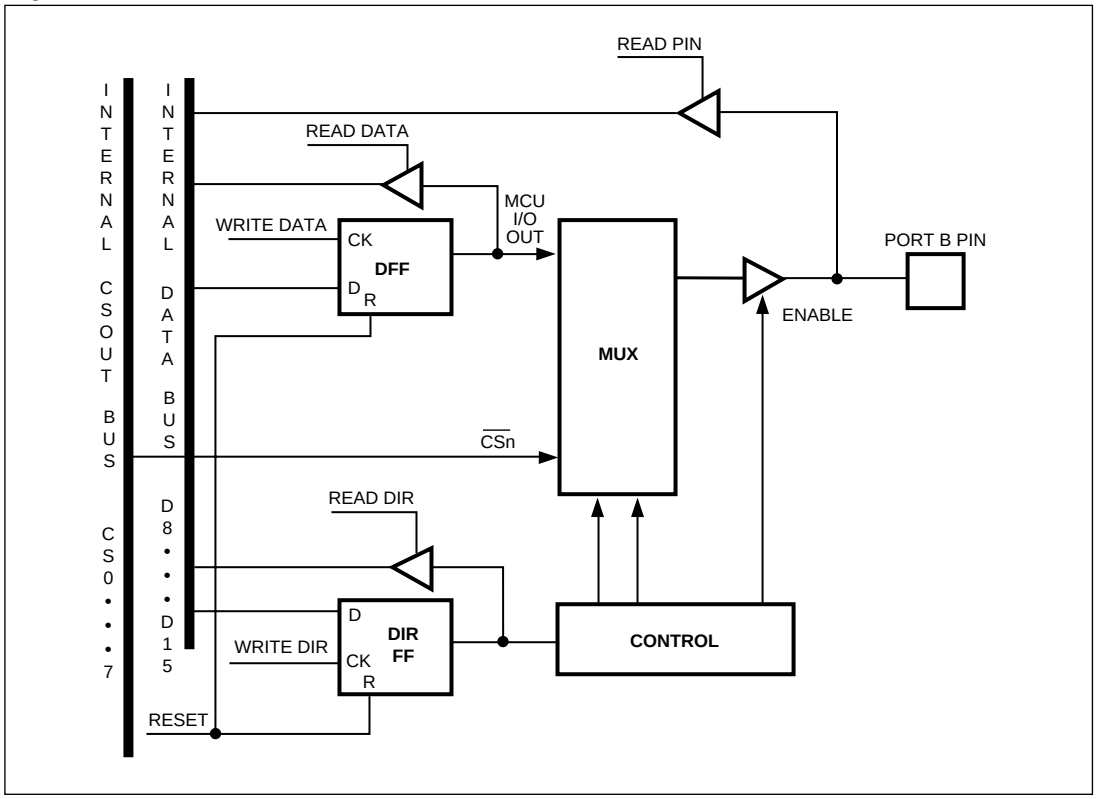
Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0-PB7 can provide $\overline{CS0}$-$\overline{CS7}$, respectively. The functionality of these pins is not limited to chip selects only; they can be used for generic combinatorial logic as well. Each of the $\overline{CS0}$-$\overline{CS3}$ signals is comprised of four product terms, and each of the $\overline{CS4}$-$\overline{CS7}$ signals is comprised of two product terms.

The control registers of Port B are located in CSIOPORT space; see Table 5. Each pin of Port B can be individually configured. The following table summarizes what the control registers (in CSIOPORT space) for Port B do:

Register Name	0 Value	1 Value	Default Value (Note 1)
Port B Pin Register	Sampled logic level at pin = '0'	Sampled logic level at pin = '1'	X
Port B Direction Register	Pin is configured as input	Pin is configured as output	0
Port B Data Register	Data in DFF = '0'	Data in DFF = '1'	0

NOTE: 1. Default value is the value after reset.

Figure 6. Port B Pin Structure



10.0 I/O Port Functions (Cont.)

10.4 Port C (PC0-PC2)

Each pin of Port C (Figure 7) can be configured as an input to PAD A and PAD B, or as an output from PAD B. As inputs, the pins are referenced as A16-A18. Although the pins are given this reference, they can be used for any address or logic input. [For example, A8-A10 could be connected to those pins to improve the resolution (boundaries) of $\overline{CS0}$-$\overline{CS7}$ to 256 bytes.] How they are defined in the PSDsoft design file determines:

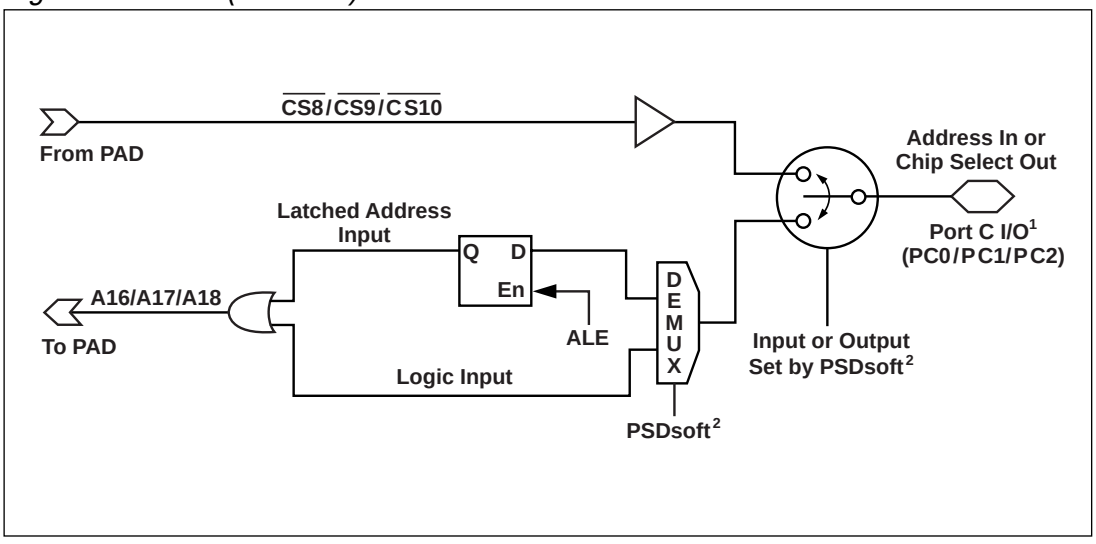
- Whether they are address or logic inputs
- Whether the input is transparent or latched by the trailing edge of ALE/AS.

Notes:

1) If the inputs are addresses, they are routed to PAD A and B, and can be used in any or all PAD equations.
2) If the inputs are logic, they are routed to PAD B and can be used for Boolean equations that are implemented in any or all of the $\overline{CS0}$-$\overline{CS10}$ PAD B outputs.
3) If Port C pins are configured as inputs, they can not be individually configured as address or logic and latched or transparent. They must be configured as a group to be address or logic and latched or transparent.

Alternately, PC0-PC2 can become $\overline{CS8}$-$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals ($\overline{CS8}$-$\overline{CS10}$) is comprised of one product term.

Figure 7. Port C (PC0-PC2) Pin Structure



NOTES: 1. Port C pins can be individually configured as inputs **or** outputs, but **not** both.
2. PSDsoft sets this configuration prior to run-time based on your PSDsoft design file.

11.0 PSD Memory

The following sections explain the EPROM memory block and how to program and erase the PSD211R.

11.1 EPROM

For all PSD211R devices, the EPROM is built using Zero-power technology. This means that the EPROM powers up only when the address changes. It consumes power for the necessary time to latch data on its outputs. After this, it powers down and remains in standby mode until the next address change. This happens automatically, and the designer has to do nothing special.

The 32K x 8 EPROM is divided into eight equal-sized banks. Each bank can be placed in any address location by programming the PAD. Bank0-Bank7 are selected by PAD A outputs ES0-ES7, respectively. There is one product term for each bank select (ESi).

11.2 Programming and Erasure

Programming the device can be done using the following methods:

- WSI's main programmer—PSDpro—which is accessible through a parallel port.
- WSI's programmer used specifically with the PSD211R—PEP300.
- WSI's discontinued programmer—Magic Pro.
- A 3rd party programmer, such as Data I/O.

Information for programming the device is available directly from WSI. Please contact your local sales representative. Also, check our web site (waferscale.com) for information related to 3rd party programmers.

Upon delivery from WSI, or after each erasure (using windowed part), the PSD211R device has all bits in the PAD and EPROM in the HI state (logic 1). The configuration bits are in the LO state (logic 0).

To clear all locations of their programmed contents (assuming you have a windowed version), expose the windowed device to an Ultra-Violet (UV) light source. A dosage of 30 W second/cm^2 is required for PSD211R devices, and 40 W second/cm^2 for low-voltage (V suffix) devices. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 40 to 45 minutes for the PSD211R and 55 to 60 minutes for the low-voltage (V suffix) devices. The device should be approximately 1 inch (2.54 cm) from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD211R devices will erase with light sources having wavelengths shorter than 4000 Å. However, the erasure times will be much longer than when using the recommended 2537 Å wavelength. Note: exposure to sunlight will eventually erase the device. If used in such an environment, the package window should be covered with an opaque substance.

12.0 Control Signals

Consult your MCU data sheet to determine which control signals your MCU generates, and how they operate. This section is intended to show which control signals should be connected to what pins on the PSD211R. You will then use PSDsoft to configure the PSD211R, based on the combination of control signals that your MCU outputs, for example $\overline{RD}$, $\overline{WR}$, and $\overline{PSEN}$.

The PSD211R is compatible with the following control signals:

- ALE or AS (polarity is programmable)
- $\overline{WR}$ or R/$\overline{W}$
- $\overline{RD}$/E
- $\overline{PSEN}$
- A19/$\overline{CSI}$
- RESET (polarity is programmable except on low voltage versions with the V suffix).

12.0 Control Signals (Cont.)

12.1 ALE or AS

Connect the ALE or AS signal from your MCU to this pin where applicable, and program the polarity using PSDsoft. The trailing edge (when the signal goes inactive) of ALE or AS latches the address on the appropriate address pins.

12.2 $\overline{WR}$ or R/$\overline{W}$

Your MCU should output a stand-alone write signal (WR) or a multiplexed read/write signal (R/W). In either case, the signal should be connected to this pin.

12.3 $\overline{RD}$/E

Your MCU should output either $\overline{RD}$ or E (clock). In either case, connect the appropriate signal to this pin. Note: if you have an MCU that outputs $\overline{DS}$, it will not be compatible with the PSD211R, and you must use a PSD3XX family device.

12.4 $\overline{PSEN}$

- ❏ If your MCU does not output $\overline{PSEN}$ (or some program select enable equivalent signal), tie this pin to Vcc (through a series resistor), and skip to the next signal.
- ❏ If you use an 8-bit 8031 compatible MCU that outputs a separate signal when accessing program space, such as $\overline{PSEN}$, connect it to this pin. You would then use PSDsoft to configure the EPROM in the PSD211R to respond to $\overline{PSEN}$ only or $\overline{PSEN}$ and $\overline{RD}$. If you have an 8031 compatible MCU, refer to the “Program/Data Space and the 8031” section for further information.

12.5 A19/$\overline{CSI}$

This pin is configured using PSDsoft to be either a chip select for the entire PSD device or an additional PAD input. If your MCU can generate a chip-select signal, and you wish to save power, use the PSD chip select feature. Otherwise, use this pin as an address or logic input.

- ❏ When configured as $\overline{CSI}$ (active-low PSD chip select): a low on this pin keeps the PSD in normal operation. However, when a high is detected on the pin, the PSD enters Power-down Mode. See Tables 7A and 7B for information on signal states during Power-down Mode. See section 16 for details about the reduction of power consumption.
- ❏ When configured as A19, the pin can be used as an additional input to the PADs. It can be used for address or logic. It can also be ALE/AS dependent or a transparent input, which is determined by your PSDsoft design file. In A19 mode, the PSD is always enabled.

Table 7A. Signal States During Power-down Mode

Port	Configuration Mode(s)	State
AD0–AD15	All	Input (Hi-Z)
Port Pins PA0–PA7	MCU I/O	Unchanged
	Latched Address Out	Logic 1
Port Pins PB0–PB7	MCU I/O	Unchanged
	Chip Select Outputs, $\overline{CS0}$–$\overline{CS7}$, CMOS	Logic 1
	Chip Select Outputs, $\overline{CS0}$–$\overline{CS7}$, Open Drain	Hi-Z
Port Pins PC0–PC2	Address or Logic Inputs, A16-A18	Input (Hi-Z)
	Chip Select Outputs, $\overline{CS8}$–$\overline{CS10}$, CMOS only	Logic 1

12.0 Control Signals (Cont.)

Table 7B. Internal States During Power-down

Component	Internal Signal	Internal Signal State During Power-Down
PAD A and PAD B	$\overline{CS0}$–$\overline{CS10}$	Logic 1 (inactive)
	CSIOPORT, ES0–ES7	Logic 0 (inactive)
All registers in CSIOPORT address space, including: ✓ Direction ✓ Data ✓ PMR (turbo bit, ZPSD only)	N/A	All unchanged

NOTE: N/A = Not Applicable

12.6 Reset Input

This is an asynchronous input to initialize the PSD device.

Refer to tables 8A and 8B for information on device status during and after reset.

The standard-voltage PSD211R and ZPSD211R (non-V) devices require a reset input. In this case, the reset input must be asserted for at least 100 nsec. The PSD will be functional immediately after reset is de-asserted. For these standard-voltage devices, the polarity of the reset input signal is programmable using PSDsoft (active-high or active-low), to match the functionality of your MCU reset.

Note: It is not recommended to drive the reset input of the MCU and the reset input of the PSD with a simple RC circuit between power on ground. The input threshold of the MCU and the PSD devices may differ, causing the devices to enter and exit reset at different times because of slow ramping of the signal. This may result in the PSD not being operational when accessed by the MCU. It is recommended to drive both devices actively. A supervisory device or a gate with hysteresis is recommended.

For low-voltage ZPSD211RV devices only, the reset input must be asserted for at least 500 nsec. The ZPSD211RV will not be functional for an additional 500 nsec after reset is de-asserted (see Figure 8). These low voltage ZPSD211RV devices require an active-low polarity signal for reset. Unlike the PSD211R, the polarity of the reset input is not programmable for the ZPSD211RV. If your MCU operates with an active high reset, you must invert this signal before driving the ZPSD211RV reset input.

You must design your system to ensure that the PSD comes out of reset and the PSD is active before the MCU makes its first access to PSD memory. Depending on the characteristics and speed of your MCU, a delay between the PSD reset and the MCU reset may be needed.

12. Control Signals (Cont.)

Table 8A. External PSD Signal States During and Just After Reset

Port	Configured Mode of Operation		Signal State During Reset	Signal State Just After Reset (Note 1)
AD0/A0-AD15/A15	All		Input (Hi-Z)	MCU address and/or data
Port Pins PA0-PA7	MCU I/O		Input (Hi-Z)	Input (Hi-Z)
	Latched Address Out	PSD211R, ZPSD211R	Logic 0	MCU address
		ZPSD211RV	Hi-Z	MCU address
Port Pins PB0-PB7	MCU I/O		Input (Hi-Z	Input (Hi-Z)
	Chip Select Outputs, CS0-CS7, CMOS	PSD211R, ZPSD211R	Logic 1	Per CS equations
		ZPSD211RV	Hi-Z	Per CS equations
	Chip Select Outputs, CS0-CS7, Open Drain	PSD211R, ZPSD211R	Hi-Z	Per CS equations
		ZPSD211RV	Hi-Z	Per CS equations
Port Pins PC0-PC2	Address or Logic Inputs, A16-A18		Input (Hi-Z)	Input (Hi-Z)
	Chip Select Outputs, CS8-CS10, CMOS	PSD211R, ZPSD211R	Logic 1	Per CS equations
		ZPSD211RV	Hi-Z	Per CS equations

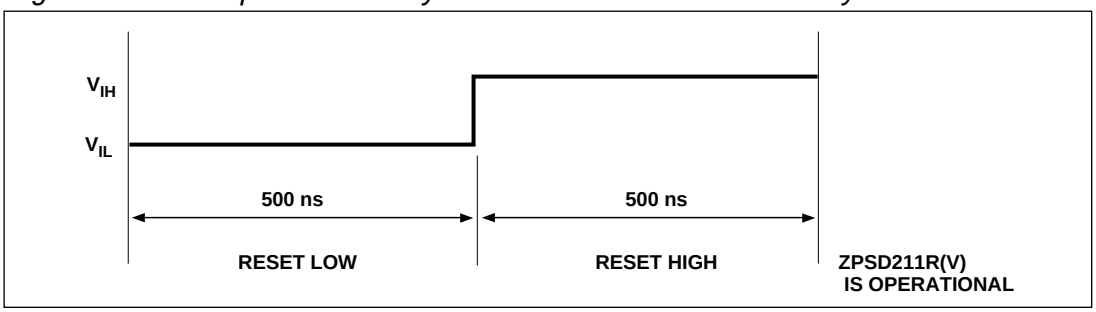
NOTE: 1. Signal is valid immediately after reset for non-V devices. ZPSD211RV devices need an additional 500 nsec after reset before signal is valid.

Table 8B. Internal PSD Signal States During and Just After Reset

Component	Internal Signal	Internal Signal State During Reset	Internal Signal State During Power-Down
PAD A and PAD B	CS0-CS10	Logic 1 (inactive)	Per CS Equations
	CSIOPORT, ES0-ES7	Logic 0 (inactive)	Per equations for each internal signal
All registers in CSIOPORT address space, including: ✓ Direction ✓ Data ✓ PMR (turbo bit, ZPSD only)	N/A	Logic 0 in all bit of all registers	Logic 0 until changed by MCU

NOTE: N/A = Not Applicable

Figure 8. The Required Reset Cycle for ZPSD211RV Devices Only.



13.0 Program/Data Space and the 8031

This section only applies to users who have an 8031 or compatible MCU that outputs a signal such as PSEN when accessing program space. If this applies to you, be aware of the following: the PSD211R can be configured using PSDsoft such that the EPROM is either 1) accessed by PSEN only (Figure 10); or 2) accessed by PSEN or RD (Figure 9). The default is PSEN only unless changed in PSDsoft.

Figure 9. Combined Address Space

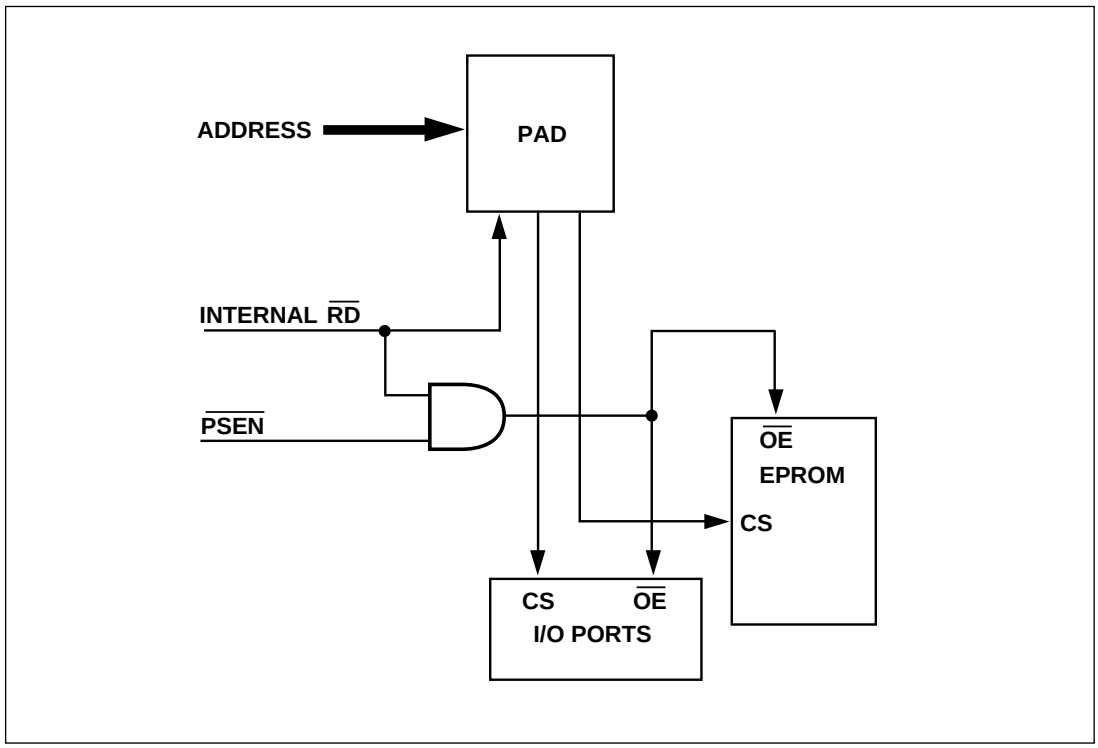
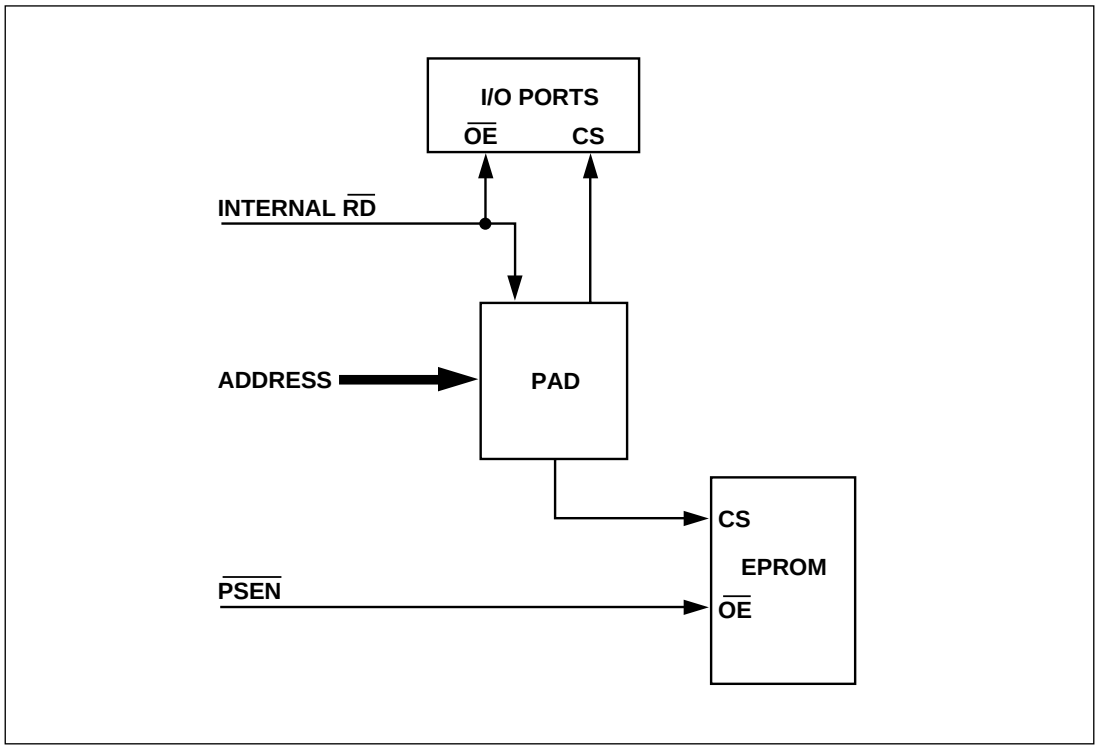


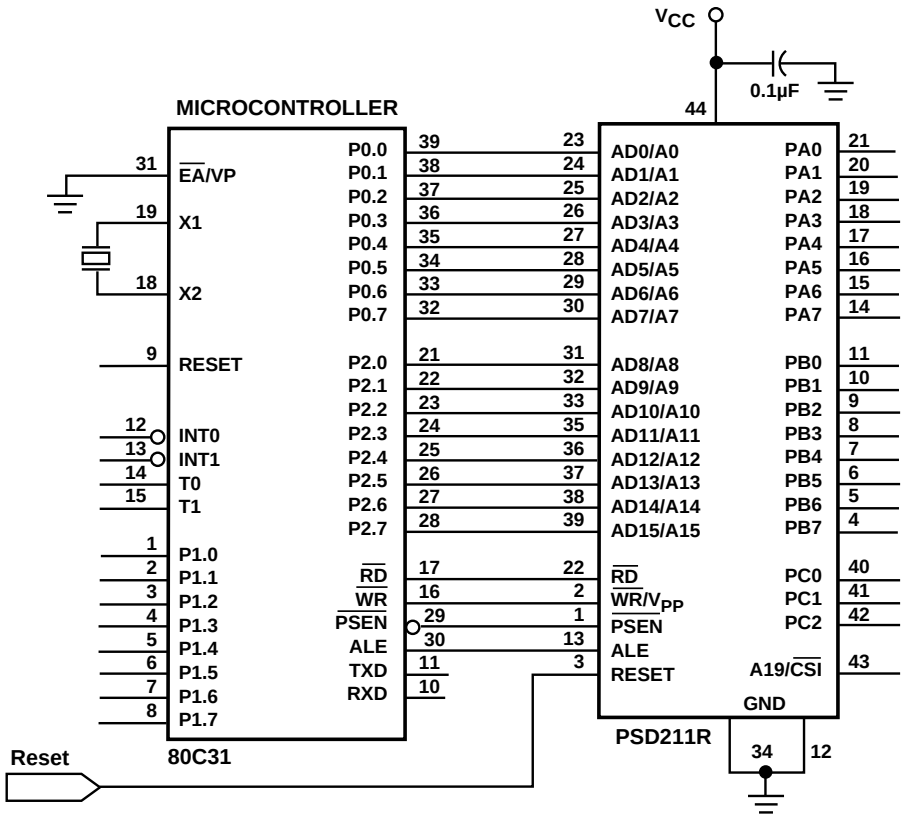
Figure 10. 8031-Compatible Separate Code and Data Address Spaces



14.0 System Applications

In Figure 11, the PSD211R is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. Only the necessary connections are shown.

Figure 11. Interface With Intel's 80C31

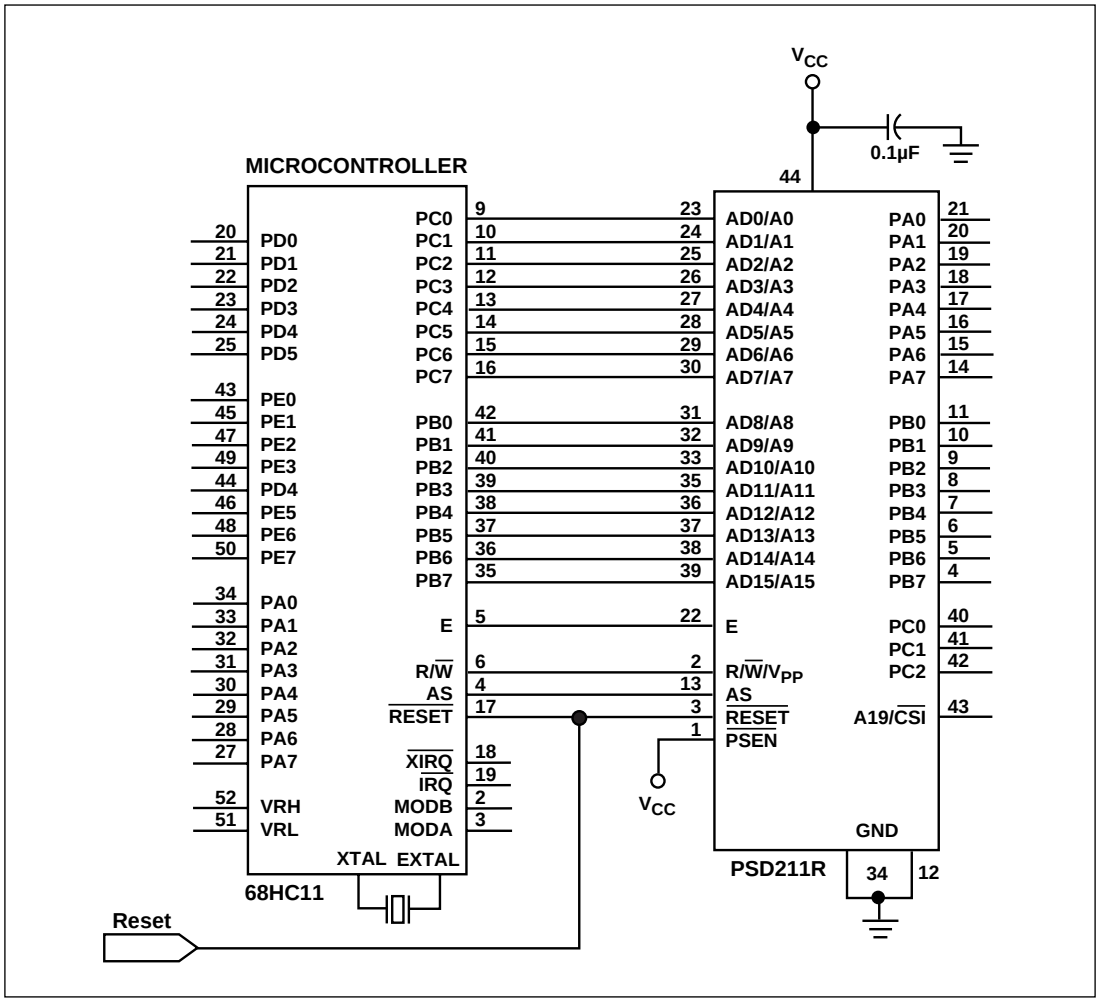


NOTE: RESET to the PSD211R must be the output of a RESET chip or buffer. If RESET to the 80C31 is the output of an RC circuit, a separate buffered RC RESET to the PSD211R (shorter than the 80C31 RC RESET) must be provided to avoid a race condition.

14.0 System Applications (cont.)

In Figure 12, the PSD211R is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. Only the necessary connections are shown.

Figure 12. Interface With Motorola's 68HC11



15.0 Security Mode

Security Mode in the PSD211R locks the contents of PAD A, PAD B, and all the configuration bits. The EPROM and I/O contents can be accessed only through the PAD. The Security Mode must be set by PSDsoft prior to run-time. The Security Bit can only be erased on the UV parts using a full-chip erase. If Security Mode is enabled, the contents of the PSD211R can not be uploaded (copied) on a device programmer.

16.0 Power Management

PSDs from all 211R families use zero-power memory techniques that place memory into Standby Mode between MCU accesses. The memory becomes active briefly after an address transition, then delivers new data to the outputs, latches the outputs, and returns to Standby. This is done automatically and the designer has to do nothing special to benefit from this feature.

In addition to the benefits of Zero-power memory technology, there are ways to gain additional savings. The following factors determine how much current the entire PSD device uses:

- Use of $\overline{CSI}$ (Chip Select Input)
- Setting of the CMiser bit
- Setting of the Turbo Bit (ZPSD only)
- The number of product terms used in the PAD
- The composite frequency of the input signals to the PAD
- The loading on I/O pins.

The total current consumption for the PSD is calculated by summing the currents from memory, PAD logic, and I/O pins, based on your design parameters and the power management options used.

16.1 $\overline{CSI}$ Input

Driving the $\overline{CSI}$ pin inactive (logic 1) disables the inputs of the PSD and forces the entire PSD to enter Power-down Mode, independent of any transition on the MCU bus (address and control) or other PSD inputs. During this time, the PSD device draws only standby current (micro-amps). Alternately, driving a logic 0 on the $\overline{CSI}$ pin returns the PSD to normal operation. See Tables 7A and 7B for information on signal states during Power-down Mode.

The CSI pin feature is available only if enabled in the PSDsoft Configuration utility.

16.2 CMiser bit

In addition to power savings resulting from the Zero-power technology used in the memory, the CMiser feature saves even more power under certain conditions. Savings are significant when the PSD is configured for an 8-bit data path because the CMiser feature turns off half of the array when memory is being accessed (the memory is divided internally into odd and even arrays). See the DC characteristics table for current usage related to the CMiser bit.

You should keep the following in mind when using this bit:

- Setting of this bit is accomplished with PSDsoft at the design stage, prior to run-time.
- Memory access times are extended by 10 nsec for standard voltage (non-V) devices, and 20 nsec for low voltage (V) devices.

16. Power Management (cont.)

16.3 Turbo Bit (ZPSD only)

The turbo bit is controlled by the MCU at run-time and is accessed through bit zero of the Power Management Register (PMR). The PMR is located in CSIOPORT space at offset 10h.

Power Management Register (PMR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	*	Turbo bit
1=OFF	1=OFF	1=OFF	1=OFF	1=OFF	1=OFF	1=OFF	1=OFF

*Future Configuration bits are reserved and should be set to one when writing to this register.

The default value at reset of all bits in the PMR is logic 0, which means the Turbo feature is enabled. The PAD logic (PAD A and PAD B) of the PSD will operate at full speed and full power. When the Turbo bit is set to logic 1, the Turbo feature is disabled. When disabled, the PAD logic will draw only standby current (micro-amps) while no PAD inputs change. Whenever there is a transition on any PAD input (including MCU address and control signals), the PAD logic will power up and will generate new outputs, latch those outputs, then go back to Standby Mode. Keep in mind that the signal propagation delay through the PAD logic increases by 10 nsec for non-V devices, and 20 nsec for V devices while in non-turbo mode. Use of the Turbo bit does not affect the operation or power consumption of memory.

Tremendous power savings are possible by setting the Turbo bit and going into non-turbo mode. This essentially reduces the DC power consumption of the PAD logic to zero. It also reduces the AC power consumption of PAD logic when the composite frequency of all PAD inputs change at a rate less than 40 MHz for non-V devices, and less than 20 MHz for V devices. Use figures 13 and 14 to calculate AC and DC current usage in the PAD with the Turbo bit on and off. You will need to know the number of product terms that are used in your design and you will have to calculate the composite frequency of all signals entering the PAD logic.

16.4 Number of Product Terms in the PAD Logic

The number of product terms used in your design relates directly to how much current the PADs will draw. Therefore, minimizing this number will be in your best interest if power is a concern for you. Basically, the amount of product terms your design will use is based on the following (see Figure 4):

- Each of the EPROM block selects, ES0-ES7 uses one product term (for a total of 8).
- The CSIOPORT select uses one product term.
- Port B, pins PB0-PB3 are allocated four product terms each if used as outputs.
- Port B, pins PB4-PB7 are allocated two product terms each if used as outputs.
- Port C, pins PC0-PC2 are allocated one product term each if used as outputs.

Given the above product term allocation, keep the following three points in mind when calculating the total number of product terms your design will require:

1) The EPROM block selects and CSIOPORT select will use a product term whether you use these blocks or not. This means you start out with 9 product terms, and go up from there.
2) For Port B, if you use a pin as an output and your logic equation requires only one product term, you still have to include all the available product terms for that pin for power consumption, even though only one product term is specified. For example, if the output equation for pin PB0 uses just one product term, you will have to count PB0 as contributing four product terms to the overall count. With this in mind, you should use Port C for the outputs that only require one product term and PB4-7 for outputs that require two product terms. Use pins PB0-3 if you need outputs requiring more than two product terms or you have run out of outputs.
3) The following PSD functions do not consume product terms: MCU I/O mode, Latched Address Output, and PAD inputs (logic or address).

16.0 Power Management (cont.)

16.5 Composite Frequency of the Input Signals to the PAD Logic

The composite frequency of the input signals to the PADs is calculated by considering all transitions on any PAD input signal (including the MCU address and control inputs). Once you have calculated the composite frequency and know the number of product terms used, you can determine the total AC current consumption of the PAD by using Figure 13 or Figure 14. From the figures, notice that the DC component (f = 0 MHz) of PAD current is essentially zero when the turbo feature is disabled, and that the AC component increases as frequency increases.

When the turbo feature is disabled, the PAD logic can achieve low power consumption by becoming active briefly, only when inputs change. For standard voltage (non-V) devices, the PAD logic will stay active for 25 nsec after it detects a transition on any input. If there are more transitions on any PAD input within the 25 nsec period, these transitions will not add to power consumption because the PAD logic is already active. This effect helps reduce the overall composite frequency value. In other words, narrowly spaced groups of transitions on input signals may count as just one transition when estimating the composite frequency.

Note that the “knee” frequency in Figure 13 is 40 MHz, which means that the PAD will consume less power only if the composite frequency of all PAD inputs is less than 40 MHz. When the composite frequency is above 40 MHz, the PAD logic never gets a chance to shut down (inputs are spaced less than 25 nsec) and no power savings can be achieved. Figure 14 is for low-voltage devices in which the “knee” frequency is 20 MHz.

Take the following steps to calculate the composite frequency:

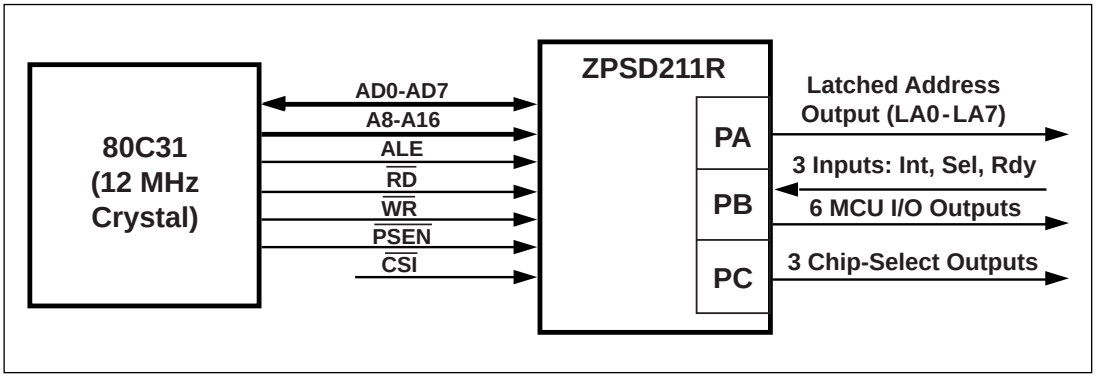
1) Determine your highest frequency input for either PAD A or PAD B.
2) Calculate the period of this input and use this period as a basis for determining the composite frequency.
3) Examine the remaining PAD input signals within this base period to determine the number of distinct transitions.
4) Signal transitions that are spaced further than 25 nsec apart count as a distinct transition (50 nsec for low-voltage V devices). Signal transitions spaced closer than 25 nsec count as the same transition.
5) Count up the number of distinct transitions and divide that into the value of the base period.
6) The result is the period of the composite frequency. Divide into one to get the composite frequency value.

Unfortunately, this procedure is complicated and usually not deterministic since different inputs may be changing in various cycles. Therefore, we recommend you think of the situation that has the most activity on the inputs to the PLD and use this to calculate the composite frequency. Then you will have a number that represents your best estimate at the worst case scenario.

Since this is a complicated process, the following example should help.

Example Composite Frequency Calculation

Suppose you had the following circuit:

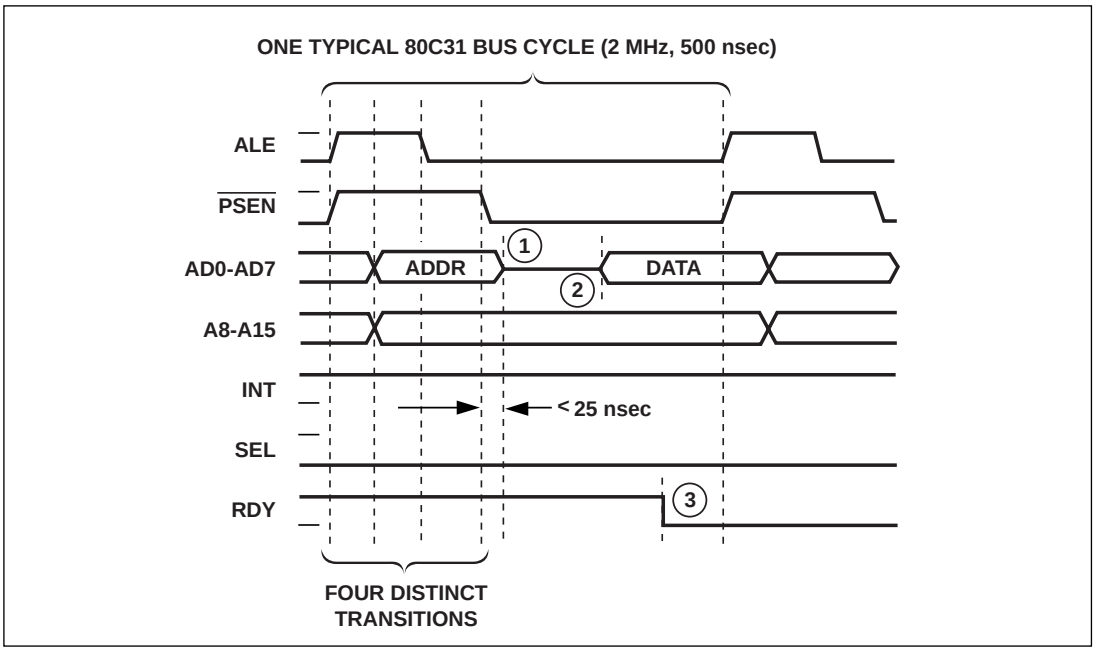


16.0 Power Management (cont.)

All the inputs shown, except CSI, go to the PAD logic. These signals must be taken into consideration when calculating the composite frequency. Before we make the calculation, let's establish the following conditions:

- The input with the highest frequency is ALE, which is 2 MHz. So our base period is 500 nsec for this example.
- Only the address information from the multiplexed signals AD0-AD7 reach the PAD logic because of the internal address latch. Signal transitions from data on AD0-AD7 do not reach the PADs.
- The three inputs (Int, Sel, or Rdy) change state very infrequently relative to the 80C31 bus signals.

Now, lets assume the following is a snapshot in time of all the input signals during a typical 80C31 bus cycle. We'll use a code fetch as an example since that happens most often.



The calculation of the composite frequency is as follows:

- There are four distinct transitions (first four dotted lines) within the base period of 500 nsec. These first four transitions all count toward the final composite frequency.
- The transition at (1) in the diagram does not count as a distinct transition because it is within 25 nsec of a neighboring transition (use 50 nsec for a ZPSD211RV device).
- Transition (2) above does not add to the composite frequency because only the internally latched address signals reach the PADs, the data signal transitions do not.
- The transition at (3) just happens to appear in this snapshot, but its frequency is so low that it is not a significant contributor to the overall composite frequency, and will not be used.
- Divide the 500 nsec base period by the four (distinct transitions), yielding 125 nsec. 1/125 nsec = 8 MHz.
- Use 8 MHz as the composite frequency of PAD inputs when calculating current consumption. (See the next section for a sample current calculation.)

16.6 Loading on I/O pins

A final consideration when calculating the current usage for the entire PSD device is the loading on I/O pins. All specifications for PSD current consumption in this document assume zero current flowing through PSD I/O pins (including ADIO). I/O current is dictated by the individual design implementation, and must be calculated by the designer. Be aware that I/O current is a function of loading on the pins and the frequency at which the signals toggle.

17.0 Calculating Power

Once you have read the “Power Management” section, you should be able to calculate power. The following is a sample power calculation:

Conditions		
Part Used	=	ZPSD211R (V_{CC} = 5.0 V)
MCU ALE Clock Frequency	=	2.0 MHz
Composite ZPLD input Frequency	=	8.0 MHz (see example in above section)
% EPROM Access	=	80%
% I/O access	=	20%
% Time CSI is high (standby mode)	=	90%
% Time CSI is low (normal operation mode)	=	10%
# Product terms used (see previous section)	=	10
Turbo bit	=	OFF (Turbo Mode disabled)
CMiser bit	=	ON
MCU Bus Configuration	=	8-bit multiplexed bus mode

Calculation (Based on Typical AC and DC Currents)

I_{CC} total = Istandby x % time CSI is high + [I_{CC} (AC) + I_{CC} (DC)] x % time CSI is low.

= Istandby x % time CSI is high +
[%EPROM Access x 0.8 mA/MHz x Freq. ALE
+ ZPLD AC current (Figure 13: 10 PTs, 8 MHz, Non-Turbo)]
x % time CSI is low.

= 10 µA x 0.9 + (0.8 x 0.8 mA/MHz x 2 MHz + 5.0 mA) x 0.1

= 9.0 µA + (1.28 mA + 5.0 mA) x 0.1

= 637 µA, based on the system operating in standby 90% of the time

NOTES: 1. Calculation is based on the assumption that Iout = 0 mA (no I/O pin loading).
2. I_{CC} (DC) is zero for all ZPSD devices operating in non-turbo mode.
3. 10 product terms: 8 for EPROM, 1 for CSIOPORT, 1 for CS8
4. The 5% I/O access in the conditions section is when the MCU accesses CSIOPORT space.
5. Standby Mode can also be achieved without using the $\overline{CSI}$ pin. The ZPSD device will automatically go into Standby while no inputs are changing on any pin, and Turbo Mode is disabled.

17.0 Calculating Power (cont.)

Figure 13. Typical I_{CC} vs. Frequency for the PAD (V_{CC} = 5 V)

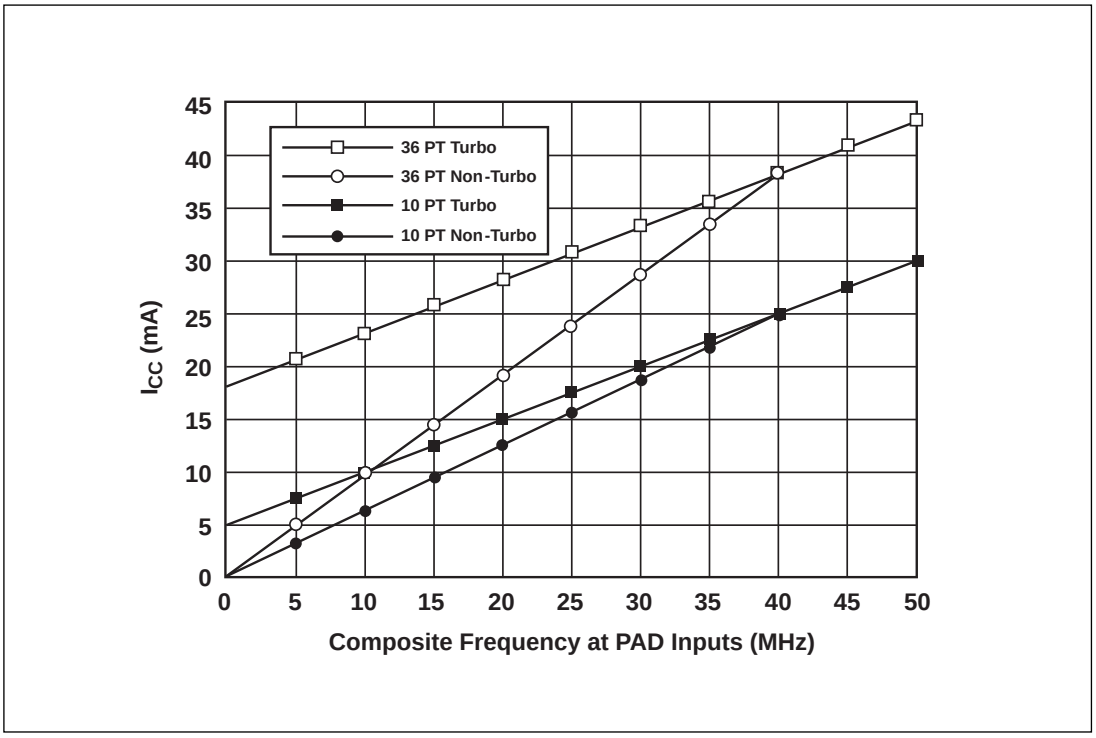


Figure 14. Typical I_{CC} vs. Frequency for the PAD (V_{CC} = 3 V)

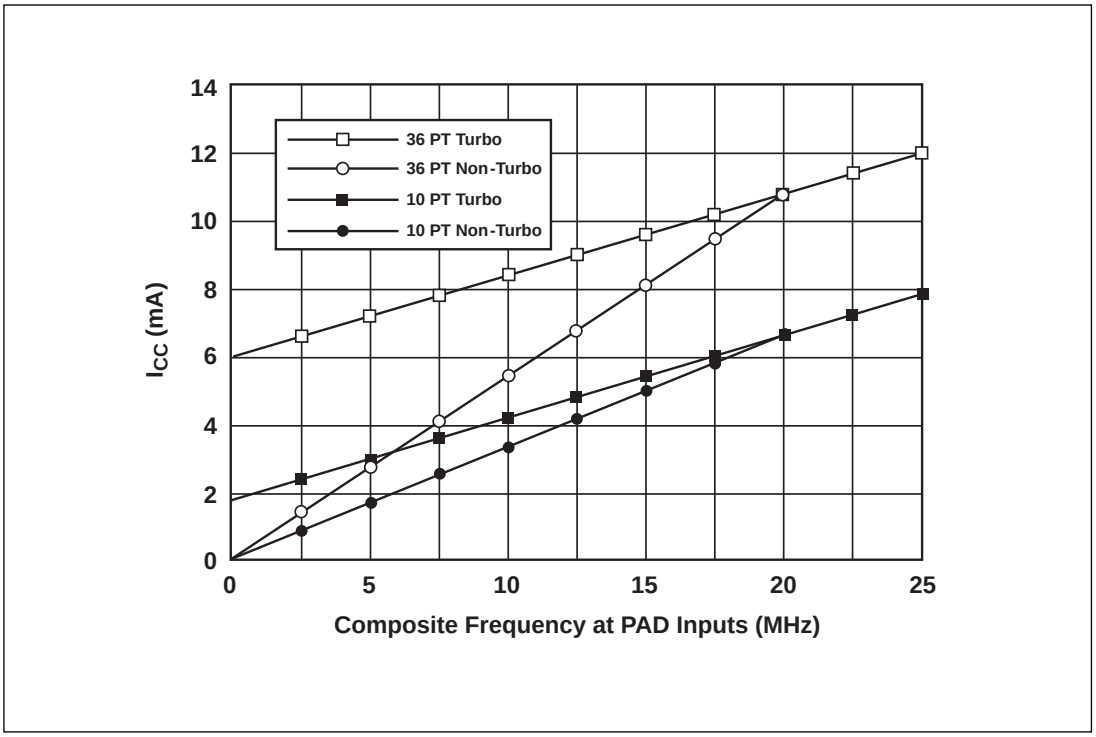


Figure 15. I_{OL} vs. V_{OL} (5 V ± 10%)

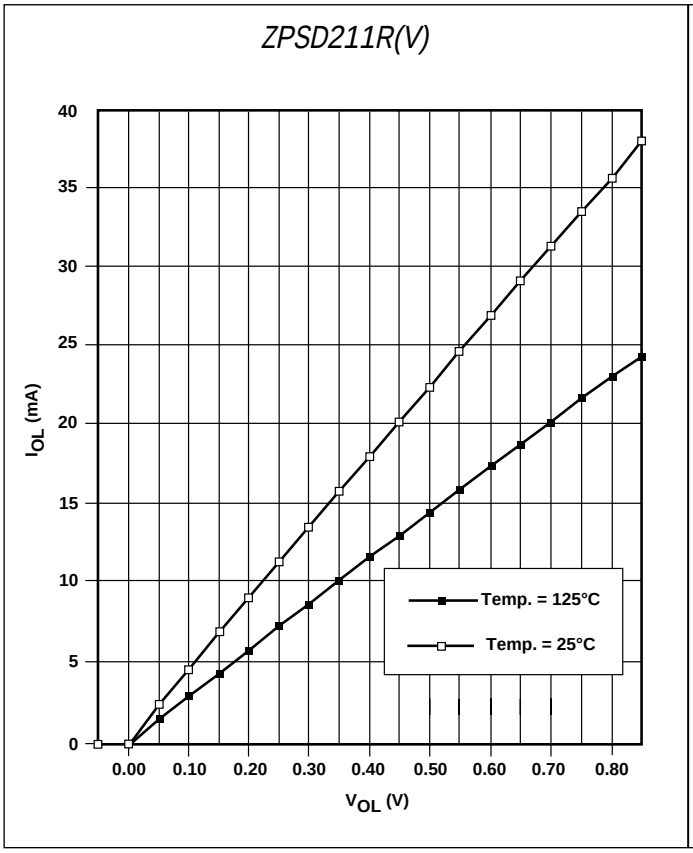


Figure 16. Normalized I_{CC} (DC vs. V_{CC}) (V_{CC} = 3.0 V)

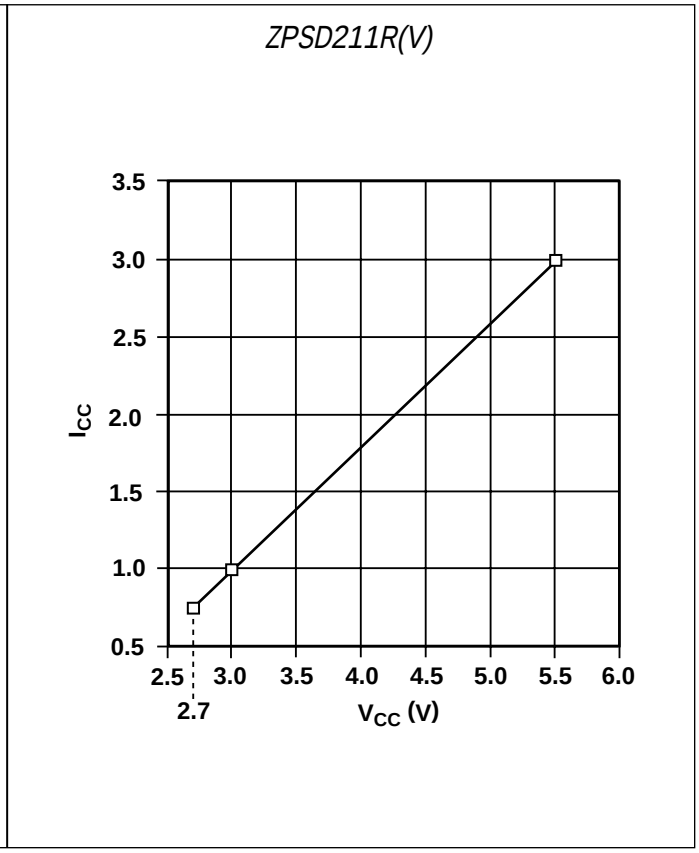


Figure 17. Normalized I_{CC} (AC) (V_{CC} = 3.0 V)

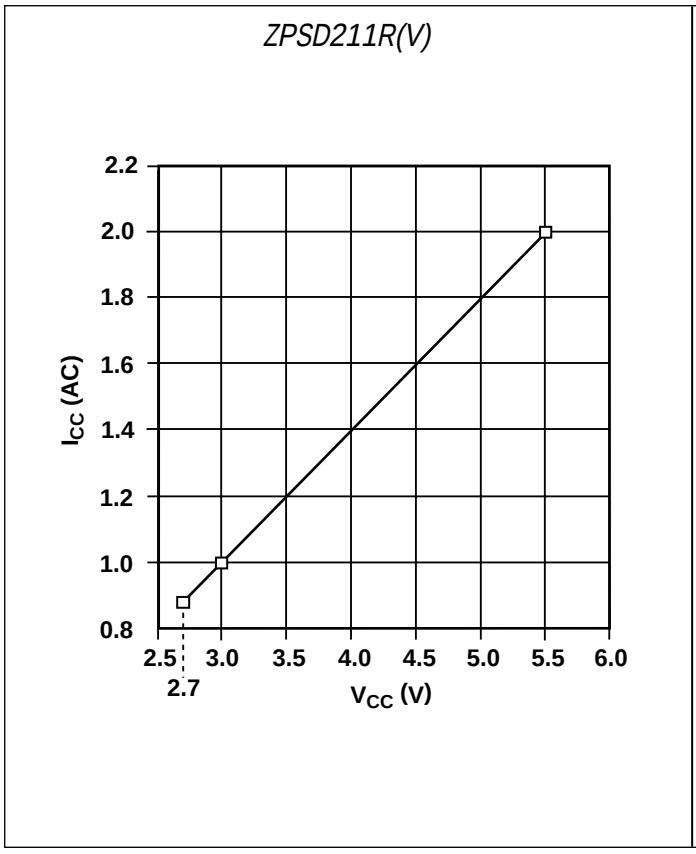
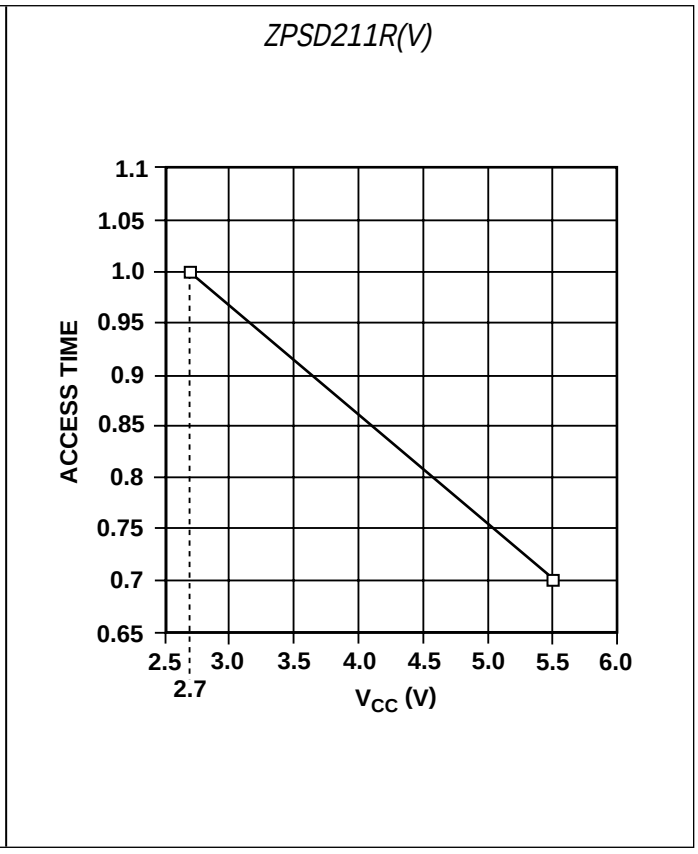


Figure 18. Normalized Access Time (T6) (V_{CC} = 3.0 V)



18.0 Specifications

18.1 Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

18.2 Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance
Commercial	0° C to +70°C	+ 3 V[1], + 5 V	± 10%
Industrial	–40° C to +85°C	+ 3 V[1], + 5 V	± 10%

NOTE: 1. 3 V available on ZPSD211RV only.

18.3 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	PSD Versions, All Speeds	4.5	5	5.5	V
V_{CC}	Supply Voltage	ZPSD V Versions Only, All Speeds	2.7	3.0	5.5	V

18.4 Pin Capacitance[1]

Symbol	Parameter	Conditions	Typical[2]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 1. This parameter is only sampled and is not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

18.5 AC/DC Characteristics – PSD211R/ZPSD211R (All 5 V devices)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage	4.5 V < V_{CC} > 5.5 V	2		V_{CC} + .1	V
V_{IL}	Low-Level Input Voltage	4.5 V < V_{CC} > 5.5 V	–0.5		0.8	V
V_{OH}	Output High Voltage	I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{OL}	Output Low Voltage (See Figure 14)	I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	V
I_{SB} (Notes 1,4)	ZPSD211R Standby Supply Current			10	20	µA
	PSD211R Standby Supply Current			50	100	µA
I_{LI}	Input Leakage Current	V_{SS} < V_{IN} > V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current	.45 < V_{IN} > V_{CC}	–10	± 5	10	µA
I_{CC} (DC) (Note 3)	ZPSD211R Operating Suppy Current	ZPLD Turbo Mode = Off, f = 0 MHz		See I_{SB}		µA
		ZPLD Turbo Mode = On, f = 0 MHz		0.5	1	mA/PT
		EPROM, f = 0 MHz		0	0	µA
		SRAM, f = 0 MHz		0	0	µA
	PSD211R Operating Supply Current	PLD, f = 0 MHz		0.5	1	mA/PT
		EPROM, f = 0 MHz		0	0	µA
		SRAM, f = 0 MHz		0	0	µA
I_{CC} (AC) (Note 3)	ZPLD AC Base	(See Figure 13)		Fig. 13	1	mA/MHz
	EPROM Access	CMiser = On and 8-Bit Bus Mode		0.8	2.0	mA/MHz
	AC Adder	CMiser = Off		1.8	4.0	mA/MHz

NOTES: 1. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
3. I_{OUT} = 0 mA.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.

18.6 AC/DC DC Characteristics ZPSD211RV (3 V devices only)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	2.7	3	5.5	V
V_{IH}	High-Level Input Voltage	2.7 V < V_{CC} > 5.5 V	.7 V_{CC}		V_{CC} + .5	V
V_{IL}	Low-Level Input Voltage	2.7 V < V_{CC} > 5.5 V	–0.5		.3 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –20 µA, V_{CC} = 2.7 V	2.6	2.69		V
		I_{OH} = –1 mA, V_{CC} = 2.7 V	2.3	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 20 µA, V_{CC} = 2.7 V		0.01	0.1	V
		I_{OL} = 4 mA, V_{CC} = 2.7 V		0.15	0.45	V
I_{SB} (Notes 1,4)	Standby Supply Current	V_{CC} = 3.0 V		1	5	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–1	.1	1	µA
I_{CC} (DC) (Note 3)	Operating Supply Current	ZPLD Turbo Mode= Off, f = 0 MHz, V_{CC} = 3.0 V	See I_{SB}			µA
		ZPLD Turbo Mode= On, f = 0 MHz, V_{CC} = 3.0 V		0.17	0.35	mA/PT
		EPROM, f = 0 MHz, V_{CC} = 3.0 V		0	0	µA
I_{CC} (AC) (Note 3)	ZPLD AC Base	See Figure 14 (V_{CC} = 3.0 V)		Fig. 14	0.5	mA/MHz
	EPROM Access AC Adder	CMiser = On and 8-Bit Bus Mode (V_{CC} = 3.0 V)		0.4	1	mA/MHz
		CMiser = Off (V_{CC} = 3.0 V)		0.9	1.7	mA/MHz

NOTES: 1. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
3. I_{OUT} = 0 mA.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.

18.7 Timing Parameters – PSD211R/ZPSD211R (All 5 V devices)

Symbol	Parameter	-70		-90		-15		CMiser On = Add	Unit
		Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	18		20		40		0	ns
T2	Address Set-up Time	5		5		12		0	ns
T3	Address Hold Time	7		8		10		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0	ns
T5	ALE Valid to Data Valid		80		100		160	10	ns
T6	Address Valid to Data Valid		70		90		150	10	ns
T7	$\overline{CSI}$ Active to Data Valid		80		100		160	10	ns
T8	Leading Edge of Read to Data Valid		20		32		55	0	ns
T8A	Leading Edge of Read to Data Valid in 8031-Based Architecture Operating with $\overline{PSEN}$ and $\overline{RD}$ in Separate Mode		32		32		55	0	ns
T9	Read Data Hold Time	0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		20		35		35	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$ Pulse Width	35		45		60		0	ns
T12A	$\overline{WR}$ Pulse Width	18		25		35		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	5		5		5		0	ns
T14	Address Valid to Trailing Edge of Write	70		120		150		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	80		130		160		0	ns
T16	Write Data Set-up Time	18		25		30		0	ns
T17	Write Data Hold Time	5		5		10		0	ns
T18	Port to Data Out Valid Propagation Delay		25		28		35	0	ns
T19	Port Input Hold Time	0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid		30		35		50	0	ns
T21	ADi[1] or Control to $\overline{CSO}$i[2] Valid	6	20	6	25	6	35	10	ns
T22	ADi[1] or Control to $\overline{CSO}$i[2] Invalid	5	20	5	25	4	35	10	ns
T23	Latched Address Outputs, Port A		22		22		28	0	ns
T30	$\overline{CSI}$ Active to $\overline{CSO}$i[2] Active	8	37	9	40	9	50	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSO}$i[2] Inactive	8	37	9	40	9	50	0	ns
T32	Direct PAD Input[3] as Hold Time	0		0		12		0	ns
T33	R/W Active to E High	18		20		30		0	ns
T34	E End to R/$\overline{W}$	18		20		30		0	ns
T35	AS Inactive to E high	0		0		0		0	ns
T36	Address to Leading Edge of Write	18		20		25		0	ns

NOTES: 1. ADi = any address line.
2. $\overline{CSO}$i = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
3. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
4. Control signals $\overline{RD}$/E or $\overline{WR}$ or R/$\overline{W}$.

18.8 Timing Parameters – ZPSD211RV (3 V devices only)

Symbol	Parameter	-20		-25		CMiser On = Add	Turbo Off = Add	Unit
		Min	Max	Min	Max			
T1	ALE or AS Pulse Width	50		60		0	0	ns
T2	Address Set-up Time	15		20		0	0	ns
T3	Address Hold Time	15		20		0	0	ns
T4	Leading Edge of Read to Data Active	0		0		0	0	ns
T5	ALE Valid to Data Valid		200		250	20	0	ns
T6	Address Valid to Data Valid		200		250	20	0	ns
T7	$\overline{CSI}$ Active to Data Valid		200		250	20	0	ns
T8	Leading Edge of Read to Data Valid		50		60	0	0	ns
T8A	Leading Edge of Read to Data Valid in 8031-Based Architecture Operating with $\overline{PSEN}$ and $\overline{RD}$ in Separate Mode		70		80	0	0	ns
T9	Read Data Hold Time	0		0		0	0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0	0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	75		85		0	0	ns
T12A	$\overline{WR}$ Pulse Width	45		55		0	0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	5		5		0	0	ns
T14	Address Valid to Trailing Edge of Write	200		250		0	0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	200		250		0	0	ns
T16	Write Data Set-up Time	40		50		0	0	ns
T17	Write Data Hold Time	12		15		0	0	ns
T18	Port to Data Out Valid Propagation Delay		50		60	0	0	ns
T19	Port Input Hold Time	0		0		0	0	ns
T20	Trailing Edge of Write to Port Output Valid		60		70	0	0	ns
T21	ADi[1] or Control to $\overline{CSOi}$[2] Valid	5	55	5	60	0	20	ns
T22	ADi[1] or Control to $\overline{CSOi}$[2] Invalid	4	55	4	60	0	20	ns
T23	Latched Address Outputs, Port A		60		60	0	0	ns

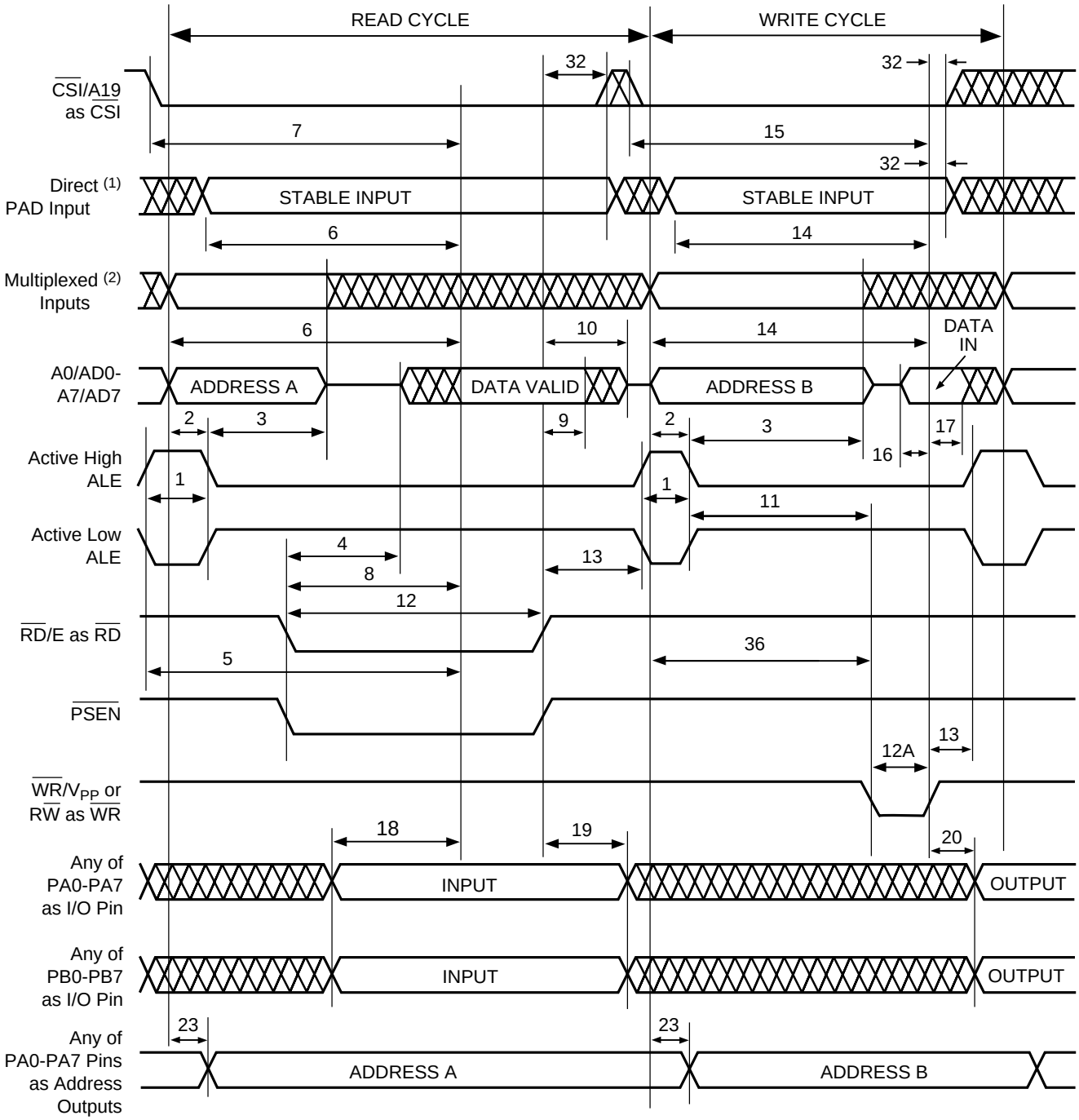
18.8 Timing Parameters – ZPSD211RV (3 V devices only) (cont.)

Symbol	Parameter	-20		-25		CMiser On = Add	Turbo Off = Add	Unit
		Min	Max	Min	Max			
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	3		3		0	0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$[2] Active	9	80	9	90	0	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$[2] Inactive	9	80	9	90	0	0	ns
T32	Direct PAD Input[3] as Hold Time	0		0		0	0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	40		50		0	0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	40		50		0	0	ns
T35	AS Inactive to E high	0		0		0	0	ns
T36	Address to Leading Edge of Write	35		40		0	0	ns

NOTES: 1. ADi = any address line.
2. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
3. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
4. Control signals $\overline{RD}$/E or $\overline{WR}$ or R/$\overline{W}$.

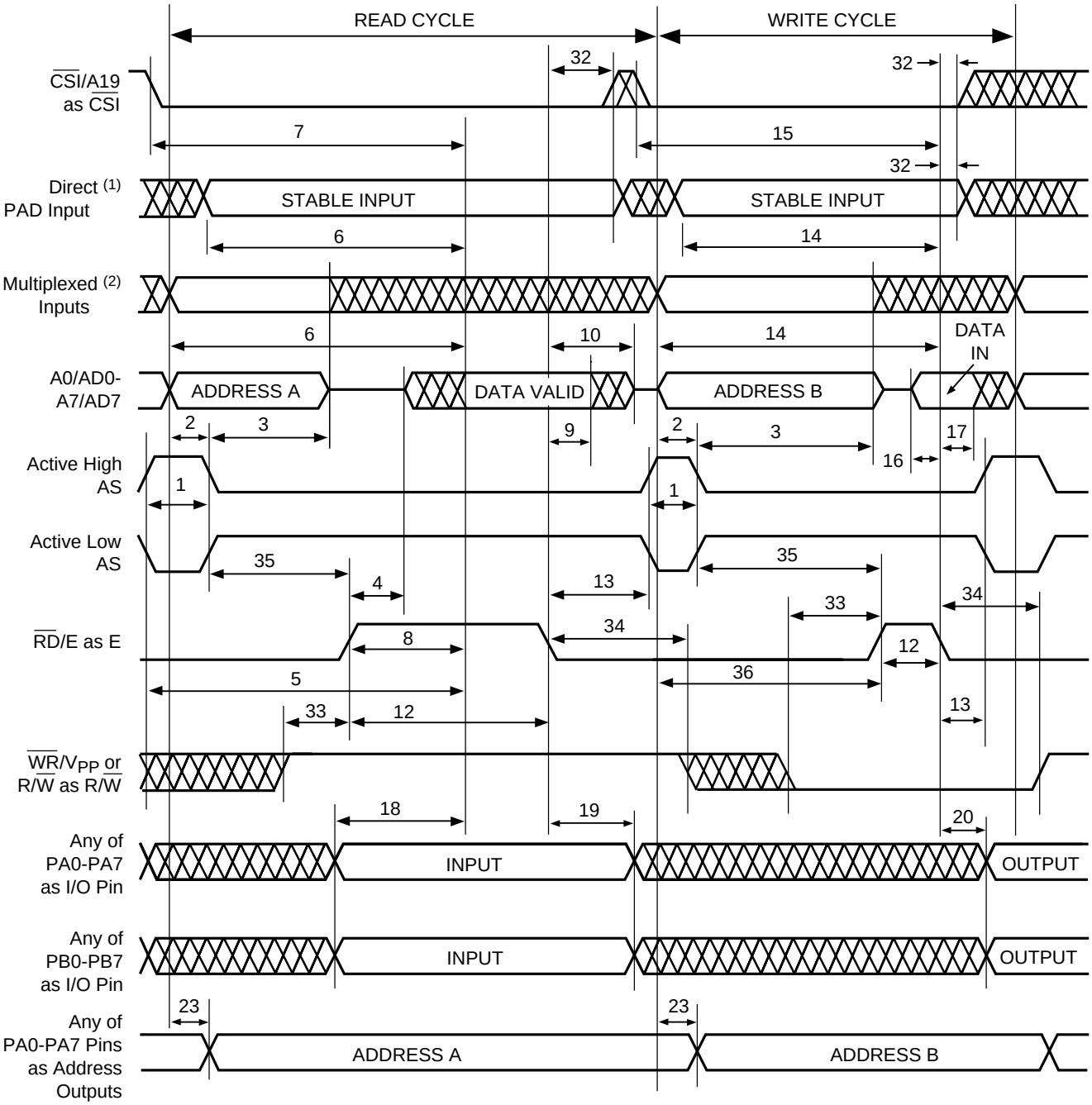
18.9 Timing Diagrams for all PSD211R Parts

Figure 19. Timing using RD and WR signals



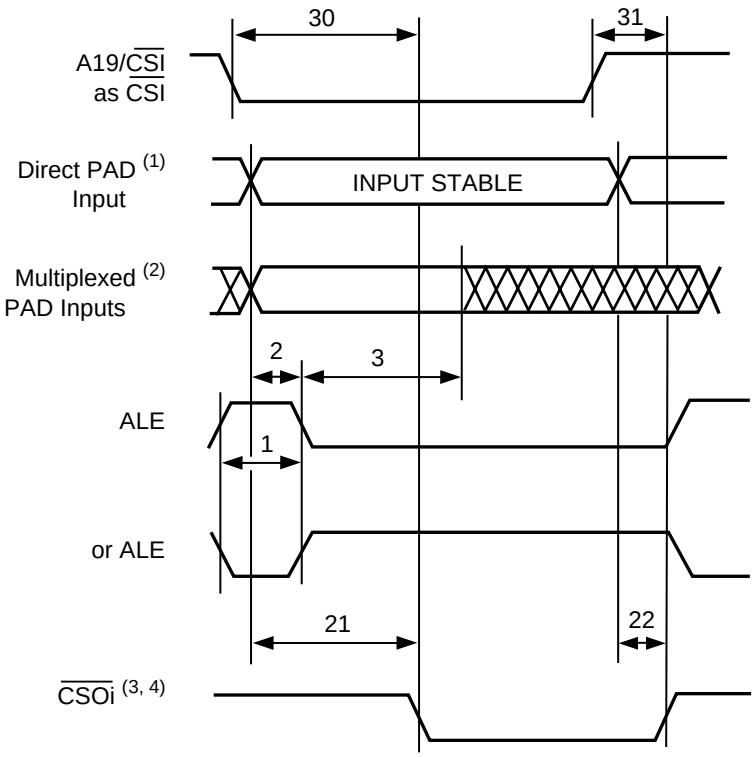
See referenced notes on page 38.

Figure 20. Timing Using R/$\overline{W}$ and E signals



See referenced notes on page 38.

Figure 21. Chip-select Output Timing



Notes for Timing Diagrams

1. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
2. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
3. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
4. CSOi product terms can include any of the PAD input signals shown in Figure 4, except for reset and CSI.

18.10. AC Testing

Figure 22A. AC Testing Input/Output Waveform (5 V Versions)

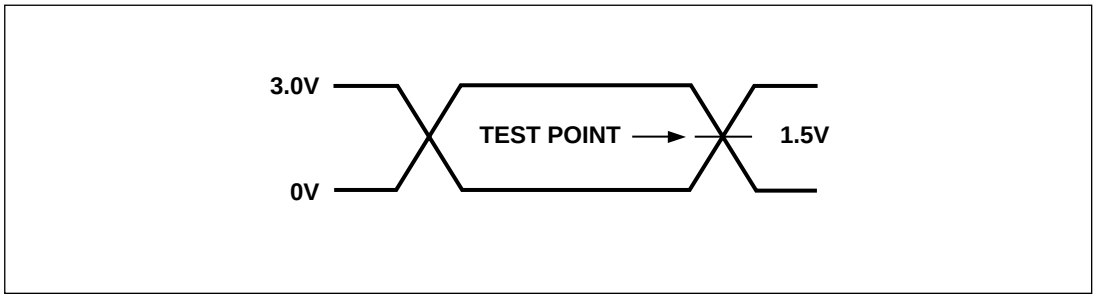


Figure 22B. AC Testing Input/Output Waveform (3 V Versions)

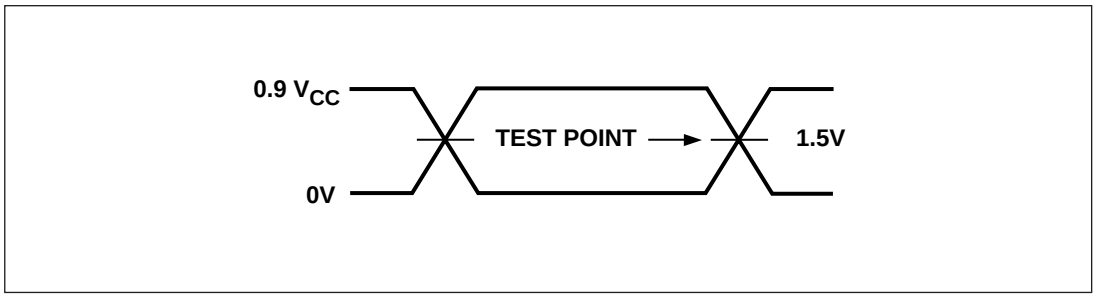


Figure 23A. AC Testing Load Circuit (5 V Versions)

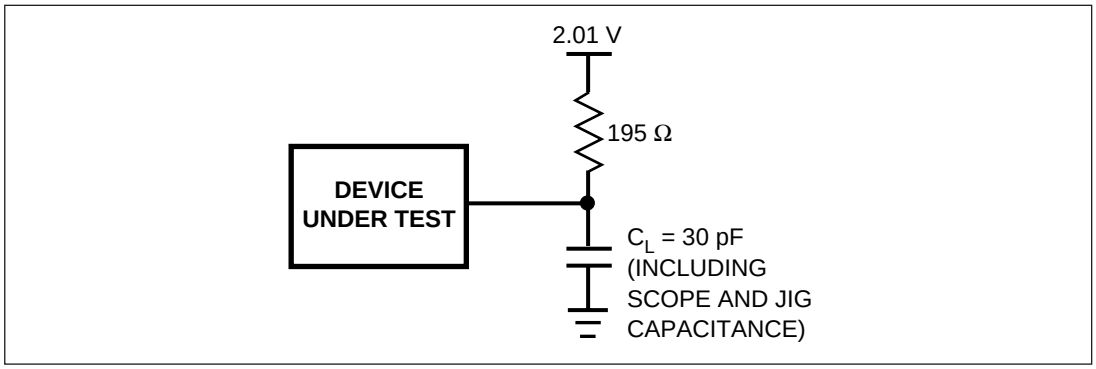
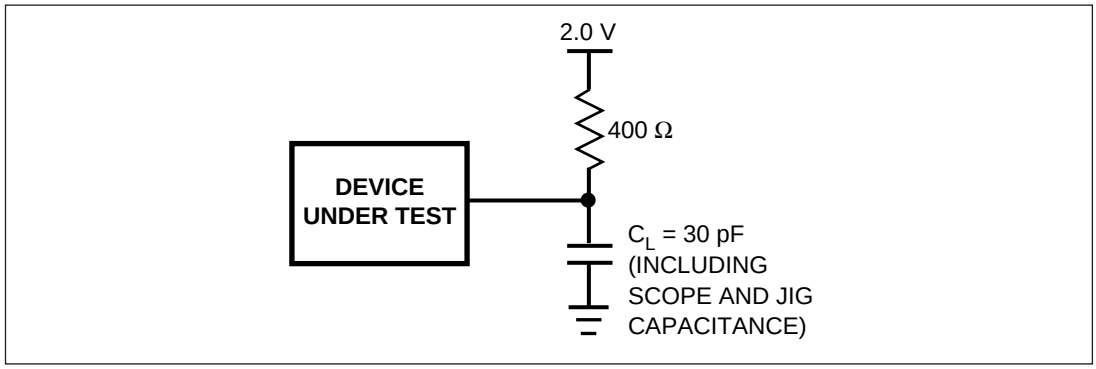


Figure 23B. AC Testing Load Circuit (3 V Versions)



19.0 Pin Assignments

Pin Assignments	Pin No. 44-Pin PLDCC/CLDCC (Package Type L/J)	Pin No. 44-Pin PQFP (Package Type M)
$\overline{PSEN}$	1	39
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	40
RESET	3	41
PB7	4	42
PB6	5	43
PB5	6	44
PB4	7	1
PB3	8	2
PB2	9	3
PB1	10	4
PB0	11	5
GND	12	6
ALE or AS	13	7
PA7	14	8
PA6	15	9
PA5	16	10
PA4	17	11
PA3	18	12
PA2	19	13
PA1	20	14
PA0	21	15
$\overline{RD}$/E	22	16
AD0/A0	23	17
AD1/A1	24	18
AD2/A2	25	19
AD3/A3	26	20
AD4/A4	27	21
AD5/A5	28	22
AD6/A6	29	23
AD7/A7	30	24
A8	31	25
A9	32	26
A10	33	27
GND	34	28
A11	35	29
A12	36	30
A13	37	31
A14	38	32
A15	39	33
PC0	40	34
PC1	41	35
PC2	42	36
A19/$\overline{CSI}$	43	37
V_{CC}	44	38

20.0 Package Information

Figure 24. Drawing L4 – 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

OR

Drawing J2 – 44 Pin Plastic Leaded Chip Carrier (PLDCC) without Window (Package Type J)

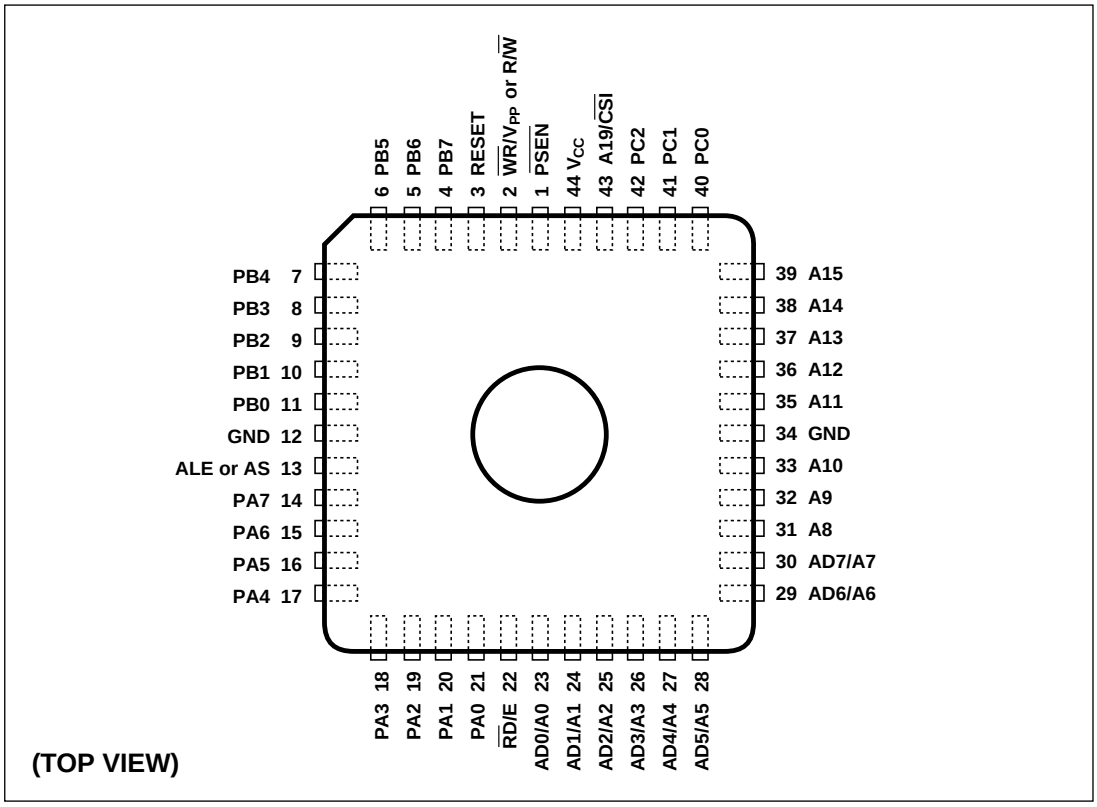
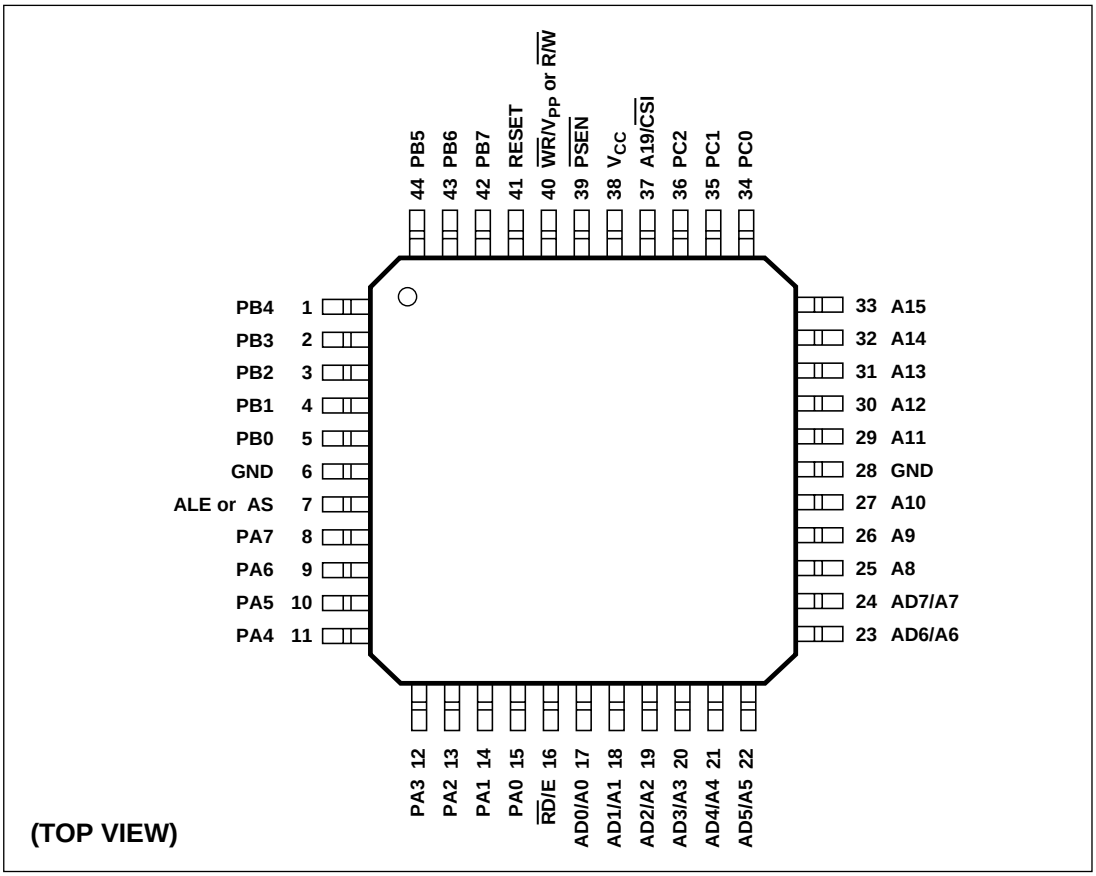
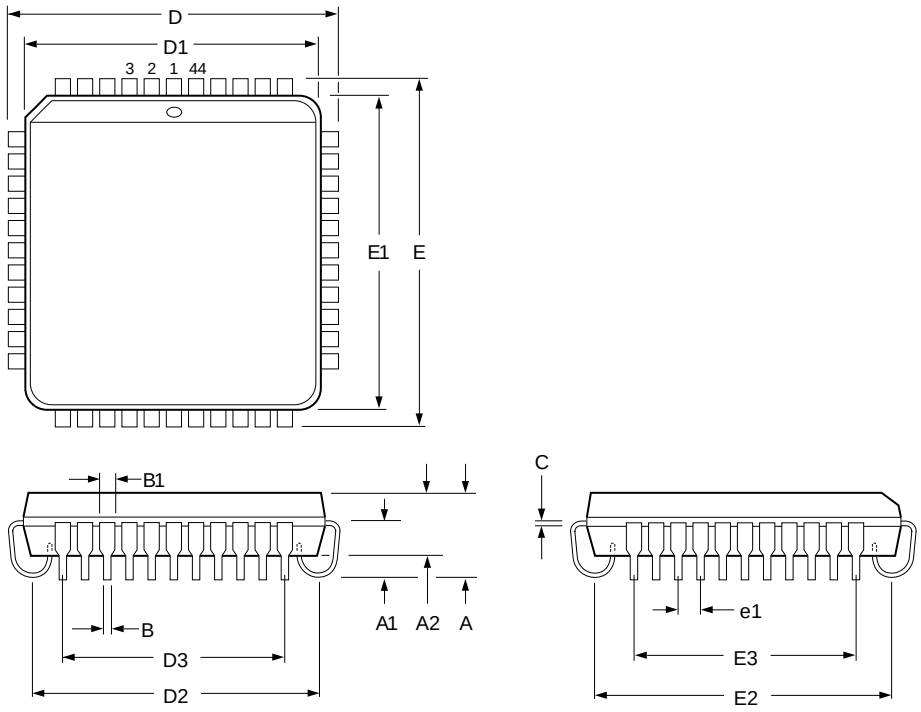


Figure 25. Drawing M1 – 44 Pin Plastic Quad Flatpack (PQFP) (Package Type M)



21.0 Package Drawings

Drawing J2 – 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



Family: Plastic Leaded Chip Carrier

	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.76	3.96		0.148	0.156	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.262		0.0097	0.0103	
D	17.40	17.65		0.685	0.695	
D1	16.51	16.61		0.650	0.654	
D2	14.99	16.00		0.590	0.630	
D3	12.70		Reference	0.500		Reference
E	17.40	17.65		0.685	0.695	
E1	16.51	16.61		0.650	0.654	
E2	14.99	16.00		0.590	0.630	
E3	12.70		Reference	0.500		Reference
e1	1.27		Reference	0.050		Reference
N	44			44		

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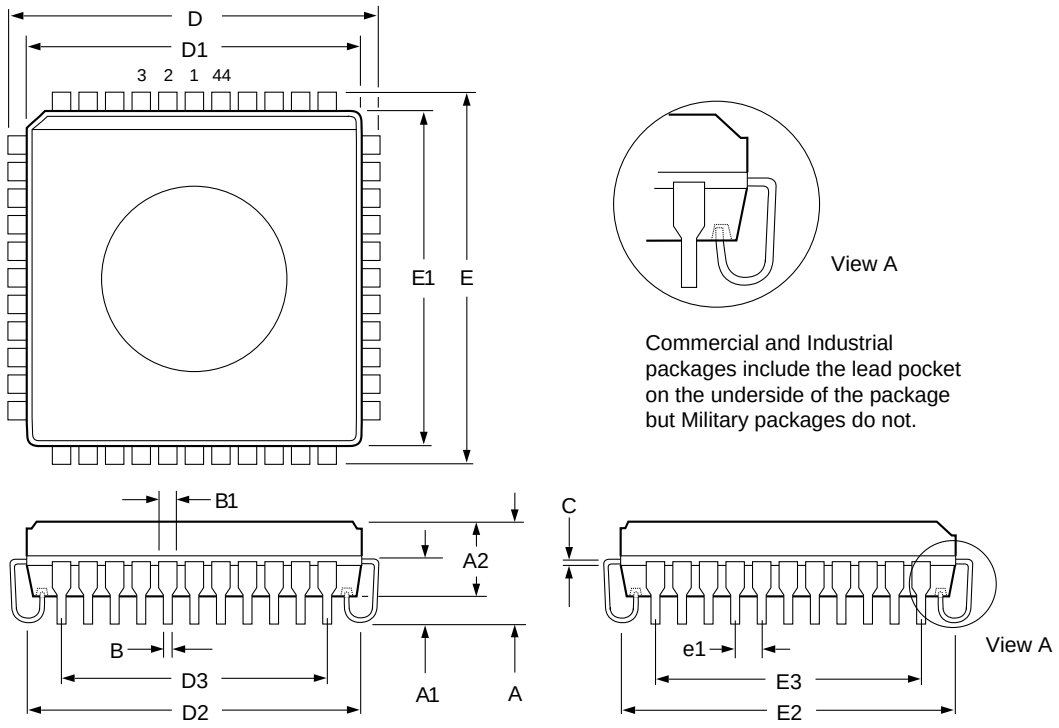
Drawing L4 – 44-Pin Pocketed Ceramic Leaded Chip Carrier (CLDCC) – CERQUAD (Package Type L)



Family: Ceramic Leaded Chip Carrier – CERQUAD

	Millimeters			*Inches*		
Symbol	*Min*	*Max*	*Notes*	*Min*	*Max*	*Notes*
A	3.94	4.57		0.155	0.180	
A1	2.29	2.92		0.090	0.115	
A2	3.05	3.68		0.120	0.145	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15	0.25		0.006	0.010	
D	17.40	17.65		0.685	0.695	
D1	16.31	16.66		0.642	0.656	
D2	14.73	16.26		0.580	0.640	
D3	12.70		Reference	0.500		Reference
E	17.40	17.65		0.685	0.695	
E1	16.31	16.66		0.642	0.656	
E2	14.73	16.26		0.580	0.640	
E3	12.70		Reference	0.500		Reference
e1	1.27		Reference	0.050		Reference
N	44			44		

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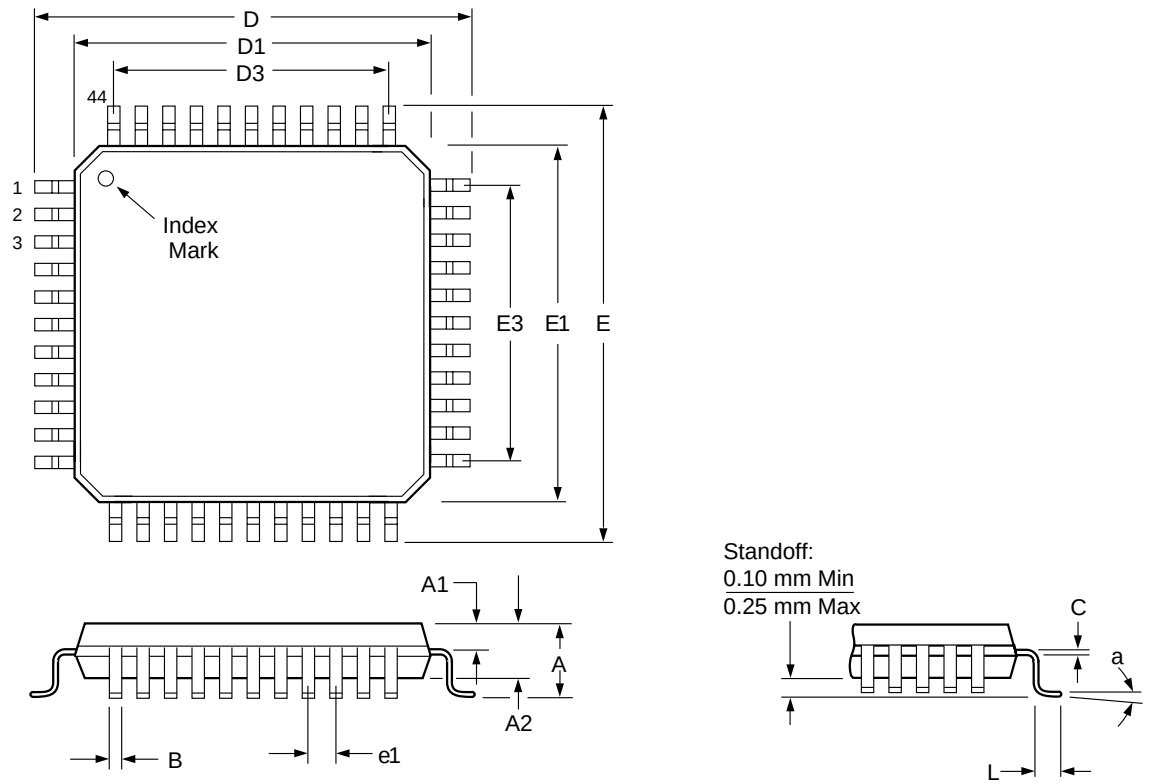
Drawing M1 – 44-Pin Plastic Quad Flatpack (PQFP) (Package Type M)



Family: Plastic Quad Flatpack (PQFP)

	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	–	2.35		–	0.092	
A1	1.075		Reference	0.042		Reference
A2	1.95	2.10		0.077	0.083	
B	0.30	0.45		0.012	0.018	
C	0.13	0.23		0.005	0.009	
D	13.20			0.520		
D1	10.00			0.394		
D3	8.00		Reference	0.315		Reference
E	13.20			0.520		
E1	10.00			0.394		
E3	8.00		Reference	0.315		Reference
e1	0.80		Reference	0.031		Reference
L	0.73	1.03		0.029	0.040	
N	44			44		

030195R4

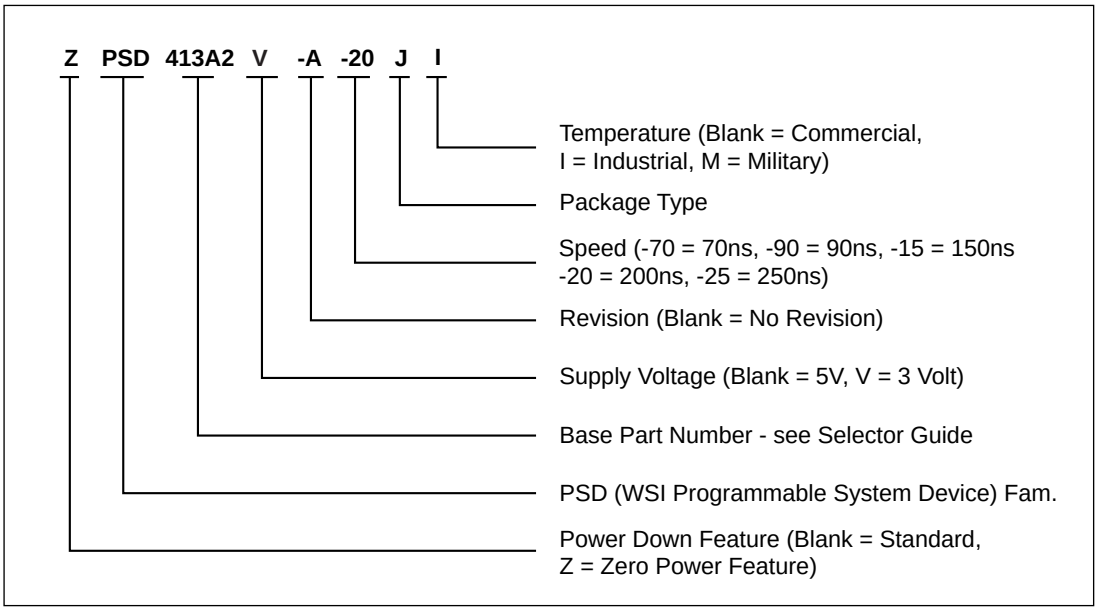
22.0 PSD211R Ordering Information

22.1 PSD211R Family – Selector Guide

Part #			MCU			PLDs/Decoders				I/O		Memory		Other	
PSD @ 5 V	ZPSD @ 5 V	ZPSD @ 2.7 V	8-Bit Data	16-Bit Data	Interface	Inputs	Product Terms	PLD Outputs	Page Reg.	Ports	Open Drain	EPROM	SRAM	Peripheral Mode	Security
PSD211R	ZPSD211R	ZPSD211RV	X		STD-M	14	40	11		19		256Kb			X

22.0 PSD211R Ordering Information (cont.)

22.2 Part Number Construction



22.3 Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
PSD211R-B-70J	70	44 Pin PLDCC	Comm'l
PSD211R-B-70L	70	44 Pin CLDCC	Comm'l
PSD211R-B-70M	70	44 Pin PQFP	Comm'l
PSD211R-B-90J	90	44 Pin PLDCC	Comm'l
PSD211R-B-90JI	90	44 Pin PLDCC	Industrial
PSD211R-B-15J	150	44 Pin PLDCC	Comm'l
PSD211R-B-15L	150	44 Pin CLDCC	Comm'l
PSD211R-B-15M	150	44 Pin PQFP	Comm'l
ZPSD211R-B-70J	70	44 Pin PLDCC	Comm'l
ZPSD211R-B-70L	70	44 Pin CLDCC	Comm'l
ZPSD211R-B-70M	70	44 Pin PQFP	Comm'l
ZPSD211R-B-90JI	90	44 Pin PLDCC	Industrial
ZPSD211R-B-90MI	90	44 Pin PQFP	Industrial
ZPSD211R-B-15J	150	44 Pin PLDCC	Comm'l
ZPSD211R-B-15L	150	44 Pin CLDCC	Comm'l
ZPSD211R-B-15M	150	44 Pin PQFP	Comm'l
ZPSD211RV-B-20J	200	44 Pin PLDCC	Comm'l
ZPSD211RV-B-20JI	200	44 Pin PLDCC	Industrial
ZPSD211RV-B-20L	200	44 Pin CLDCC	Comm'l
ZPSD211RV-B-20M	200	44 Pin PQFP	Comm'l
ZPSD211RV-B-25J	250	44 Pin PLDCC	Comm'l
ZPSD211RV-B-25JI	250	44 Pin PLDCC	Industrial

REVISION HISTORY

Table 1. Document Revision History

Date	Rev.	Description of Revision
Jan-1997	1.0	PSD211R: Document written in the WSI format. Initial release
Jul-1997	1.0	ZPSD211R, ZPSD211RV: Document written in the WSI format. Initial release
Feb-1998	1.1	Combined Data Sheets. Updated Specifications
31-Jan-2002	1.2	PSD211R, ZPSD211R, ZPSD211RV: Low Cost Field Programmable Microcontroller Peripherals Front page, and back two pages, in ST format, added to the PDF file Any references to Waferscale, WSI, EasyFLASH and PSDsoft 2000 updated to ST, ST, Flash+PSD and PSDsoft Express