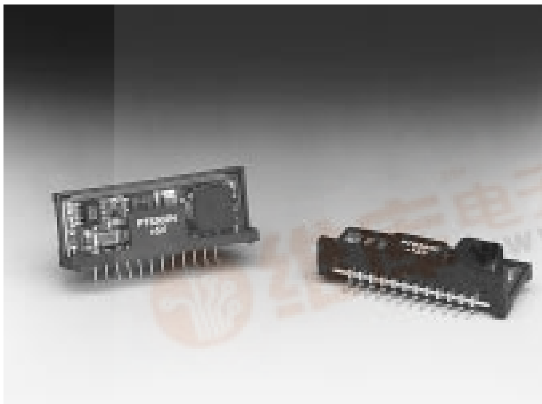
PT6300 Series

Power Trends Products from Texas Instruments

3 Amp Adjustable Positive Step-down Integrated Switching Regulators

SLTS031B
(Revised 9/30/2000)

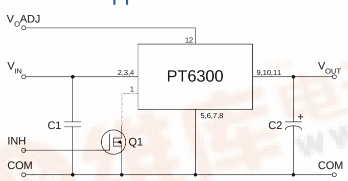


- 90% Efficiency
- Adjustable Output Voltage
- Internal Short Circuit Protection
- Over-Temperature Protection
- On/Off Control (Ground Off)
- Small SIP Footprint
- Wide Input Range

The PT6300 Series is a line of High-Performance 3 Amp, 12-Pin SIP (Single In-line Package) Integrated Switching Regulators (ISRs) designed to meet the on-board power conversion needs of battery powered or other equipment requiring high efficiency and small size. This high performance ISR family offers a unique combination of features combining 90% typical efficiency with open-collector on/off control and adjustable output voltage.

Quiescent current in the shutdown mode is typically less than 100μA.

Standard Application



C_1 = Optional 1μF ceramic
C_2 = Required 100μF electrolytic (1)
Q_1 = NFET

Pin-Out Information

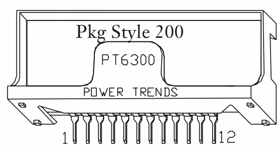
Pin	Function
1	Inhibit (30V max)
2	V_{in}
3	V_{in}
4	V_{in}
5	GND
6	GND
7	GND
8	GND
9	V_{out}
10	V_{out}
11	V_{out}
12	V_{out} Adj (5)

Ordering Information

PT6302☐ = +5 Volts
PT6303☐ = +3.3 Volts
PT6304☐ = +12 Volts
PT6314☐ = +1.5Volts

PT Series Suffix (PT1234X)

Case/Pin Configuration	
Vertical Through-Hole	N
Horizontal Through-Hole	A
Horizontal Surface Mount	C



Specifications

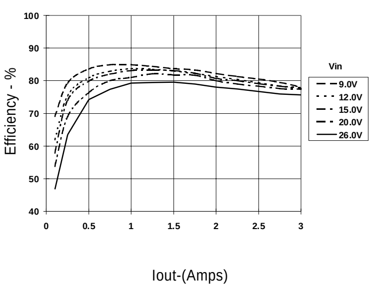
Characteristics (T_a=25°C unless noted)	Symbols	Conditions	PT6300 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range	0.1 (2)	—	3.0	A
Short Circuit Current	I_{sc}	$V_{in} = V_o + 5V$	—	5.0	—	Apk
Input Voltage Range *(Note: inhibit function cannot be used above 30V.)*	V_{in}	$0.1 \le I_o \le 3.0$ A V_o = 12V V_o = 5.0V V_o = 3.3V V_o = 1.5V	16 9 9 9.0	— — — —	30/38 (3) 30/38 (3) 26 17	V
Output Voltage Tolerance	ΔV_o	Over V_{in} Range, I_o = 3.0 A T_a = 0°C to +60°C	—	±1.0	±2.0	$\%V_o$
Line Regulation	Reg_{line}	Over V_{in} range	—	±0.25	±0.5	$\%V_o$
Load Regulation	Reg_{load}	$0.1 \le I_o \le 3.0$ A	—	±0.25	±0.5	$\%V_o$
V_o Ripple/Noise	V_n	$V_{in} = V_{in}$ min, I_o = 3.0 A	—	±2	—	$\%V_o$
Transient Response with C_o = 100μF	t_{tr} V_{os}	50% load change V_o over/undershoot	— —	100 5.0	200 —	μSec $\%V_o$
Efficiency	η	V_{in}=16V, I_o = 0.5 A, V_o = 12V V_{in}=9V, I_o = 0.5 A, V_o = 5.0V V_{in}=9V, I_o = 0.5 A, V_o = 3.3V V_{in}=9V, I_o =0.5A, V_o = 1.5V	— — — —	91 89 84 72	— — — —	%
Switching Frequency	f_o	Over V_{in} and I_o ranges, V_o = 12V V_o = 3.3V/5V V_o = 1.5V	600 400 350	750 500 450	900 600 550	kHz
Shutdown Current	I_{sc}	V_{in} = 15V	—	100	—	μA
Quiescent Current	I_{nl}	I_o = 0A, V_{in} =10V	—	10	—	mA
Absolute Maximum Operating Temperature Range	T_a	Over V_{in} range	-40	—	+85 (4)	°C
Thermal Resistance	θ_{ja}	Free Air Convection (40-60LFM)	—	30	—	°C/W
Storage Temperature	T_s	—	-40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3, 1 msec, Half Sine, mounted to a fixture	—	500	—	G's
Mechanical Vibration		Per Mil-STD-883D, Method 2007.2, 20-2000 Hz,Soldered in a PC board	—	10	—	G's
Weight	—	—	—	6.5	—	grams

Notes:
(1) The PT6300 Series requires a 100μF electrolytic or tantalum output capacitor for proper operation in all applications.
(2) The ISR will operate to no load with reduced specifications.
(3) Input voltage cannot exceed 30V when the inhibit function is used.
(4) See Thermal Derating charts.
(5) Consult the related application note for guidance on adjusting the output voltage.

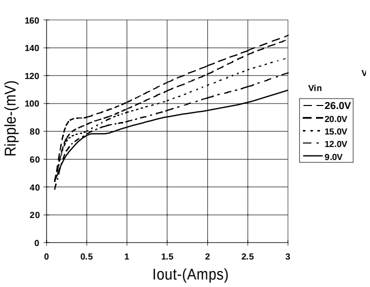
Typical Characteristics

PT6303, 3.3 VDC (See Note A)

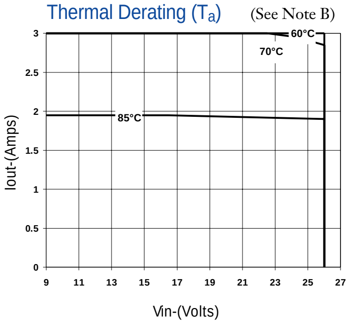
Efficiency vs Output Current



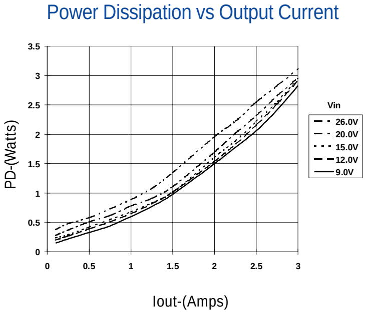
Ripple vs Output Current



Thermal Derating (T_a) (See Note B)

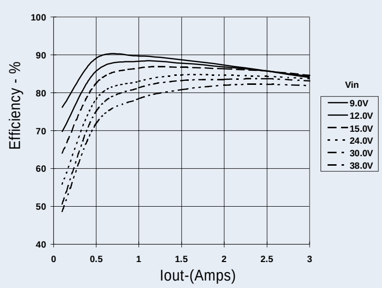


Power Dissipation vs Output Current

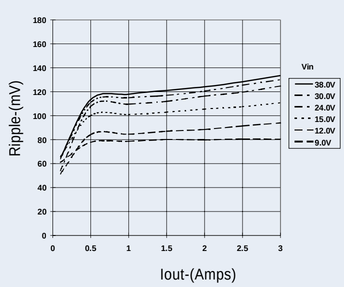


PT6302, 5.0 VDC (See Note A)

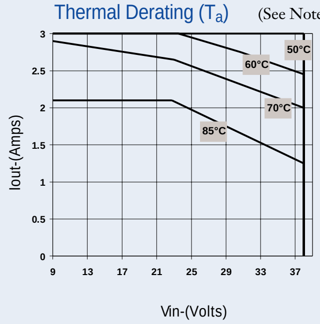
Efficiency vs Output Current



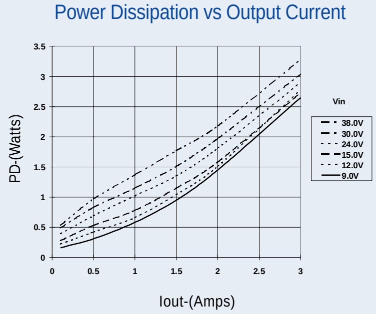
Ripple vs Output Current



Thermal Derating (T_a) (See Note B)

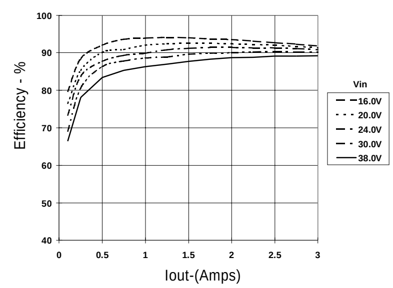


Power Dissipation vs Output Current

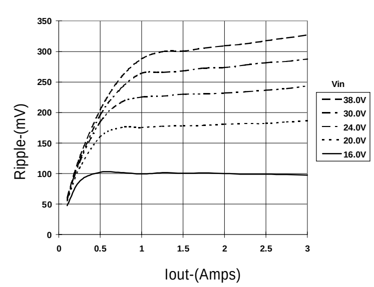


PT6304, 12.0 VDC (See Note A)

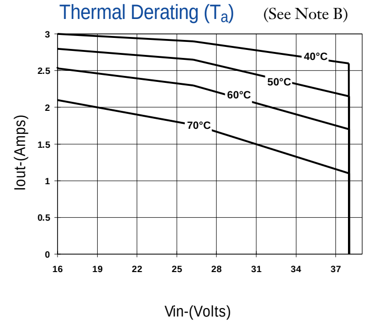
Efficiency vs Output Current



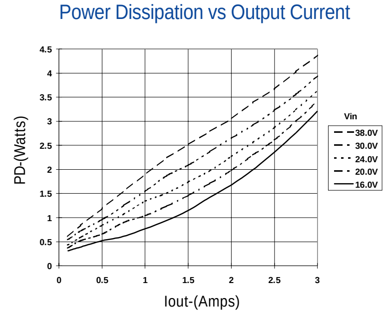
Ripple vs Output Current



Thermal Derating (T_a) (See Note B)



Power Dissipation vs Output Current



Note A: *Characteristic data listed in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR*

Note B: *Thermal derating graphs are developed in free air convection cooling of 40-60 LFM. (See Thermal Application note.)*

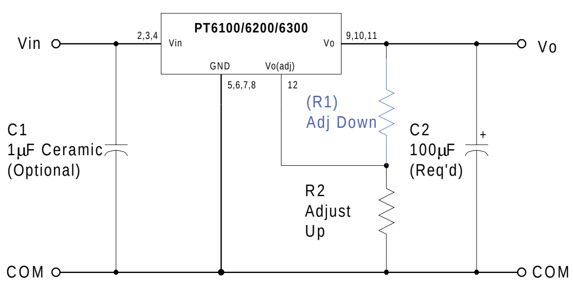
Adjusting the Output Voltage of Power Trends' Wide Input Range Bus ISRs

The output voltage of the Power Trends' Wide Input Range Series ISRs may be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor. Table 1 accordingly gives the allowable adjustment range for each model for either series as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R2, between pin 12 (V_o adjust) and pins 5-8 (GND).

Adjust Down: Add a resistor (R1), between pin 12 (V_o adjust) and pins 9-11(V_{out}).

Figure 1



The values of (R1) [adjust down], and R2 [adjust up], can also be calculated using the following formulas. Refer to Figure 1 and Table 2 for both the placement and value of the required resistor; either (R1) or R2 as appropriate.

$$(R1) = \frac{R_o\,(V_a - 1.25)}{V_o - V_a} \quad k\Omega$$

$$R2 = \frac{1.25\,R_o}{V_a - V_o} \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
R_o = The resistance value fromTable 1

Table 1

ISR ADJUSTMENT RANGE AND FORMULA PARAMETERS

1Adc Rated		PT6102	PT6101		PT6103
2Adc Rated	PT6216	PT6213		PT6212	PT6214
3Adc Rated	PT6314	PT6303		PT6302	PT6304
V_o (nom)	1.5	3.3	5.0	5.0	12.0
V_a (min)	1.3	1.8	1.88	2.18	2.43
V_a (max)	1.9	6.07	11.25	8.5	22.12
R_o (kΩ)	8.25	66.5	150.0	90.9	243.0

Notes:

1. Use only a single 1% resistor in either the (R1) or R2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from V_o adjust to either GND or V_{out}. Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
3. Adjustments to the output voltage may place additional limits on the maximum and minimum input voltage for the part. The revised maximum and minimum input voltage limits must comply with the following requirements. The limits are model dependant.

PT6216/PT6314:

V_{in} (max) = (10 x V_a)V or 17V, whichever is less.

V_{in} (min) = 9.0V

All other models:

V_{in} (max) = (8 x V_a)V or as specified.

V_{in} (min) = (V_a + 4)V or 9V, whichever is greater.

Table 2

ISR ADJUSTMENT RESISTOR VALUES

1Adc Rated		PT6102	PT6101		PT6103
2Adc Rated	PT6216	PT6213		PT6212	PT6214
3Adc Rated	PT6314	PT6303		PT6302	PT6304
V_o (nom)	1.5	3.3	5.0	5.0	12.0
V_a (req.d)					
1.3	(2.1kΩ)				
1.4	(12.4kΩ)				
1.5					
1.6	103.0kΩ				
1.7	51.6kΩ				
1.8	34.4kΩ	(24.4)kΩ			
1.9	25.8kΩ	(30.9)kΩ	(31.5)kΩ		
2.0		(38.4)kΩ	(37.5)kΩ		
2.1		(47.1)kΩ	(44.0)kΩ		
2.2		(57.4)kΩ	(50.9)kΩ	(30.8)kΩ	
2.3		(69.8)kΩ	(58.3)kΩ	(35.4)kΩ	
2.4		(85.0)kΩ	(66.3)kΩ	(40.2)kΩ	
2.5		(104.0)kΩ	(75.0)kΩ	(45.5)kΩ	(32.0)kΩ
2.6		(128.0)kΩ	(84.4)kΩ	(51.1)kΩ	(34.9)kΩ
2.7		(161.0)kΩ	(94.6)kΩ	(57.3)kΩ	(37.9)kΩ
2.8		(206.0)kΩ	(106.0)kΩ	(64.0)kΩ	(40.9)kΩ
2.9		(274.0kΩ	(118.0)kΩ	(71.4)kΩ	(44.1)kΩ
3.0		(388.0)kΩ	(131.0)kΩ	(79.5)kΩ	(47.3)kΩ
3.1		(615.0)kΩ	(146.0)kΩ	(88.5)kΩ	(50.5)kΩ
3.2		(1300.0)kΩ	(163.0)kΩ	(98.5)kΩ	(53.8)kΩ
3.3		(181.0)kΩ	(110.0)kΩ	(57.3)kΩ	
3.4		831.0kΩ	(202.0)kΩ	(122.0)kΩ	(60.8)kΩ
3.5		416.0kΩ	(225.0)kΩ	(136.0)kΩ	(64.3)kΩ
3.6		227.0kΩ	(252.0)kΩ	(153.0)kΩ	(68.0)kΩ
3.7		208.0kΩ	(283.0)kΩ	(171.0)kΩ	(71.7)kΩ
3.8		166.0kΩ	(319.0)kΩ	(193.0)kΩ	(75.6)kΩ
3.9		139.0kΩ	(361.0)kΩ	(219.0)kΩ	(79.5)kΩ
4.0		119.0kΩ	(413.0)kΩ	(250.0)kΩ	(83.5)kΩ
4.1		104.0kΩ	(475.0)kΩ	(288.0)kΩ	(87.7)kΩ
4.2		92.4kΩ	(533.0)kΩ	(335.0)kΩ	(91.9)kΩ
4.3		83.1kΩ	(654.0)kΩ	(396.0)kΩ	(96.3)kΩ
4.4		75.6kΩ	(788.0)kΩ	(477.0)kΩ	(101.0)kΩ
4.5		69.3kΩ	(975.0)kΩ	(591.0)kΩ	(105.0)kΩ
4.6		63.9kΩ	(1260.0)kΩ	(761.0)kΩ	(110.0)kΩ
4.7		59.4kΩ	(1730.0)kΩ	(1050.0)kΩ	(115.0)kΩ
4.8		55.4kΩ		(1610.0)kΩ	(120.0)kΩ
4.9		52.0kΩ			(125.0)kΩ
5.0		48.9kΩ			(130.0)kΩ
5.1		46.2kΩ	1880.0kΩ	1140.0kΩ	(136.0)kΩ
5.2		43.8kΩ	937.0kΩ	568.0kΩ	(141.0)kΩ
5.3		41.6kΩ	625.0kΩ	379.0kΩ	(147.0)kΩ
5.4		39.6kΩ	469.0kΩ	284.0kΩ	(153.0)kΩ
5.5		37.8kΩ	375.0kΩ	227.0kΩ	(159.0)kΩ
5.6		36.1kΩ	313.0kΩ	189.0kΩ	(165.0)kΩ
5.7		34.6kΩ	268.0kΩ	162.0kΩ	(172.0)kΩ
5.8		33.3kΩ	234.0kΩ	142.0kΩ	(178.0)kΩ
5.9		32.0kΩ	208.0kΩ	126.0kΩ	(185.0)kΩ
6.0		30.8kΩ	188.0kΩ	114.0kΩ	(192.0)kΩ

ISR ADJUSTMENT RESISTOR VALUES (Cont)

1Adc Rated	PT6101		PT6103
2Adc Rated		PT6212	PT6214
3Adc Rated		PT6302	PT6304
V_o (nom)	5.0	5.0	12.0
V_a (req.d)			
6.2	156.0kΩ	94.7kΩ	(207.0)kΩ
6.4	134.0kΩ	81.2kΩ	(223.0)kΩ
6.6	117.0kΩ	71.0kΩ	(241.0)kΩ
6.8	104.0kΩ	63.1kΩ	(259.0)kΩ
7.0	93.8kΩ	56.8kΩ	(279.0)kΩ
7.2	85.2kΩ	51.6kΩ	(301.0)kΩ
7.4	78.1kΩ	47.3kΩ	(325.0)kΩ
7.6	72.1kΩ	43.7kΩ	(351.0)kΩ
7.8	67.0kΩ	40.6kΩ	(379.0)kΩ
8.0	62.5kΩ	37.9kΩ	(410.0)kΩ
8.2	58.6kΩ	35.5kΩ	(444.0)kΩ
8.4	55.1kΩ	33.4kΩ	(483.0)kΩ
8.6	52.1kΩ		(525.0)kΩ
8.8	49.3kΩ		(573.0)kΩ
9.0	46.9kΩ		(628.0)kΩ
9.5	41.7kΩ		(802.0)kΩ
10.0	37.5kΩ		(1060.0)kΩ
10.5	34.1kΩ		(1500.0)kΩ
11.0	31.3kΩ		
11.5			
12.0			
12.5			608.0kΩ
13.0			304.0kΩ
13.5			203.0kΩ
14.0			152.0kΩ
14.5			122.0kΩ
15.0			101.0kΩ
15.5			86.8kΩ
16.0			75.9kΩ
16.5			67.5kΩ
17.0			60.8kΩ
17.5			55.2kΩ
18.0			50.6kΩ
18.5			46.7kΩ
19.0			43.4kΩ
19.5			40.5kΩ
20.0			38.0kΩ
20.5			35.7kΩ
21.5			33.8kΩ
21.5			32.0kΩ
22.0			30.4kΩ

R1 = (Blue) R2 = Black

Using the Inhibit Function on Power Trends' Wide Input Range Bus ISRs

For applications requiring output voltage On/Off control, the 12pin ISR products incorporate an inhibit function. The function has uses in areas such as battery conservation, power-up sequencing, or any other application where the regulated output from the module is required to be switched off. The On/Off function is provided by the Pin 1 (*Inhibit*) control.

The ISR functions normally with Pin 1 open-circuit, providing a regulated output whenever a valid source voltage is applied to V_{in}, (pins 2, 3, & 4). When a low-level[2] ground signal is applied to Pin 1, the regulator output will be disabled.

Figure 1 shows an application schematic, which details the typical use of the Inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pull-up with a maximum open-circuit voltage of 8.3VDC. Only devices with a true open-collector or open-drain output can be used to control this pin. A discrete bipolar transistor or MOSFET is recommended.

Equation 1 may be used to determine the approximate current drawn by Q1 when the inhibit is active.

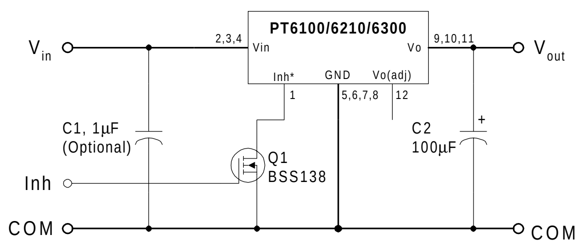
Equation 1

$$I_{stby} = V_{in} \div 155k\Omega \quad \pm 20\%$$

Notes:

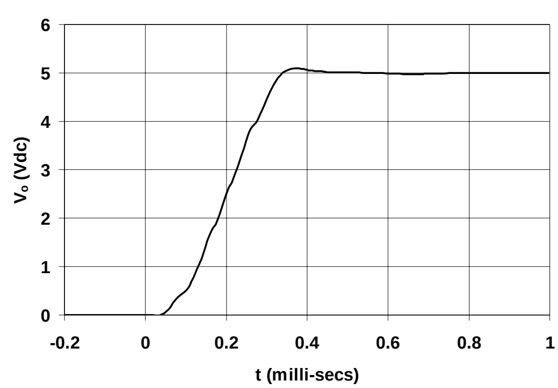
1. The Inhibit control logic is similar for all Power Trends' modules, but the flexibility and threshold tolerances will be different. For specific information on the inhibit function of other ISR models, consult the applicable application note.
2. Use only a true open-collector device (preferably a discrete transistor) for the Inhibit input. Do Not use a pull-up resistor, or drive the input directly from the output of a TTL or other logic gate. To disable the output voltage, the control pin should be pulled low to less than +1.5VDC.
3. When the Inhibit control pin is active, i.e. pulled low, the maximum allowed input voltage is limited to +30Vdc.
4. Do not control the Inhibit input with an external DC voltage. This will lead to erratic operation of the ISR and may over-stress the regulator.
5. Avoid capacitance greater than 500pF at the Inhibit control pin. Excessive capacitance at this pin will cause the ISR to produce a pulse on the output voltage bus at turn-on.
6. Keep the On/Off transition to less than 10µs. This prevents erratic operation of the ISR, which can cause a momentary high output voltage.

Figure 1



Turn-On Time: The output of the ISR is enabled automatically when external power is applied to the input. The *Inhibit* control pin is pulled high by its internal pull-up resistor. The ISR produces a fully regulated output voltage within 1-msec of either the release of the Inhibit control pin, or the application of power. The actual turn-on time will vary with the input voltage, output load, and the total amount of capacitance connected to the output Using the circuit of Figure 1, Figure 2 shows the typical rise in output voltage for the PT6101 following the turn-off of Q1 at time t =0. The waveform was measured with a 9Vdc input voltage, and 5-Ohm resistive load.

Figure 2



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