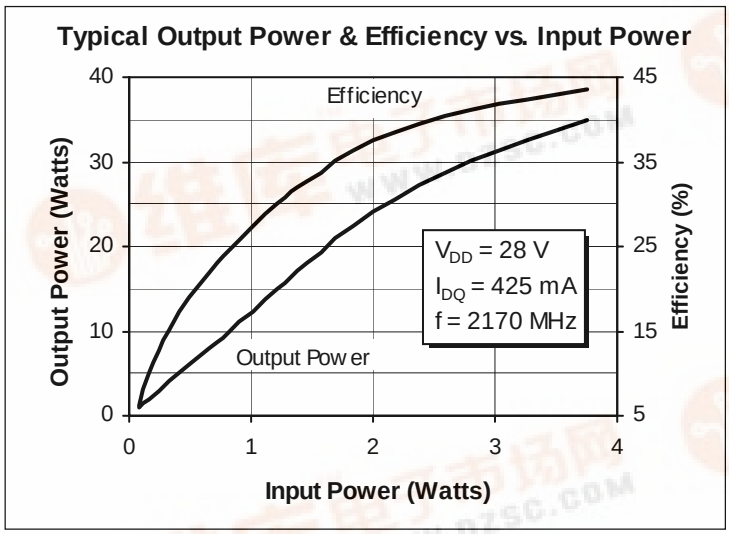
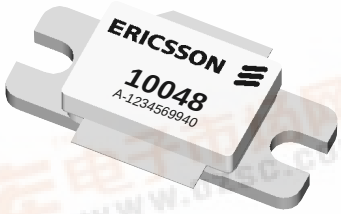
PTF 10048
30 Watts, 2.1–2.2 GHz, W-CDMA
GOLDMOS® Field Effect Transistor

Description

The PTF 10048 is an internally matched 30–watt *GOLDMOS* FET intended for WCDMA applications from 2.1 to 2.2 GHz. It operates at 40% efficiency with 10.5 dB typical gain. Nitride surface passivation and full gold metallization ensure excellent device lifetime and reliability.

- ***INTERNALLY MATCHED***
- **Guaranteed Performance at 2.17 GHz, 28 V**
  - **Output Power = 30 Watts Min**
  - **Gain = 10.5 dB Typ at 30 Watts**
- **Full Gold Metallization**
- **Silicon Nitride Passivated**
- **Excellent Thermal Stability**
- **100% Lot Traceability**





Package 20237

RF Specifications (100% Tested)

Characteristic	Symbol	Min	Typ	Max	Units
Gain (V_{DD} = 28 V, P_{OUT} = 10 W, I_{DQ} = 425 mA, f = 2.11 & 2.17 GHz)	G_{ps}	10	11	—	dB
Power Output at 1 dB Compression (V_{DD} = 28 V, I_{DQ} = 425 mA, f = 2.17 GHz)	P-1dB	30	36	—	Watts
Drain Efficiency (V_{DD} = 28 V, P_{OUT} = 30 W, I_{DQ} = 425 mA, f = 2.17 GHz)	η	30	40	—	%
Load Mismatch Tolerance (V_{DD} = 28 V, P_{OUT} = 30 W, I_{DQ} = 425 mA, f = 2.17 GHz —all phase angles at frequency of test)	Ψ	—	—	10:1	—

All published data at T_{CASE} = 25°C unless otherwise indicated.

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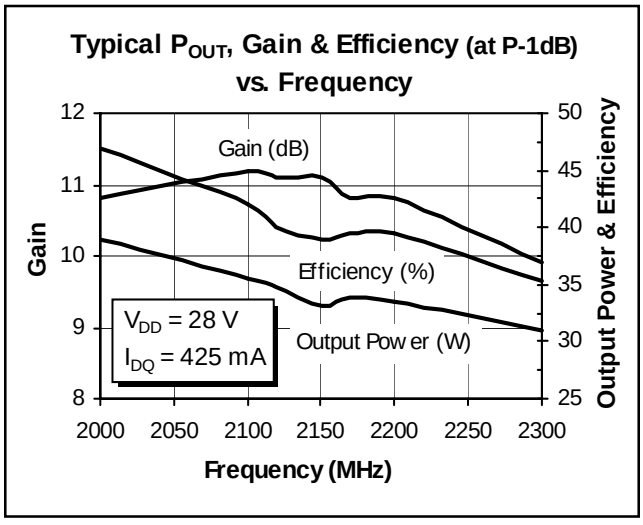
Electrical Characteristics (100% Tested)

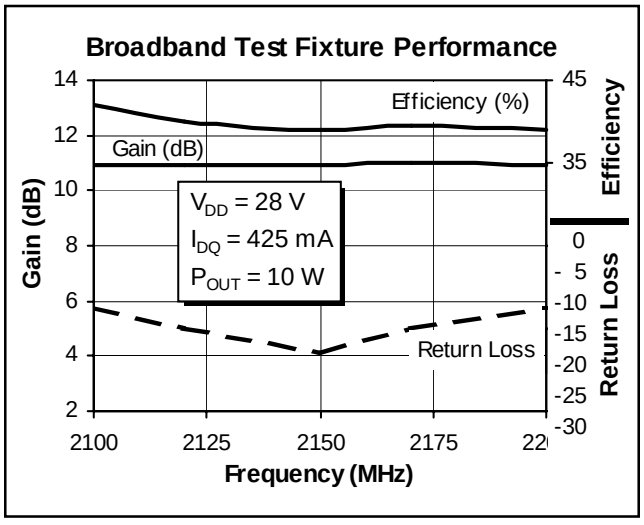
Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 50 mA	$V_{(BR)DSS}$	65	65	—	Volts
Zero Gate Voltage Drain Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	mA
Gate Threshold Voltage	V_{DS} = 10 V, I_D = 75 mA	$V_{GS(th)}$	3.0	—	5.0	Volts
Forward Transconductance	V_{DS} = 10 V, I_D = 6 A	g_{fs}	—	1.8	—	Siemens

Maximum Ratings

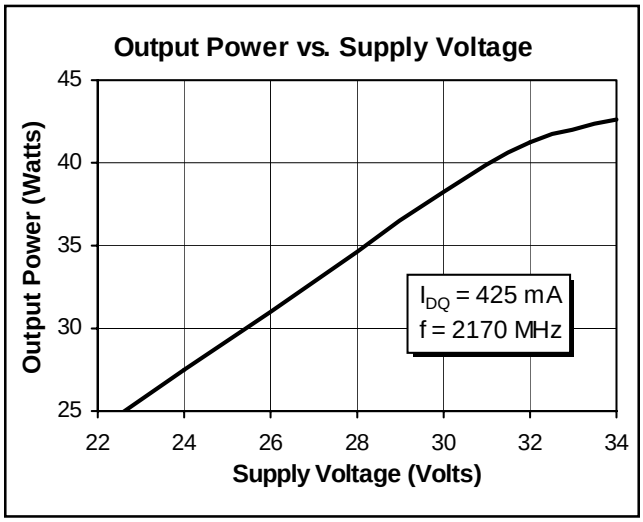
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation Above 25°C derate by	P_D	120 0.66	Watts W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C)	$R_{\theta JC}$	1.5	°C/W

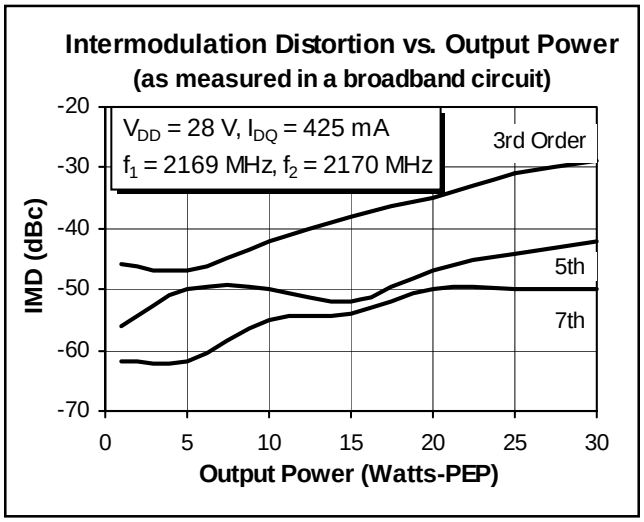
Typical Performance

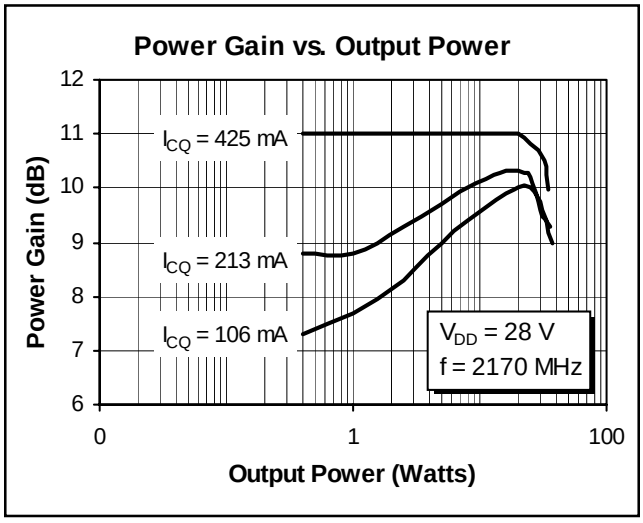


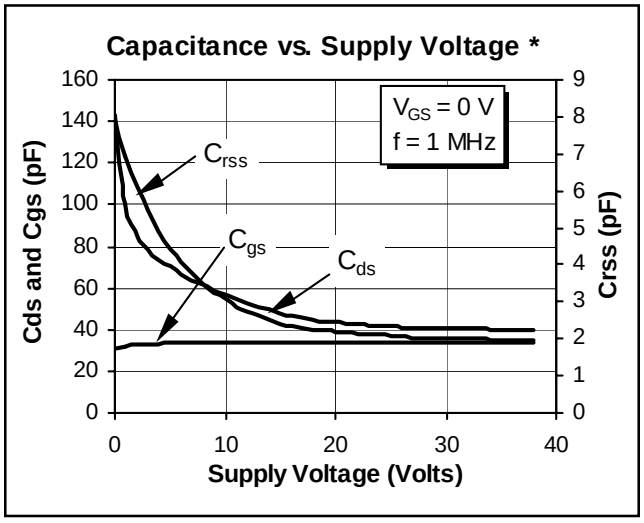


Typical Performance

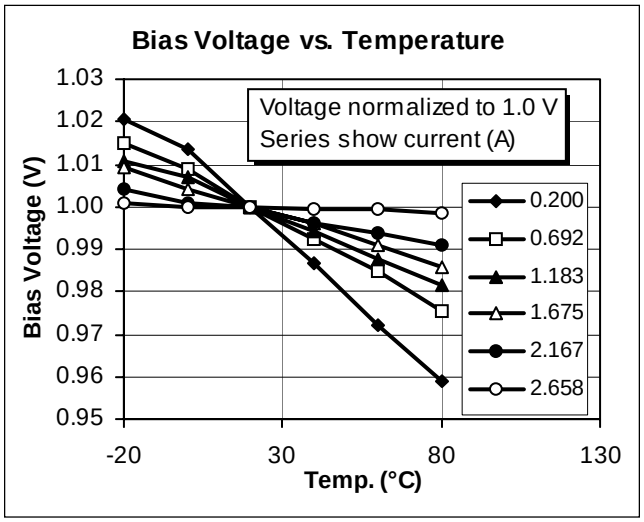








*This part is internally matched. Measurements of the finished product will not yield these figures.



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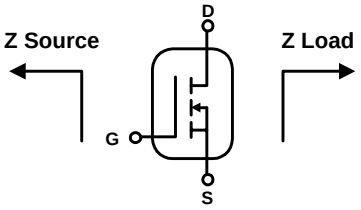
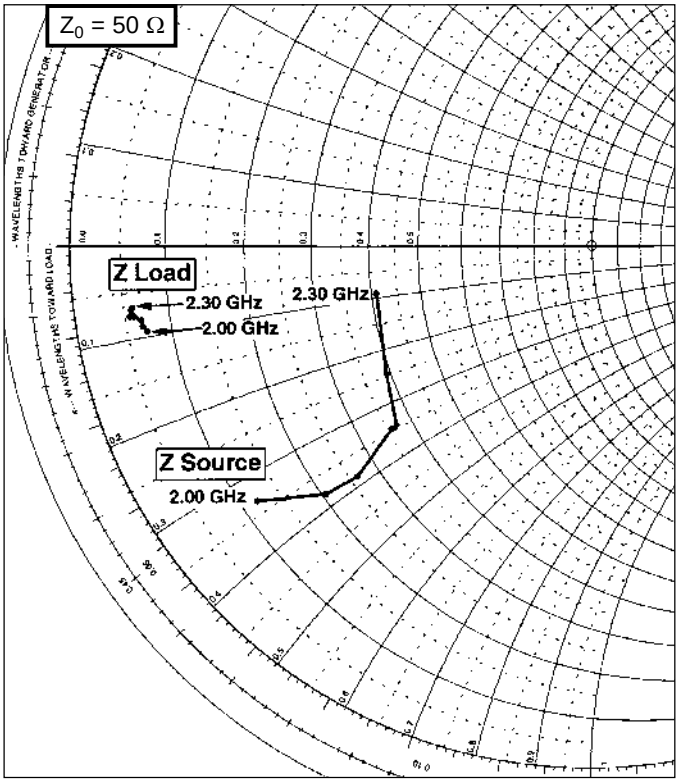
Impedance Data

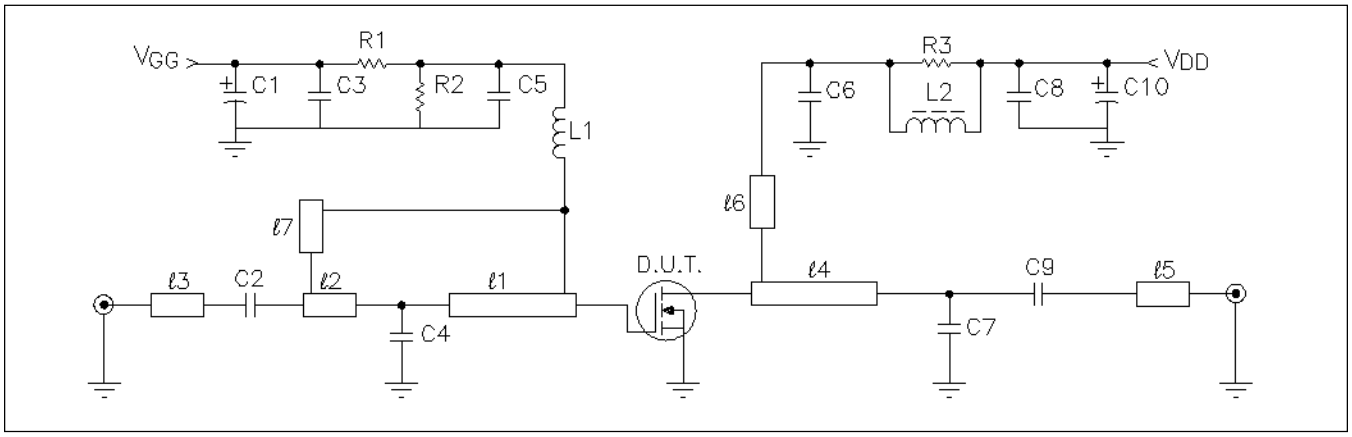
(V_{DD} = 28 V, P_{out} = 30 W, I_{DQ} = 425 mA)



Frequency	Z Source Ω		Z Load Ω	
GHz	R	jX	R	jX
2.00	6.0	-16.7	3.6	-4.7
2.10	10.3	-19.0	3.4	-4.4
2.12	13.2	-19.3	3.4	-4.1
2.15	17.9	-17.3	3.0	-3.8
2.17	18.5	-17.2	2.8	-3.8
2.20	19.6	-12.3	2.9	-3.5
2.30	20.5	-4.6	3.0	-3.3



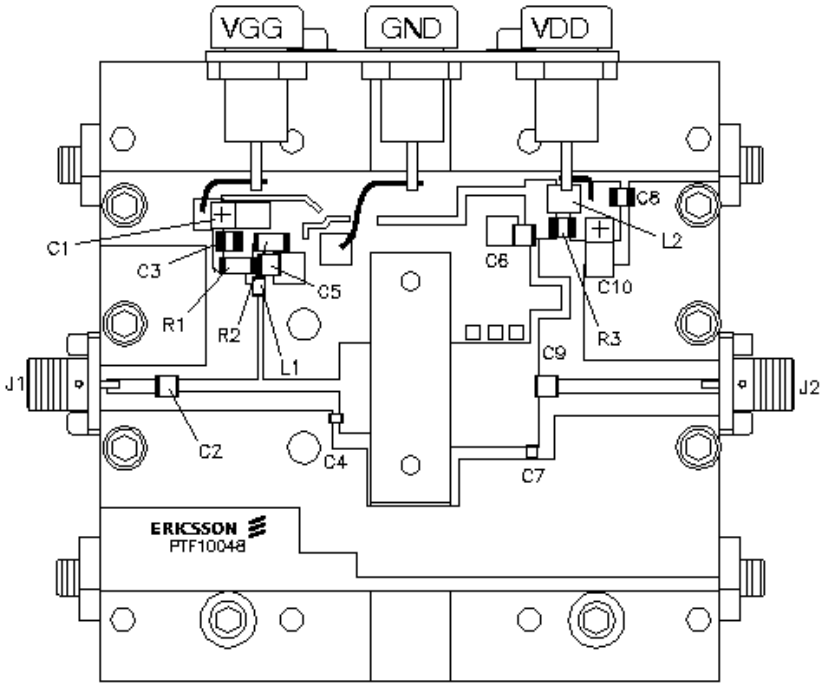
Test Circuit



Test Circuit Schematic for f = 2.15 GHz

DUT	PTF 10048	LDMOS Power Transistor
ℓ1	0.052 λ 2.15 GHz Microstrip 11.14 Ω	
ℓ2, l5	0.255 λ 2.15 GHz Microstrip 50 W	
ℓ3	0.075 λ 2.15 GHz Microstrip 50 W	
ℓ4	0.143 λ 2.15 GHz Microstrip 10.2 Ω	
ℓ6	0.250 λ 2.15 GHz Microstrip 75 Ω	
ℓ7	0.125 λ 2.15 GHz Microstrip 80 Ω	
C1, C10	10 µF	Tantulum Capacitor
C2, C5, C6, C9	10 pF	Chip Capacitor, ATC 100 B
C3, C8	0.1 µF, 50 V	Digi-Key P4525-ND
C4	0.2 pF, 50 V	Chip Capacitor, ATC 100 A
C7	0.9 pF	Chip Capacitor, ATC 100 A

J1, J2	SMA Female Connectors, Panel Mount
L1	4.7 nH
L2	6 mm SMT Ferrite Bead
R1, R2	220 Ω Chip Resistor, P220ECI
R3	1.0 Ω Chip Resistor, P1.0ECT
Circuit Board	0.031" thick, ε_r = 4.0, G200, AlliedSignal, 2 oz. copper



Parts Layout (not to scale)

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Case Outline Specifications

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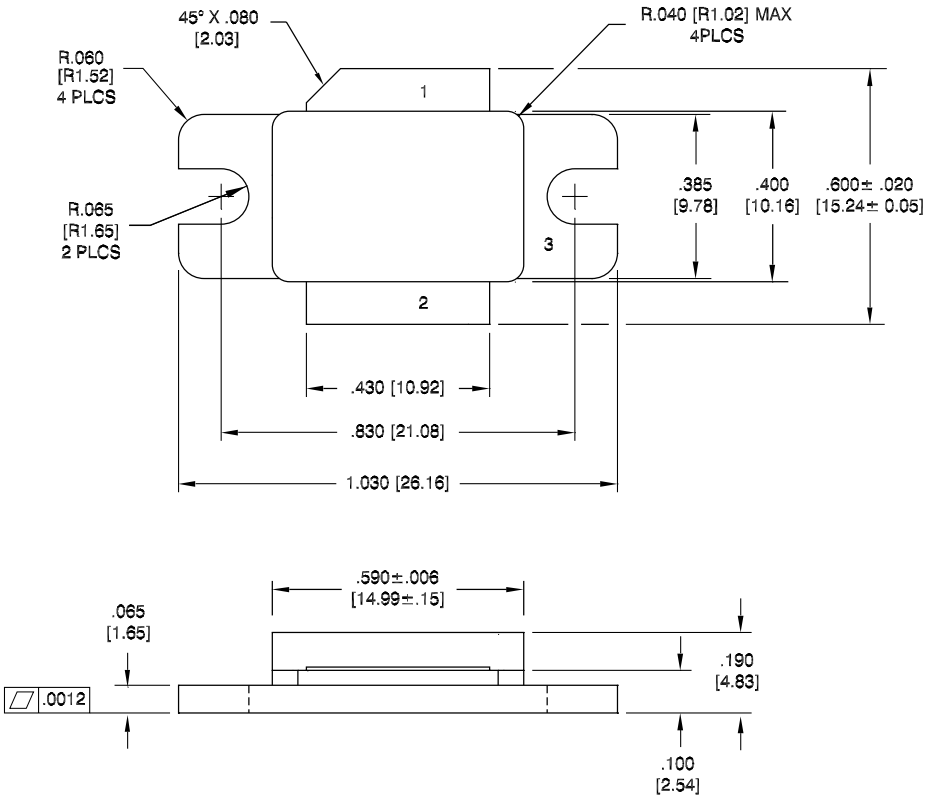

Unless otherwise specified
all tolerances ±0.005" [0.13mm]

Pins: 1.Drain 2.Gate 3.Source
Lead Thickness: 0.005 +0.002/-0.001"
[0.13 +0.05/-0.03mm]

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