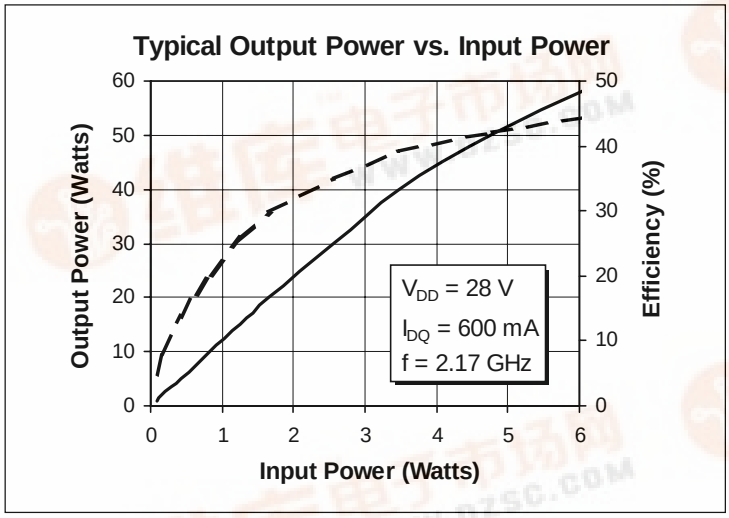
PTF 10122
50 Watts WCDMA, 2.1–2.2 GHz
GOLDMOS™ Field Effect Transistor

Description

The PTF 10122 is an internally matched common source N-channel enhancement-mode lateral MOSFET intended for WCDMA applications from 2.1 to 2.2 GHz. It is rated at 50 watts power output, with 11 dB of gain. Nitride surface passivation and full gold metallization ensure excellent device lifetime and reliability.

- ***INTERNALLY MATCHED***
- **Guaranteed Performance at 2.17 GHz, 28 V**
  - **Output Power = 50 Watts Min**
  - **Gain = 11.0 dB Typ**
  - **Efficiency = 35% Typ**
- **Full Gold Metallization**
- **Silicon Nitride Passivated**
- **Back Side Common Source**
- **Excellent Thermal Stability**
- **100% Lot Traceability**



Package 20248

RF Specifications (100% Tested)

Characteristic	Symbol	Min	Typ	Max	Units
Gain (V_{DD} = 28 V, P_{OUT} = 15 W, I_{DQ} = 600 mA, f = 2.11 GHz)	G_{ps}	10.0	11.0	—	dB
Power Output at 1 dB Compression (V_{DD} = 28 V, I_{DQ} = 600 mA, f = 2.17 GHz)	P-1dB	50	—	—	Watts
Drain Efficiency (V_{DD} = 28 V, P_{OUT} = 50 W, I_{DQ} = 600 mA, f = 2.17 GHz)	η_D	30	35	—	%
Load Mismatch Tolerance (V_{DD} = 28 V, P_{OUT} = 50 W, I_{DQ} = 600 mA, f = 2.17 GHz —all phase angles at frequency of test)	Ψ	—	—	10:1	—

All published data at T_{CASE} = 25°C unless otherwise indicated.

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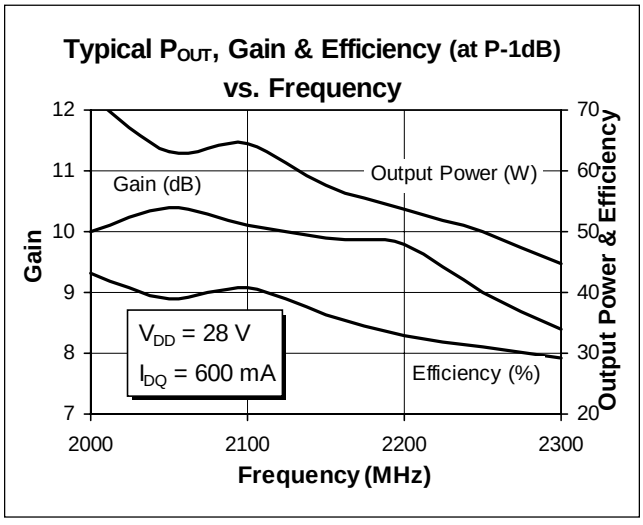
Electrical Characteristics (100% Tested)

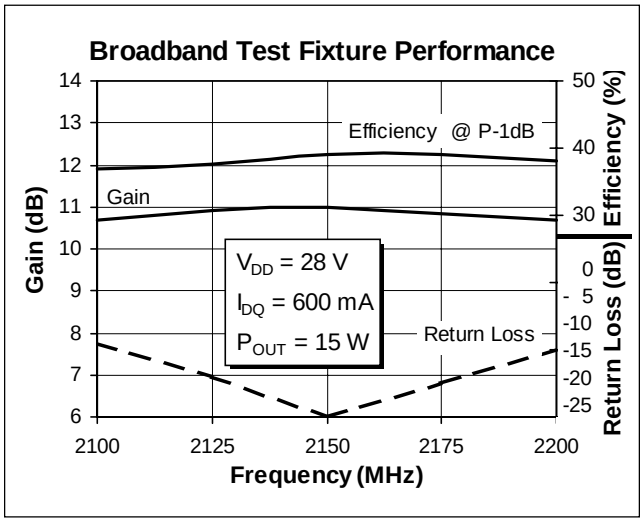
Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 100 mA	$V_{(BR)DSS}$	65	—	—	Volts
Zero Gate Voltage Drain Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	2.0	mA
Gate Threshold Voltage	V_{DS} = 10 V, I_D = 150 mA	$V_{GS(th)}$	3.0	—	5.0	Volts
Forward Transconductance	V_{DS} = 10 V, I_D = 2 A	g_{fs}	—	4.0	—	Siemens

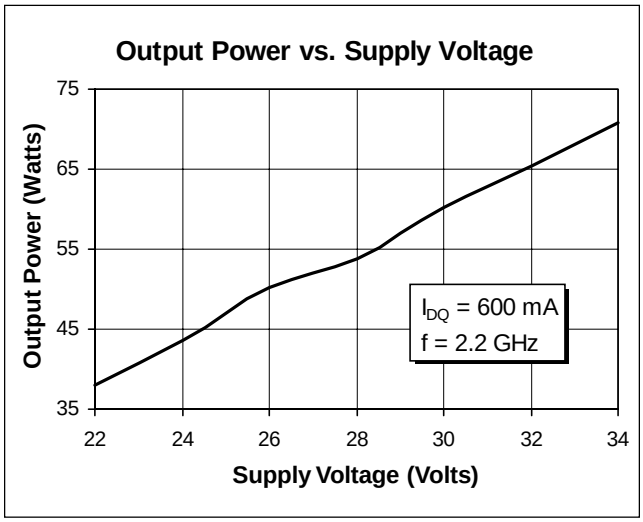
Maximum Ratings

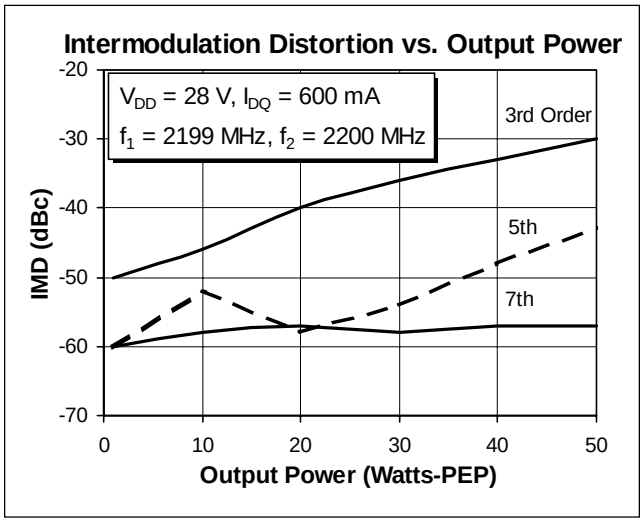
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation Above 25°C derate by	P_D	237 1.35	Watts W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C)	$R_{\theta JC}$	0.74	°C/W

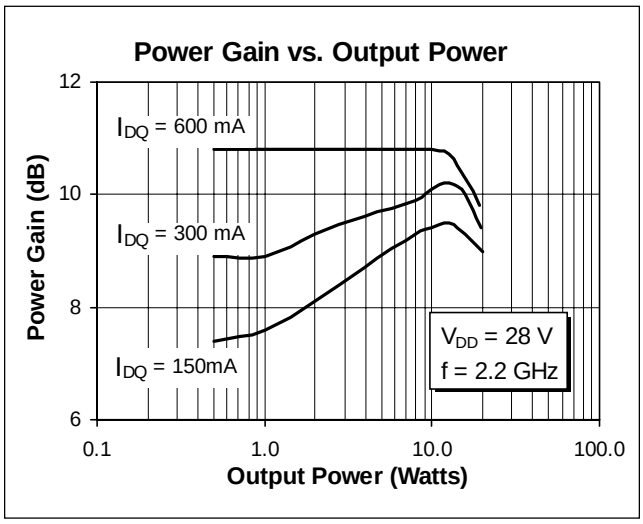
Typical Performance

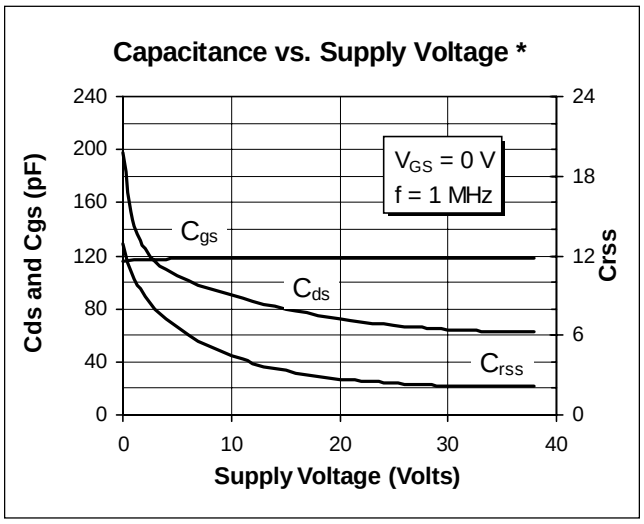




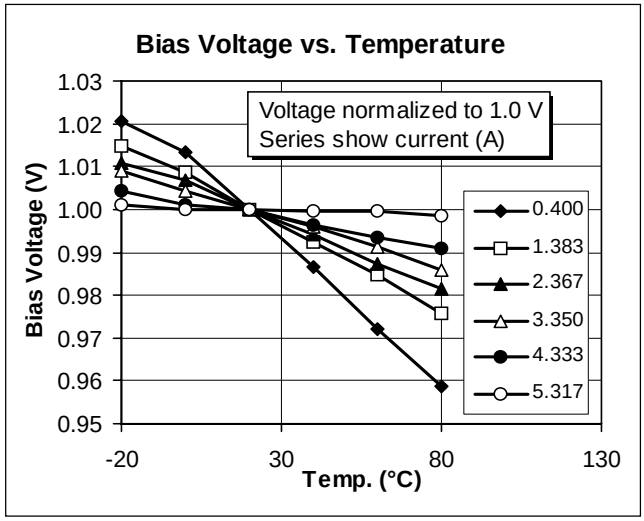






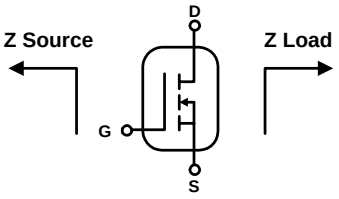


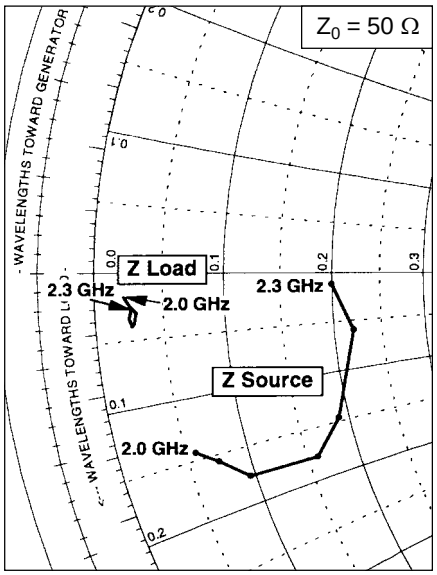
* This part is internally matched. Measurements of the finished product will not yield these results.



Impedance Data

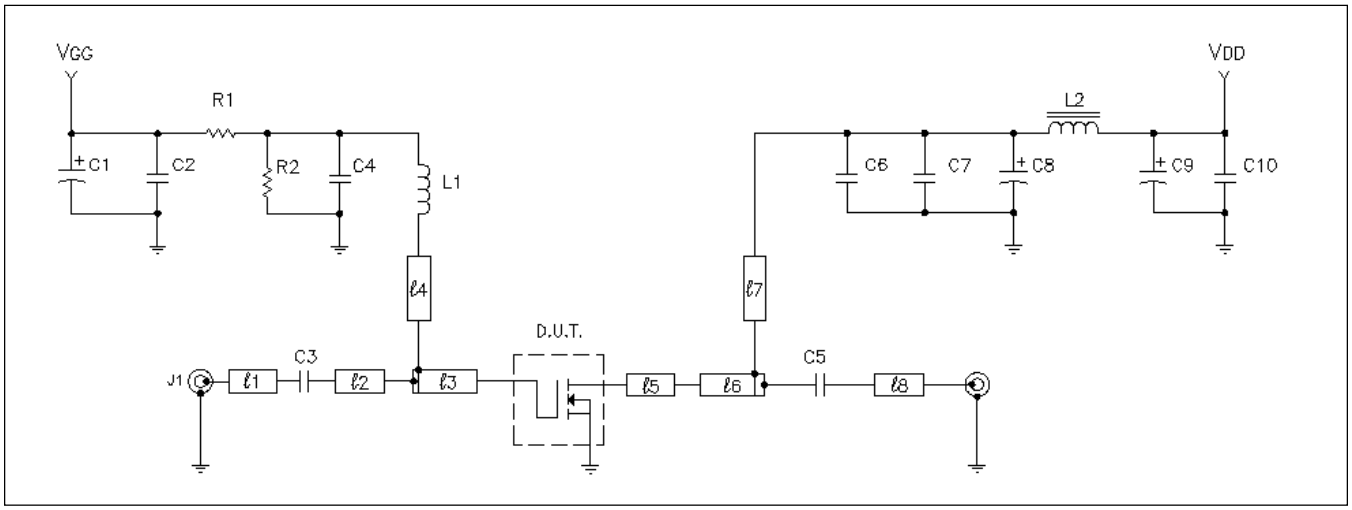
V_{DD} = 28 V, P_{OUT} = 50 W, I_{DQ} = 600 mA





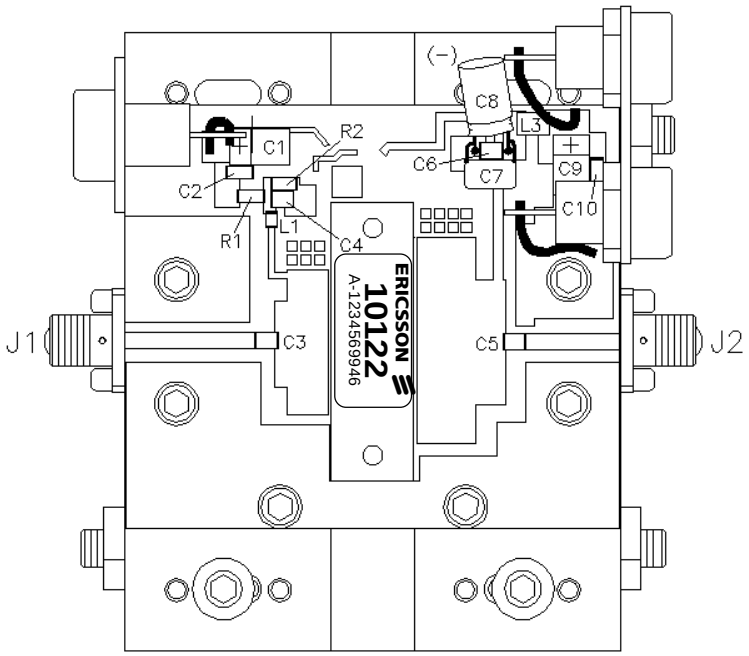
Frequency	Z Source Ω		Z Load Ω	
GHz	R	jX	R	jX
2.00	2.88	-7.20	1.05	-0.90
2.05	3.70	-7.80	1.30	-1.30
2.10	4.80	-8.80	1.50	-1.50
2.15	8.00	-8.90	1.40	-1.90
2.20	9.50	-7.30	1.30	-2.00
2.25	11.00	-3.00	1.22	-1.70
2.30	10.00	-0.60	1.30	-1.40

Test Circuit

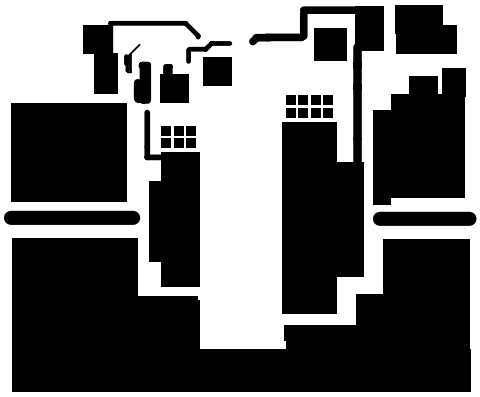


Test Circuit Block Diagram for f = 2.1–2.2 GHz

Q1	PTF 10122	LDMOS RF Transistor
ℓ1	.240 λ @ 2.15 GHz	Microstrip 50 Ω
ℓ2	.0281 λ @ 2.15 GHz	Microstrip 14.7 Ω
ℓ3	.085 λ @ 2.15 GHz	Microstrip 9.5 Ω
ℓ4	.104 λ @ 2.15 GHz	Microstrip 78 Ω
ℓ5	.120 λ @ 2.15 GHz	Microstrip 6.82 Ω
ℓ6	.063 λ @ 2.15 GHz	Microstrip 10.88 Ω
ℓ7	.216 λ @ 2.15 GHz	Microstrip 65 Ω
ℓ8	.174 λ @ 2.15 GHz	Microstrip 50 Ω
C1, C9	10 μF Chip Cap	ATC 100 B
C2, C10	0.1 μF Chip Cap	ATC 100 B
C3, C4, C5, C6	— 10 pF Chip Cap	ATC 100 B
C7	0.1 μF, 50 V	Digi-Key Capacitor 2.2 QBK
C8	100 μF, 50 V	Digi-Key Capacitor
L1	2.7 nH	Chip Inductor
L2	6mm	SMT Ferrite Bead
R1, R2	220 Ω Chip Resistor	Digi-Key 2.2 QBK
Circuit Board — Dielectric Thickness = 0.050", ε_r = 6.0 @ 1 MHz, 2 oz. Copper, TMM6, Rogers		



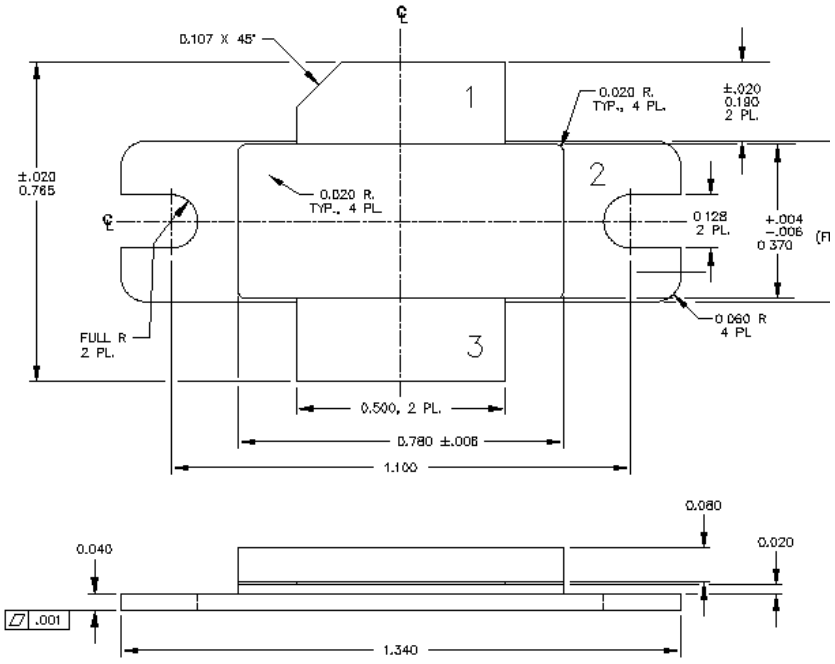
Parts Layout (not to scale)



Artwork (not to scale)

Package Mechanical Specifications

Package 20248



Unless otherwise specified
all tolerance ±0.005”

Pins: 1.Drain 2.Source 3.Gate
Lead Thickness: 0.004 +0.002/-0.001”

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