NOMINAL SIZE = 0.87 in x 0.5 in (22,1 mm x 12,57 mm)

Features

- V_{TT} Bus Termination Output (Output Tracks the System V_{REF})
- 6 A Output Current (8 A Peak)
- 3.3-V, 5-V or 12-V Input Voltage
- DDR & QDR Compatible
- On/Off Inhibit (for V_{TT} Standby)
- Under-Voltage Lockout
- Operating Temp: –40 to +85 °C
- Efficiencies up to 88 %
- 50 W/in³ Power Density
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Safety Agency Approvals (Pending): UL/cUL60950, EN60950, VDE
- Point-of-Load Alliance (POLA) Compatible

Description

The PTHxx050Y are a series of ready-to-use switching regulator modules from Texas Instruments designed specifically for bus termination in DDR and QDR memory applications. Operating from either a 3.3-V, 5-V or 12-V input, the modules generate a V_{TT} output that will source or sink up to 6 A of current (8 A transient) to accurately track their V_{REF} input. V_{TT} is the required bus termination supply voltage, and V_{REF} is the reference voltage for the memory and chipset bus receiver comparators. V_{REF} is usually set to half the V_{DDQ} power supply voltage.

Both the PTHxx050Y series employs an actively switched synchronous rectifier output to provide state-of-the-art step-down switching conversion. The products are small in size (0.87 in × 0.5 in), and are an ideal choice where space, performance, and high efficiency are desired, along with the convenience of a ready-to-use module.

Operating features include an on/off inhibit and output over-current protection (source mode only). The on/off inhibit feature allows the V_{TT} bus to be turned off to save power in a standby mode of operation.

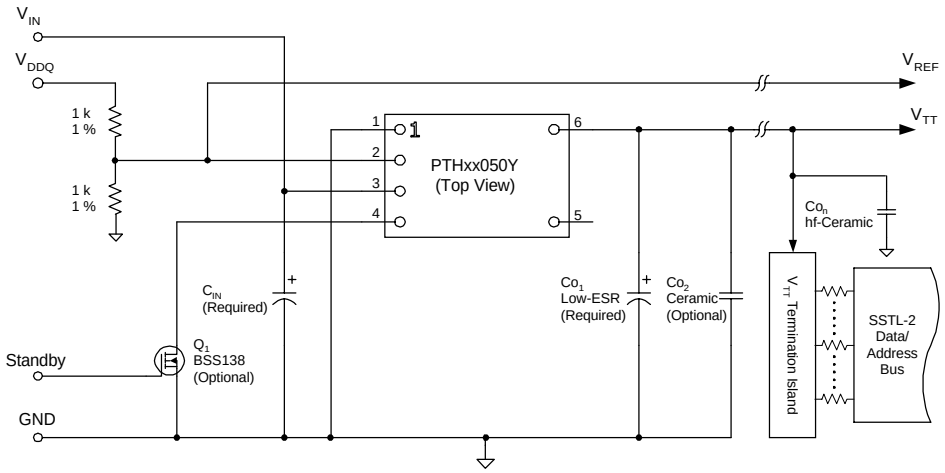
Package options include both through-hole and surface mount configurations.

Pin Configuration

Pin	Function
1	GND
2	V_{REF}
3	V_{IN}
4	Inhibit *
5	No Connect
6	V_{TT}

* *Denotes negative logic:*
Open = V_{TT} Output On
Ground = V_{TT} Output Off

Standard Application



C_{in} = Required electrolytic capacitor; 220 µF (3.3-/5-V input), 560 µF (12-V input).
Co_1 = Required low-ESR electrolyitic capacitor; 470 µF (3.3-/5-V input), 940 µF (12-V input).
Co_2 = Ceramic capacitance for optimum response to a 3-A (±1.5-A) load transient.; 200 µF (3.3-/5-V input), 400 µF (12-V input).
Co_n = Distributed hf-ceramic decoupling capacitors for V_{TT} bus; as recommended for DDR memory appications.

Ordering Information

Input Voltage (PTH❐❐050Yxx)

Code	Input Voltage
03	3.3 V
05	5 V
12	12 V

Package Options (PTHxx050Y❐❐) (1)

Code	Description	Pkg Ref. (2)
AH	Horiz. T/H	(EUU)
AS	SMD, Standard (3)	(EUV)

Notes: *(1) Add "T" to end of part number for tape and reel on SMD packages only.*
(2) Reference the applicable package reference drawing for the dimensions and PC board layout
(3) "Standard" option specifies 63/37, Sn/Pb pin solder material.

Pin Descriptions

V_{IN}: The positive input voltage power node to the module, which is referenced to common *GND*.

GND: This is the common ground connection for the V_{IN} and V_{TT} power connections. It is also the 0-VDC reference for the control inputs.

V_{REF}: The module senses the voltage at this input to regulate the output voltage, V_{TT}. The voltage at V_{REF} is also the reference voltage for the system bus receiver comparators. It is normally set to precisely half the bus driver supply voltage ($V_{DDQ} \div 2$), using a resistor divider (see standard application). The Thevenin impedance of the network driving the V_{REF} pin should not exceed 500 Ω.

V_{TT}: This is the regulated power output from the module with respect to the GND node, and the tracking termination supply for the application data and address buses. It is precisely regulated to the voltage applied to the module's V_{REF} input, and is active active about 20 ms after a valid input source is applied to the module. Once active it will track the voltage applied at V_{REF}.

Inhibit: The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a low-level ground signal to this input turns off the output voltage, V_{TT}. When the Inhibit is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open circuit, the module will produce an output whenever a valid input source is applied.

Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Control Input Voltage	V_{REF}		–0.3	—	V_{in} + 0.3	V
Operating Temperature Range	T_a	Over V_{in} Range	–40 (i)	—	85	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module body or pins			235 (ii)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	—	20	—	G's
Weight	—		—	2.9	—	grams
Flammability	—	Meets UL 94V-O				

Notes: *(i) For operation below 0 °C the external capacitors m ust have stable characteristics. use either a low ESR tantalum, Os-Con, or ceramic capacitor.*
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

Specifications (Unless otherwise stated, T_a =25 °C; nominal V_{in}; V_{REF} =1.25 V; C_{in}, Co_1, & Co_2 =typical values; and I_o =$I_o$max)

Characteristics	Symbols	Conditions		PTHxx050Y Min	Typ	Max	Units
Output Current	I_o	Over ΔV_{REF} range,	Continuous	0	—	±6 (1)	A
			Repetitive pulse	—	—	±8 (2)	A
Input Voltage Range	V_{in}	Over I_o range	PTH03050Y	2.95	—	3.65	V
			PTH05050Y	4.5	—	5.5	
			PTH12050Y	10.8	—	13.2	
Tracking Range for V_{REF}	ΔV_{REF}			0.55	—	1.8	V
Tracking Tolerance to V_{REF}	$\lvert V_{TT} - V_{REF} \rvert$	Over line, load and temperature		–10	—	+10	mV
Efficiency	η	I_o =4 A	PTH03050Y	—	88	—	%
			PTH05050Y	—	87	—	
			PTH12050Y	—	84	—	
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth		—	20	—	mVpp
Over-Current Threshold	I_o trip	Reset, followed by auto-recovery		—	12	—	A
Load Transient Response		15 A/µs load step, from –1.5 A to +1.5 A (See note 5)					
	t_{tr}		Recovery Time	—	80	—	µSec
	ΔV_{tr}		V_o over/undershoot	—	25	40	mV
Under-Voltage Lockout	UVLO	V_{in} increasing	PTH03050Y	—	2.45	2.8	V
			PTH05050Y	—	4.3	4.45	
			PTH12050Y	—	9.5	10.4	
		V_{in} decreasing	PTH03050Y	2.2	2.40	—	V
			PTH05050Y	3.4	3.7	—	
			PTH12050Y	8.8	9	—	
Inhibit Control (pin4)		Referenced to GND					
Input High Voltage	V_{IH}			V_{in} –0.5	—	Open (3)	V
Input Low Voltage	V_{IL}			–0.2	—	0.6	
Input Low Current	I_{IL} inhibit	Pin to GND		—	–130	—	µA
Input Standby Current	I_{in} inh	Inhibit (pin 4) to GND		—	10	—	mA
Switching Frequency	f_s	Over V_{in} & I_o ranges	PTH03050Y/PTH05050Y	550	600	650	kHz
			PTH12050Y	200	250	300	
External Input Capacitance	C_{in}		PTH03050Y/PTH05050Y	220 (4)	—	—	µF
			PTH12050Y	560 (4)	—	—	
External Output Capacitance	Co_1, Co_2	Capacitance value: non-ceramic	PTH03050Y/PTH05050Y	0	470 (5)	3,300 (6)	µF
			PTH12050Y	—	940 (5)	3,300 (6)	
		ceramic	PTH03050Y/PTH05050Y	0	200 (5)	300	µF
			PTH12050Y	0	400 (5)	600	
		Equiv. series resistance (non-ceramic)		4 (7)	—	—	mΩ
Reliability	MTBF	Per Bellcore TR-332 50 % stress, T_a =40 °C, ground benign		6	—	—	10^6 Hrs

Notes: *(1) Rating is conditional on the module being directly soldered to a 4-layer PCB with 1 oz. copper. See the SOA curves or contact the factory for appropriate derating. The PTH03050Y and PTH05050Y require no derating up to 85 °C operating temperature and natural convection airflow.*

(2) Up to 10 ms pulse period at 10 % maximum duty.

(3) This control pin has an internal pull-up to the input voltage Vin. If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.

(4) An input capacitor is required for proper operation. The capacitor must be rated for a minimum of 300 mA rms (750 mA rms for 12-V input) of ripple current.

(5) The typical value of external output capacitance value ensures that V_{TT} meets the specified transient performance requirements for the memory bus terminations. Lower values of capacitance may be possible when the measured peak change in output current is consistently less than 3 A.

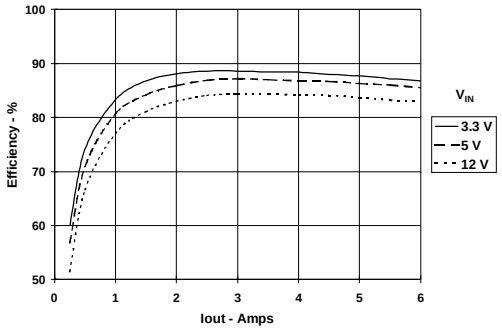
(6) This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult the application notes for further guidance.

(7) This is the typcial ESR for all the electrolytic (non-ceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

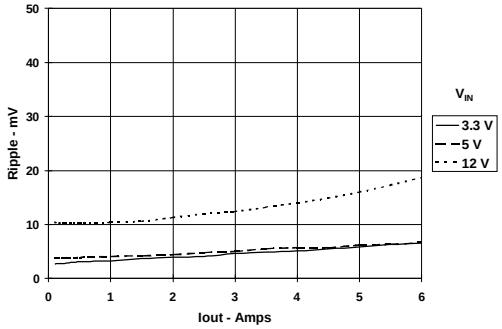
Typical Characteristics

Characteristic Data; V_{REF} =1.25 V *(See Note A)*

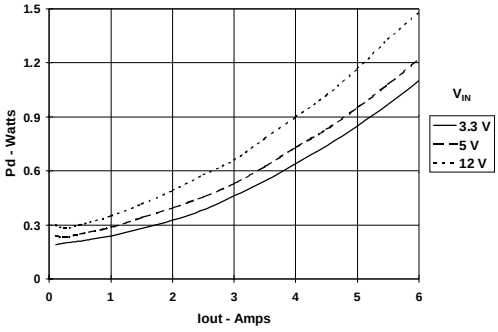
Efficiency vs Load Current



Output Ripple vs Load Current *(See Note 2 to Table)*

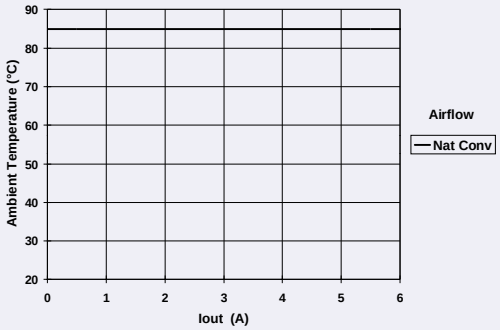


Power Dissipation vs Load Current

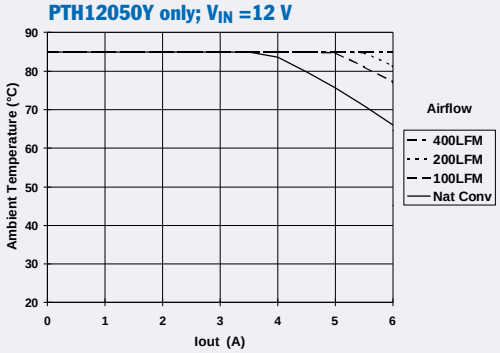


Safe Operating Area; V_{REF} =1.25 V *(See Note B)*

PTH03050Y/PTH05050Y at nominal V_{IN}

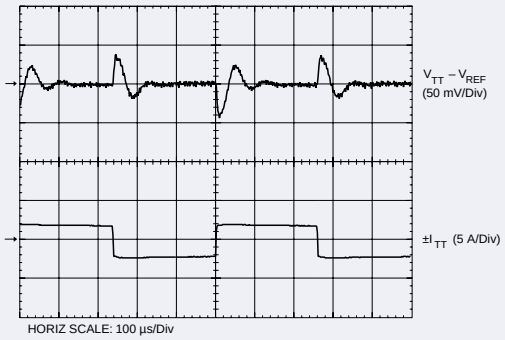


PTH12050Y only; V_{IN} =12 V



Transient Performance for Δ4-A Load Change

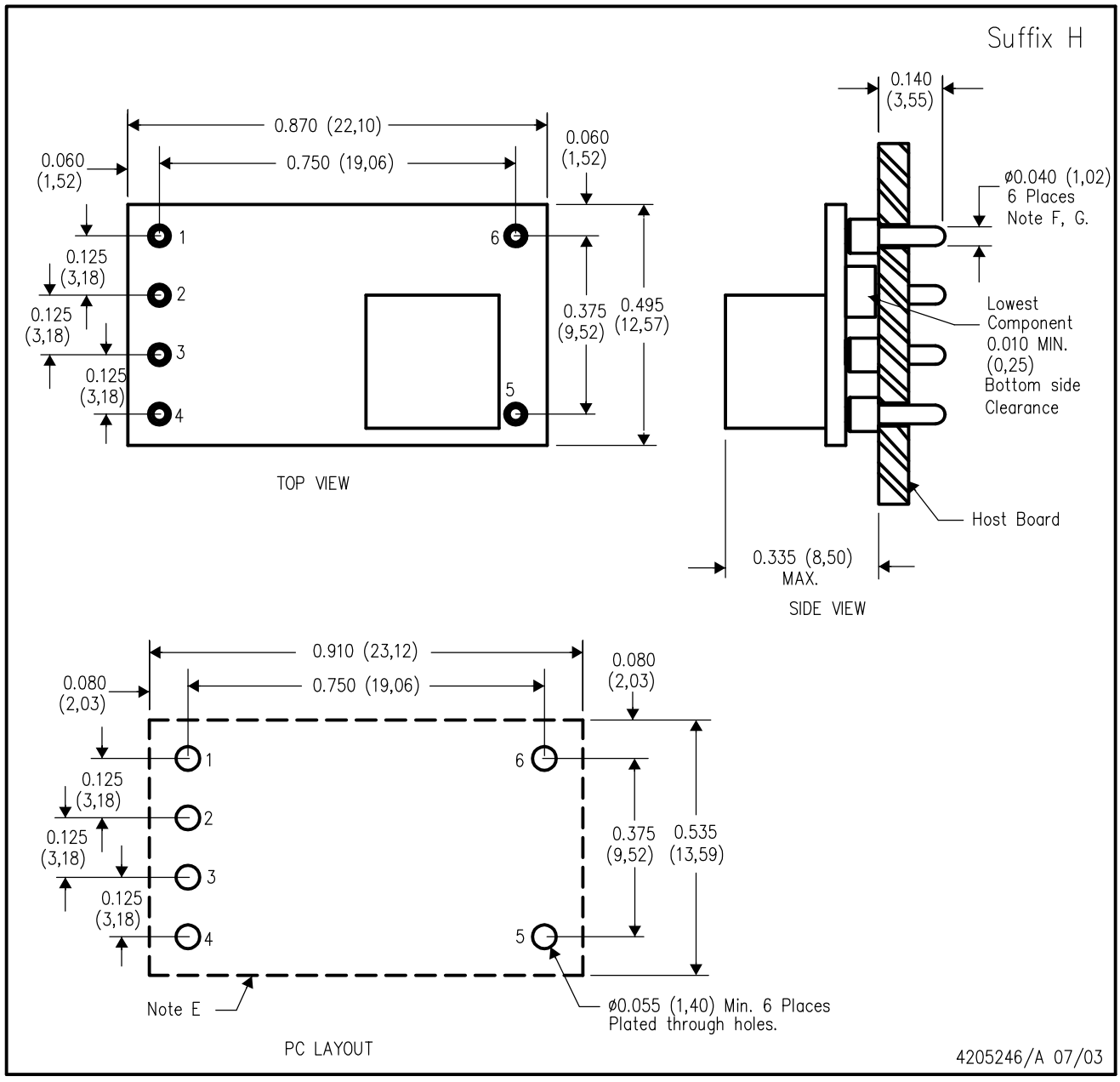
PTH03050Y: Sink to Source Transient



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*

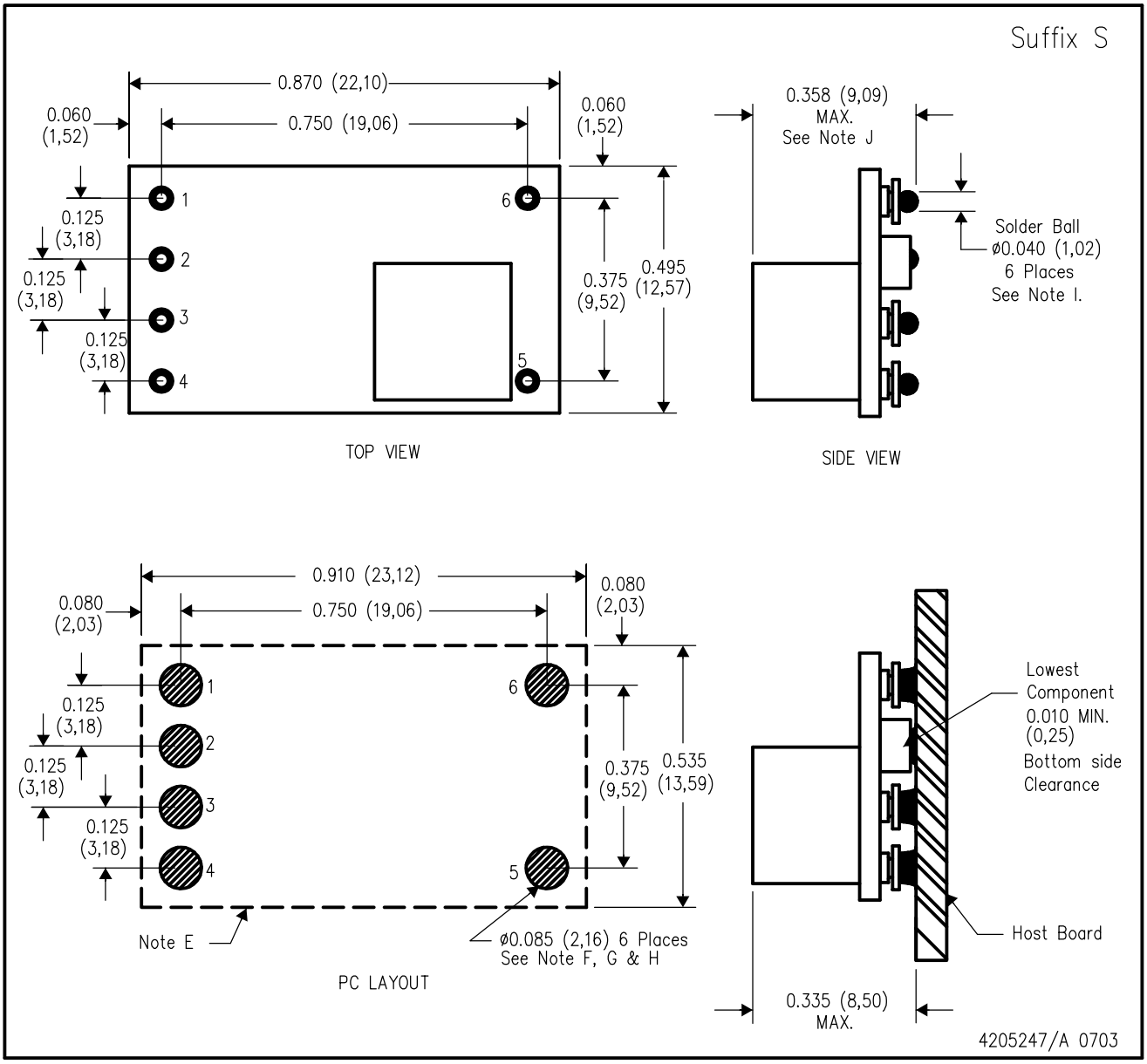
Note B: *SOA graphs represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in × 4 in. double-sided PCB with 1 oz. copper.*

EUU (R–PDSS–T6) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EUV (R–PDSS–B6) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

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