1.5-A, WIDE-INPUT ADJUSTABLE SWITCHING REGULATOR

FEATURES

- 1.5-A Output Current
- Wide-Input Voltage (7 V to 36 V)
- Wide-Output Voltage Adjust (2.5 V to 12.6 V)
- High Efficiency (Up to 95%)
- On/Off Inhibit
- Output Current Limit
- Overtemperature Shutdown
- Operating Temp: –40°C to 85°C
- Surface Mount Package

APPLICATIONS

- General-Purpose, Industrial Controls, HVAC Systems, Test and Measurement, Medical Instrumentation, AC/DC Adaptors, Vehicles, Marine and Avionics

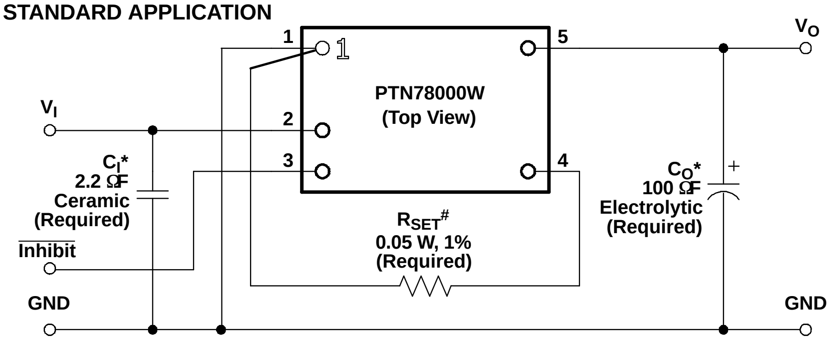
DESCRIPTION

The PTN78000W is a series of high-efficiency, step-down Integrated Switching Regulator (ISR), that represent the third generation in the evolution of the popular 78ST100 series of products. In new designs it may be considered in place of the 78ST100, PT78ST100, PT5100, and PT6100 series of single in-line pin (SIP) products. The PTN78000 is smaller and lighter than its predecessors, and has either similar or improved electrical performance characteristics. The case-less, double-sided package, also exhibits improved thermal characteristics, and is compatible with TI's roadmap for RoHS and lead-free compliance.

Operating from a wide-input voltage range of 7 V to 36 V, the PTN78000 provides high-efficiency, step-down voltage conversion for loads of up to 1.5 A. The output voltage is set using a single external resistor, and may be set to any value within the range, 2.5 V to 12.6 V. The output voltage can be as little as 2 V lower than the input, allowing operation down to 7 V, with an output voltage of 5 V.

The PTN78000 has an integral on/off inhibit, and is suited to a wide variety of general-purpose applications that operate off 12-V, 24-V, or 28-V dc power.

STANDARD APPLICATION



*See The Application Information for Capacitor Recommendation.
#R_{SET} is Required to Adjust the Output Voltage Higher Than 2.5 V. See The Application Information for Values.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PTN78000 (Basic Model)			
Output Voltage	**Part Number**	**Description**	**Package Designator**
2.5 V - 12.6 V	PTN78000WAH	Horizontal T/H	EUS
	PTN78000WAS (1)	Horizontal SMD	EUT

(1) Add a T suffix for tape and reel option on SMD packages.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range unless otherwise noted
all voltages with respect to GND (pin 2),

			UNIT
T_A	Operating free-air temperature	Over V_I range	–40°C to 85°C
	Solder reflow temperature	Surface temperature of module body or pins	235°C
T_{stg}	Storage temperature		–40°C to 125°C
V_I	Input surge voltage, 10 ms maximum		38 V
V_{INH}	Inhibit (pin 3) input voltage		–0.3 V to 5 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_I	Input voltage	7	36	V
T_A	Operating free-air temperature	–40	85	°C

PACKAGE SPECIFICATIONS

PTN78000x (Suffix AH and AS)			
Weight			2 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		500 Gs (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	Horizontal T/H (suffix AH)	20 Gs (1)
		Horizontal SMD (suffix AS)	15 Gs (1)

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 20 V, V_O = 5 V, I_O = I_O (max), C_I = 2.2 µF, C_O = 100 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_O	Output current	T_A = 85°C, natural convection airflow	0		1.5	A
V_I	Input voltage range	Over I_O range	7 (1)		36 (2)	V
V_O	Set-point voltage tolerance	T_A = 25°C			±2% (3)	
	Temperature variation	–40°C to +85°C		±0.5%		
	Line regulation	Over V_I range		±10		mV
	Load regulation	Over I_O range		±10		mV
	Total Output Voltage Variation	Includes set point, line, load –40 < T_A < 85°C			±3% (3)	
V_O (adj)	Output Voltage Adjust Range	V_I < 12 V	2.5		V_I – 2	V
		12 V ≤ V_I ≤ 15.1 V	2.5		V_I – 2.5	
		15.1 V < V_I ≤ 25 V	2.5		12.6	
		V_I > 25 V	0.1 × V_I		12.6	
η	Efficiency	V_I = 24 V, R_{SET} = 732 Ω, V_O = 12 V		91%		
		V_I = 15 V, R_{SET} = 21 kΩ, V_O = 5 V		86%		
		V_I = 15 V, R_{SET} = 78.7 kΩ, V_O = 3.3 V		82%		
	Output Voltage Ripple	20 MHz bandwith		1% V_O		$V_{(PP)}$
$I_{O\ (LIM)}$	Current Limit Threshold	ΔV_O = –50 mV		3.2		A
	Transient response	1 A/µs load step from 50% to 100% $I_O$max				
		Recovery time		100		µs
		V_O over/undershoot		2.5		%V_O
	Inhibit control (pin 3)	Input high voltage (V_{IH})	1		Open (4)	V
		Input low voltage (V_{IL})	–0.1		0.3	
		Input low current (I_{IL})		–0.25		mA
$I_{I(stby)}$	Input standby current	Pin 3 connected to GND		17		mA
F_S	Switching frequency	Over V_I and I_O ranges	440	550	660	kHz
C_I	External input capacitance		2.2 (5)			µF
C_O	External output capacitance	ceramic or non-ceramic	100 (6)			µF
		ceramic			200	
		non-ceramic			1,000	
		Equiv. series resistance (nonceramic)	10 (7)			mΩ
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign	8.9			10^6 Hrs

(1) For output voltages less than 10 V, the minimum input voltage is 7 V or (V_O + 2) V, whichever is greater. For output voltages of 10 V and higher, the minimum input voltage is (V_O + 2.5) V. Consult the Application Information for further guidance.
(2) For output voltages less than 3.6 V, the maximum input voltage is 10 × V_O . Consult the Application Information for further guidance.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with with 100 ppm/°C or better temperature stability.
(4) This control pin has an internal pullup, and if left open circuit the module will operate when input power is applied. The open-circuit voltage is typically 1.5 V. A small low-leakage (< 100 nA) MOSFET is recommended for control. Refer to the application information for further guidance.
(5) An external 2.2-µF ceramic capacitor is required across the input (V_I and GND) for proper operation. Locate the capacitor close to the module.
(6) 100 µF of output capacitance is required for proper operation. Refer to the application information for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 mΩ as the minimum when using maximum ESR values to calculate.

PIN ASSIGNMENT

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1		This is the common ground connection for the V_I and V_O power connections. It is also the 0 VDC reference for the *Inhibit* and V_O *Adjust* control inputs.
V_I	2	I	The positive input voltage power node to the module, which is referenced to common GND.
Inhibit	3	I	The Inhibit pin is an open-collector/drain active-low input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module will produce an output whenever a valid input source is applied.
V_O Adjust	4	I	A 1% resistor must be connected between this pin and GND (pin 1) to set the output voltage of the module higher than 2.5 V. If left open-circuit, the output voltage will default to this value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 2.5 V to 12.6 V. The standard resistor value for a number of common output voltages is provided in the application information.
V_O	5	O	The regulated positive power output with respect to the GND node.

TYPICAL CHARACTERISTICS (7-V INPUT)(1)(2)

EFFICIENCY
vs
OUTPUT CURRENT

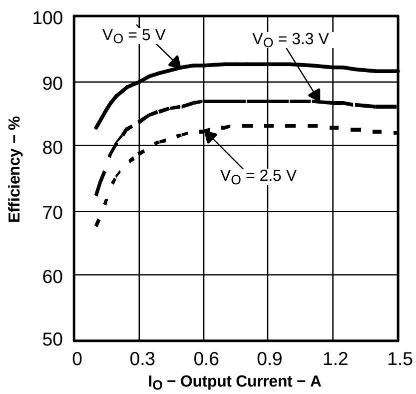


Figure 1.

OUTPUT VOLTAGE RIPPLE
vs
OUTPUT CURRENT

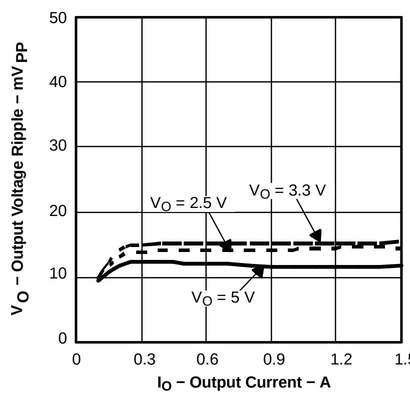


Figure 2.

POWER DISSIPATION
vs
OUTPUT CURRENT

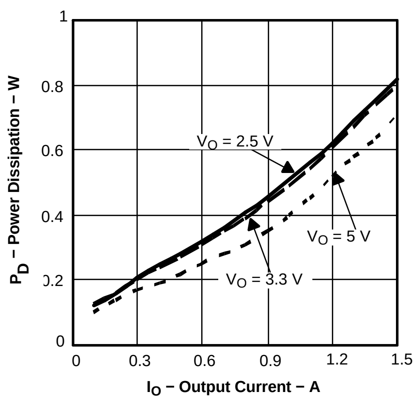


Figure 3.

TEMPERATURE DERATING
vs
OUTPUT CURRENT; $V_O \leq 5$ V

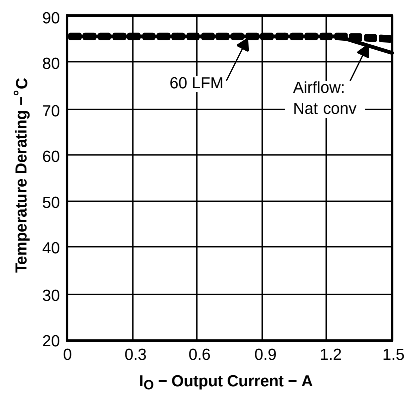


Figure 4.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.
(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 4.

TYPICAL CHARACTERISTICS (15-V INPUT)(3)(4)

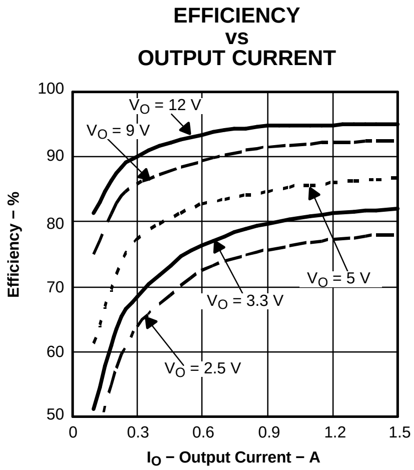


Figure 5.

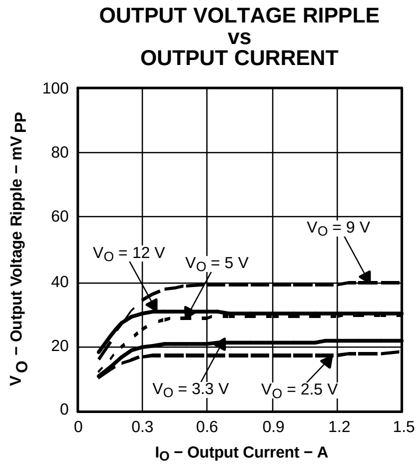


Figure 6.

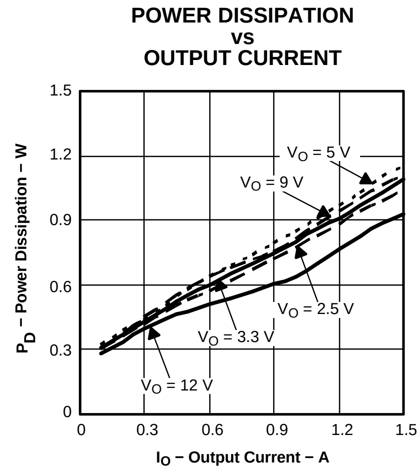


Figure 7.

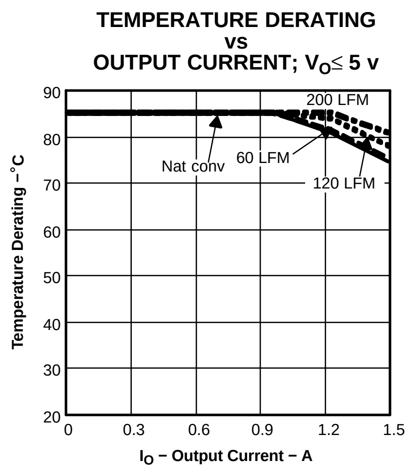


Figure 8.

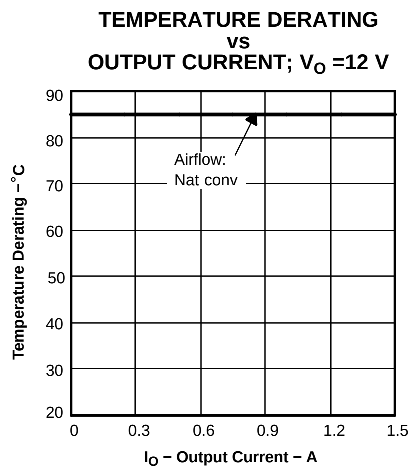


Figure 9.

(3) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 5, Figure 6, and Figure 7.

(4) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2 oz. copper. Applies to Figure 8 and Figure 9.

TYPICAL CHARACTERISTICS (24-V INPUT)(5)(6)

EFFICIENCY vs OUTPUT CURRENT

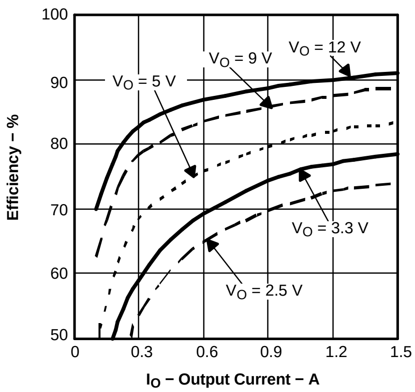


Figure 10.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

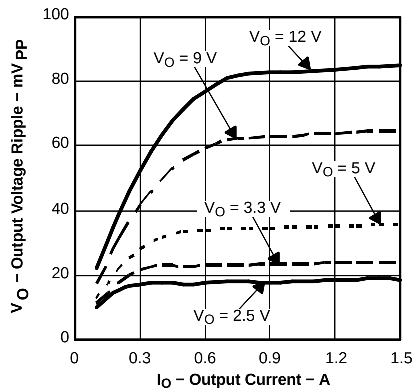


Figure 11.

POWER DISSIPATION vs OUTPUT CURRENT

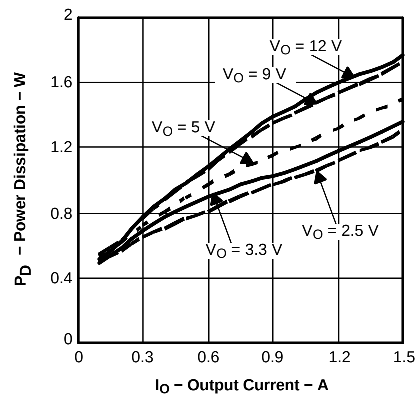


Figure 12.

TEMPERATURE DERATING vs OUTPUT CURRENT; V_O =3.3 V

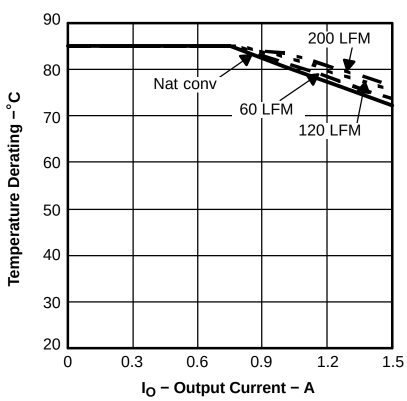


Figure 13.

TEMPERATURE DERATING vs OUTPUT CURRENT; V_O =5 V

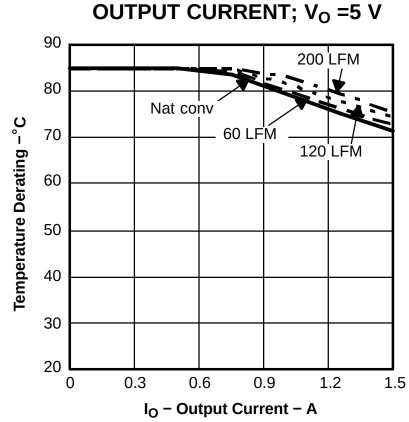


Figure 14.

TEMPERATURE DERATING; vs OUTPUT CURRENT V_O =12 V

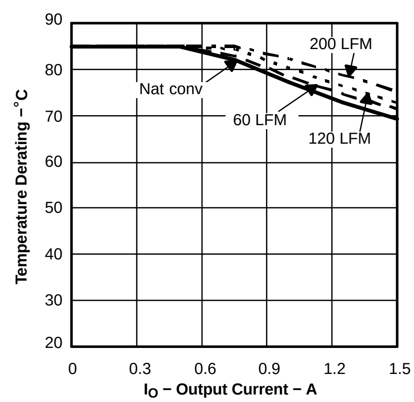


Figure 15.

(5) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 10, Figure 11, and Figure 12.
(6) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2 oz. copper. Applies to Figure 13, Figure 14, and Figure 15.

TYPICAL CHARACTERISTICS (32-V INPUT)[(7)(8)]

EFFICIENCY vs OUTPUT CURRENT

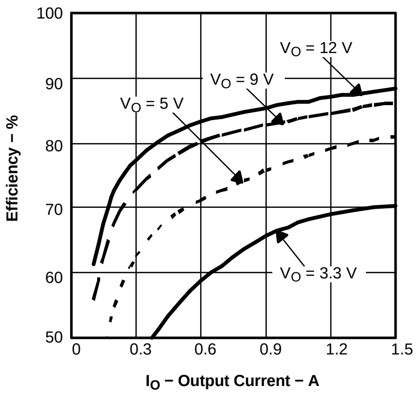


Figure 16.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

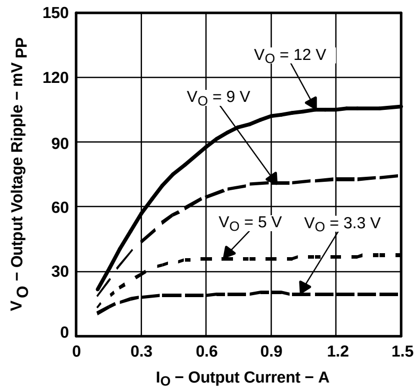


Figure 17.

POWER DISSIPATION vs OUTPUT CURRENT

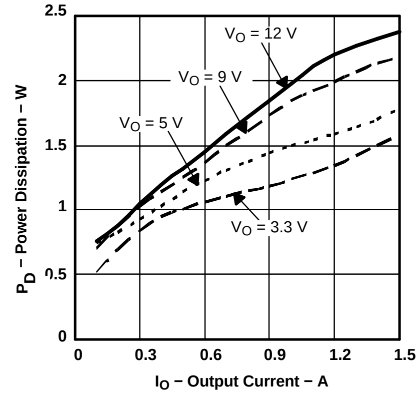


Figure 18.

TEMPERATURE DERATING vs OUTPUT CURRENT; V_O = 3.3 V

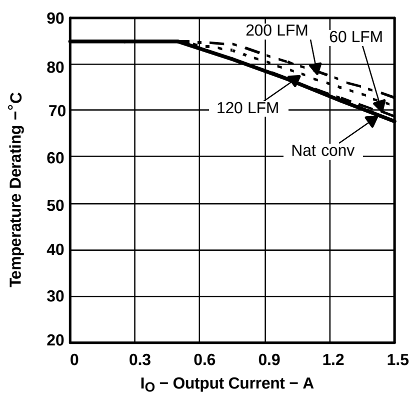


Figure 19.

TEMPERATURE DERATING vs OUTPUT CURRENT; V_O = 5 V

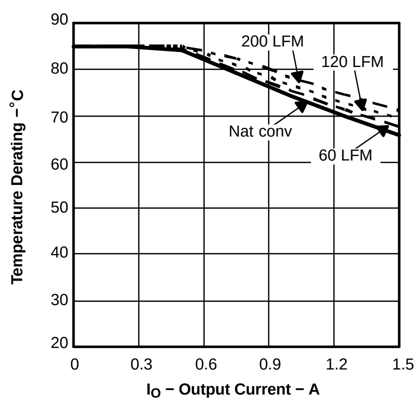


Figure 20.

TEMPERATURE DERATING vs OUTPUT CURRENT; V_O = 12 V

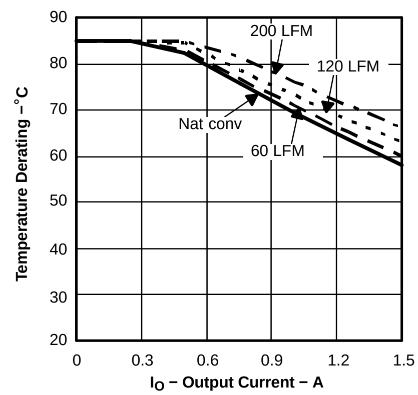


Figure 21.

(7) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 16, Figure 17, and Figure 18.

(8) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2 oz. copper. Applies to Figure 19, Figure 20, and Figure 21.

APPLICATION INFORMATION

Adjusting the Output Voltage of the PTN78000W Wide-Output Adjust Power Modules

General

A resistor must be connected between the *V_O Adjust* control (pin 4) and *GND* (pin 1) to set the output voltage higher than 2.5 V. The adjustment range is from 2.5 V to 12.6 V. If pin 4 is left open, the output voltage will default to the lowest value, 2.5 V.

Table 1 gives the preferred value of the external resistor for several standard voltages, with the actual output voltage that the value provides. For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 22 shows the placement of the required resistor.

$$R_{SET} = 54.9\ k\Omega \times \frac{1.25\ V}{V_O - 2.5\ V} - 6.49\ k\Omega$$

Input Voltage Considerations

The PTN78000 is a step-down switching regulator. In order that the output remains in regulation, the input voltage must exceed the output by a minimum differential voltage.

Another consideration is the pulse width modulation (PWM) range of the regulator's internal control circuit. For stable operation, its operating duty cycle should not be lower than some minimum percentage. This defines the maximum advisable ratio between the regulator's input and output voltage magnitudes.

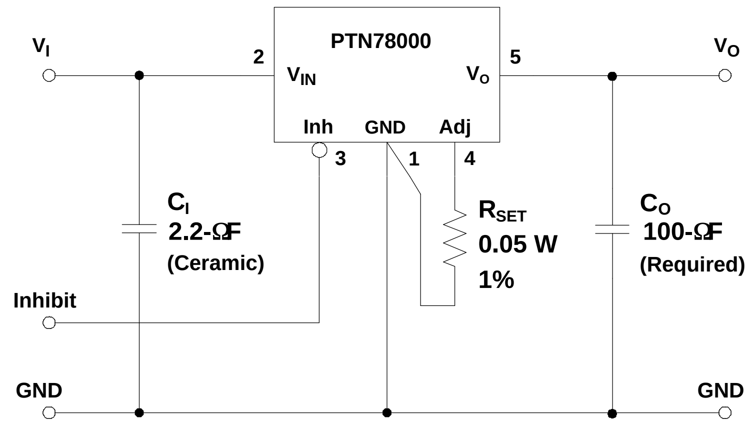
For satisfactory performance, the operating input voltage range of the PTN78000 must adhere to the following requirements.

1. For output voltages lower than 10 V, the minimum input voltage is (V_O+ 2 V) or 7 V, whichever is higher.
2. For output voltages equal to 10 V and higher, the minimum input voltage is (V_O+ 2.5 V) .
3. The maximum input voltage is (10 × V_O) or 36 V, whichever is less.

As an example, Table 1 gives the operating input voltage range for the common output bus voltages. In addition, the Electrical Characteristics define the available output voltage adjust range for various input voltages.

Table 1. Standard Values of R_{set} for Common Output Voltages

V_O (Required)	R_{SET} (Standard Value)	V_O (Actual)	Operating V_I Range
2.5 V	Open	2.5 V	7 V to 25 V
3.3 V	78.7 kΩ	3.306 V	7 V to 33 V
5 V	21 kΩ	4.996 V	7 V to 36 V
12 V	732 Ω	12.002 V	14.5 V to 36 V



(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 1 using dedicated PCB traces.

(2) Never connect capacitors from V_O *Adjust* to either *GND* or V_{out}. Any capacitance added to the V_O *Adjust* pin will affect the stability of the regulator.

Figure 22. V_O Adjust Resistor Placement

Table 2. Output Voltage Set-Point Resistor Values

V_a Req'd	R_{set}	V_a Req'd	R_{set}	V_a Req'd	R_{set}	V_a Req'd	R_{set}
2.50 V	Open	3.7 V	50.7 kΩ	6.1 V	12.6 kΩ	9.0 V	4.07 kΩ
2.55 V	1.37 MΩ	3.8 V	46.3 kΩ	6.2 V	12.1 kΩ	9.2 V	3.75 kΩ
2.60 V	680 kΩ	3.9 V	42.5 kΩ	6.3 V	11.6 kΩ	9.4 V	3.46 kΩ
2.65 V	451 kΩ	4.0 V	39.3 kΩ	6.4 V	11.1 kΩ	9.6 V	3.18 kΩ
2.70 V	337 kΩ	4.1 V	36.4 kΩ	6.5 V	10.7 kΩ	9.8 V	2.91 kΩ
2.75 V	268 kΩ	4.2 V	33.9 kΩ	6.6 V	10.2 kΩ	10.0 V	2.66 kΩ
2.80 V	222 kΩ	4.3 V	31.6 kΩ	6.7 V	9.85 kΩ	10.2 V	2.42 kΩ
2.85 V	190 kΩ	4.4 V	29.6 kΩ	6.8 V	9.47 kΩ	10.4 V	2.20 kΩ
2.90 V	165 kΩ	4.5 V	27.8 kΩ	6.9 V	9.11 kΩ	10.6 V	1.98 kΩ
2.95 V	146 kΩ	4.6 V	26.2 kΩ	7.0 V	8.76 kΩ	10.8 V	1.78 kΩ
3.00 V	131 kΩ	4.7 V	24.7 kΩ	7.1 V	8.43 kΩ	11.0 V	1.58 kΩ
3.05 V	118 kΩ	4.8 V	23.3 kΩ	7.2 V	8.11 kΩ	11.2 V	1.40 kΩ
3.10 V	108 kΩ	4.9 V	22.1 kΩ	7.3 V	7.81 kΩ	11.4 V	1.22 kΩ
3.15 V	99.1 kΩ	5.0 V	21.0 kΩ	7.4 V	7.52 kΩ	11.6 V	1.05 kΩ
3.20 V	91.5 kΩ	5.1 V	19.9 kΩ	7.5 V	7.24 kΩ	11.8 V	889 Ω
3.25 V	85.0 kΩ	5.2 V	18.9 kΩ	7.6 V	6.97 kΩ	12.0 V	734 Ω
3.30 V	79.3 kΩ	5.3 V	18.0 kΩ	7.7 V	6.71 kΩ	12.2 V	585 Ω
3.35 V	74.2 kΩ	5.4 V	17.2 kΩ	7.8 V	6.46 kΩ	12.4 V	442 Ω
3.40 V	69.8 kΩ	5.5 V	16.4 kΩ	7.9 V	6.22 kΩ	12.6 V	305 Ω
3.45 V	65.7 kΩ	5.6 V	15.6 kΩ	8.0 V	5.99 kΩ		
3.50 V	62.1 kΩ	5.7 V	15.0 kΩ	8.2 V	5.55 kΩ		
3.55 V	58.9 kΩ	5.8 V	14.3 kΩ	8.4 V	5.14 kΩ		
3.60 V	55.9 kΩ	5.9 V	13.7 kΩ	8.6 V	4.76 kΩ		
3.65 V	53.2 kΩ	6.0 V	13.1 kΩ	8.8 V	4.40 kΩ		

CAPACITOR RECOMMENDATIONS for the PTN78000 WIDE-OUTPUT ADJUST POWER MODULES

Input Capacitor

The minimum requirements for the input is 2.2 µF of ceramic capacitance, in either an X5R or X7R temperature characteristic. Ceramic capacitors should be located within 0.5 in. (1,27 cm) of the regulator's input pins. Electrolytic capacitors can be used at the input, but only in addition to the required ceramic capacitance. The minimum ripple current rating for any nonceramic capacitance must be at least 400 mA rms for V_O≤5.5, For V_O >5.5V, the minimum ripple current rating is 650 mA rms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input. This ripple current requirement can be reduced by placing more ceramic capacitors at the input, in addition to the minimum required 2.2 µF.

Tantalum capacitors are not recommended for use at the input bus, as none were found to meet the minimum voltage rating of 2 × (maximum dc voltage + ac ripple). The 2× rating is standard practice for regular tantalum capacitors to ensure reliability. Polymer-tantalum capacitors are more reliable and are available with a maximum rating of typically 20 V. These can be used with input voltages up to 16 V.

Output Capacitor

The minimum capacitance required to insure stability is a 100 µF. Either ceramic or electrolytic-type capacitors can be used. The minimum ripple current rating for the nonceramic capacitance must be at least 150 mA rms. The stability of the module and voltage tolerances will be compromised if the capacitor is not placed near the output bus pins. A high-quality, computer-grade electrolytic capacitor should be adequate. A ceramic capacitor can be also be located within 0.5 in. (1,27 cm) of the output pin.

For applications with load transients (sudden changes in load current), the regulator response improves with additional capacitance. Additional electrolytic capacitors should be located close to the load circuit. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz. Aluminum electrolytic capacitors are suitable for ambient temperatures above 0°C. For operation below 0°C, tantalum or Os-Con type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 10 mΩ (17 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of capacitors and vendors are identified in Table 3, the recommended capacitor table.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors becomes less effective. To further reduce the reflected input ripple current, or the output transient response, multilayer ceramic capacitors must be added. Ceramic capacitors have low ESR and their resonant frequency is higher than the bandwidth of the regulator. When placed at the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 200 µF. Also, to prevent the formation of local resonances, do not place more than three identical ceramic capacitors with values of 10 µF or greater in parallel.

Tantalum Capacitors

Tantalum type capacitors may be used at the output, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510/T520 capacitors series are suggested over many other tantalum types due to their rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying Os-Con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

Capacitor Table

The capacitor table, Table 3, identifies the characteristics of capacitors from various vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type. This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The rms rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Designing for Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation of any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed those specified in the data sheet, the selection of output capacitors becomes more important. Review the minimum ESR in the characteristic data sheet for details on the capacitance maximum.

Table 3. Recommended Input/Output Capacitors

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE (µF)	EQUIVALENT SERIES RESISTANCE (ESR) (Ω)	85°C MAXIMUM RIPPLE CURRENT (I_{rms}) (mA)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Panasonic WA (SMD)	16	100	0.039	2500	8 × 6,9	1 (1)	≤ 3	EEFWA1C101P (V_I < 14 V)
FC(Radial)	50	180	0.119	850	10 × 16	1	1	EEUFC1H181
FC (SMD)	3	100	0.015	670	10 × 10,2	1 (1)	1	EEVFC1V101P
United Chemi-Con PXA (SMD)	16	180	0.016	4360	8 × 12	1 (1)	≤ 1	PXA16VC180MF60
FS	20	150	0.024	3200	8 × 10,5	1 (1)	≤ 2	10FS100M (V_I < 16 V)
LXZ	50	120	0.160	620 x 2	10 × 12,5	2	1	LXZ50VB121M10X12LL
MVY(SMD)	50	100	0.300	500	10 × 10	1	1	MVY50VC101M10X10TP (V_O≤ 5.5 V)
Nichicon UWG (SMD)	50	100	0.300	500	10 × 10	1	1	UWG1H101MNR1GS
F559 (Tantalum)	10	100	0.055	2000	7.7 × 4,3	N/R (1)	≤ 3(2)	F551A107MN (V_O≤ 5 V)
HD	50	100	0.074	724	8 × 11,5	1	1	UHD1H101MPR
Sanyo Os-Con SVP (SMD)	20	100	0.024	2500	8 × 12	1 (1)	≤ 2	20SVP100M (V_I≤ 16 V)
SP	16	100	0.032	2890	10 × 5	1 (1)	≤ 2	16SP100M (V_I≤ 14 V)
AVX Tantalum TPS (SMD)	20	100	0.085	1543	7,3 L × 4,3 W × 4,1 H	N/R (3)	≤ 3	TPSV107M020R0085 (V_O≤ 10 V)
	20	100	0.200	> 817		N/R (3)	≤ 3	TPSE107M020R0200
Murata X5R Ceramic	6.3	100	0.002	>1000	1210	N/R (1)	≤ 2	GRM32ER60J107M (V_O≤ 5.5 V)
TDK X5R Ceramic	6.3	100	0.002	>1000	3225	N/R (1)	≤ 2	C3225X5R0J107MT (V_O≤ 5.5 V)
Murata X5R Ceramic	16	47	0.002	>1000	1210	1 (1)	≤ 4	GRM32ER61C476M (V_o ~ V_I≤ 13.5 V)
Kemet X5R Ceramic	6.3	47	0.002	>1000	1210	N/R (1)	≤ 4	C1210C476K9PAC (V_O≤ 5.5 V)
TDK X5R Ceramic	6.3	47	0.002	>1000	3225	N/R (1)	≤ 4	C3225X5R0J476MT (V_O≤ 5.5 V)
Murata X5R Ceramic	6.3	47	0.002	>1000	3225	N/R (1)	≤ 4	GRM422X5R476M6.3 (V_O≤ 5.5 V)
TDK X7R Ceramic	25	2.2	0.002	>1000	SMD	≥ 1 (4)	1	C3225X7R0J225KT/MT (V_O≤ 20 V)
Murata X7R Ceramic	25	2.2	0.002	>1000	1210 case	≥ 1 (4)	1	GRM32RR71J225K (V_O≤ 20 V)

(1) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with the next higher voltage rating.
(2) The maximum voltage rating of the capacitor must be selected for the desired set-point voltage (V_O). To operate at a higher output voltage, select a capacitor with a higher voltage rating.
(3) Not reccomended (N/R). The voltage rating does not meet the minimum operating limits in most applications.
(4) The maximum rating of the ceramic capacitor limits the regulator's operating input voltage to 20 V. Select a alternative ceramic component to operate at a higher input voltage.

Table 3. Recommended Input/Output Capacitors (continued)

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE (µF)	EQUIVALENT SERIES RESISTANCE (ESR) (Ω)	85°C MAXIMUM RIPPLE CURRENT (I_{rms}) (mA)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Kemet X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 1 (4)	1	C1210C225K3RAC (V_O≤ 20 V)
AVX X7R Ceramic	25	2.2	0.002	>1000		≥ 1 (4)	1	12103C225KAT2A (V_O≤ 20 V)
Kemet X7R Ceramic	50	1	0.002	>1000	SMD	≥ 2 (5)	1	C1210C105K5RAC
Murata X7R Ceramic	50	4.7	0.002	>1000		≥ 1	1	GRM32ER71H475KA88L
TDK X7R Ceramic	50	2.2	0.002	>1000		≥ 1	1	C3225X7R1H225KT
Murata X7R Ceramic	50	1	0.002	>1000	1210 case	≥ 2 (5)	1	GRM32RR71H105KA01L
TDK X7R Ceramic	50	1	0.002	>1000	3225	≥ 2 (5)	1	C3225X7R1H105KT
Kemet Radial Through-hole	50	1	0.002	>1000	5,08 × 7,62 × 9,14 H	≥ 2 (5)	1	C330C105K5R5CA
Murata Radial Through-hole	50	2.2	0.004	>1000	10 H × 10 W × 4 D	1	1	RPER71H2R2KK6F03

(5) A total capacitance of 2 µF is an acceptable replacement value for a single 2.2-µF ceramic capacitor

Power-Up Characteristics

When configured per the standard application, the PTN78000 power module produces a regulated output voltage following the application of a valid input source voltage. During power up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay (typically 5–10 ms) into the power-up characteristic. This is from the point that a valid input source is recognized. Figure 23 shows the power-up waveforms for a PTN78000W, operating from a 12-V input and with the output voltage adjusted to 5 V. The waveforms were measured with a 1.5-A resistive load.

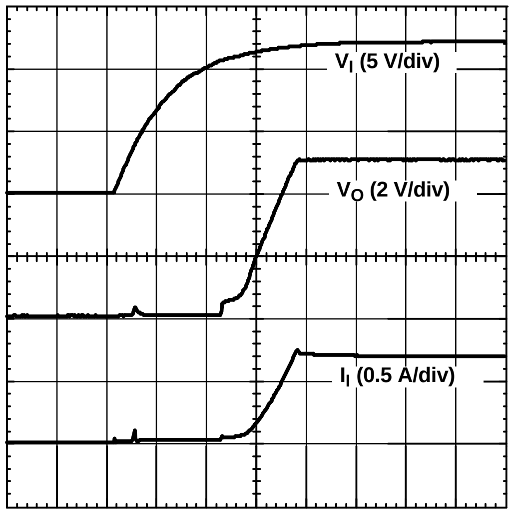


Figure 23. Power-Up Waveforms

Current Limit Protection

The PTN78000 modules protect against load faults with a continuous current limit characteristic. Under a load fault condition, the output current cannot exceed the current limit value. Attempting to draw current that exceeds the current limit value causes the module to progressively reduce its output voltage. Current is continuously supplied to the fault until it is removed. On removal of the fault, the output voltage promptly recovers. When limiting output current, the regulator experiences higher power dissipation, which increases its temperature. If the temperature increase is excessive, the module's overtemperature protection begins to periodically turn the output voltage completely off.

Overtemperature Protection

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in temperature may be the result of a drop in airflow, a high ambient temperature, or a sustained current-limit condition. If the junction temperature of the internal control IC rises excessively, the module turns itself off, reducing the output voltage to zero. The module instantly restarts when the sensed temperature decreases by a few degrees.

NOTE:

Overtemperature protection is a last resort mechanism to prevent damage to the module. It should not be relied on as permanent protection against thermal stress. Always operate the module within its temperature derated limits, for the worst-case operating conditions of output current, ambient temperature, and airflow. Operating the module above these limits, albeit below the thermal shutdown temperature, reduces the long-term reliability of the module.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTN78000 power module incorporates an output on/off Inhibit control (pin 3). The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power module functions normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND. Figure 24 shows the the circuit used to demonstrate the inhibit function. Note the discrete transistor (Q1). Turning Q1 on applies a low voltage to the *Inhibit* control pin and turns the module off. The output voltage decays as the load circuit discharges the capacitance. The current drawn at the input is reduced to typically 17 mA. If Q1 is then turned off, the module executes a soft-start power up. A regulated output voltage is produced within 20 msec. Figure 25 shows the typical rise in the output voltage, following the turn off of Q1. The turn off of Q1 corresponds to the fall in the waveform, Q1 Vgs. The waveforms were measured with a 1.5-A resistive load.

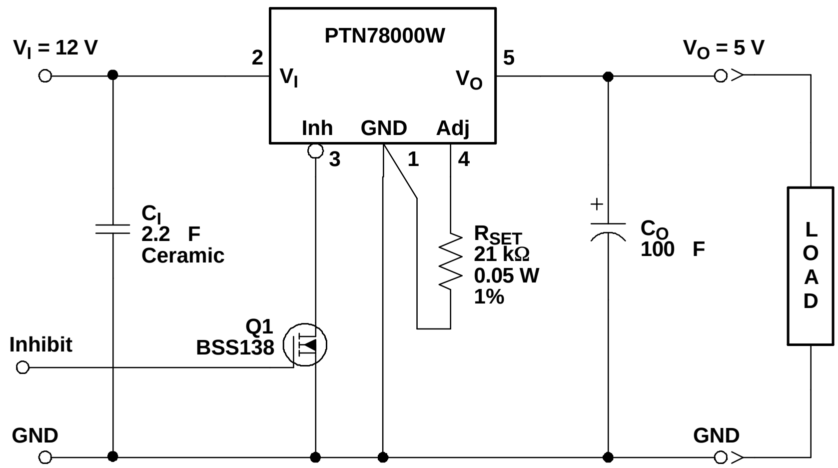


Figure 24. On/Off Inhibit Control Circuit

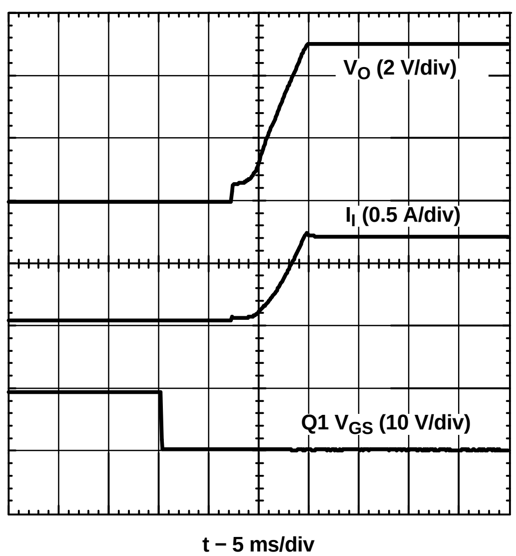


Figure 25. Power Up Response From Inhibit Control

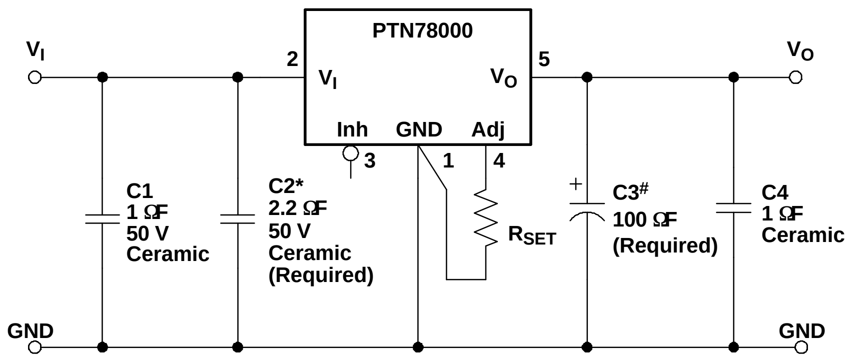
Optional Input/Output Filters

Power modules include internal input and output ceramic capacitors in all their designs. However, some applications require much lower levels of either input reflected or output ripple/noise. This application describes various filters and design techniques found to be successful in reducing both input and output ripple/noise.

Input/Output Capacitors

The easiest way to reduce output ripple and noise is to add one or more 1-µF ceramic capacitors, such as C4 shown in Figure 26. Ceramic capacitors should be placed close to the output power terminals. A single 1-µF capacitor reduces the output ripple/noise by 10% to 30% for modules with a rated output current of less than 3 A. (Note: C3 is recommended to improve the regulators transient response and does not reduce output ripple and noise.)

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple/noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of C2, minimum 1-µF ceramic capacitor, near the input power pins, reduces reflected conducted ripple/noise by 30% to 50%.



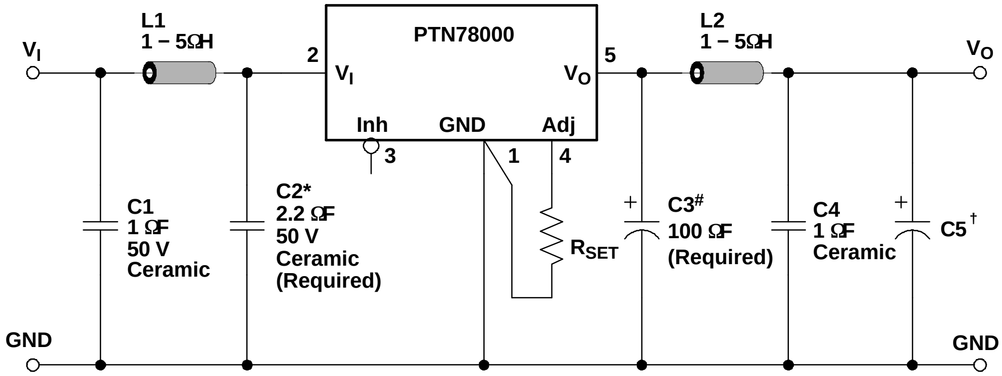
* See specifications for required value and type
\# See Application Information for suggested value and type

Figure 26. Adding High-Frequency Bypass Capacitors To The Input and Output

π Filters

If a further reduction in ripple/noise level is required for an application, higher order filters must be used. A π (pi) filter, employing a ferrite bead (Fair-Rite Pt. No. 2673000701 or equivalent) in series with the input or output terminals of the regulator reduces the ripple/noise by at least 20 db (see Figure 27 and Figure 28). In order for the inductor to be effective in reduction of ripple and noise ceramic capacitors are required. (Note: see Capacitor Recommendations for the PTN78000W for addtional information on vendors and component suggestions.)

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency (650 kHz - 1 MHz). The placement of this filter is critical. It must be located as close as possible to the input or output pins to be efffective. The ferrite bead is small (12,5 mm × 3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite also manufactures a surface-mount bead (Pt. No. 2773021447), through hole (Pt. No. 2673000701) rated to 5 A, but in this application, it is effective to 5 A on the output bus. Inductors in the range of 1 µH to 5 µH can be used in place of the ferrite inductor bead.



* See specifications for required value and type.
# See the Application Information for suggested value and type.
† Recommended whenever I_O is greater than 2 A.

Figure 27. Adding π Filters ($I_O \leq$ 3 A)

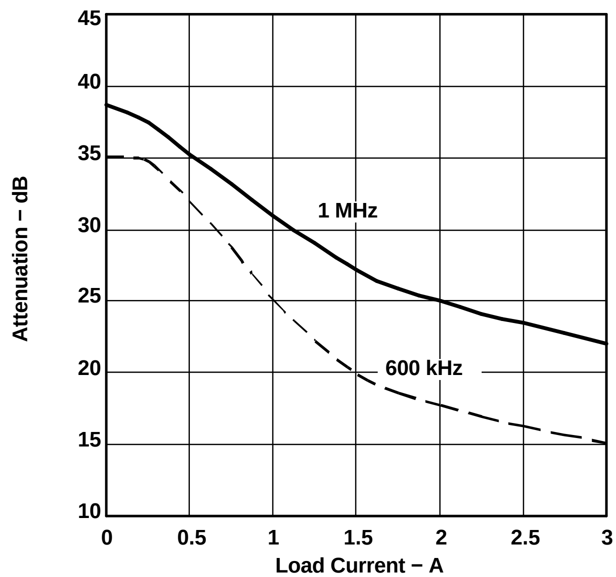
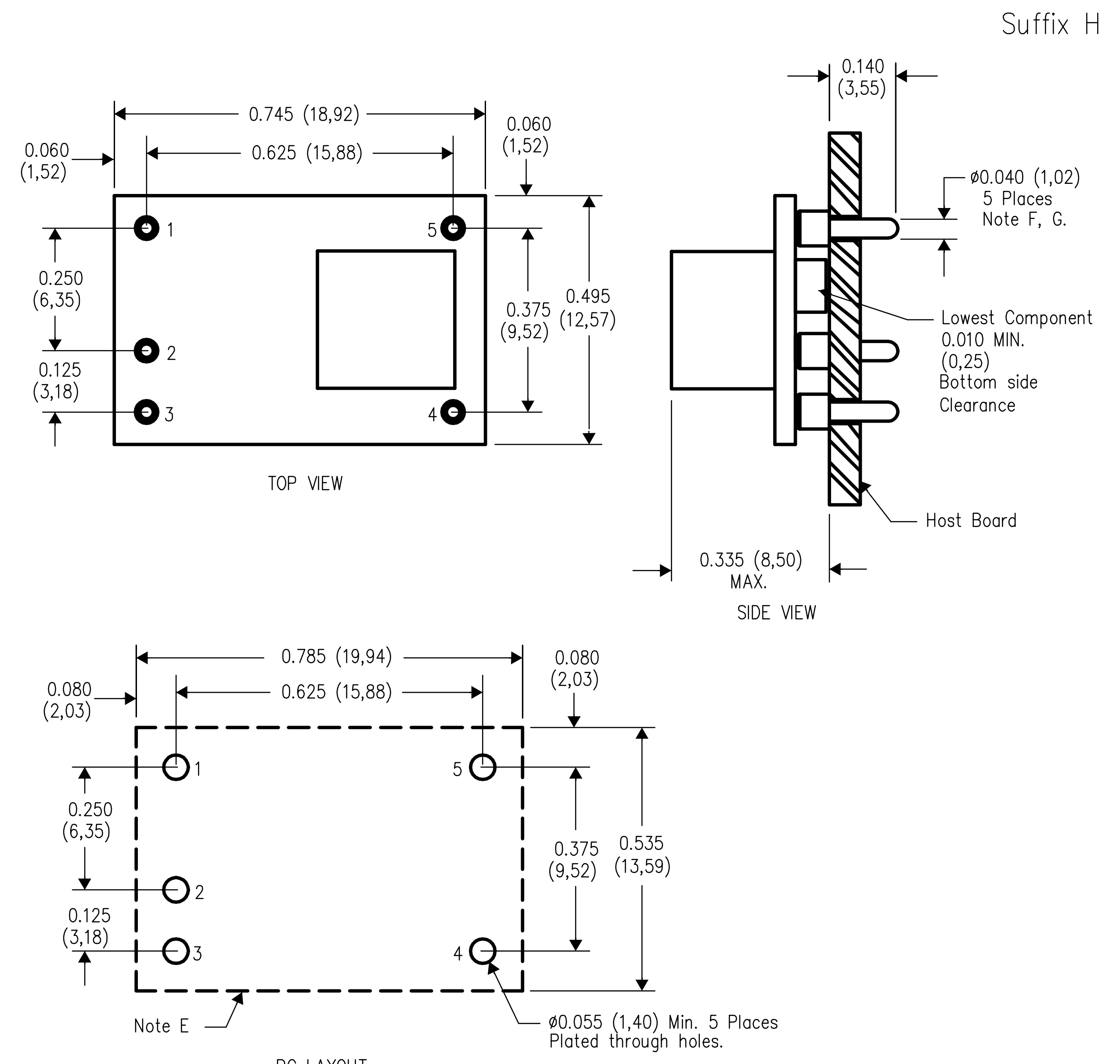


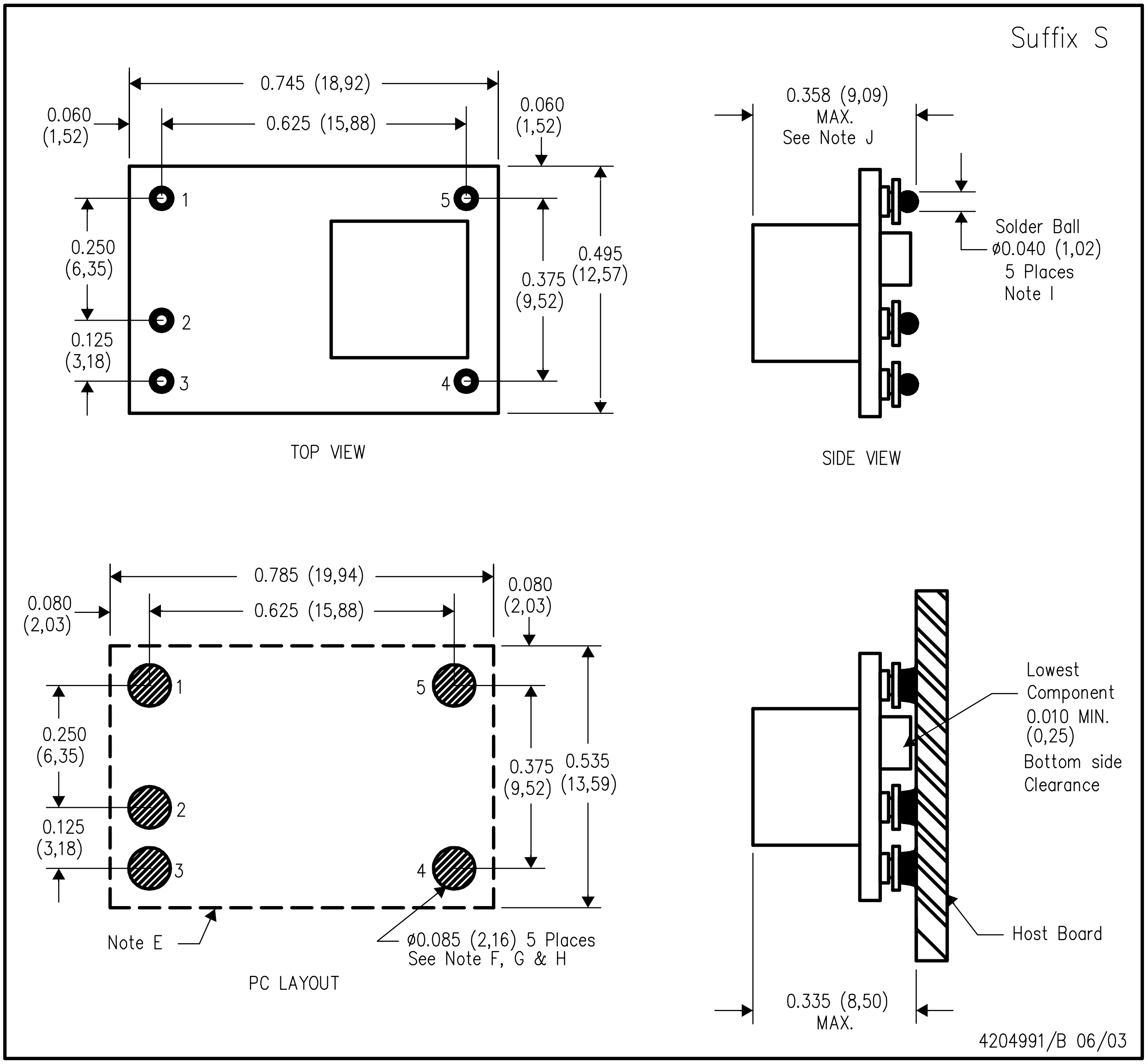
Figure 28. π-Filter Attenuation vs. Load Current



4204990/B 06/03

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EUT (R–PDSS–B5) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265