Rockwell

R6545/R6545E
CRT Controller (CRTC)

DESCRIPTION

The R6545/R6545E CRT Controller (CRTC) interfaces an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500, R6500/* and R65C00 microprocessor, microcomputer and peripheral device products.

The R6545 and R6545E devices differ only in the character clock frequency (CCLK) specifications. The maximum CCLK frequency is 2.5 MHz for the R6545 and 3.7 MHz for the R6545E. Throughout this document, the nomenclature R6545 applies to both devices, unless specified otherwise.

The R6545 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input (CCLK). Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows noninterlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

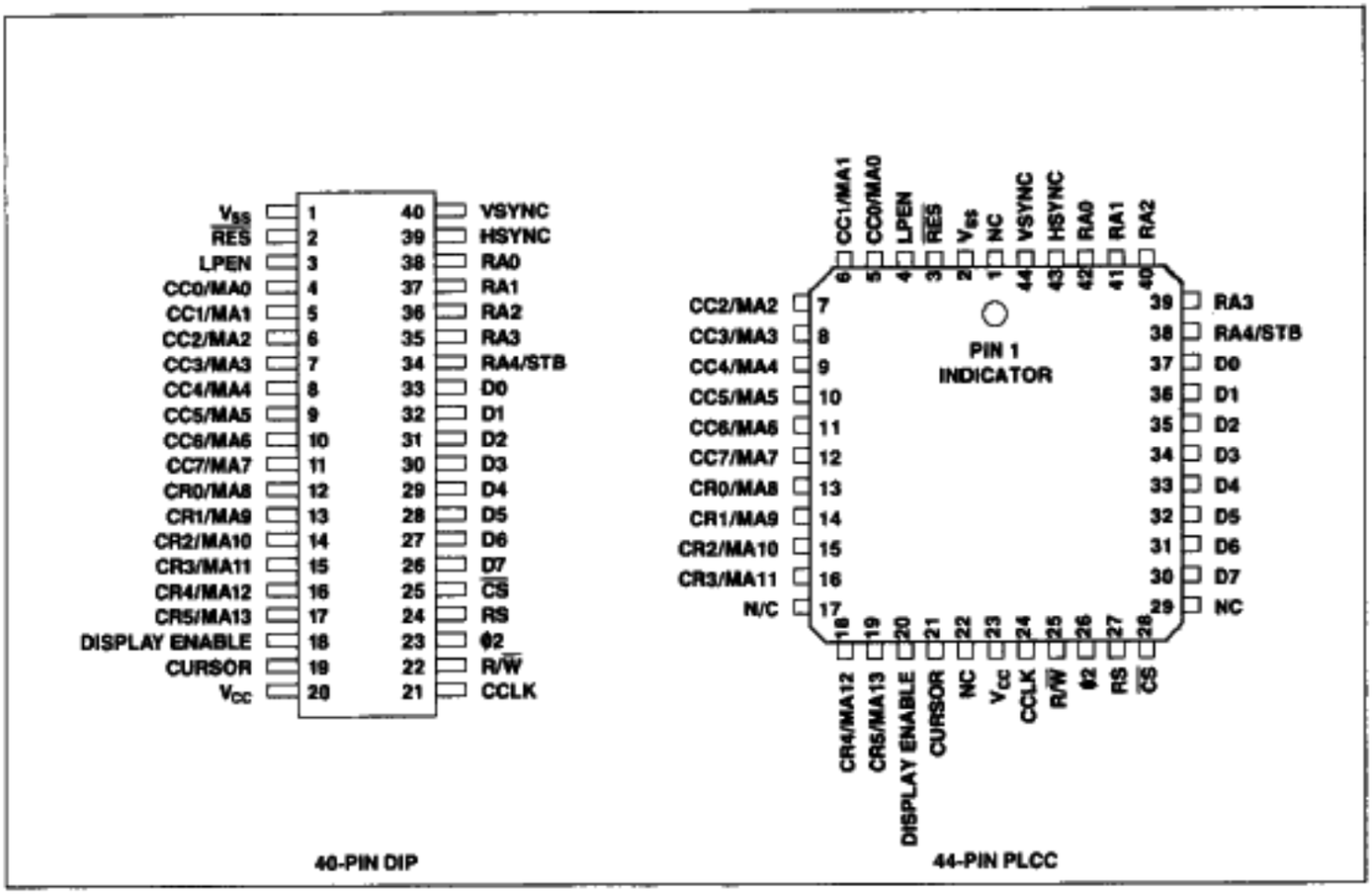
FEATURES

- Compatible with 8-bit microprocessors
- 3.7 MHz character clock operation (R6545E)
- 2.5 MHz character clock operation (R6545)
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable vertical sync width
- Fully programmable display (rows, columns, character matrix)
- Video display RAM may be configured as part of microprocessor memory field or independently slaved to R6545 (Transparent Addressing)
- Interlaced or non-interlaced scan
- 50/60 Hz refresh rate
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-pin ceramic or plastic DIP
- Pin-compatible with MC6845R
- Single +5 ±5% Vdc power supply

ORDERING INFORMATION

Part Number:
R6545

- Operating Temperature (T_L to T_H)
  - No Letters = 0°C to 70°C
  - E = −40°C to 85°C
- Package
  - P = 40-Pin Plastic DIP
  - C = 40-Pin Ceramic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)
- Operating Frequency (Bus)
  - No Letter = 1 MHz
  - A = 2 MHz
- Character Clock Frequency (CCLK)
  - No Letter = 2.5 MHz
  - E = 3.7 MHz



R6545/R6545E Pin Configuration

INTERFACE SIGNAL DESCRIPTION

Figure 1 illustrates the interface between the CPU, the R6545, and the video circuitry. Figure 2 shows typical timing waveforms at the video interface.

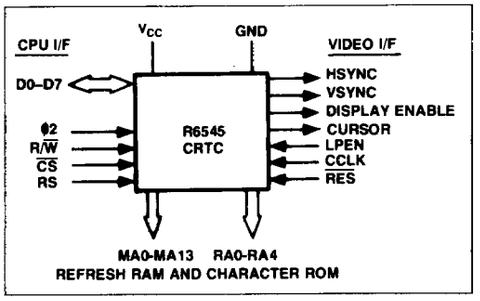


Figure 1. R6545 Interface Diagram

CPU INTERFACE

ϕ2 (Phase 2 Clock)

The Phase 2 (ϕ2) input clock triggers all data transfers between the system processor (CPU) and the R6545. Since there is no maximum limit to the allowable ϕ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545, a low on the R/$\overline{W}$ pin allows data on data lines D0–D7 to be written into the R6545.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545 is selected when CS is low. Then, data may be written to, or read from, the R6545 depending on the state of RS and R/$\overline{W}$.

RS (Register Select)

The Register Select input allows access to internal registers. A low on this pin permits writing (R/$\overline{W}$ = low) into the Address Register and reading (R/$\overline{W}$ = high) from the Status Register. The Address Register selects the register accessed when RS is high.

D0–D7 (Data Bus)

The eight data lines (D0–D7) transfer data between the processor and the R6545. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC active-high output signal determines the start of the horizontal raster line. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC active-high output signal determines the start of the vertical frame. Like HSYNC, VSYNC may drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE active-high output signal indicates when the R6545 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed one character time by setting bit 4 of R8 to a 1.

CURSOR (Cursor Coincidence)

The CURSOR active-high output signal indicates when the scan coincides with the programmed cursor position. The cursor position is programmable to any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the cursor start scan line and end scan line are both programmable. The cursor output may be delayed by one character time by setting Bit 5 of R8 to a 1.

LPEN (Light Pen Strobe)

The LPEN edge-sensitive input signal loads the internal Light Pen Register. A low-to-high transition activates LPEN.

CCLK (Clock)

The CCLK character timing clock input signal is the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ active-low input signal initializes all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters stop and clear and all scan and video outputs go low; control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing initiates when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can synchronize display frame timing with line frequency. $\overline{RES}$ may also synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 active-high output signals address the refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = 0), characters are stored in successive memory locations. Thus, the software design must translate row and column character coordinates into sequentially-numbered addresses for Refresh memory operations.

In the row/column mode (R8, Mode Control, bit 2 = 1), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row address CR0-CR5. In this case, the software manipulates characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

RA0-RA4 (Raster Address Lines)

These five active-high output signals select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the R6545 is programmed to operate in the "Transparent Address Mode." In this case the strobe is an active-high output and is true at the time the Refresh RAM updates address gates on to the address lines, MA0-MA13. In this way, updates and readouts of the Refresh RAM can be made under control of the R6545 with only a small amount of external circuitry.

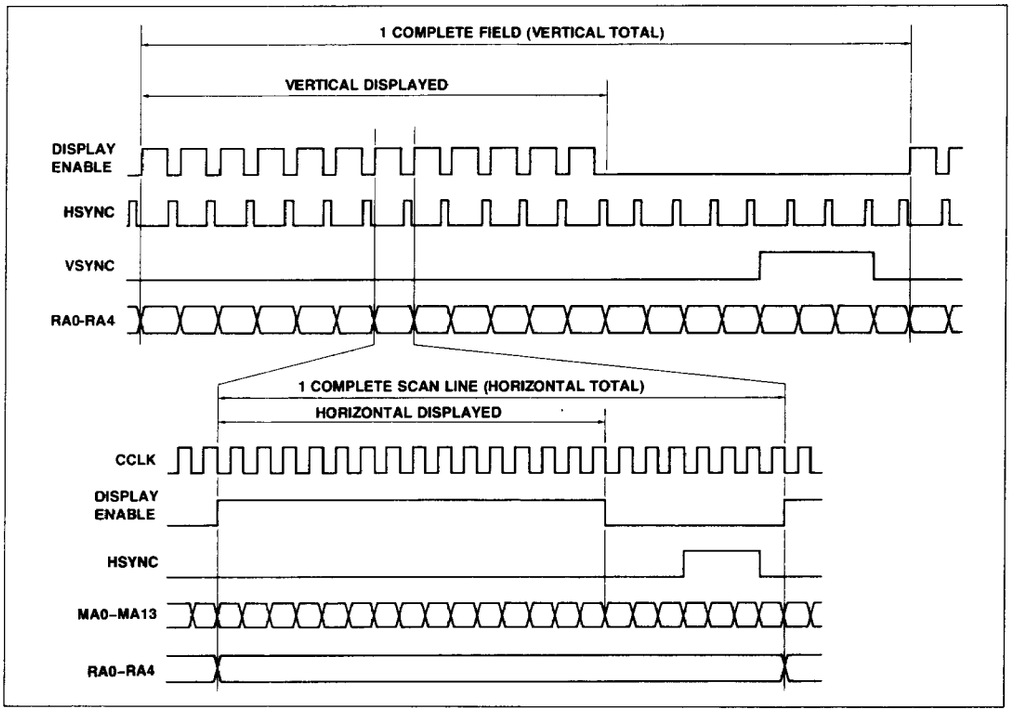


Figure 2. Vertical and Horizontal Timing

INTERNAL REGISTER DESCRIPTION

Table 1 summarizes the internal registers and indicates their address selection and read/write capabilities.

ADDRESS REGISTER

7	6	5	4	3	2	1	0
—	—	—	A_4	A_3	A_2	A_1	A_0

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. It contains the number of the desired register (0–31). When RS is low, this register may be loaded; when RS is high, the selected register is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

7	6	5	4	3	2	1	0
UR	LRF	VRT	—	—	—	—	—

This 3-bit register contains the status of the CRTC.

SR 7 UR —Update Ready

0 Register R31 has been either read or written by the CPU.

1 An update strobe has occurred.

SR 6 LRF —LPEN Register Full

0 Register R16 or R17 has been read by the CPU.

1 LPEN strobe has been received.

SR 5 VRT —Vertical Re-Trace

0 Scan is not currently in the vertical re-trace time.

1 Scan is currently in its vertical re-trace time.

NOTE: This bit goes to a 1 when vertical re-trace starts. It goes to a 0 five character clock times before vertical re-trace ends to ensure that critical timings for refresh RAM operations are met.

SR 4–0 —Not used.

Table 1. Internal Register Summary

		Address Reg.					Reg.						Register Bit							
$\overline{CS}$	RS	4	3	2	1	0	No.	Register Name	Stored Info.	RD	WR	7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—												
0	0	—	—	—	—	—	—	Address Reg.	Reg. No.		✓				A_4	A_3	A_2	A_1	A_0
0	0	—	—	—	—	—	—	Status Reg.		✓		UR	LRF	VRT					
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac. – 1		✓	•	•	•	•	•	•	•	•
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		✓	•	•	•	•	•	•	•	•
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		✓	•	•	•	•	•	•	•	•
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char. Times		✓	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	# Charac. Row – 1		✓		•	•	•	•	•	•	•
0	1	0	0	1	0	1	R5	Vert. Total Adjust	# Scan Lines		✓				•	•	•	•	•
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		✓		•	•	•	•	•	•	•
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		✓		•	•	•	•	•	•	•
0	1	0	1	0	0	0	R8	Mode Control			✓	UM	US	CSK	DES	RRA	RAD	IMC	
0	1	0	1	0	0	1	R9	Scan Lines	# Scan Lines – 1		✓				•	•	•	•	•
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		✓		B_1	B_0	•	•	•	•	•
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		✓				•	•	•	•	•
0	1	0	1	1	0	0	R12	Display Start Addr (H)			✓			•	•	•	•	•	•
0	1	0	1	1	0	1	R13	Display Start Addr (L)			✓	•	•	•	•	•	•	•	•
0	1	0	1	1	1	0	R14	Cursor Position (H)		✓	✓			•	•	•	•	•	•
0	1	0	1	1	1	1	R15	Cursor Position (L)		✓	✓	•	•	•	•	•	•	•	•
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		✓				•	•	•	•	•	•
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		✓		•	•	•	•	•	•	•	•
0	1	1	0	0	1	0	R18	Update Address Reg (H)			✓			•	•	•	•	•	•
0	1	1	0	0	1	1	R19	Update Address Reg (L)			✓	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: • Designates used bit in register

Designates unused bit in register. Reading this bit is always 0, except for R31, which does not drive the data bus.

R0—HORIZONTAL TOTAL CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS – 1							

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. This register determines the frequency of HSYNC.

R1—HORIZONTAL DISPLAYED CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS							

This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

7	6	5	4	3	2	1	0
HORIZONTAL SYNC POSITION							

This 8-bit write-only register contains the position of HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

7	6	5	4	3	2	1	0
V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0

This 8-bit write-only register contains the widths of both HSYNC and VSYNC as follows:

HVSW
7–4 VSYNC Pulse Width
The width of the vertical sync pulse (VSYNC) expressed as the number of scan lines. When bits 4–7 are all 0, VSYNC is 16 scan lines wide.

HVSW
3–0 HSYNC Pulse Width
The width of the horizontal sync pulse (HSYNC) expressed as the number of character clock times (CCLK). When bits 0–3 are all zero, HSYNC is 16 bit times wide.

Control of these parameters allows the R6545 to interface with a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

7	6	5	4	3	2	1	0
—	NO. OF CHAR. ROWS – 1						

The 7-bit Vertical Total Register contains the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES				

The 5-bit write-only Vertical Total Line Adjust Register (R5) contains the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

7	6	5	4	3	2	1	0
—	DISPLAYED CHAR. ROWS						

This 7-bit write-only register contains the number of displayed character rows in each frame. This determines the vertical size of the displayed text.

R7—VERTICAL SYNC POSITION

7	6	5	4	3	2	1	0
—	VERTICAL POSITION						

This 7-bit write-only register selects the character row time at which the vertical SYNC pulse occurs and, thus, positions the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

7	6	5	4	3	2	1	0
UM(T)	US(T)	CSK	DES	RRA	RAD	IMC	

This 8-bit write-only register selects the operating modes of the R6545, as follows:

MC
7 UM(T)—Update/Read Mode (Transparent Mode)
0 Update occurs during horizontal and vertical blanking times with update strobe.
1 Update interleaves during Ø2 portion of cycle.

MC
6 US(T)—Update Strobe (Transparent Mode)
0 Pin 34 functions as memory address (RA4).
1 Pin 34 functions as update strobe (STB).

MC
5 CSK —Cursor Skew
0 No delay.
1 Delays Cursor one character time.

MC
4 DES —Display Enable Skew
0 No delay.
1 Display Enable delays one character time.

MC 3	RRA —Refresh RAM Access
0	Shared memory access
1	Transparent memory access

MC 2	RAD —Refresh RAM Addressing Mode
0	Straight binary addressing
1	Row/column addressing

MC1-MC0 IMC —Interlace Mode Control

MC 1	MC 0	Operation
X	0	Non-interlace
0	1	Interlace SYNC raster scan
1	1	Interlace SYNC and video raster scan

R9—ROW SCAN LINES

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES −1				

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE

7	6	5	4	3	2	1	0
—	B_1	B_0	START SCAN LINE				

R11—CURSOR END LINE

7	6	5	4	3	2	1	0
—	—	—	END SCAN LINE				

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

B_1	B_0	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor
1	0	Blink cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

R12—DISPLAY START ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	DISPLAY START ADDRESS HIGH					

R13—DISPLAY START ADDRESS LOW

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS LOW							

These registers together form a 14-bit register whose contents are the memory address of the first character to be displayed (the character on the top left of the video display, as in Figure 4). Subsequent memory addresses are generated by the R6545 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address of the first character of the first line of text to be displayed. Entire pages of text may be scrolled or changed as well via R12 and R13.

R14—CURSOR POSITION HIGH

7	6	5	4	3	2	1	0
—	—	CURSOR POSITION HIGH					

R15—CURSOR POSITION LOW

7	6	5	4	3	2	1	0
CURSOR POSITION LOW							

These registers together form a 14-bit register whose contents are the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of several cursor options.

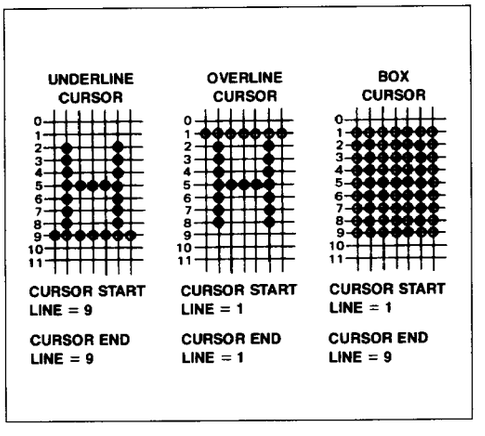


Figure 3. Cursor Display Scan Line Control Examples

R16—LIGHT PEN HIGH

7	6	5	4	3	2	1	0
—	—	LPEN HIGH					

R17—LIGHT PEN LOW

7	6	5	4	3	2	1	0
LPEN LOW							

These registers together form a 14-bit register whose contents are the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

R18—UPDATE ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	UPDATE ADDRESS HIGH					

R19—UPDATE ADDRESS LOW

7	6	5	4	3	2	1	0
UPDATE ADDRESS LOW							

These registers together comprise a 14-bit register whose contents are the memory address at which the next read or update will occur (for transparent address mode only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. The section on REFRESH RAM ADDRESSING describes this more fully.

R31—DUMMY LOCATION

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

This register does not store any data, but is required to detect transparent addressing updates. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = 0
(2) Row/Column, if register R8, bit 2 = 1. In this case the low byte is the Character Column and the high byte is the Character Row.

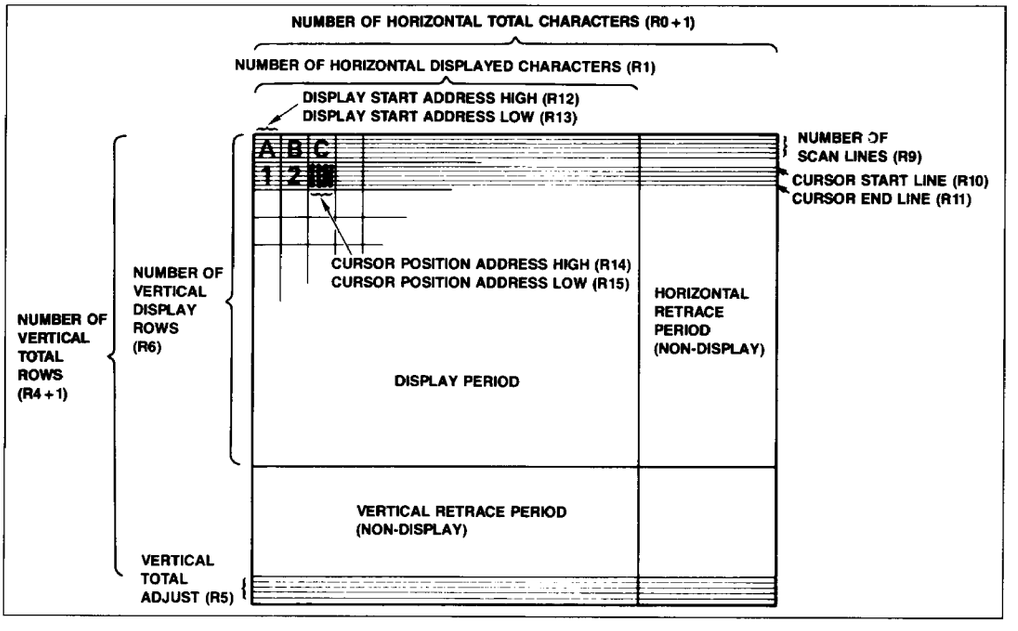


Figure 4. Video Display Format

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 4 indicates the relationship of the various program registers in the R6545 and the resulant video display.

Non-displayed areas of the Video Display are for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

There are two modes of addressing for the video display memory:

Shared Memory Mode (R8, BIT 3 = 0)

In this mode, the Refresh RAM address lines (MA0–MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided externally to the CRTC. In the Row/Column address mode, lines MA0–MA7 become character column addresses (CC0–CC7) and MA8–MA13 become character row addresses (CR0–CR5). Figure 5 illustrates the system configuration.

Transparent Memory Addressing (R8, BIT 3 = 1)

For this mode, the display RAM is not directly accessible by the CPU, but is controlled entirely by the R6545. All CPU accesses are made via the R6545 and a small amount of external circuitry. Figure 6 shows the system configuration for this approach.

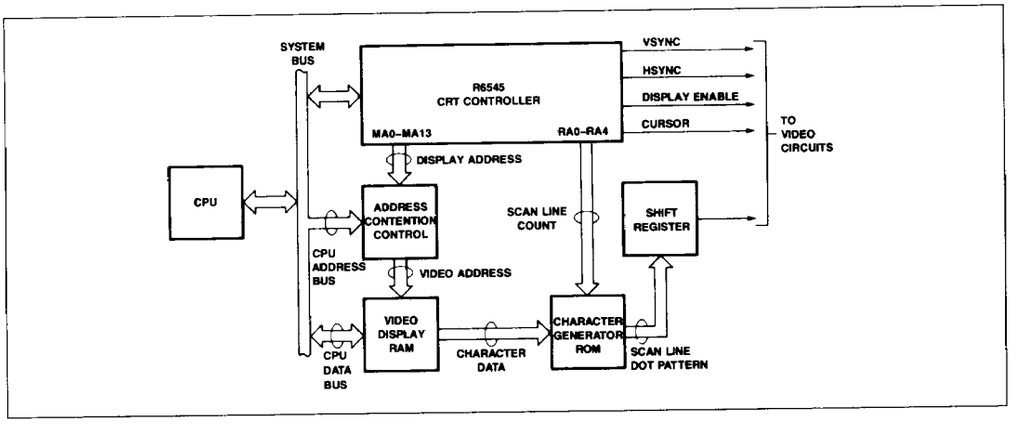


Figure 5. Shared Memory System Configuration

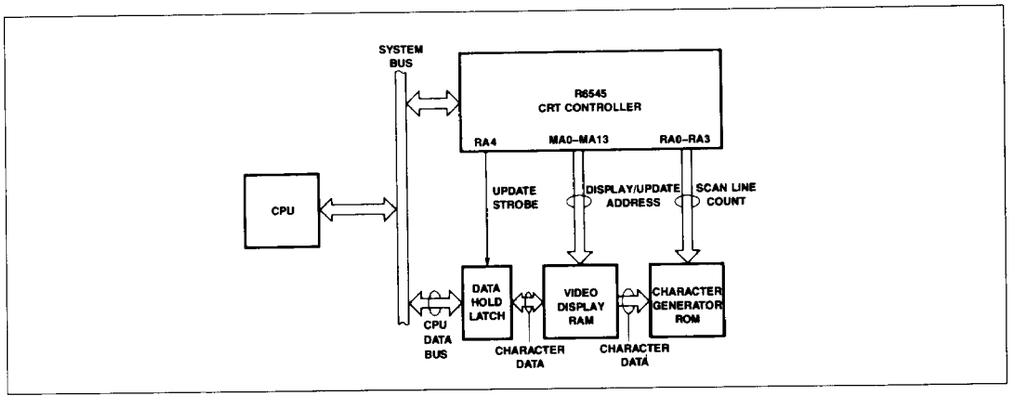


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch Needed for Horizontal/Vertical Blanking Updates, Only).

ADDRESSING MODES

Figure 7 illustrates the address sequence for both modes of the Refresh RAM address.

Row/Column

In this mode, the CRTC address lines (MA0–MA13) generate 8 column (MA0–MA7) and 6 row (MA8–MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM (register R8, bit 2 is a 1).

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity increases since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential (register R8, bit 2 is a 0).

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545 permits use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 7 illustrates Refresh RAM addressing for both row/column and binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

Note that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, gaps exist. This requires that the system be equipped with more memory than actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

The user selects whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column minimizes software requirements.

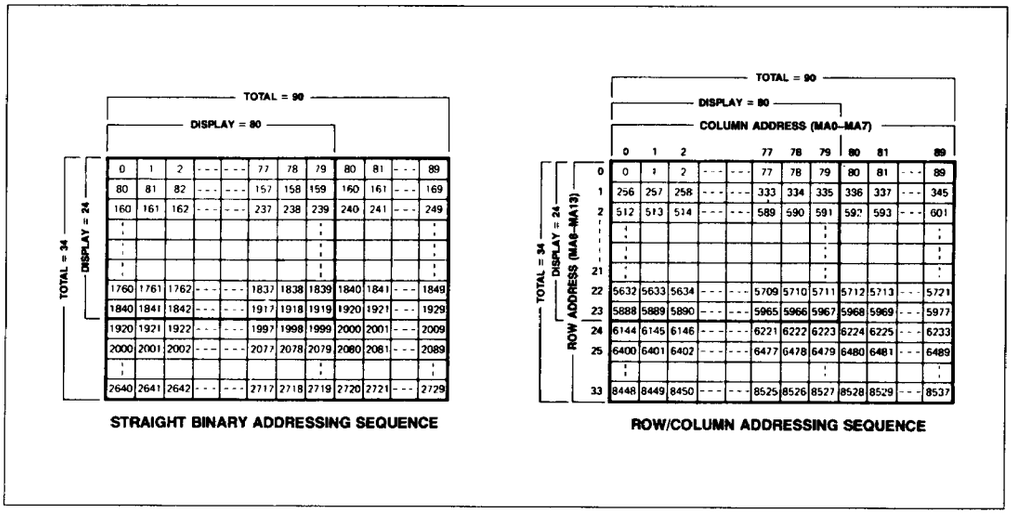


Figure 7. Display Address Sequences (with Start Address = 0) for 80 × 24 Example

MEMORY CONTENTION SCHEMES FOR SHARED MEMORY ADDRESSING

From the diagram of Figure 5, it is clear that both the R6545 and the system CPU must address the video display memory. The R6545 repetitively fetches character information to generate the video signals in order to keep the screen display active. The CPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- **CPU Priority**

  In this technique, the address lines to the video display memory are normally driven by the R6545 unless the CPU needs access, in which case the CPU addresses immediately override those from the R6545 giving the CPU immediate access.

- **ϕ1 and ϕ2 Memory Interleaving**

  This method permits both the R6545 and the CPU to access the video display memory by time-sharing. During the ϕ1 portion of each cycle (the time when ϕ2 is low), the R6545 address outputs are gated to the video display memory. During ϕ2 time, the CPU address lines are switched in. This way, both the R6545 and the CPU have unimpeded access to the memory. Figure 8 illustrates these timings.

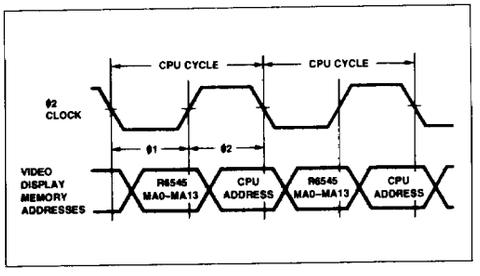


Figure 8. ϕ1 and ϕ2 Interleaving

- **Vertical Blanking**

  With this approach, the address circuitry is identical to the case for CPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the CPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a 1). In this way, no visible screen perturbations result. See Figure 10 for details.

TRANSPARENT MEMORY ADDRESSING

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the R6545. In effect, the contention is handled by the R6545. As a result, the schemes for accomplishing CPU memory access are different:

- **ϕ1 and ϕ2 Interleaving**

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the ϕ2 address is generated from the Update Address Register (R18 and R19) in the R6545. The CPU loads the address to be accessed into R18/R19. This address is then gated onto the MA lines during ϕ2. Figure 9 shows the timing.

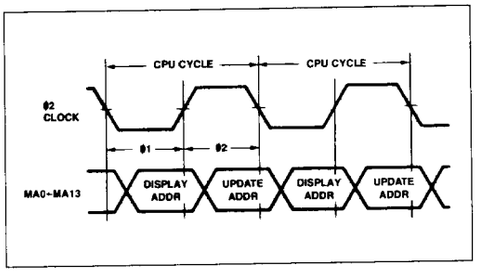


Figure 9. ϕ1 and ϕ2 Transparent Interleaving

- **Horizontal/Vertical Blanking**

  In this mode, the CPU loads the Update Address into R18 and R19. This address is gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. Pin 34 can be programmed, by R8 bit 6, to function as an update strobe which signals the presence of an update address on the MA lines. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system CPU is not halted waiting for the blanking time to arrive. Figure 11 illustrates the address and strobe timing for this mode.

CURSOR AND DISPLAY ENABLE SKEW CONTROL

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

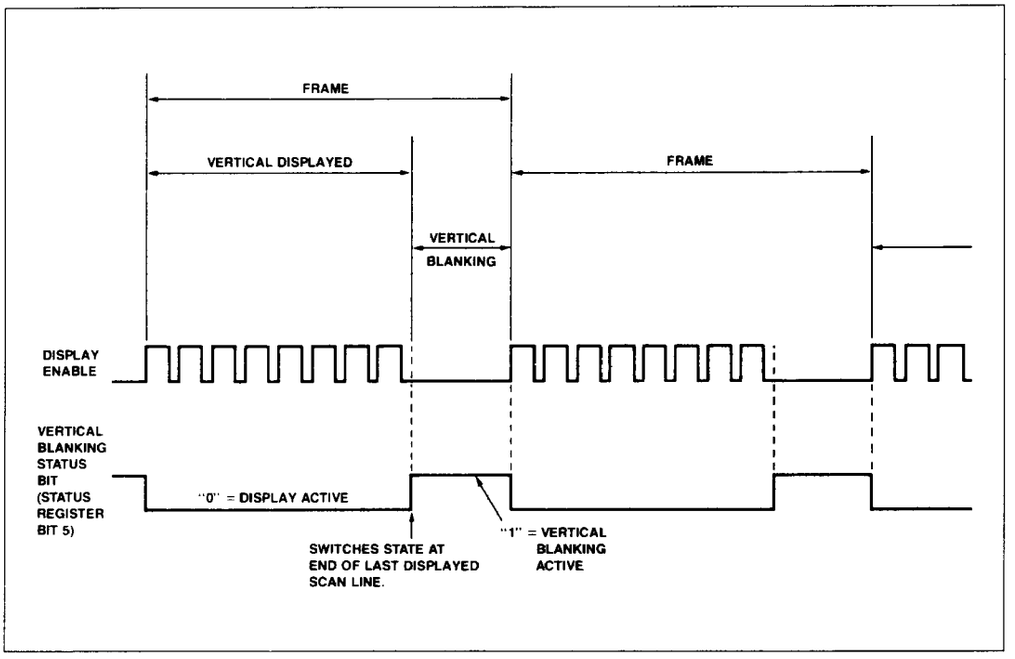


Figure 10. Operation of Vertical Blanking Status Bit

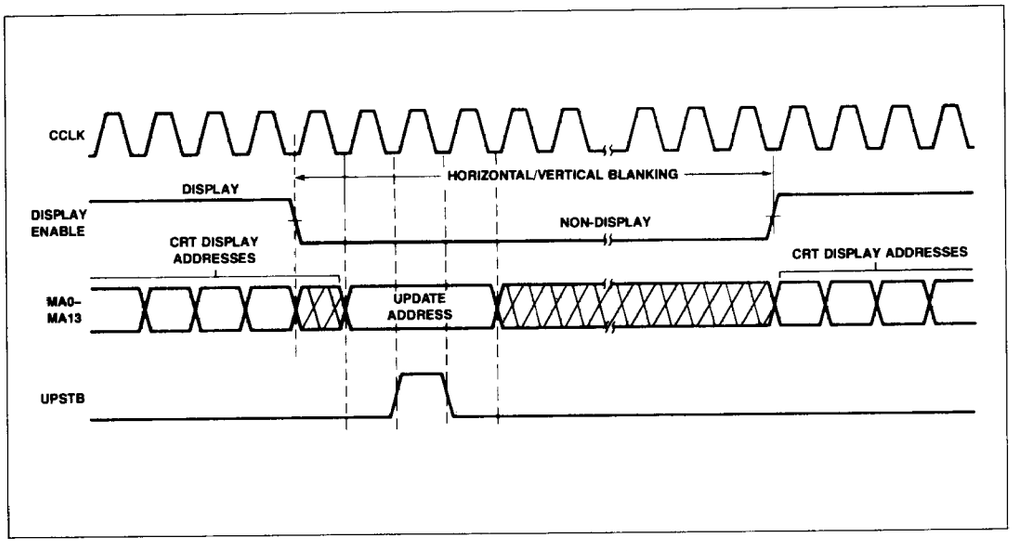


Figure 11. Retrace Update Timing

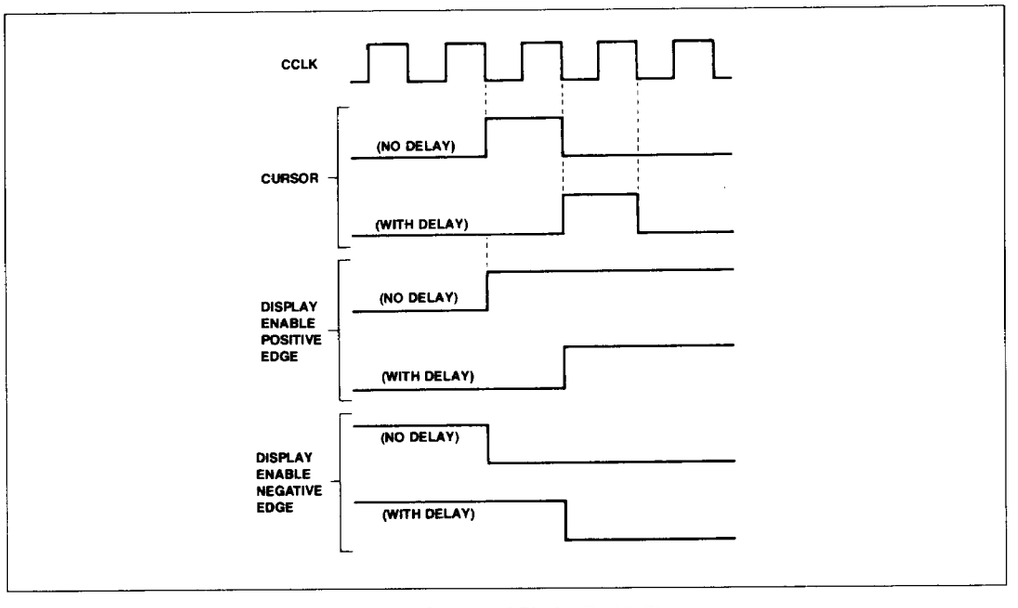


Figure 12. Cursor and Display Enable Skew

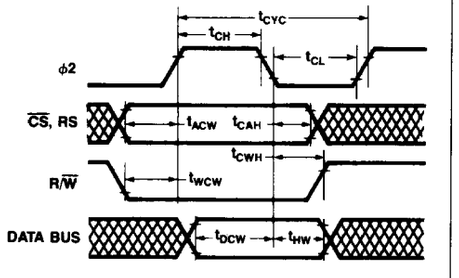
BUS WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_{CH}	Ø2 Pulse Width High	440	—	200	—	ns
t_{CL}	Ø2 Pulse Width Low	420	—	190	—	ns
t_{ACW}	Address Set-Up Time	80	—	40	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	80	—	40	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	165	—	60	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns
(t_R and t_F = 10 to 30 ns)						

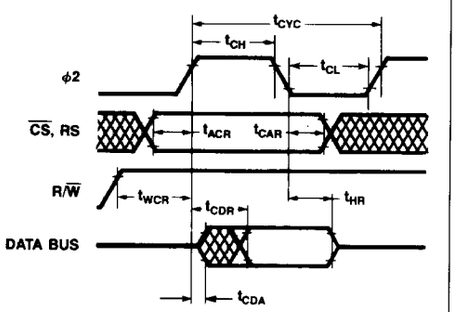
BUS READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_{CH}	Ø2 Pulse Width	440	—	200	—	ns
t_{CL}	Ø2 Pulse Width Low	420	—	190	—	ns
t_{ACR}	Address Set-Up Time	80	—	40	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	80	—	40	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	290	—	150	ns
t_{HR}	Read Hold Time	10	—	10	—	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	—	40	—	ns
(t_R and t_F = 10 to 30 ns)						

BUS WRITE TIMING WAVEFORMS



BUS READ TIMING WAVEFORMS

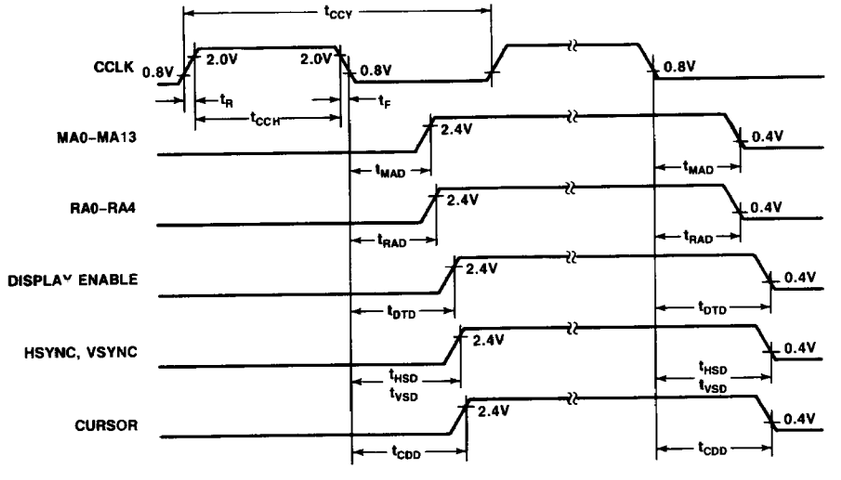


MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Parameter	R6545			R6545E			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CCH}	Minimum Clock Pulse Width, High	200			130			ns
t_{CCY}	Clock Frequency			2.5			3.7	MHz
t_R, t_F	Rise and Fall Time for Clock Input			20			20	ns
t_{MAD}	Memory Address Delay Time		180	300		100	160	ns
t_{RAD}	Raster Address Delay Time		180	300		100	160	ns
t_{DTD}	Display Timing Delay Time		240	450		160	300	ns
t_{HSD}	Horizontal Sync Delay Time		240	450		160	300	ns
t_{VSD}	Vertical Sync Delay Time		240	450		160	300	ns
t_{CDD}	Cursor Display Timing Delay Time		240	450		160	300	ns

MEMORY AND VIDEO INTERFACE WAVEFORMS



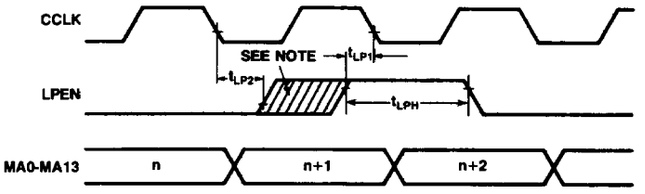
LIGHT PEN STROBE TIMING CHARACTERISTICS (For Reference Only)

Symbol	Characteristic	R6545		R6545A		Unit
		Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Hold Time	150	—	100	—	ns
t_{LP1}	LPEN Setup Time	—	120	—	120	ns
t_{LP2}	CCLK to LPEN Delay	—	0	—	0	ns

Note: t_R, t_F = 20 ns (max)

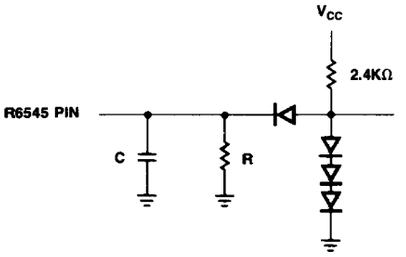
2

LIGHT PEN STROBE TIMING WAVEFORMS



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register.
t_{LP2} and t_{LP1} are time positions causing uncertain results.

TEST LOAD



R = 11KΩ FOR D0-D7
= 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D0-D7
= 30 pF ALL OTHER OUTPUTS

CRTC Register Comparison

REGISTER	MC6845R HD6845R	HD6845S	R6545-1	R6545/R6545E
GENERAL FUNCTIONS				
R0 HORIZONTAL TOT	TOT-1	TOT-1	TOT-1	TOT-1
R1 HORIZONAL DISP	ATUAL	ACTUAL	ACTUAL	ACTUAL
R2 HORIZONTAL SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R3 HORIZ AND VERT SYNC WIDTH	HORIZONTAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL
R4 VERTICAL TOT	TOT-1	TOT-1	TOT-1	TOT-1
R5 VERTICAL TOT ADJ	ANY VALUE	ANY VALUE	ANY VALUE EXCEPT R5 = R9H• X	ANY VALUE
R6 VERTICAL DISP	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4
R7 VERTICAL SYNC POS	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R8 MODE REG BITS 0 and 1	INTERLACE MODE SELECT	INTERLACE MODE SELECT	—	INTERLACE MODE SELECT
BITS 2	—	—	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING
BITS 3	—	—	SHARED OR TRANSPARENT ADDR	SHARED OR TRANSPARENT ADDR
BITS 4	—	DISPEN SKEW	DISPEN SKEW	DISPEN SKEW
BITS 5	—	DISPEN SKEW	CURSOR SKEW	CURSOR SKEW
BITS 6	—	CURSOR SKEW	RA4/UPSTB	RA4/UPSTB
BITS 7	—	CURSOR SKEW	TRANSPARENT MODE SELECT	TRANSPARENT MODE SELECT
R9 SCAN LINES	TOT-1	TOT-1	TOT-1	TOT-1
R10 CURSOR START	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R11 CURSOR END	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R12/R13 DISP ADDR	WRITE ONLY	READ/WRITE	WRITE ONLY	WRITE ONLY
R14/R15 CURSOR POS	WRITE ONLY	READ/WRITE	READ/WRITE	READ/WRITE
R16/R17 LPEN REG	READ ONLY	READ ONLY	READ ONLY	READ ONLY
R18/R19 UPDATE ADDR REG	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
R31 DUMMY REG	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
STATUS REG	NO	NO	YES	YES
INTERLACE SYNC				
R0	TOT-1 = ODD	TOT-1 = ODD	—	TOT-1 = ODD OR EVEN
R4 VERTICAL	TOT-1	TOT-2	—	TOT-1
R6 VERT DISP	TOT/2	TOT	—	TOT
R7 VERT SYNC	ACTUAL	ACTUAL	—	ACTUAL
R9 SCAN LINES	TOT-1 EVEN ONLY	TOT-2 ODD/EVEN	TOT-1 ODD/EVEN	TOT-1 ODD/EVEN
R10 CURSOR START R11 CURSOR END	BOTH ODD OR BOTH EVEN	ODD/EVEN ODD/EVEN	— —	ODD/EVEN ODD/EVEN
CHARACTER CLOCK FREQUENCY				
CCLK	2.5 MHz	3.7 MHz	2.5 MHz	3.7 MHz*

Notes: — = Does not apply

* R6545 = 2.5 MHz R6545E = 3.7 MHz

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

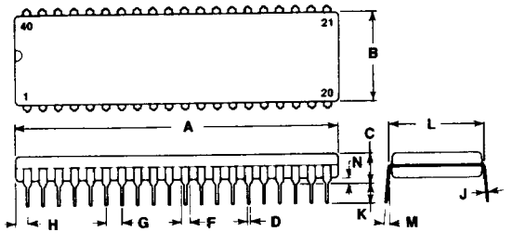
DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Ø2, R/W, RES, CS, RS, LPEN, CCLK	I_{IN}	—		2.5	µA	
Three-State Input Leakage D0–D7	I_{TSI}	—		±10.0	µA	V_{IN} = 0.4V to 2.4V
Output High Voltage D0–D7 All other outputs	V_{OH}	2.4		—	V	 I_{LOAD} = 205 µA I_{LOAD} = 100 µA
Output Low Voltage	V_{OL}	—		0.4	V	I_{LOAD} = 1.6 mA
Input Capacitance Ø2, R/W, RES, CS, RS, LPEN, CCLK D0–D7	C_{IN}	 — —		 10.0 12.5	pF	V_{IN} = 0V T_A = 25°C f = 1MHz
Output Capacitance	C_{OUT}	—		10.0	pF	
Power Dissipation Commercial Industrial	P_D	—	 350 350	 700 800	mW	V_{CC} = 5.25V

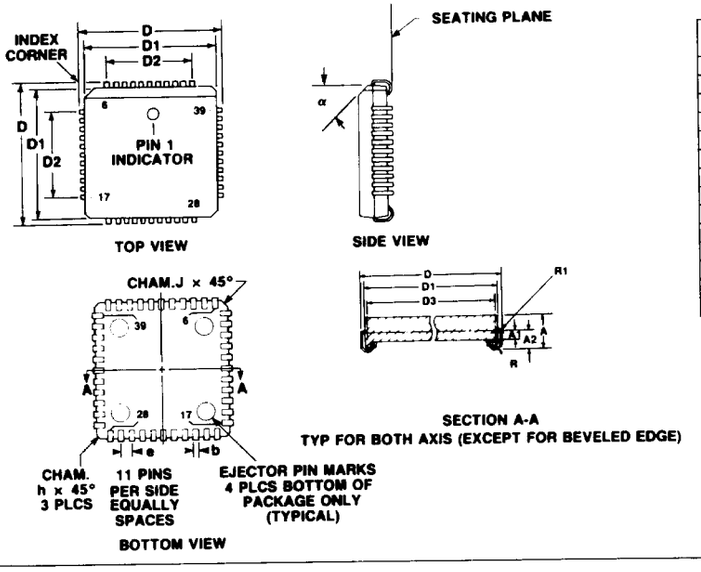
PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.06	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	