FAIRCHILD
SEMICONDUCTOR ™

RC5054A

Programmable Synchronous DC-DC Converter Controller for Low Voltage Microprocessors

Features

- Drives Two N-Channel MOSFETs
- Operates from +5V Power Input
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- Excellent Output Voltage Regulation
- TTL Compatible 5 Bit Digital-to-Analog Output Voltage Selection
  - Wide Range - $1.3V_{DC}$ to $3.5V_{DC}$
  - 0.1V Binary Steps from $2.1V_{DC}$ to $3.5V_{DC}$
  - 0.05V Binary Steps from $1.3V_{DC}$ to $2.1V_{DC}$
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
  - Does Not Require Extra Current Sensing Element, Uses MOSFET's $R_{DS(ON)}$
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator Programmable from 50kHz to 1MHz

Applications

- Power Supply for Pentium®, Pentium Pro, PowerPC™ and Alpha™ Microprocessors
- High-Power 5V to 3.xV DC-DC Regulators
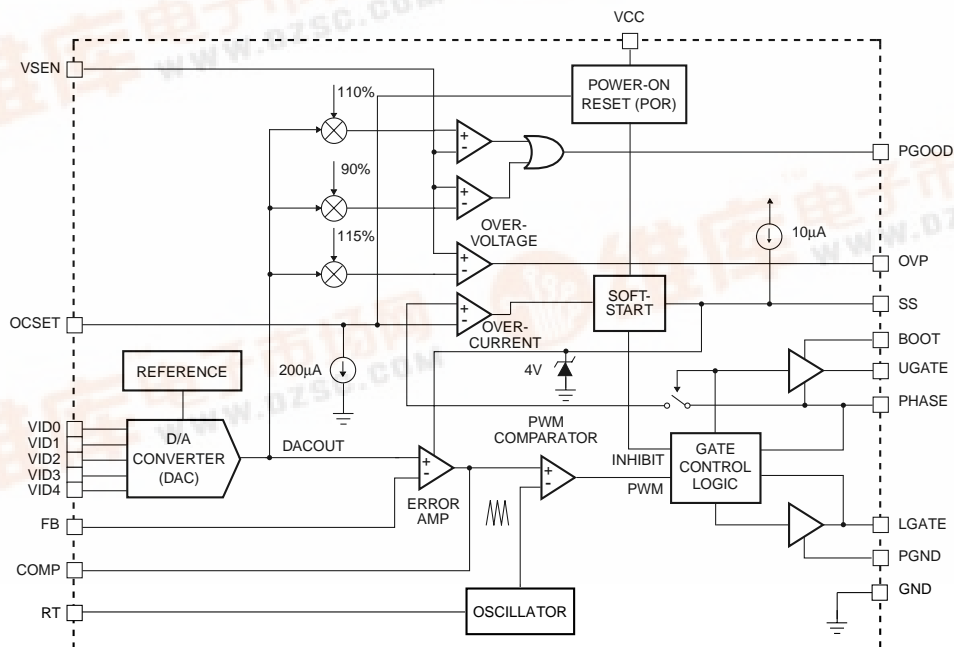- Low-Voltage Distributed Power Supplies

Description

The RC5054A provides complete control and protection for a DC-DC converter optimized for high-performance micro-processor applications. It is designed to drive two N-Channel MOSFETs in a synchronous-rectified buck topology. The RC5054A integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The output voltage of the converter is easily adjusted and precisely regulated. The RC5054A includes a 5-input digital-to-analog converter (DAC) that adjusts the output voltage from $2.1V_{DC}$ to $3.5V_{DC}$ in 0.1V increments and from $1.3V_{DC}$ to $2.1V_{DC}$ in 0.05V steps.

The RC5054A provides simple, single feedback loop, volt-

Block Diagram

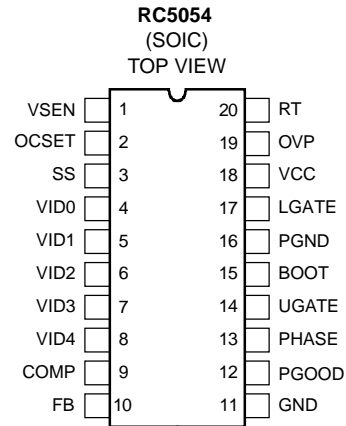Alpha is a trademark of Digital Equipment Corporation. Pentium is a registered trademark of Intel Corporation. PowerPC is a trademark of IBM.

age-mode control with fast transient response. It includes a 200KHz free-running triangle-wave oscillator that is adjustable from 50KHz to 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 6V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0% to 100%.

The RC5054A monitors the output voltage with a window comparator that tracks the DAC output and issues a Power Good signal when the output is within ±10%. The RC5054A protects against over-current conditions by inhibiting PWM operation. Built-in over-voltage protection triggers an external SCR to crowbar the input supply. The RC5054A monitors the current by using the $R_{DS(ON)}$ of the upper MOSFET which eliminates the need for a current sensing resistor.

Pin Assignments

RC5054
(SOIC)
TOP VIEW

VSEN	1	20	RT
OCSET	2	19	OVP
SS	3	18	VCC
VID0	4	17	LGATE
VID1	5	16	PGND
VID2	6	15	BOOT
VID3	7	14	UGATE
VID4	8	13	PHASE
COMP	9	12	PGOOD
FB	10	11	GND

Pin Definitions

Pin Number	Pin Names	Pin Function Description
1	VSEN	This pin is connected to the converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.
2	OCSET	Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 200μA current source (I_{OCS}), and the upper MOSFET on-resistance ($R_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation: $$I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{R_{DS(ON)}}$$ An over-current trip cycles the soft-start function.
3	SS	Connect a capacitor from this pin to ground. This capacitor, along with an internal 10μA current source, sets the soft-start interval of the converter.
4-8	VID0-VID4	VID0-4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage. It also sets the PGOOD and OVP thresholds. Table 1 specifies DACOUT for the 32 combinations of DAC inputs.
9	COMP	COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.
10	FB	
11	GND	Signal ground for the IC. All voltage levels are measured with respect to this pin.
12	PGOOD	PGOOD is an open collector output used to indicate the status of the converter output voltage. This pin is pulled low when the converter output is not within ±10% of the DACOUT reference voltage.
13	PHASE	Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.
14	UGATE	Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.
15	BOOT	This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.
16	PGND	This is the power ground connection. Tie the lower MOSFET source to this pin.

Pin Definitions (continued)

Pin Number	Pin Names	Pin Function Description
17	LGATE	Connect LGATE to the lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.
18	VCC	Provide a 12V bias supply for the chip to this pin.
19	OVP	The OVP pin can be used to drive an external SCR in the event of an overvoltage condition.
20	RT	This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200KHz switching frequency is increased according to the following equation: $$F_S = 200\text{kHz} + \frac{3.5 \times 10^6 [\text{KHz x Kohm}]}{R_T [\text{Kohm}]} \qquad (R_T \text{ to GND})$$ Conversely, connecting a pull-up resistor (RT) from this pin to VCC reduces the switching frequency according to the following equation: $$F_S = 200\text{kHz} - \frac{3 \times 10^5 [\text{KHz x Kohm}]}{R_T [\text{Kohm}]} \qquad (R_T \text{ to 12V})$$

Absolute Maximum Ratings

	Min.	Max.
Power Input Voltage, V_{IN}		6V
Supply Voltage, V_{CC}		+13.5V
Boot Voltage, V_{BOOT} - V_{PHASE}		+13.5V
V_{CC} or I/O Voltage	GND -0.3V	V_{CC} + 0.3V
ESD Classification		Class 2

Recommended Operating Conditions

	Min.	Max.
Supply Voltage, V_{CC}	+12V -10%	+12V +10%
Ambient Temperature Range	0°C	70°C
Junction Temperature Range	0°C	125°C

Thermal Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance[1] θ_{JA} SOIC Package SOIC Package	 With 3in[2] of Copper		 110 86		 °C/W °C/W
Maximum Junction Temperature	Plastic Package			150	°C
Maximum Storage Temperature Range		-65		150	°C
Maximum Lead Temperature	Soldering 10s			300	°C

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications (Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VCC Supply Current						
I_{CC}	Nominal Supply	UGATE and LGATE Open	–	22	–	mA
	Power-On Reset					
	Rising VCC Threshold	V_{OCSET} = 4.5V	–	–	10.4	V
	Falling VCC Threshold	V_{OCSET} = 4.5V	8.8	–	–	V
	Rising V_{OCSET} Threshold		–	1.26	–	V
Oscillator						
	Free Running Frequency	RT = OPEN	185	200	215	KHz
ΔV_{OSC}	Ramp Amplitude	RT = Open	–	1.9	–	V_{P-P}
Reference and DAC						
	Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.000V	1.980	2.000	2.020	V
		V_{OUT} = 1.550V	1.534	1.550	1.566	V
Error Amplifier						
	DC Gain		–	88	–	dB
GBW	Gain-Bandwidth Product		–	15	–	MHz
SR	Slew Rate	COMP = 10pF	–	6	–	V/µs
Gate Drivers						
I_{UGATE}	Upper Gate Source	V_{BOOT} - V_{PHASE} = 12V	350	500	–	mA
I_{UGATE}	Upper Gate Sink	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
I_{LGATE}	Lower Gate Source	V_{CC} = 12V, V_{LGATE} = 6V	300	450	–	mA
I_{LGATE}	Lower Gate Sink	V_{UGATE} - V_{PHASE} = 1V	–	100	–	mA
Protection						
	Over-Voltage Trip (V_{SEN}/DACOUT)		–	115	120	%
I_{OCSET}	OCSET Current Source	V_{OCSET} = 4.5VDC	170	200	230	µA
I_{OVP}	OVP Sourcing Current	V_{SEN} = 5.5V, V_{OVP} = 0V	60	–	–	mA
I_{SS}	Soft Start Current		–	10	–	µA
Power Good						
	Upper Threshold (V_{SEN}/DACOUT)	VSEN Rising	106	–	111	%
	Lower Threshold (V_{SEN}/DACOUT)	VSEN Falling	89	–	94	%
	Hysteresis (V_{SEN}/DACOUT)	Upper and Lower Threshold	–	2	–	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -5mA	–	0.5	–	V

Functional Description

Initialization

The RC5054A automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias volt-age at the V_{CC} pin and the input voltage (V_{IN}) on the OCSET pin. The level on OCSET is equal to V_{IN} less a fixed voltage drop (see over-current protection). The POR function initiates soft start operation after both input supply voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{CC} are equivalent and the +12V power source must exceed the rising V_{CC} threshold before POR initiates operation.

Soft Start

The POR function initiates the soft start sequence. An internal 10μA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. Soft start clamps the error amplifier output (COMP pin) and reference input (+ terminal of error amp) to the SS pin voltage. Figure 1 shows the soft start interval with C_{SS} = 0.1μF. Initially the clamp on the error amplifier (COMP pin) controls the converter's output voltage. At t_1 in Figure 1, the SS voltage reaches the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to t_2. With sufficient output voltage, the clamp on the reference input controls the output voltage. This is the interval between t_2 and t_3 in Figure 1. At t_3 the SS voltage exceeds the DACOUT voltage and the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The PGOOD signal toggles 'high' when the output voltage (VSEN pin) is within ±5% of DACOUT. The 2% hysteresis built into the power good comparators prevents PGOOD oscillation due to nominal output voltage ripple.
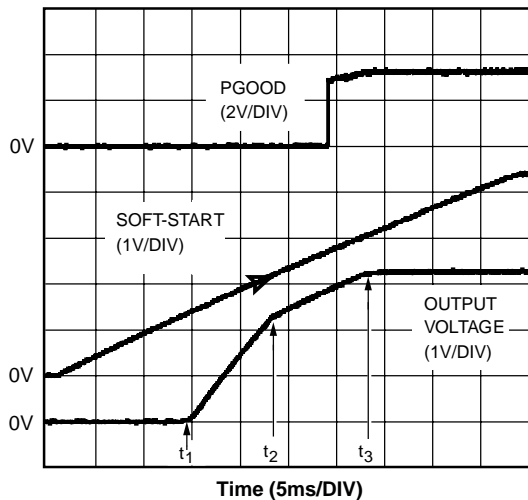

Figure 1. Soft Start Interval

Over-Current Protection

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the over-current trip level. An internal 200μA current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET}, the over-current function initiates a soft-start sequence. The soft-start function discharges C_{SS} with a 10μA current sink and inhibits PWM operation. The soft-start function recharges C_{SS}, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C_{SS}, the soft start function inhibits PWM operation while fully charging C_{SS} to 4V to complete its cycle. Figure 2 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the CSS charging interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 2 is 2.5W.

The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

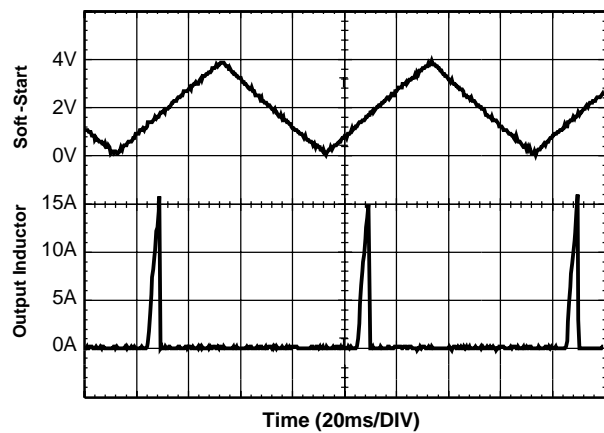$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{R_{DS(ON)}}$$

Figure 2. Over-Current Operation

where I_{OCSET} is the internal OCSET current source (200μA typical). The OC trip point varies mainly due to the MOSFET's $R_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

- The maximum $R_{DS(ON)}$ at the highest junction temperature.
- The minimum I_{OCSET} from the specification table.
- Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection.'

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Output Voltage Program

The output voltage of a RC5054A converter is programmed to discrete levels between $1.3V_{DC}$ and $3.5V_{DC}$. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a 5-bit digital-to-analog converter

(DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the 32 combinations of open or short connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection.

Grounding any combination of the VID pins increases the DACOUT voltage.

Table 1. Output Voltage Table

PIN NAME					NOMINAL OUTPUT VOLTAGE	PIN NAME					NOMINAL OUTPUT VOLTAGE
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	SHDN
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

Note:

1. 0 = connected to GND or V_{SS}, 1 = OPEN

Typical Application
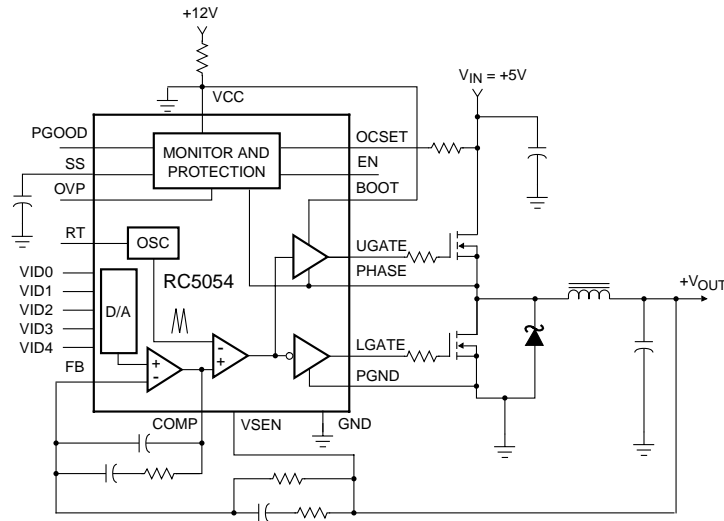
Applications Discussion

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

Figure 3 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board The components shown in Figure 3 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the RC5054A within 3 inches of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the RC5054A must be sized to handle up to 1A peak current.

Figure 4 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS} close to the SS pin because the internal current source is only 10μA. Provide local V_{CC} decoupling between V_{CC} and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.
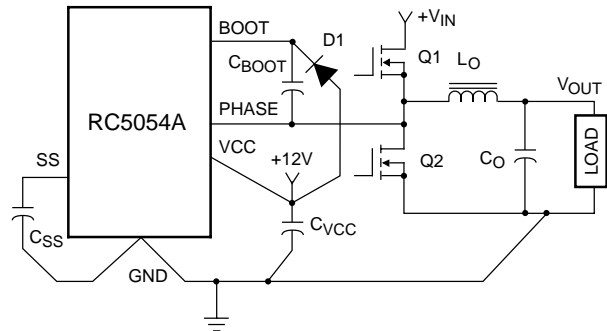
**Figure 4. Printed Circuit Board
Small Signal Layout Guidelines**

Feedback Compensation

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

**Figure 3. Printed Circuit Board
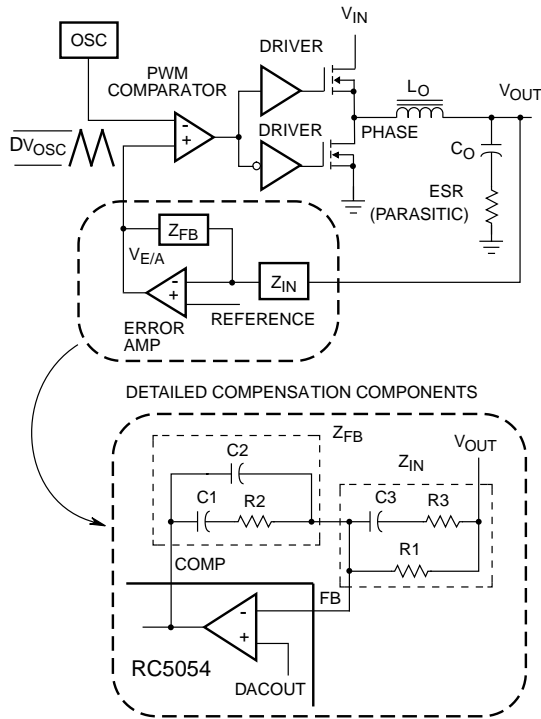Power and Ground Planes or Islands**

**Figure 5. Voltage-Mode Buck
Converter Compensation Design**

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break freaquency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad\qquad F_{ESR} = \frac{1}{2\pi \bullet ESR \bullet C_O}$$

The compensation network consists of the error amplifier (internal to the RC5054A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 5. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth

2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})

3. Place 2ND Zero at Filter's Double Pole

4. Place 1ST Pole at the ESR Zero

5. Place 2ND Pole at Half the Switching Frequency

6. Check Gain against Error Amplifier's Open-Loop Gain

7. Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \qquad\qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\dfrac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad\qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

Figure 6 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 6. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.
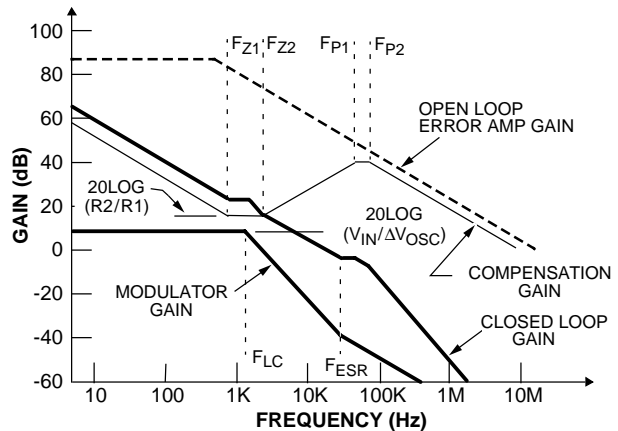

Figure 6. Asymptotic Bode Plot of Converter Gain

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1μF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{FS \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the RC5054A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the DACOUT setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MVGX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The RC5054A requires 2 N-Channel power MOSFETs. These should be selected based upon $R_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the upper MOSFET has switching losses, since the Schottky rectifier clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the RC5054A and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{LOWER} = I_O^2 \times R_{DS(ON)} \times (1 - D)$$

$$P_{UPPER} = I_O^2 \times R_{DS(ON)} \times D + \frac{1}{3} I_O \times V_{IN} \times t_{SW} \times F_S$$

Where: D is the duty cycle = V_{OUT}/V_{IN},
         t_{SW} is the switching interval, and
         F_S is the switching frequency

Standard-gate MOSFETs are normally recommended for use with the RC5054A. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFET's absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 7 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT} develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of V_{CC} less the boot diode drop (V_D) when the lower MOSFET, Q2 turns on. Logic-level MOSFETs can only be used if the MOSFET's absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.
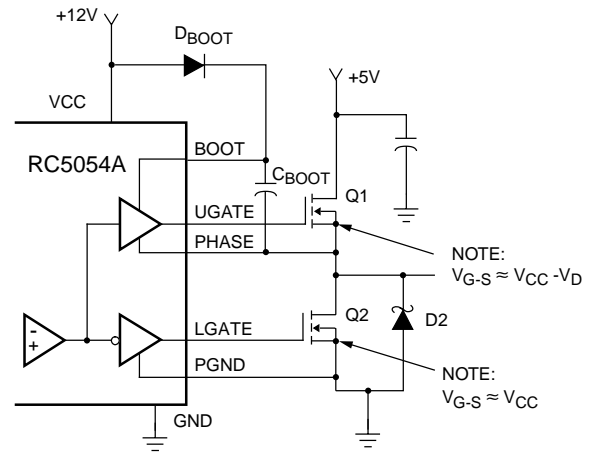

Figure 7. Upper Gate Drive - Bootstrap Option

Figure 8 shows the upper gate drive supplied by a direct connection to V_{CC}. This option should only be used in converter systems where the main input voltage is $+5V_{DC}$ or less. The peak upper gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and +12VDC for the bias, the gate-to-source voltage of Q1 is 7V. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.
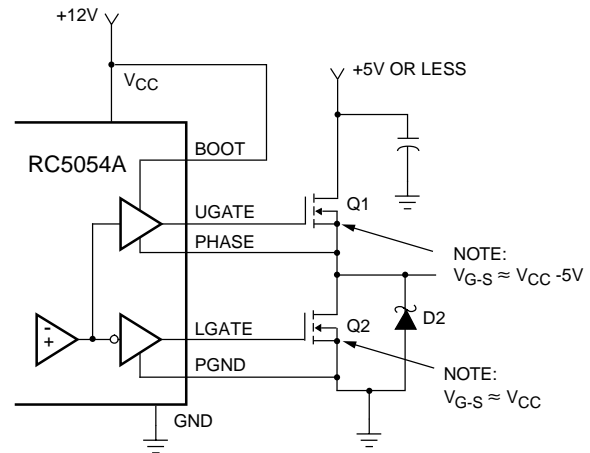

Figure 8. Upper Gate Drive - Direct V_{CC} Drive Option

Schottky Selection

Rectifier D2 is a clamp that catches the negative inductor swing during the dead time between turning off the lower MOSFET and turning on the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency will drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

RC5054A DC-DC Converter
Application Circuit

Figure 10 shows an application circuit of a DC-DC Converter
for an Intel Pentium Pro microprocessor.
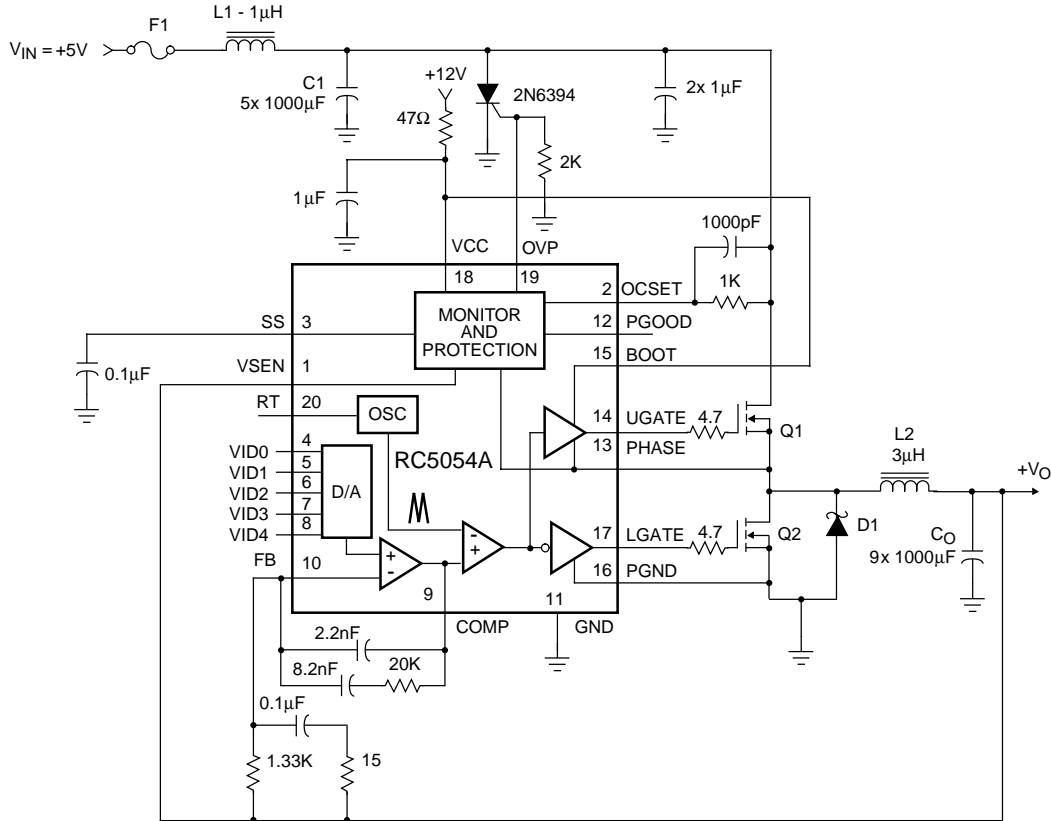
Component Selection Notes;

    C_0 - 9 Each 1000µF 6.3W VDC, Sanyo MV-GX or Equivalent
    C1 - 5 Each 1000µF 25W VDC, Sanyo MV-GX or Equivalent
    L2 - Core: Micrometals T50-52B; Each Winding: 10 Turns of 16AWG
    L1 - Core: Micrometals T50-52; Winding: 5 Turns of 18AWG
   D1 - 3A, 40V Schottky, Motorola MBR340 or Equivalent
    Q1, Q2 - Fairchild FDB6030L

Figure 9. Pentium Pro DC-DC Converter

Mechanical Dimensions (20 Lead SOIC)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.
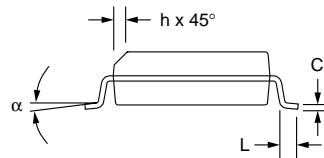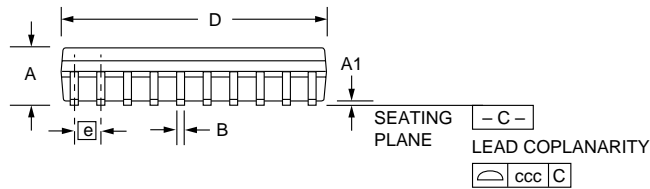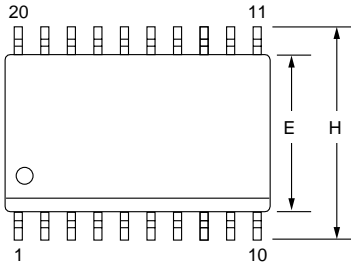
Ordering Information

Part Number	Temperature Range (°C)	Package
RC5054AM	0 to 70	20 Ld SOIC