查询AD8361ARM-REEL供应商

LF to 2.5 GHz TruPwr™ Detector

AD8361

FEATURES

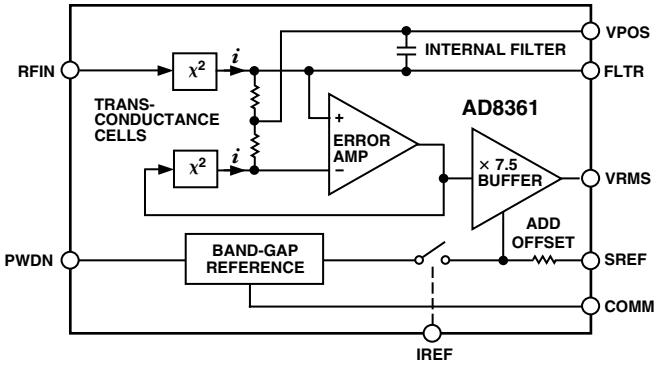
Calibrated RMS Response
Excellent Temperature Stability
Up to 30 dB Input Range at 2.5 GHz
700 mV rms, 10 dBm re 50 Ω Maximum Input
±0.25 dB Linear Response Up to 2.5 GHz
Single Supply Operation: 2.7 V to 5.5 V
Low Power: 3.3 mW at 3 V Supply
Rapid Power-Down to Less than 1 μA

APPLICATIONS

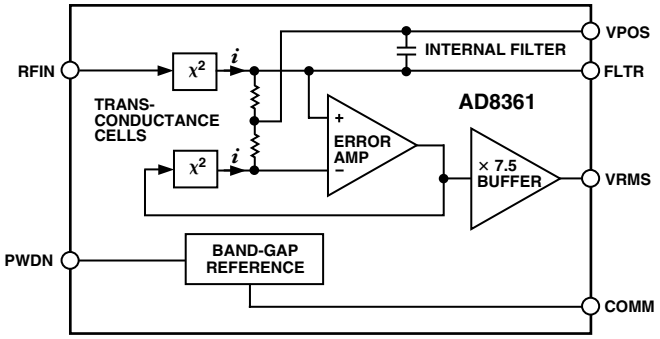
Measurement of CDMA, W-CDMA, QAM, Other Complex Modulation Waveforms
RF Transmitter or Receiver Power Measurement

FUNCTIONAL BLOCK DIAGRAMS

micro_SOIC



SOT-23-6L



PRODUCT DESCRIPTION

The AD8361 is a mean-responding power detector for use in high-frequency receiver and transmitter signal chains, up to 2.5 GHz. It is very easy to apply. It requires only a single supply between 2.7 V and 5.5 V, power supply decoupling capacitor and an input coupling capacitor in most applications. The output is a linear-responding dc voltage with a conversion gain of 7.5 V/V rms. An external filter capacitor can be added to increase the averaging time constant.

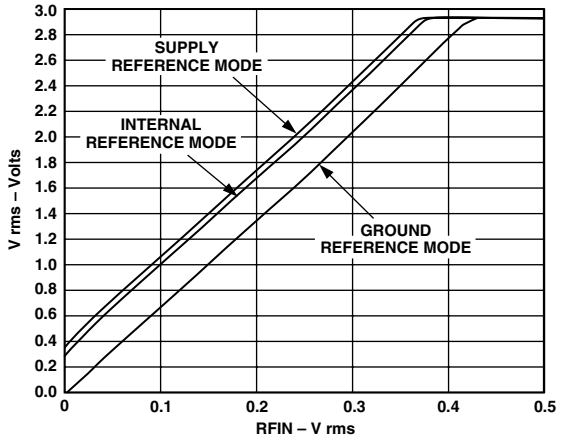


Figure 1. Output in the Three Reference Modes, Supply 3 V, Frequency 1.9 GHz (SOT-23-6L Package Ground Reference Mode Only)

The AD8361 is intended for true power measurement of simple and complex waveforms. The device is particularly useful for measuring high crest-factor (high peak-to-rms ratio) signals, such as CDMA and W-CDMA.

The AD8361 has three operating modes to accommodate a variety of analog-to-digital converter requirements:

1. Ground referenced mode, in which the origin is zero;
2. Internal reference mode, which offsets the output 350 mV above ground;
3. Supply reference mode, which offsets the output to $V_S/7.5$.

The AD8361 is specified for operation from –40°C to +85°C and is available in 8-lead micro_SOIC and 6-lead SOT packages. It is fabricated on a proprietary high f_T silicon bipolar process.

TruPwr is a trademark of Analog Devices, Inc.

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AD8361–SPECIFICATIONS (T_A = 25°C, V_S = 3 V, f_{RF} = 900 MHz, ground reference output mode, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	(Input RFIN)				
Frequency Range[1]				2.5	GHz
Linear Response Upper Limit	V_S = 3 V		390		mV rms
	Equivalent dBm re 50 Ω		4.9		dBm
	V_S = 5 V		660		mV rms
	Equivalent dBm re 50 Ω		9.4		dBm
Input Impedance[2]			225‖1		Ω‖pF
RMS CONVERSION	(Input RFIN to Output V rms)				
Conversion Gain			7.5		V/V rms
	f_{RF} = 100 MHz, V_S = 5 V	6.5		8.5	V/V rms
Dynamic Range	Error Referred to Best Fit Line[3]				
±0.25 dB Error[4]	CW Input, –40°C < T_A < +85°C		14		dB
±1 dB Error	CW Input, –40°C < T_A < +85°C		23		dB
±2 dB Error	CW Input, –40°C < T_A < +85°C		26		dB
	CW Input, V_S = 5 V, –40°C < T_A < +85°C		30		dB
Intercept-Induced Dynamic	Internal Reference Mode		1		dB
Range Reduction[5, 6]	Supply Reference Mode, V_S = 3.0 V		1		dB
	Supply Reference Mode, V_S = 5.0 V		1.5		dB
Deviation from CW Response	5.5 dB Peak-to-Average Ratio (IS95 Reverse Link)		0.2		dB
	12 dB Peak-to-Average Ratio (W-CDMA 4 Channels)		1.0		dB
	18 dB Peak-to-Average Ratio (W-CDMA 15 Channels)		1.2		dB
OUTPUT INTERCEPT[5]	Inferred from Best Fit Line[3]				
Ground Reference Mode (GRM)	0 V at SREF, V_S at IREF		0		V
	f_{RF} = 100 MHz, V_S = 5 V	–50		+150	mV
Internal Reference Mode (IRM)	0 V at SREF, IREF Open		350		mV
	f_{RF} = 100 MHz, V_S = 5 V	300		500	mV
Supply Reference Mode (SRM)	0 V at IREF, 3 V at SREF		400		mV
	f_{RF} = 100 MHz, V_S = 5 V	590		750	mV
	0 V at IREF, V_S at SREF		V_S/7.5		V
POWER-DOWN INTERFACE					
PWDN HI Threshold	2.7 ≤ V_S ≤ 5.5 V, –40°C < T_A < +85°C	V_S – 0.5			V
PWDN LO Threshold	2.7 ≤ V_S ≤ 5.5 V, –40°C < T_A < +85°C			0.1	V
Power-Up Response Time	2 pF at FLTR Pin, 224 mV rms at RFIN		5		µs
	100 nF at FLTR Pin, 224 mV rms at RFIN		320		µs
PWDN Bias Current			<1		µA
POWER SUPPLIES					
Operating Range	–40°C < T_A < +85°C	2.7		5.5	V
Quiescent Current	0 mV rms at RFIN, PWDN Input LO[7]		1.1		mA
Power-Down Current	GRM or IRM, 0 mV rms at RFIN, PWDN Input HI		<1		µA
	SRM, 0 mV rms at RFIN, PWDN Input HI		10 × V_S		µA

NOTES
[1]Operation at arbitrarily low frequencies is possible; see Applications section.
[2]Figure 13 and Figure 40 show impedance vs. frequency for the micro_SOIC and SOT respectively.
[3]Calculated using linear regression.
[4]Compensated for output reference temperature drift; see Applications section.
[5]SOT-23-6L operates in ground reference mode only.
[6]The available output swing, and hence the dynamic range, is altered by both supply voltage and reference mode; see Figures 35 and 36.
[7]Supply current is input level dependant; see Figure 12.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage V_S	5.5 V
SREF, PWDN	0 V, V_S
IREF	V_S – 0.3 V, V_S
RFIN	1 V rms
Equivalent Power re 50 Ω	13 dBm
Internal Power Dissipation[2]	200 mW
SOT-23-6L	170 mW
micro_SOIC	200 mW
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

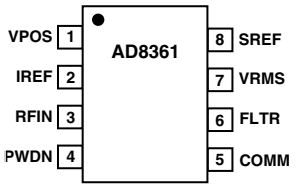
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

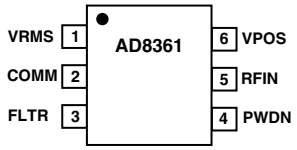
[2]Specification is for the device in free air.
SOT-23-6L: θ_{JA} = 230°C/W; θ_{JC} = 92°C/W.
micro_SOIC: θ_{JA} = 200°C/W; θ_{JC} = 44°C/W.

PIN CONFIGURATIONS

micro_SOIC



SOT-23-6L



PIN FUNCTION DESCRIPTIONS

Pin Micro	Pin SOT	Name	Description
1	6	VPOS	Supply Voltage Pin. Operational range 2.7 V to 5.5 V.
2		IREF	Output Reference Control Pin. Internal reference mode enabled when pin is left open. Otherwise, this pin should be tied to VPOS. DO NOT ground this pin.
3	5	RFIN	Signal Input Pin. Must be driven from an ac-coupled source. The low frequency real input impedance is 225 Ω.
4	4	PWDN	Power-Down Pin. For the device to operate as a detector it needs a logical low input (less than 100 mV). When a logic high (greater than V_S – 0.5 V) is applied, the device is turned off and the supply current goes to nearly zero (ground and internal reference mode less than 1 μA, supply reference mode V_S divided by 100 kΩ).
5	2	COMM	Device Ground Pin.
6	3	FLTR	By placing a capacitor between this pin and VPOS, the corner frequency of the modulation filter is lowered. The on-chip filter is formed with 27 pF‖2 kΩ for small input signals.
7	1	VRMS	Output Pin. Near-rail-to-rail voltage output with limited current drive capabilities. Expected load >10 kΩ to ground.
8		SREF	Supply Reference Control Pin. To enable supply reference mode this pin must be connected to VPOS, otherwise it should be connected to COMM (ground).

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8361ARM*	–40°C to +85°C	Tube, 8-Lead micro_SOIC	RM-8
AD8361ARM-REEL		13" Tape and Reel	
AD8361ARM-REEL7		7" Tape and Reel	
AD8361ART-REEL		13" Tape and Reel	RT-6
AD8361ART-REEL7		7" Tape and Reel	
AD8361-EVAL		Evaluation Board micro_SOIC	
AD8361ART-EVAL		Evaluation Board SOT-23-6L	

*Device branded as J3A.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8361 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8361–Typical Performance Characteristics

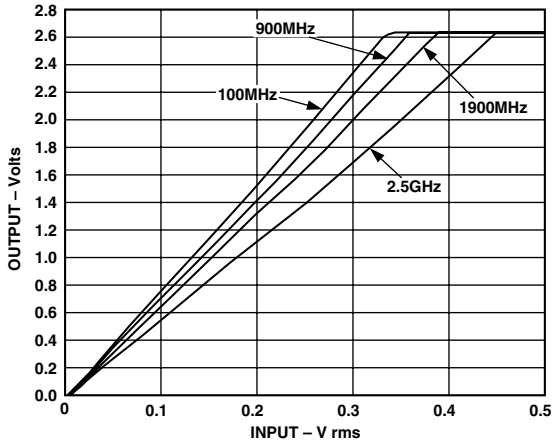


Figure 2. Output vs. Input Level, Frequencies 100 MHz, 900 MHz, 1900 MHz, and 2500 MHz, Supply 2.7 V, Ground Reference Mode, micro_SOIC

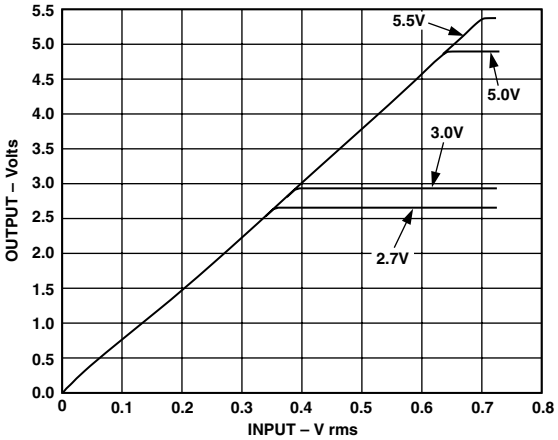


Figure 3. Output vs. Input Level, Supply 2.7 V, 3.0 V, 5.0 V, and 5.5 V, Frequency 900 MHz

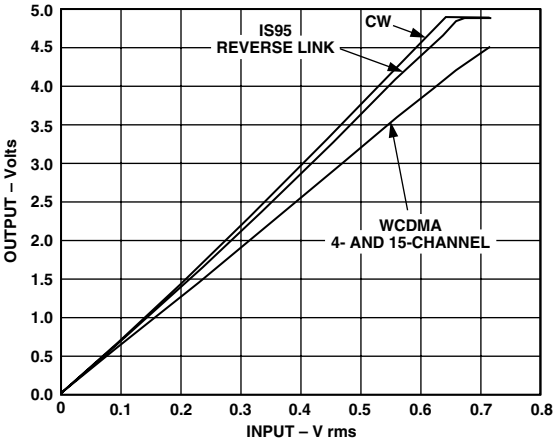


Figure 4. Output vs. Input Level with Different Waveforms Sine Wave (CW), IS95 Reverse Link, W-CDMA 4-Channel and W-CDMA 15-Channel, Supply 5.0 V

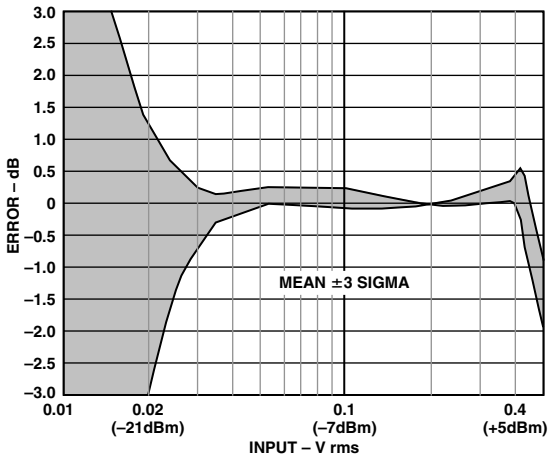


Figure 5. Error from Linear Reference vs. Input Level, 3 Sigma to Either Side of Mean, Sine Wave, Supply 3.0 V, Frequency 900 MHz

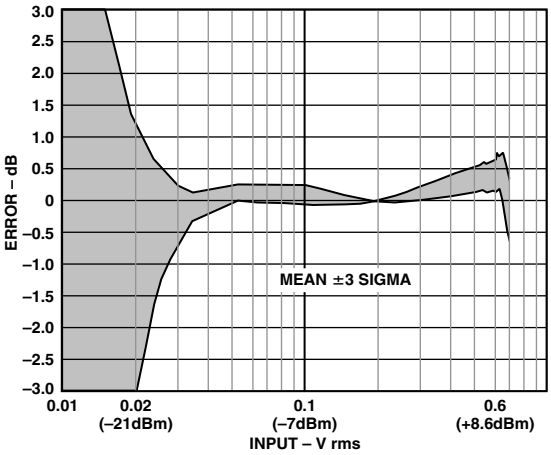


Figure 6. Error from Linear Reference vs. Input Level, 3 Sigma to Either Side of Mean, Sine-Wave, Supply 5.0 V, Frequency 900 MHz

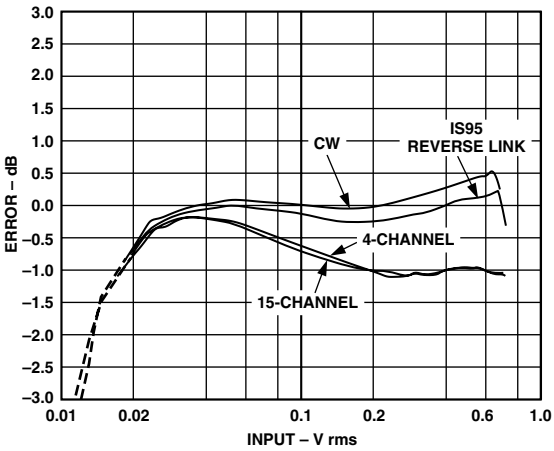


Figure 7. Error from CW Linear Reference vs. Input with Different Waveforms Sine Wave (CW), IS95 Reverse Link, W-CDMA 4-Channel and W-CDMA 15-Channel, Supply 3.0 V, Frequency 900 MHz

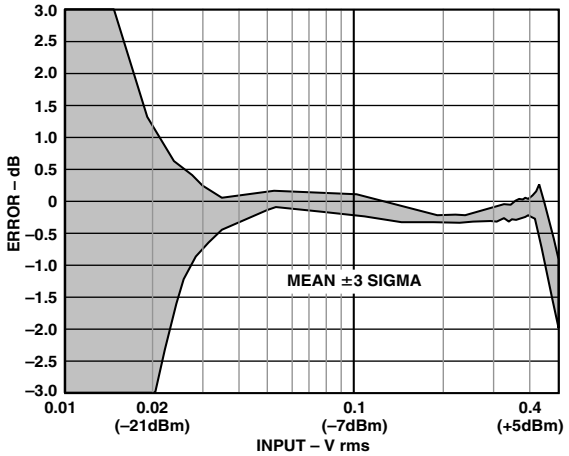


Figure 8. Error from CW Linear Reference vs. Input, 3 Sigma to Either Side of Mean, IS95 Reverse Link Signal, Supply 3.0 V, Frequency 900 MHz

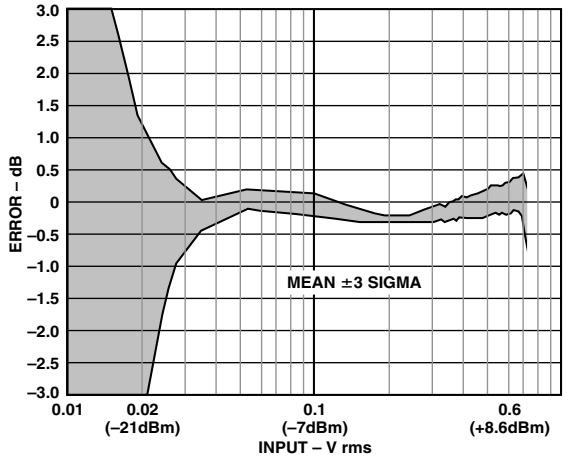


Figure 9. Error from CW Linear Reference vs. Input Level, 3 Sigma to Either Side of Mean, IS95 Reverse Link Signal, Supply 5.0 V, Frequency 900 MHz

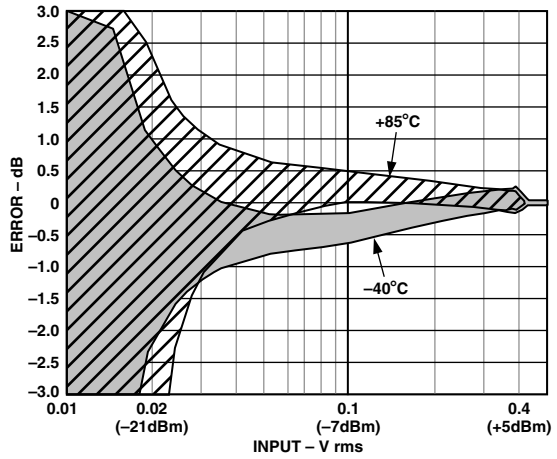


Figure 10. Output Delta from +25°C vs. Input Level, 3 Sigma to Either Side of Mean Sine Wave, Supply 3.0 V, Frequency 900 MHz, Temperature –40°C to +85°C

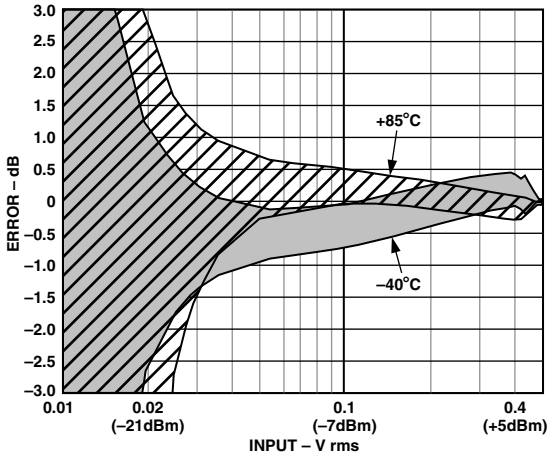


Figure 11. Output Delta from +25°C vs. Input Level, 3 Sigma to Either Side of Mean Sine Wave, Supply 3.0 V, Frequency 1900 MHz, Temperature –40°C to +85°C

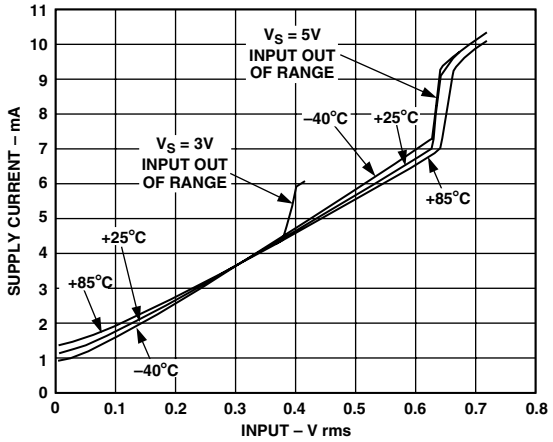


Figure 12. Supply Current vs. Input Level, Supplies 3.0 V, and 5.0 V, Temperatures –40°C, +25°C, and +85°C

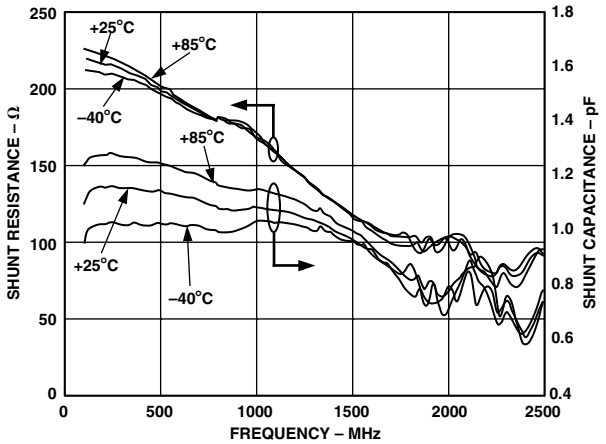


Figure 13. Input Impedance vs. Frequency, Supply 3 V, Temperatures –40°C, +25°C, and +85°C, micro_SOIC (See Applications for SOT-23-6L Data)

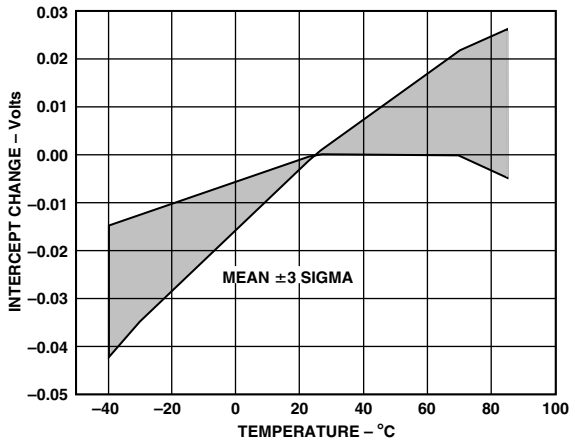


Figure 14. Output Reference Change vs. Temperature, Supply 3 V, Ground Reference Mode

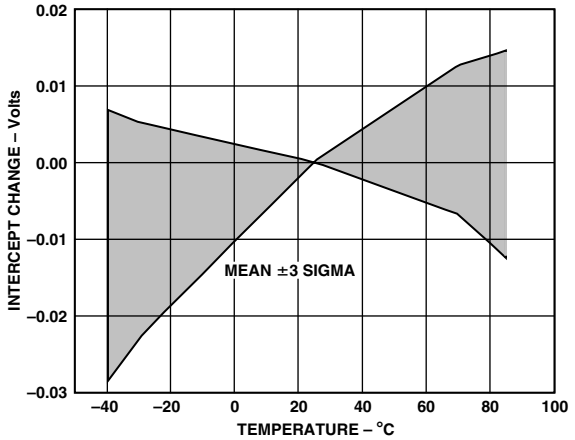


Figure 15. Output Reference Change vs. Temperature, Supply 3 V, Internal Reference Mode (micro_SOIC Only)

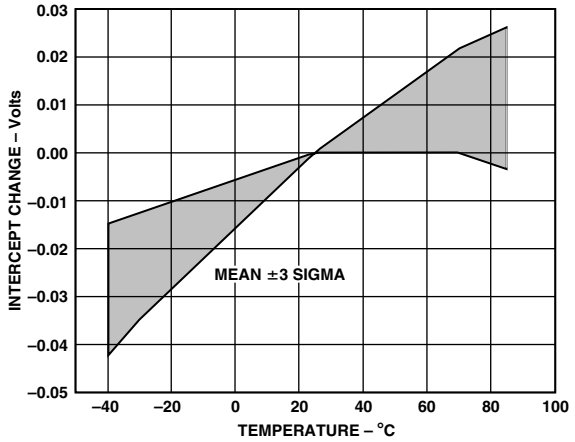


Figure 16. Output Reference Change vs. Temperature, Supply 3 V, Supply Reference Mode (micro_SOIC Only)

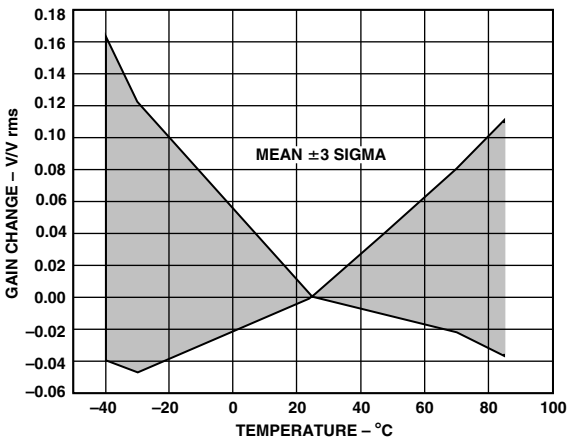


Figure 17. Conversion Gain Change vs. Temperature, Supply 3 V, Ground Reference Mode, Frequency 900 MHz

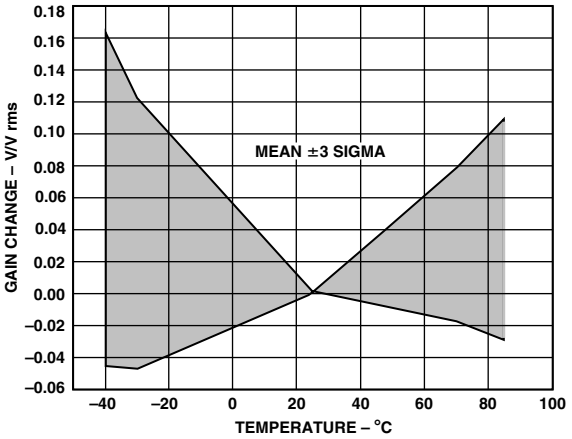


Figure 18. Conversion Gain Change vs. Temperature, Supply 3 V, Internal Reference Mode, Frequency 900 MHz (micro_SOIC Only)

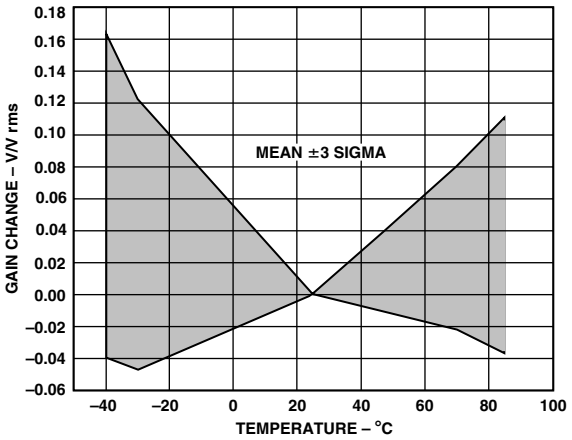


Figure 19. Conversion Gain Change vs. Temperature, Supply 3 V, Supply Reference Mode, Frequency 900 MHz (micro_SOIC Only)

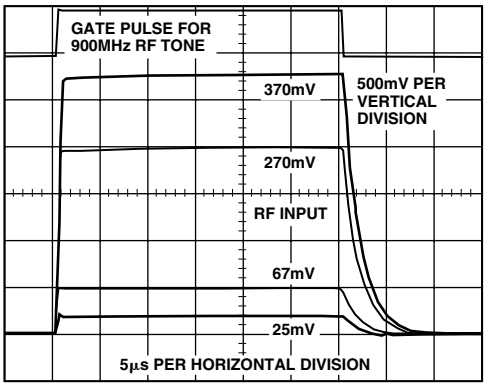


Figure 20. Output Response to Modulated Pulse Input for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, No Filter Capacitor

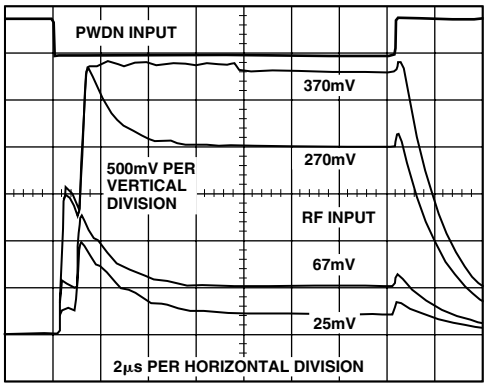


Figure 23. Output Response Using Power-Down Mode for Various RF Input Levels, Supply 3 V, Frequency 900 MHz, No Filter Capacitor

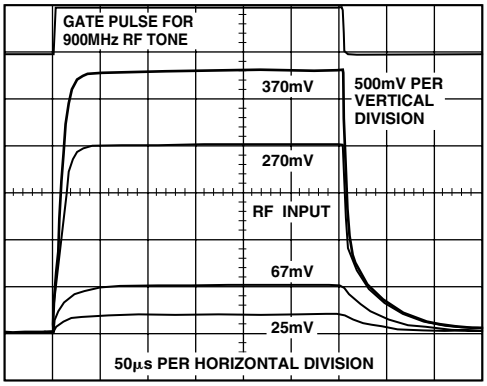


Figure 21. Output Response to Modulated Pulse Input for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, 0.01 μF Filter Capacitor

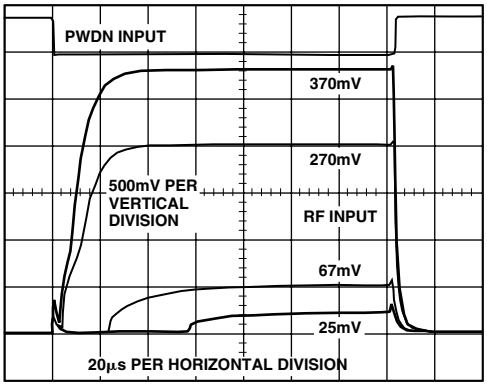


Figure 24. Output Response Using Power-Down Mode for Various RF Input Levels, Supply 3 V, Frequency 900 MHz, 0.01 μF Filter Capacitor

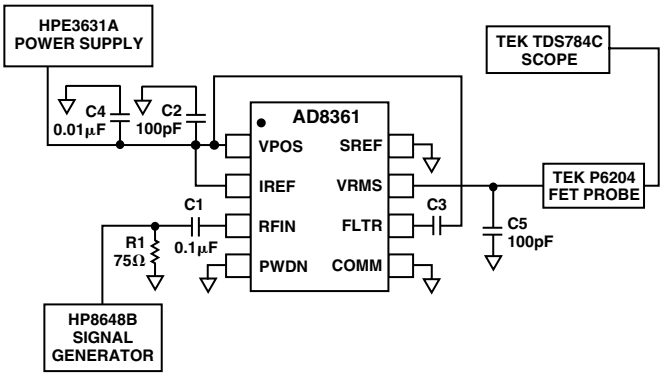


Figure 22. Hardware Configuration for Output Response to Modulated Pulse Input

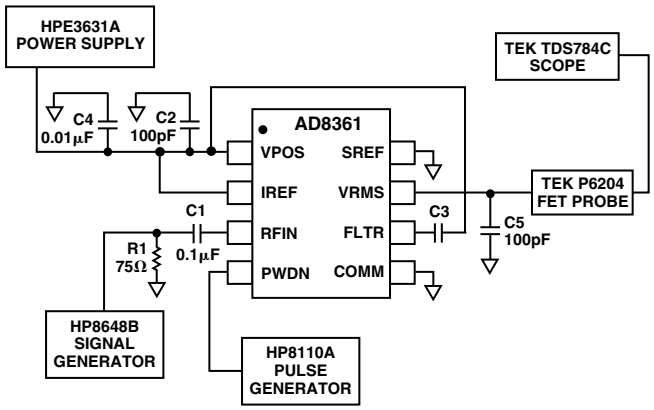


Figure 25. Hardware Configuration for Output Response Using Power-Down Mode

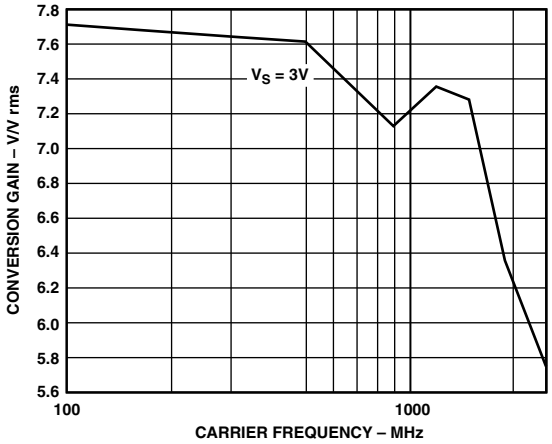


Figure 26. Conversion Gain Change vs. Frequency, Supply 3 V, Ground Reference Mode, Frequency 100 MHz to 2500 MHz, Representative Device

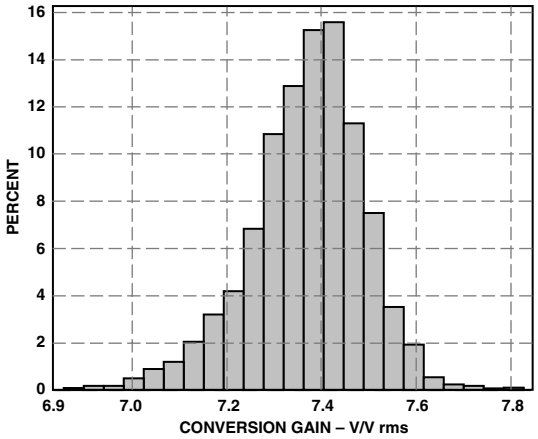


Figure 29. Conversion Gain Distribution Frequency 100 MHz, Supply 5 V, Sample Size 3000

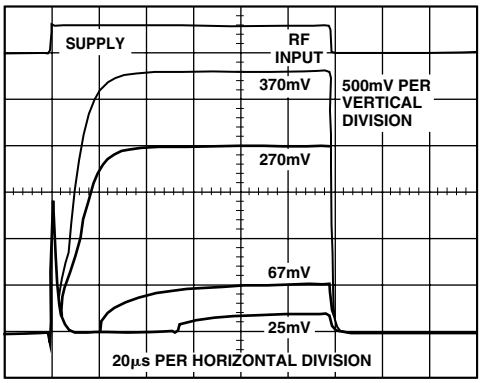


Figure 27. Output Response to Gating On Power Supply, for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, 0.01 µF Filter Capacitor

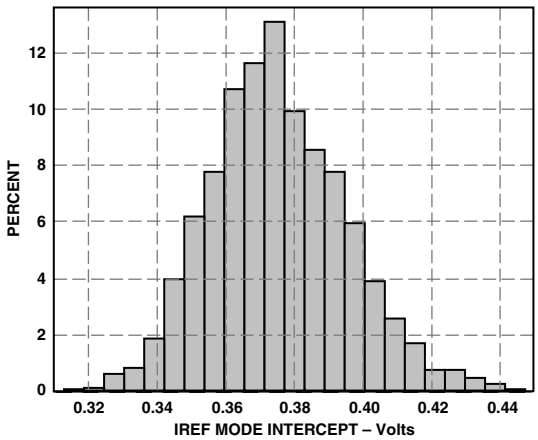


Figure 30. Output Reference, Internal Reference Mode, Supply 5 V, Sample Size 3000 (micro_SOIC Only)

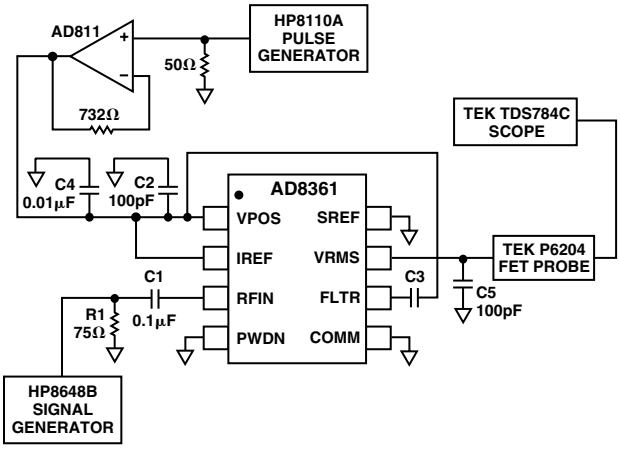


Figure 28. Hardware Configuration for Output Response to Power Supply Gating Measurements

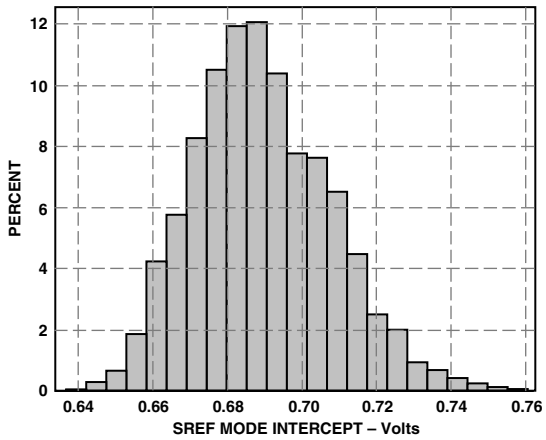


Figure 31. Output Reference, Supply Reference Mode, Supply 5 V, Sample Size 3000 (micro_SOIC Only)

CIRCUIT DESCRIPTION

The AD8361 is an rms-responding (mean power) detector providing an approach to the exact measurement of RF power that is basically independent of waveform. It achieves this function through the use of a proprietary technique in which the outputs of two identical squaring cells are balanced by the action of a high-gain error amplifier.

The signal to be measured is applied to the input of the first squaring cell, which presents a nominal (LF) resistance of 225 Ω between the pin RFIN and COMM (connected to the ground plane). Since the input pin is at a bias voltage of about 0.8 V above ground, a coupling capacitor is required. By making this an external component, the measurement range may be extended to arbitrarily low frequencies.

The AD8361 responds to the voltage, V_{IN}, at its input, by squaring this voltage to generate a current proportional to V_{IN} squared. This is applied to an internal load resistor, across which is connected a capacitor. These form a low-pass filter, which extracts the mean of V_{IN} squared. Although essentially voltage-responding, the associated input impedance calibrates this port in terms of equivalent power. Thus 1 mW corresponds to a voltage input of 447 mV rms. In the Application section it is shown how to match this input to 50 Ω.

The voltage across the low-pass filter, whose frequency may be arbitrarily low, is applied to one input of an error-sensing amplifier. A second identical voltage-squaring cell is used to close a negative feedback loop around this error amplifier. This second cell is driven by a fraction of the quasi-dc output voltage of the AD8361. When the voltage at the input of the second squaring cell is equal to the rms value of V_{IN}, the loop is in a stable state, and the output then represents the rms value of the input. The feedback ratio is nominally 0.133, making the rms-dc conversion gain ×7.5, that is

$$V_{OUT} = 7.5 \times V_{IN}\ rms$$

By completing the feedback path through a second squaring cell, identical to the one receiving the signal to be measured, several benefits arise. First, scaling effects in these cells cancel; thus, the overall calibration may be accurate, even though the open-loop response of the squaring cells taken separately need not be. Note that in implementing rms-dc conversion, no reference voltage enters into the closed-loop scaling. Second, the tracking in the responses of the dual cells remains very close over temperature, leading to excellent stability of calibration.

The squaring cells have very wide bandwidth with an intrinsic response from dc to microwave. However, the dynamic range of such a system is fairly small, due in part to the much larger dynamic range at the output of the squaring cells. There are practical limitations to the accuracy with which very small error signals can be sensed at the bottom end of the dynamic range, arising from small random offsets; these set the limit to the attainable accuracy at small inputs.

On the other hand, the squaring cells in the AD8361 have a "Class-AB" aspect; the peak input is not limited by their quiescent bias condition, but is determined mainly by the eventual loss of square-law conformance. Consequently, the top end of their response range occurs at a fairly large input level (about 700 mV rms) while preserving a reasonably accurate square-law response. The maximum usable range is, in practice, limited by the output swing. The rail-to-rail output stage can swing from a few millivolts above ground to less than 100 mV below the supply. An example of the output induced limit: given a gain of 7.5 and assuming a maximum output of 2.9 V with a 3 V supply; the maximum input is (2.9 V rms)/7.5 or 390 mV rms.

Filtering

An important aspect of rms-dc conversion is the need for averaging (the function is *root-MEAN-square*). For complex RF waveforms such as occur in CDMA, the filtering provided by the on-chip low-pass filter, while satisfactory for CW signals above 100 MHz, will be inadequate when the signal has modulation components that extend down into the kilohertz region. For this reason, the FLTR pin is provided: a capacitor attached between this pin and VPOS can extend the averaging time to very low frequencies.

Offset

An offset voltage can be added to the output (when using the micro_SOIC version) to allow the use of A/D converters whose range does not extend down to ground. However, accuracy at the low end will be degraded because of the inherent error in this added voltage. This requires that the pin IREF (*internal reference*) should be tied to VPOS and SREF (*supply reference*) to ground.

In the IREF mode, the intercept is generated by an internal reference cell, and is a fixed 350 mV, independent of the supply voltage. To enable this intercept, IREF should be open-circuited, and SREF should be grounded.

In the SREF mode, the voltage is provided by the supply. To implement this mode, tie IREF to VPOS and SREF to VPOS. The offset is then proportional to the supply voltage, and is 400 mV for a 3 V supply and 667 mV for a 5 V supply.

USING THE AD8361

Basic Connections

Figures 32, 33, and 34 show the basic connections for the micro_SOIC version AD8361 in its three operating modes. In all modes, the device is powered by a single supply of between 2.7 V and 5.5 V. The VPOS pin is decoupled using 100 pF and 0.01 μF capacitors. The quiescent current of 1.1 mA in operating mode can be reduced to 1 μA by pulling the PWDN pin up to VPOS.

A 75 Ω external shunt resistance combines with the ac-coupled input to give an overall broadband input impedance near 50 Ω. Note that the coupling capacitor must be placed between the input and the shunt impedance. Input impedance and input coupling are discussed in more detail below.

The input coupling capacitor combines with the internal input resistance (Figure 13) to give a high-pass corner frequency given by the equation

$$f_{3\ dB} = \frac{1}{2\ \pi \times C_C \times R_{IN}}$$

With the 100 pF capacitor shown in Figures 32–34, the high-pass corner frequency is about 8 MHz.

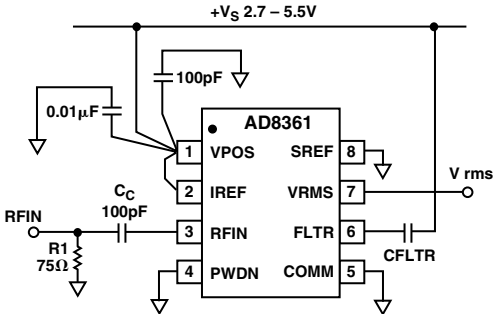


Figure 32. Basic Connections for Ground Referenced Mode

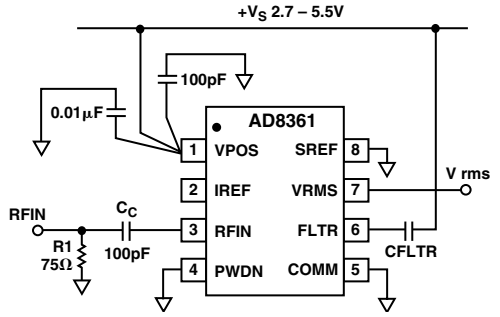


Figure 33. Basic Connections for Internal Reference Mode

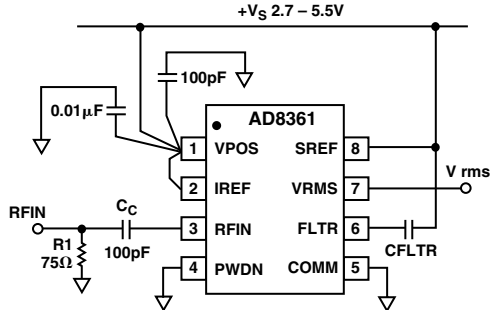


Figure 34. Basic Connections for Supply Referenced Mode

The output voltage is nominally 7.5 times the input rms voltage (a conversion gain of 7.5 V/V rms). Three different modes of operation are set by the pins SREF and IREF. In addition to the ground referenced mode shown in Figure 32, where the output voltage swings from around near ground to 4.9 V on a 5.0 V supply, two additional modes allow an offset voltage to be added to the output. In the internal reference mode, (Figure 33), the output voltage swing is shifted upward by an internal reference voltage of 350 mV. In supply referenced mode (Figure 34), an offset voltage of $V_S/7.5$ is added to the output voltage. Table I summarizes the connections, output transfer function and minimum output voltage (i.e., zero signal) for each mode.

Output Swing

Figure 35 shows the output swing of the AD8361 for a 5 V supply voltage for each of the three modes. It is clear from Figure 35, that operating the device in either internal reference mode or supply referenced mode, will reduce the effective dynamic range as the output headroom decreases. The response for lower supply voltages is similar (in the supply referenced mode, the offset is smaller), but the dynamic range will be reduced further, as headroom decreases. Figure 36 shows the response of the AD8361 to a CW input for various supply voltages.

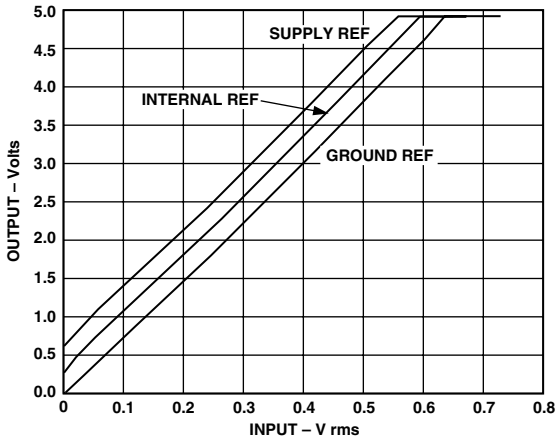


Figure 35. Output Swing for Ground, Internal and Supply Referenced Mode. VPOS = 5 V (micro_SOIC Only)

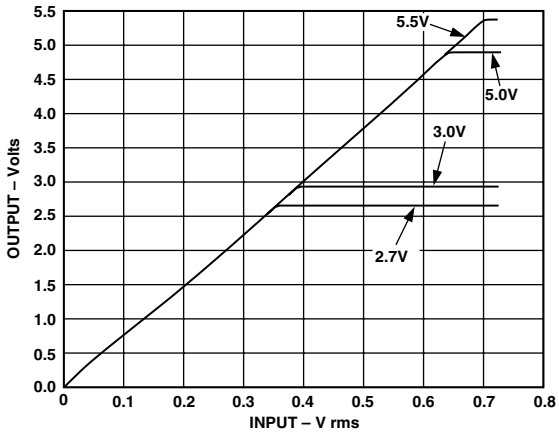


Figure 36. Output Swing for Supply Voltages of 2.7 V, 3.0 V, 5.0 V and 5.5 V (micro_SOIC Only)

Dynamic Range

Because the AD8361 is a linear responding device with a nominal transfer function of 7.5 V/V rms, the dynamic range in dB is not clear from plots such as Figure 35. As the input level is increased in constant dB steps, the output *step size* (per dB) will also increase. Figure 37 shows the relationship between the output step size (i.e., mV/dB) and input voltage for a nominal transfer function of 7.5 V/V rms.

Table I. Connections and Nominal Transfer Function for Ground, Internal, and Supply Reference Modes

Reference Mode	IREF	SREF	Output Intercept (No Signal)	Output
Ground	VPOS	COMM	Zero	$7.5\ V_{IN}$
Internal	OPEN	COMM	0.350 V	$7.5\ V_{IN} + 0.350$ V
Supply	VPOS	VPOS	$V_S/7.5$	$7.5\ V_{IN} + V_S/7.5$

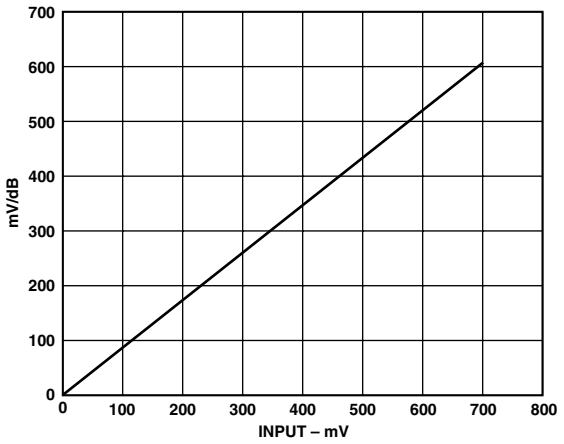


Figure 37. Idealized Output Step Size as Function of Input Voltage

Plots of output voltage vs. input voltage result in a straight line. It may sometimes be more useful to plot the error on a logarithmic scale, as shown in Figure 38. The deviation of the plot for the ideal straight line characteristic is caused by output clipping at the high end and by signal offsets at the low end. It should however be noted that offsets at the low end can be either positive or negative, so that this plot could also trend upwards at the low end. Figures 5, 6, 8, and 9 show a ±3 sigma distribution of device error for a large population of devices.

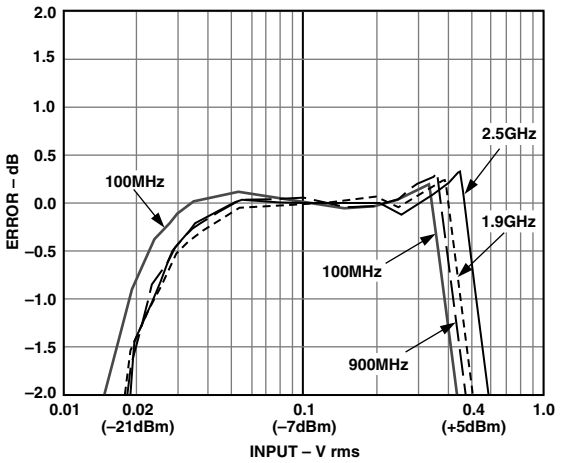


Figure 38. Representative Unit, Error in dB vs. Input Level, V_S = 2.7 V

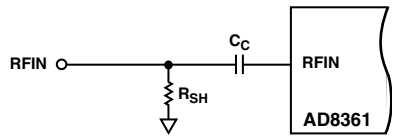
It is also apparent in Figure 38 that the error plot tends to shift to the right with increasing frequency. Because the input impedance decreases with frequency, the voltage actually applied to the input will also tend to decrease (assuming a constant source impedance over frequency). The dynamic range is almost constant over frequency, but with a small decrease in conversion gain at high frequency.

Input Coupling and Matching

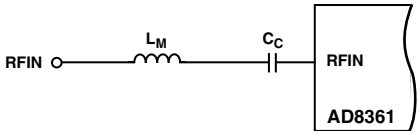
The input impedance of the AD8361 decreases with increasing frequency in both its resistive and capacitive components (Figure 13). The resistive component varies from 225 Ω at 100 MHz down to about 95 Ω at 2.5 GHz.

A number of options exist for input matching. For operation at multiple frequencies, a 75 Ω shunt to ground, as shown in Figure 39a, will provide the best overall match. For use at a single frequency, a resistive or a reactive match can be used. By plotting the input impedance on a Smith Chart, the best value for a resistive match can be calculated. The VSWR can be held below 1.5 at frequencies up to 1 GHz, even as the input impedance varies from part to part. (Both input impedance and input capacitance can vary by up to ±20% around their nominal values.) At very high frequencies (i.e., 1.8 GHz to 2.5 GHz), a shunt resistor will not be sufficient to reduce the VSWR below 1.5. Where VSWR is critical, remove shunt component and insert an inductor in series with the coupling capacitor as shown in Figure 39b.

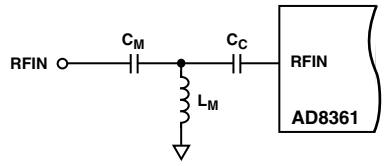
Table II gives recommended shunt resistor values for various frequencies and series inductor values for high frequencies. The coupling capacitor, C_C, essentially acts as an ac-short and plays no intentional part in the matching.



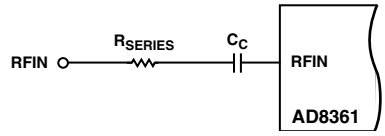
a. Broadband Resistor Match



b. Series Inductor Match



c. Narrowband Reactive Match



d. Attenuating the Input Signal

Figure 39. Input Coupling/Matching Options

Table II. Recommended Component Values for Resistive or Inductive Input Matching (Figures 39a and 39b)

Frequency	Matching Component
100 MHz	63.4 Ω Shunt
800 MHz	75 Ω Shunt
900 MHz	75 Ω Shunt
1800 MHz	150 Ω Shunt or 4.7 nH Series
1900 MHz	150 Ω Shunt or 4.7 nH Series
2500 MHz	150 Ω Shunt or 2.7 nH Series

Alternatively, a reactive match can be implemented using a shunt inductor to ground and a series capacitor as shown in Figure 39c. A method for hand calculating the appropriate matching components is shown on page 12 of the AD8306 data sheet.

Matching in this manner results in very small values for C_M, especially at high frequencies. As a result, a stray capacitance as small as 1 pF can significantly degrade the quality of the match. The main advantage of a reactive match is the increase in sensitivity that results from the input voltage being "gained up" (by the square root of the impedance ratio) by the matching network. Table III shows recommended values for reactive matching.

Table III. Recommended Values for a Reactive Input Match (Figure 39c)

Frequency MHz	C_M pF	L_M nH
100	16	180
800	2	15
900	2	12
1800	1.5	4.7
1900	1.5	4.7
2500	1.5	3.3

Input Coupling Using a Series Resistor

Figure 39d shows a technique for coupling the input signal into the AD8361, which may be applicable where the input signal is much larger than the input range of the AD8361. A series resistor combines with the input impedance of the AD8361 to attenuate the input signal. Since this series resistor forms a divider with the frequency-dependent input impedance, the apparent gain changes greatly with frequency. However, this method has the advantage of very little power being "tapped off" in RF power transmission applications. If the resistor is large compared to the transmission line's impedance then the VSWR of the system is relatively unaffected.

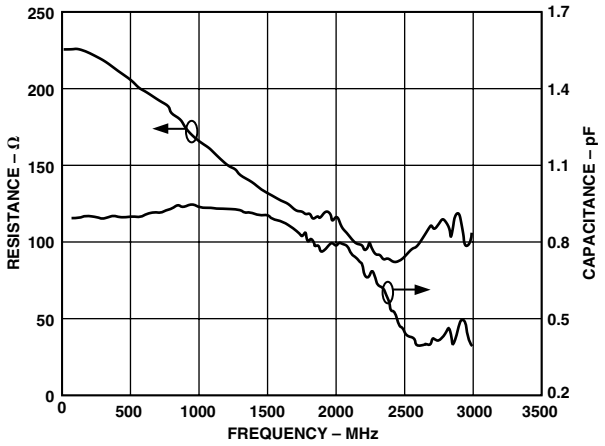


Figure 40. Input Impedance vs. Frequency, Supply 3 V, SOT-23-6L

Selecting the Filter Capacitor

The AD8361's internal 27 pF filter capacitor is connected in parallel with an internal resistance that varies with signal level from 2 kΩ for small signals to 500 Ω for large signals. The resulting low-pass corner frequency between 3 MHz and 12 MHz provides adequate filtering for all frequencies above 240 MHz (i.e., ten times the frequency at the output of the squarer, which is twice the input frequency). However, signals with high peak-to-average ratios, such as CDMA or W-CDMA signals, and with low frequency components, require additional filtering. TDMA signals, such as GSM, PDC, or PHS have a peak-to-average ratio that is close to that of a sinusoid, and the internal filter is adequate.

The filter capacitance of the AD8361 can be augmented by connecting a capacitor between Pin 6 (FLTR) and VPOS. Table IV shows the effect of several capacitor values for various communications standards with high peak-to-average ratios along with the residual ripple at the output, in peak-to-peak and rms volts. Note that large filter capacitors will increase the enable and pulse response times, as discussed below.

Table IV. Effect of Waveform and C_{FILT} on Residual AC

Waveform	C_{FILT}	Output V dc	Residual AC mV p-p	Residual AC mV rms
IS95 Reverse Link	Open	0.5	550	100
		1.0	1000	180
		2.0	2000	360
	0.01 µF	0.5	40	6
		1.0	160	20
		2.0	430	60
	0.1 µF	0.5	20	3
		1.0	40	6
		2.0	110	18
IS95 8-Channel Forward Link	0.01 µF	0.5	290	40
		1.0	975	150
		2.0	2600	430
	0.1 µF	0.5	50	7
		1.0	190	30
		2.0	670	95
W-CDMA 15 Channel	0.01 µF	0.5	225	35
		1.0	940	135
		2.0	2500	390
	0.1 µF	0.5	45	6
		1.0	165	25
		2.0	550	80

Operation at Low Frequencies

Although the AD8361 is specified for operation up to 2.5 GHz, there is no lower limit on the operating frequency. It is only necessary to increase the input coupling capacitor to reduce the corner frequency of the input high-pass filter (use an input resistance of 225 Ω for frequencies below 100 MHz). It is also necessary to increase the filter capacitor so that the signal at the output of the squaring circuit is free of ripple. The corner frequency will be set by the combination of the internal resistance of 2 kΩ and the external filter capacitance.

Power Consumption, Enable and Power-On

The quiescent current consumption of the AD8361 varies with the size of the input signal from about 1 mA for no signal up to 7 mA at an input level of 0.66 V rms (9.4 dBm re 50 Ω). If the input is driven beyond this point, the supply current increases steeply (see Figure 12). There is little variation in quiescent current with power supply voltage.

The AD8361 can be disabled either by pulling the PWDN (Pin 4) to VPOS or by simply turning off the power to the device. While turning off the device obviously eliminates the current consumption, disabling the device reduces the leakage current to less than 1 µA. Figures 23 and 24 show the response of the output of the AD8361 to a pulse on the PWDN pin, with no capacitance and with a filter capacitance of 0.01 µF respectively; the turn-on time is a function of the filter capacitor. Figure 27 shows a plot of the output response to the supply being turned on (i.e., PWDN is grounded and VPOS is pulsed) with a filter capacitor of 0.01 µF Again, the turn-on time is strongly influenced by the size of the filter capacitor.

If the input of the AD8361 is driven while the device is disabled (PWDN = VPOS), the leakage current of less than 1 µA will increase as a function of input level. When the device is disabled, the output impedance increases to around 16 kΩ.

Volts to dBm Conversion

In many of the plots, the horizontal axis is scaled in both rms volts and dBm. In all cases, dBm are calculated relative to an impedance of 50 Ω. To convert between dBm and volts in a 50 Ω. system, the following equations can be used. Figure 40 shows this conversion in graphical form.

$$Power\,(dBm) = 10\log\left[\frac{\dfrac{(V\ rms)^2}{50\ \Omega}}{0.001\ W}\right] = 10\ \log\ (20\ (V\ rms)^2)$$

$$V\ rms = \sqrt{0.001\ W \times 50\ \Omega \times \log^{-1}\left(\frac{dBm}{10}\right)} = \sqrt{\frac{\log^{-1}\left(dBm/10\right)}{20}}$$

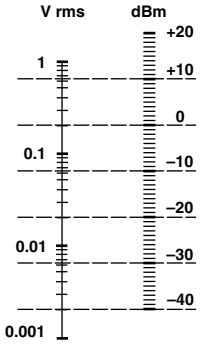
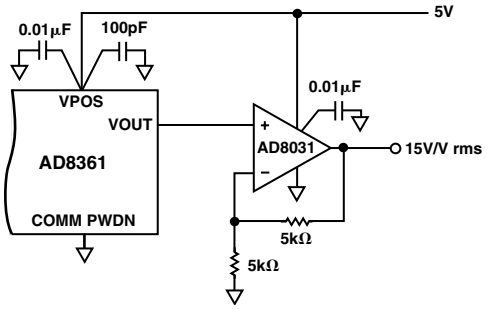


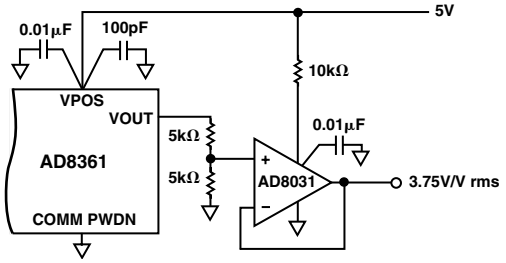
Figure 41. Conversion from dBm to rms Volts

Output Drive Capability and Buffering

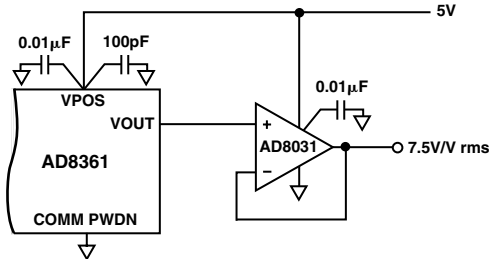
The AD8361 is capable of sourcing an output current of approximately 3 mA. If additional current is required, a simple buffering circuit can be used as shown in Figure 42c. Similar circuits can be used to increase or decrease the nominal conversion gain of 7.5 V/V rms (Figure 42a and 42b). In Figure 42b, the AD8031 buffers a resistive divider to give a slope of 3.75 V/V rms. In Figure 42a, the op amp's gain of two increases the slope to 15 V/V rms. Using other resistor values, the slope can be changed to an arbitrary value. The AD8031 rail-to-rail op amp, used in these examples can swing from 50 mV to 4.95 V on a single 5 V supply and operate at supply voltages down to 2.7 V. If high output current is required (>10 mA), the AD8051, which also has rail-to-rail capability, can be used, down to a supply voltage of 3 V. It can deliver up to 45 mA of output current.



a. Slope of 15 V/V rms



b. Slope of 3.75 V/V rms



c. Slope of 7.5 V/V rms

Figure 42. Output Buffering Options

OUTPUT REFERENCE TEMPERATURE DRIFT COMPENSATION

The error due to low temperature drift of the AD8361 can be reduced if the temperature is known. Many systems incorporate a temperature sensor; the output of the sensor is typically digitized, facilitating a software correction. Using this information, only a two-point calibration at ambient is required.

The output voltage of the AD8361 at ambient (25°C) can be expressed by the equation:

$$V_{OUT} = \left(GAIN \times V_{IN}\right) + V_{OS}$$

where *GAIN* is the conversion gain in V/V rms and V_{OS} is the extrapolated output voltage for an input level of 0 V. GAIN and V_{OS} (also referred to as Intercept and Output Reference) can be calculated at ambient using a simple two-point calibration; that is, by measuring the output voltages for two specific input levels. Calibration at roughly 35 mV rms (–16 dBm) and 250 mV rms (+1 dBm) is recommended for maximum linear dynamic range. However, alternative levels and ranges can be

chosen to suit the application. GAIN and V_{OS} are then calculated using the equations:

$$GAIN = \frac{\left(V_{OUT2} - V_{OUT1}\right)}{\left(V_{IN2} - V_{IN1}\right)}$$

$$V_{OS} = V_{OUT1} - \left(GAIN \times V_{IN1}\right)$$

Both *GAIN* and V_{OS} drift over temperature. However, the drift of V_{OS} has a bigger influence on the error relative to the output. This can be seen by inserting data from Figures 14 and 17 (conversion gain and intercept drift) into the equation for V_{OUT}. These plots are consistent with Figures 10 and 11 which show that the error due to temperature drift decreases with increasing input level. This results from the offset error having a diminishing influence with increasing level on the overall measurement error.

From Figure 14, the average Intercept drift is 0.43 mV/°C from –40°C to +25°C and 0.17 mV/°C from +25°C to +85°C. For a less rigorous compensation scheme, the average drift over the complete temperature range can be calculated:

$$DRIFT_{VOS}\left(V/°C\right) = \left(\frac{0.010\,V - \left(-0.028\,V\right)}{+85°C - \left(-40°C\right)}\right)$$

$$= 0.000304 \text{ V/°C}$$

With the drift of V_{OS} included, the equation for V_{OUT} becomes:

$$V_{OUT} = \left(GAIN \times V_{IN}\right) + V_{OS} + DRIFT_{VOS} \times \left(TEMP - 25°C\right)$$

The equation can be rewritten to yield a temperature compensated value for V_{IN}.

$$V_{IN} = \frac{\left(V_{OUT} - V_{OS} - DRIFT_{VOS} \times \left(TEMP - 25°C\right)\right)}{GAIN}$$

EVALUATION BOARD

Figures 43 and 46 show the schematic of the AD8361 evaluation board. Note that uninstalled components are drawn in as dashed. The layout and silkscreen of the component side are shown in Figures 44, 45, 47, and 48. The board is powered by a single supply in the range, 2.7 V to 5.5 V. The power supply is decoupled by 100 pF and 0.01 µF capacitors. Additional decoupling, in the form of a series resistor or inductor in R6, can also be added. Table V details the various configuration options of the evaluation board.

Table V. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	Ground and Supply Vector Pins.	Not Applicable
SW1	Device Enable. When in Position A, the PWDN pin is connected to $+V_S$ and the AD8361 is in power-down mode. In Position B, the PWDN pin is grounded, putting the device in operating mode.	SW1 = B
SW2/SW3	Operating Mode. Selects either Ground Referenced Mode, Internal Reference Mode or Supply Reference Mode. See Table I for more details.	SW2 = A, SW3 = B (Ground Reference Mode)
C1, R2	Input Coupling. The 75 Ω resistor in position R2 combines with the AD8361's internal input impedance to give a broadband input impedance of around 50 Ω. For more precise matching at a particular frequency, R2 can be replaced by a different value (see Input Matching and Figure 39).	R2 = 75 Ω (Size 0402) C1 = 100 pF (Size 0402)
	Capacitor C1 ac-couples the input signal and creates a high-pass input filter whose corner frequency is equal to approximately 8 MHz. C1 can be increased for operation at lower frequencies. If resistive attenuation is desired at the input, series resistor R1, which is nominally 0 Ω, can be replaced by an appropriate value.	
C2, C3, R6	Power Supply Decoupling. The nominal supply decoupling of 0.01 µF and 100 pF. A series inductor or small resistor can be placed in R6 for additional decoupling.	C2 = 0.01 µF (Size 0402) C3 = 100 pF (Size 0402) R6 = 0 Ω (Size 0402)
C5	Filter Capacitor. The internal 50 pF averaging capacitor can be augmented by placing a capacitance in C5.	C5 = 1 nF (Size 0603)
C4, R5	Output Loading. Resistors and capacitors can be placed in C4 and R5 to load test V rms.	C4 = R5 = Open (Size 0603)

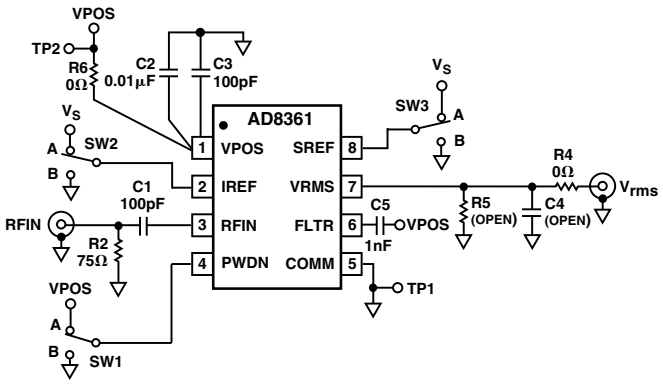


Figure 43. Evaluation Board Schematic micro_SOIC

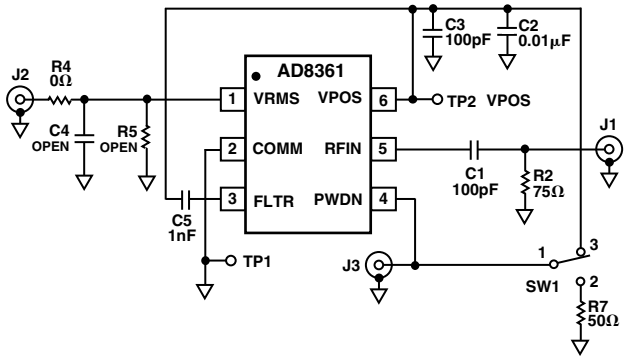


Figure 46. Evaluation Board Schematic, SOT-23-6L

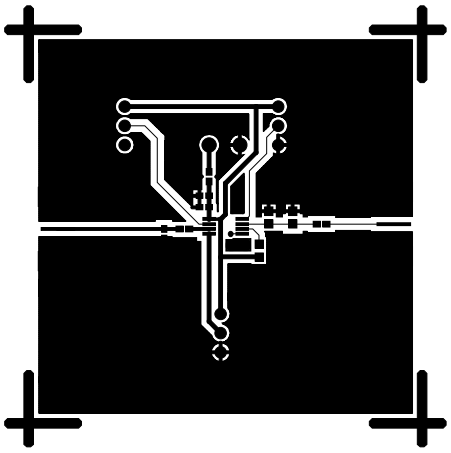


Figure 44. Layout of Component Side micro_SOIC

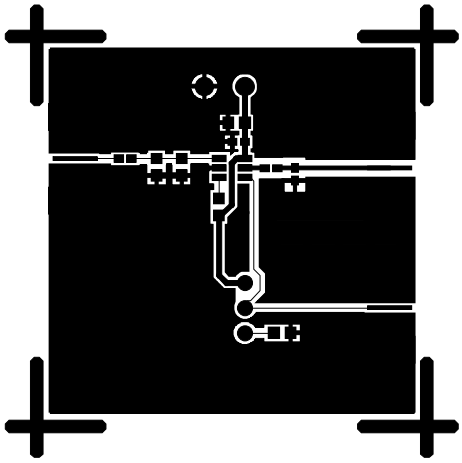


Figure 47. Layout of the Component Side, SOT-23-6L

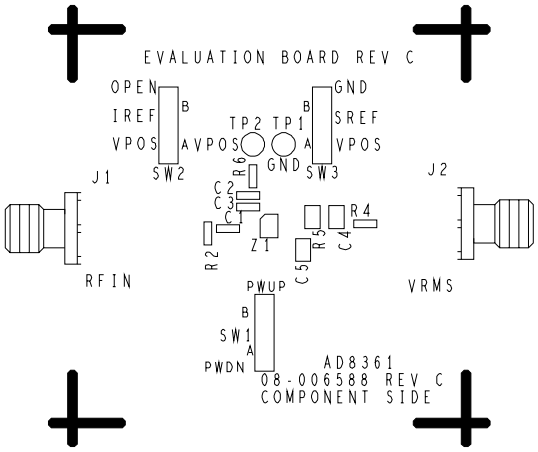


Figure 45. Silkscreen of Component Side micro_SOIC

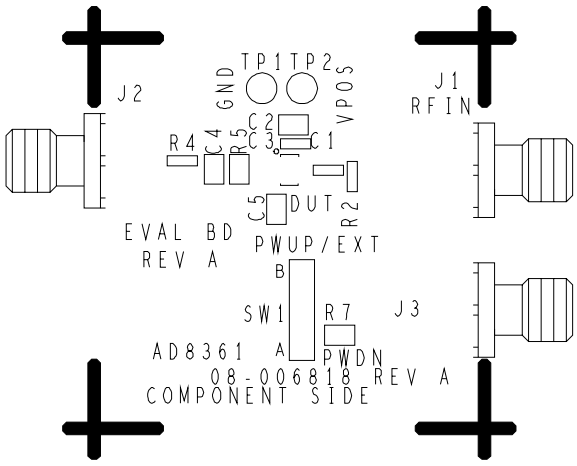


Figure 48. Silkscreen of the Component Side, SOT-23-6L

Problems caused by impedance mismatch may arise using the evaluation board to examine the AD8361 performance. One way to reduce these problems is to put a coaxial 3 dB attenuator on the RFIN SMA connector. Mismatches at the source, cable, and cable interconnection, as well as those occurring on the evaluation board can cause these problems.

A simple (and common) example of such problem is triple travel due to mismatch at both the source and the evaluation board. Here the signal from the source reaches the evaluation board and mismatch causes a reflection. When that reflection reaches the source mismatch, it causes a new reflection, which travels back to the evaluation board adding to the original signal incident at the board. The resultant voltage will vary with both cable length and frequency dependent upon the relative phase of the initial and reflected signals. Placing the 3 dB pad at the input of the board improves the match at the board and thus reduces the sensitivity to mismatches at the source. When such precautions are taken, measurements will be less sensitive to cable length and other fixturing issues. In an actual application when the distance between AD8361 and source is short and well defined, this 3 dB attenuator is not needed.

CHARACTERIZATION SETUPS

Equipment

The primary characterization setup is shown in Figure 50. The signal source used was a Rohde & Schwarz SMIQ03B, version 3.90HX. The modulated waveforms used for IS95 reverse link, IS95 nine active channels forward (Forward Link 18 setting), W-CDMA 4- and 15-channel were generated using the default settings coding and filtering. Signal levels were calibrated into a 50 Ω impedance.

Analysis

The conversion gain and output reference are derived using the coefficients of a linear regression performed on data collected in its central operating range (35 mV rms to 250 mV rms). This range was chosen to avoid areas of operation where offset distorts the linear response. Error is stated in two forms *Error from Linear Response to CW waveform* and *Output Delta from 25°C performance*.

The *Error from Linear Response to CW waveform* is the difference in output from the ideal output defined by the conversion gain and output reference. This is a measure of both the linearity of the device response to both CW and modulated waveforms. The error in dB uses the conversion gain multiplied times the input as its reference. *Error from Linear Response to CW waveform* is not a measure of absolute accuracy, since it is calculated using the gain and output reference of each device. But it does show the linearity and effect of modulation on the device response. *Error from 25°C performance* uses the performance of a given device and waveform type as the reference; it is predominantly a measure of output variation with temperature.

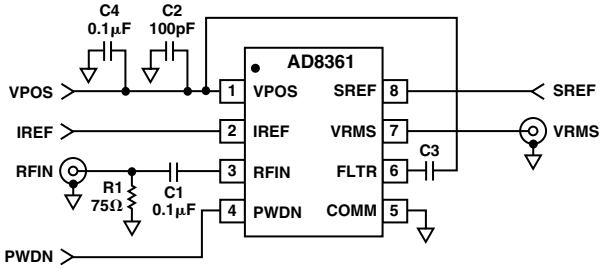


Figure 49. Characterization Board

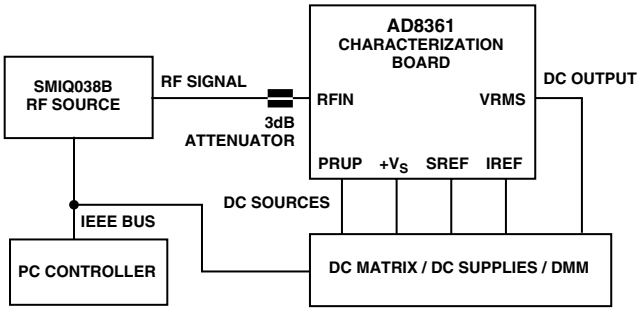
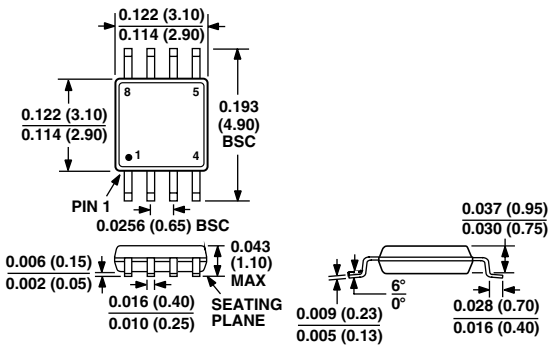


Figure 50. Characterization Setup

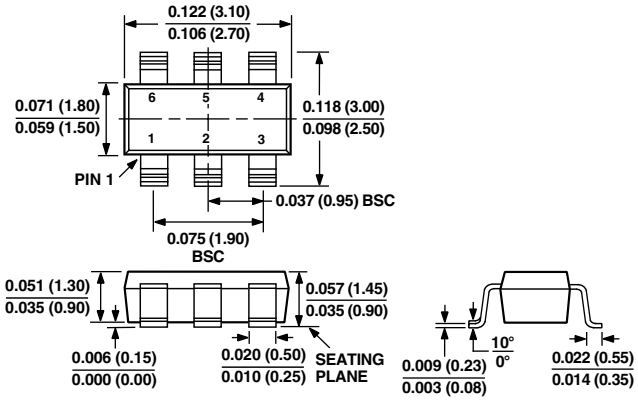
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead micro_SOIC Package (RM-8)



6-Lead SOT-23-6L Package (RT-6)



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