

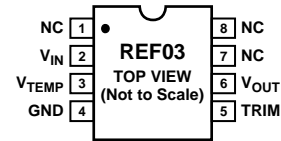
FEATURES

- 2.5 voltage output, $\pm 0.6\%$ max
- Wide input voltage range, 4.5 V to 33 V
- Supply current 1.4 mA max
- Output voltage tempco, 50 ppm/ $^{\circ}\text{C}$ max
- Line regulation, 50 ppm/V max
- Load regulation, 100 ppm/mA max
- Extended industrial temperature range, -40°C to $+85^{\circ}\text{C}$
- Low cost

GENERAL DESCRIPTION

The REF03 precision voltage reference provides a stable 2.5 V output, with minimal change for variations in supply voltage, ambient temperature, or loading conditions. Single-supply operation over an input voltage range of 4.5 V to 33 V with a current drain of 1 mA and good temperature stability is achieved using an improved band gap design. Primarily targeted at price sensitive applications, the REF03 is available in plastic mini DIPs and surface-mount small outline plastic packages. For improved performance or -40°C to $+125^{\circ}\text{C}$ operation, see the ADR03 data sheet.

PIN CONFIGURATION



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

Figure 1. 8-Lead PDIP (P-Suffix), 8-Lead SOIC (S-Suffix)

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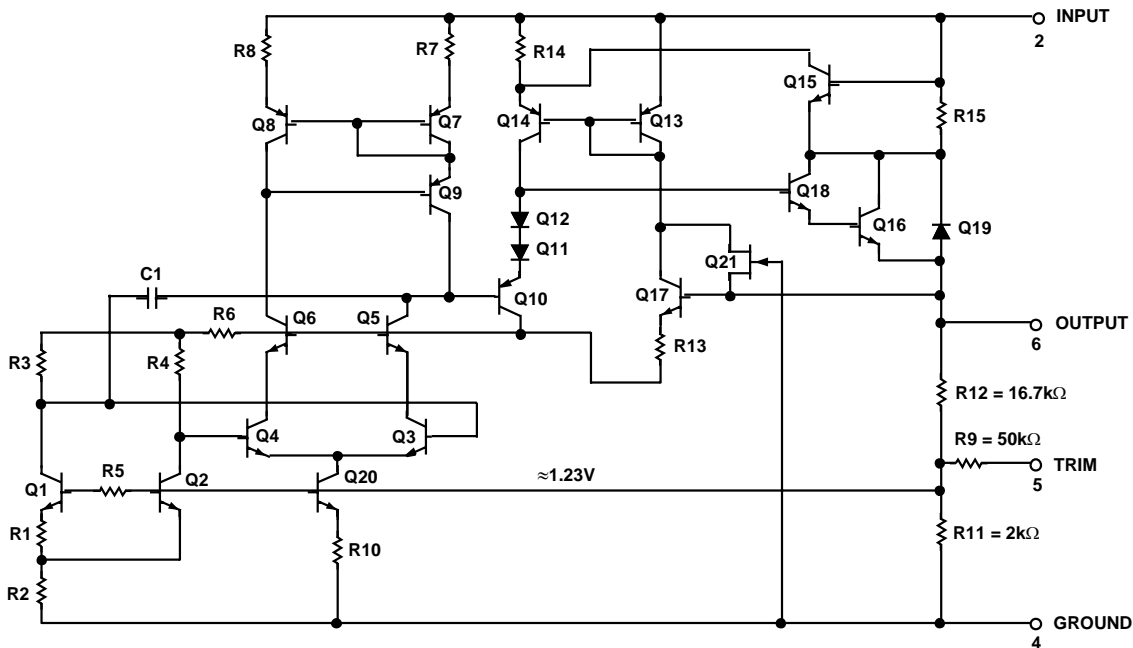


Figure 2. Simplified Schematic

00372-F-002

Rev. F

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REVISION HISTORY**6/04—Data Sheet changed from REV. E to REV. F**

Updated Formatting.....	Universal
Changes to SIMPLIFIED SCHEMATIC.....	1
Changes to ELECTRICAL SPECIFICATIONS	3
Changes to ORDERING GUIDE.....	8

2/04—Data Sheet changed from REV. D to REV. E.

Changes to SIMPLIFIED SCHEMATIC.....	1
Changes to ELECTRICAL SPECIFICATIONS	2
Changes to ORDERING GUIDE.....	3
Replaced TPC 1	4

8/03—Data Sheet changed from REV. C to REV. D.

Updated format.....	Universal
Change to FEATURES.....	1
Change to GENERAL DESCRIPTION	1
Deleted WAFER TEST LIMITS.....	2
Changes to ELECTRICAL SPECIFICATIONS	2
Changes to ORDERING GUIDE.....	3
Added OUTLINE DIMENSIONS	7

Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

@ $V_{IN} = 15\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	REF03G			Unit
			Min	Typ	Max	
Output Voltage	V_O	No Load	2.485	2.500	2.515	V
Output Voltage Tolerance		No Load		0.2	0.6	%
Output Voltage Temperature Coefficient ¹	TCV_O			10	50	ppm/ $^{\circ}\text{C}$
Line Regulation		$V_{IN} = 4.5\text{ V to }33\text{ V}$		20	50	ppm/V
Load Regulation		$I_L = 0\text{ mA to }10\text{ mA}$		0.002	0.005	%/V
Load Current (Sourcing)	I_L		10			ppm/mA
Load Current (Sinking)	I_S		-0.3	-0.5		%/mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground		24		mA
Quiescent Supply Current	I_{SY}	No Load		1.0	1.4	mA
Turn-On Settling Time ²	t_{ON}	To $\pm 0.1\%$ of Final Value		5		μs
Output Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		6		$\mu\text{V p-p}$
Output Adjustment Range	ΔV_{TRIM}	$R_{POT} = 10\text{ k}\Omega$	± 6	± 11		%
Input Voltage Range			4.5	15	33	V
Temperature Voltage Output ³	V_T			620		mV

¹ TCV_O is measured by the endpoint method, and is equal to

$$\frac{V(85^{\circ}\text{C}) - V(-40^{\circ}\text{C})}{(2.5 \times 10^{-6})(125^{\circ}\text{C})} \text{ in ppm}/^{\circ}\text{C}$$

² Guaranteed by design.

³ Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

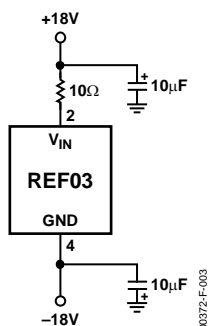


Figure 3. Burn-In Circuit

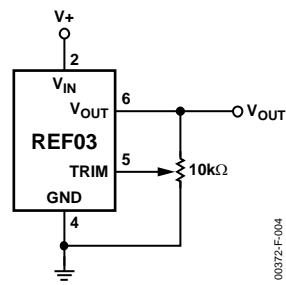


Figure 4. Output Voltage Trim Method

REF03

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Rating
Input Voltage	40 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
REF03G (P, S)	-40°C to $+85^\circ\text{C}$
Storage Temperature Range	-65°C to $+175^\circ\text{C}$
Junction Temperature Range	-65°C to $+175^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C

Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Package Thermal Resistance

Package Type	θ_{JA}^1	θ_{JC}	Unit
8-Lead PDIP (P)	110	50	$^\circ\text{C}/\text{W}$
8-Lead SOIC (S)	160	44	$^\circ\text{C}/\text{W}$

¹ θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for PDIP package; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

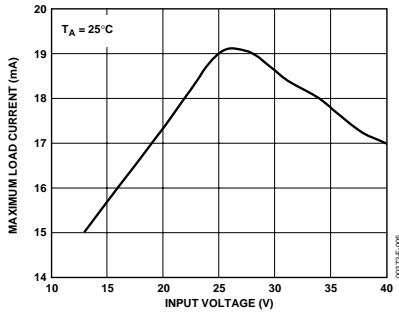


Figure 5. Maximum Load Current vs. Input Voltage

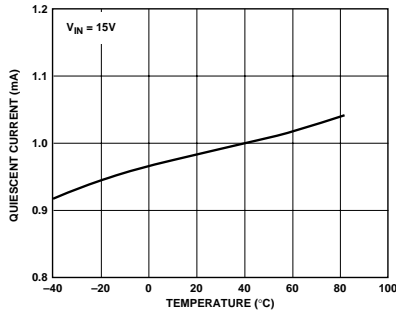


Figure 9. Quiescent Current vs. Temperature

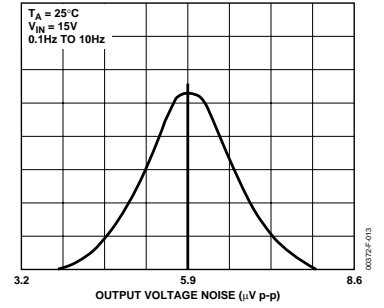


Figure 13. Typical Distribution of Output Voltage Noise

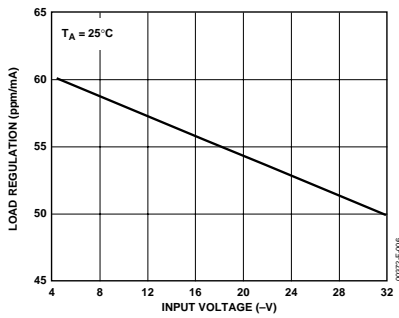


Figure 6. Load Regulation ($\Delta I_L = 10 \text{ mA}$) vs. Input Voltage

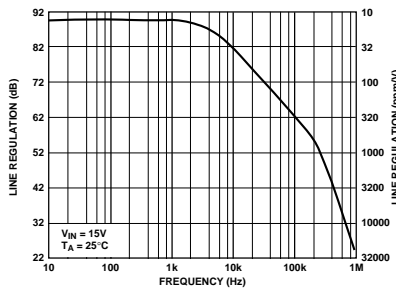


Figure 10. Line Regulation vs. Frequency

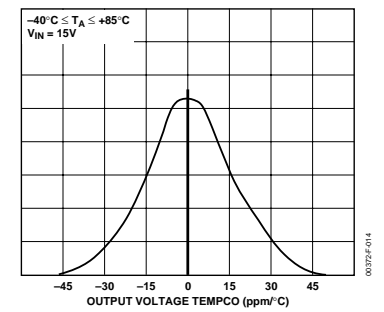


Figure 14. Typical Distribution of Output Voltage Tempco

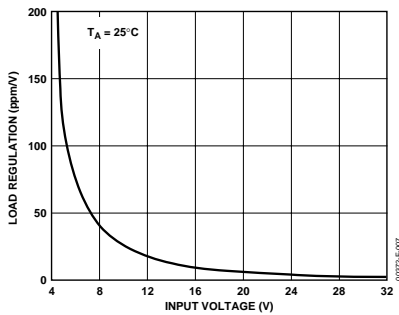


Figure 7. Line Regulation vs. Input Voltage

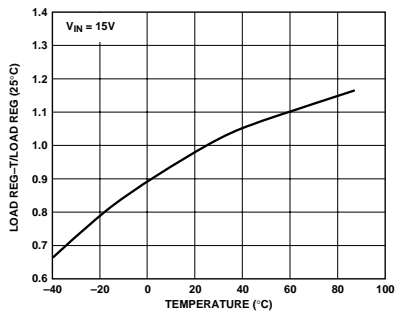


Figure 11. Normalized Load Regulation ($\Delta I_L = 10 \text{ mA}$) vs. Temperature

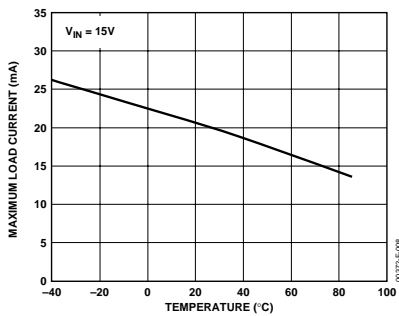


Figure 8. Maximum Load Current vs. Temperature

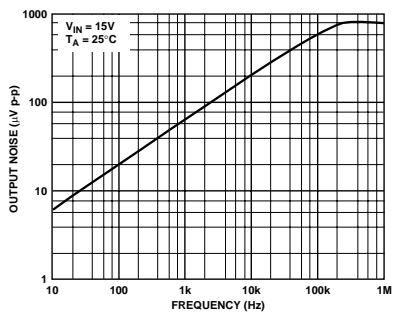


Figure 12. Wideband Output Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

APPLICATIONS

The REF03 provides a stable 2.5 V output voltage with minimal dependence on load current, line voltage, or temperature. This voltage is typically used to set an absolute reference point in data conversion circuits, or in analog circuits such as log amps, 4 to 20 mA transmitters and power supplies. The REF03 is of particular value in systems requiring a precision reference using a single 5 V supply rail.

Because an on-board operational amplifier is used to amplify the basic band gap cell voltage to 2.5 V, supply decoupling is critical to the transient performance of a voltage reference. The supply line should be bypassed with a 10 μF tantalum capacitor in parallel with a 0.01 μF to 0.1 μF ceramic capacitor for best results, as shown in Figure 15. The bypass capacitors should be located as close to the reference as possible. Inadequate bypassing can lead to instabilities.

Output bypass capacitors are not generally recommended. If necessary for high frequency output impedance reduction, the capacitance value used should be at least 1 μF .

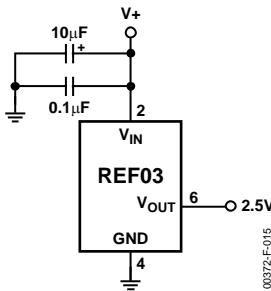


Figure 15. Basic Connections

GENERATING AN ADJUSTABLE BIPOLAR VOLTAGE REFERENCE

There is often a requirement for an adjustable bipolar reference. A simple method of generating such a reference is to connect the output of the REF03 to an op amp in an adjustable gain configuration, as shown in Figure 16. The trimmable resistor is then used to generate the desired output voltage from -2.5 V to $+2.5\text{ V}$.

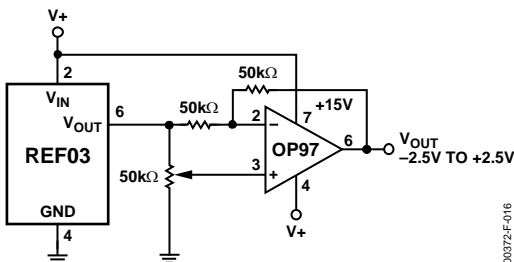


Figure 16. Adjustable Bipolar Reference

GENERATING A -2.5 V REFERENCE

Often, there is a requirement for a negative reference voltage. The simplest method of generating a -2.5 V reference with the REF03 is to connect an op amp in a gain of -1 to the output, as shown in Figure 17. This provides both positive and negative 2.5 V references. Figure 18 shows another method of obtaining a negative reference, in which the current-output element is a PNP transistor, with the REF03 in a servo loop to ensure that the output remains 2.5 V below ground.

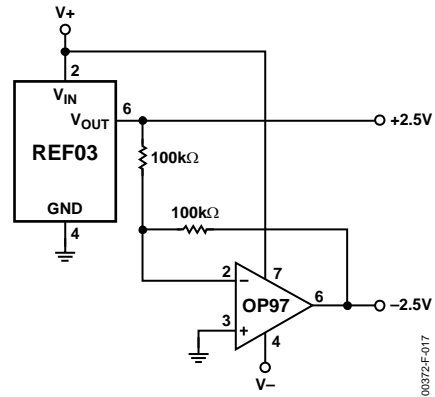


Figure 17. $\pm 2.5\text{ V}$ Reference

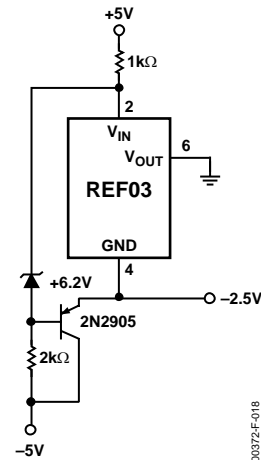


Figure 18. -2.5 V Reference

BOOST TRANSISTOR PROVIDES HIGH OUTPUT CURRENT

When applications require more than 10 mA current delivery, an external boost transistor may be added to the REF03 to pass the required current without dissipating excessive power within the IC. The maximum current output to the system is bounded only by the capabilities of the boost transistor. Figure 19 shows this technique, with and without current limiting.

Current limiting may be used to prevent damage to the boost transistor. Figure 19a is an example of no current limit, while Figure 19b shows the limit that occurs when the voltage

dropped across R2 exceeds one V_{BE} (0.6 V). The current limit is sensitive to the variations of the diodes' forward drop and the PNP's V_{BE} with temperature, and will decrease with increasing temperature.

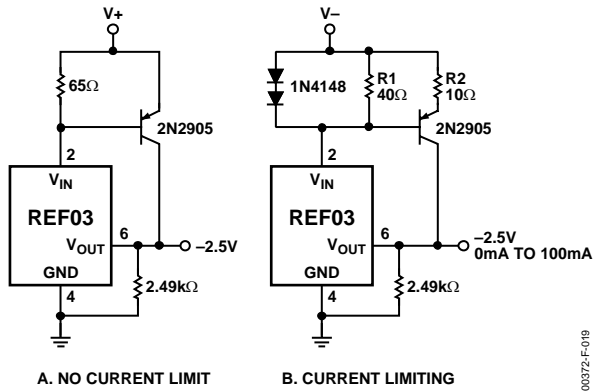
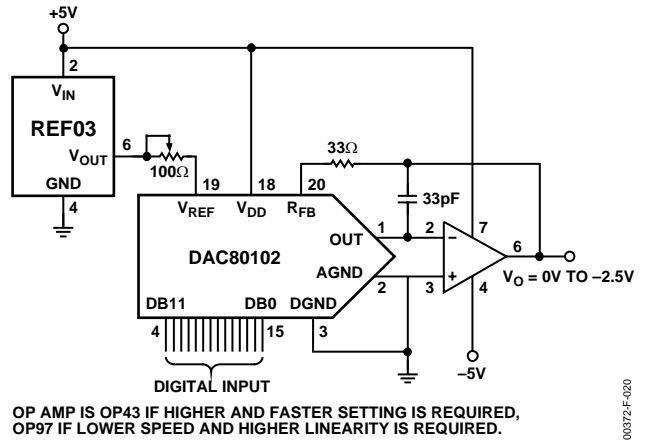


Figure 19. Output Current Boost

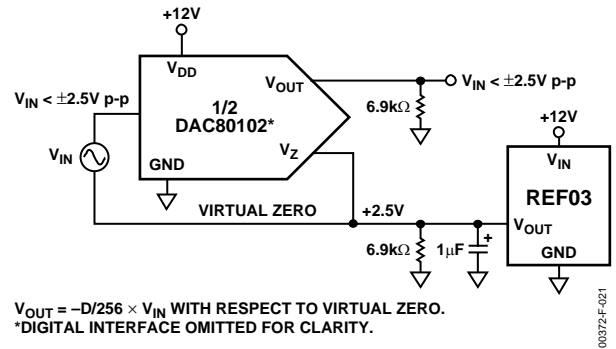
CMOS DAC REFERENCE

The REF03 makes an excellent reference for use with CMOS and bipolar DACs. Figure 20 shows the REF03 connected to the DAC8012, a 12-bit parallel loading CMOS DAC with memory. With an OP43 output amplifier for fast settling, the circuit requires less than 3 mA when driven from TTL gates, and less than 2 mA when driven from CMOS gates. In situations not requiring the higher speed of the OP43, enhanced linearity and some savings in power dissipation can be realized using an OP97 for the output amplifier. Figure 21 shows a typical multiplying DAC application using a REF03 reference.



OP AMP IS OP43 IF HIGHER AND FASTER SETTLING IS REQUIRED, OP97 IF LOWER SPEED AND HIGHER LINEARITY IS REQUIRED.

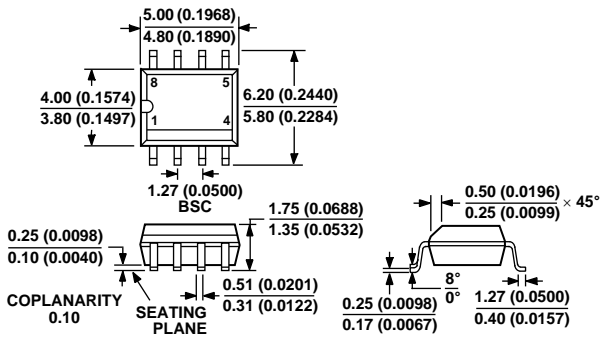
Figure 20. CMOS DAC Reference



$V_{OUT} = -D/256 \times V_{IN}$ WITH RESPECT TO VIRTUAL ZERO.
*DIGITAL INTERFACE OMITTED FOR CLARITY.

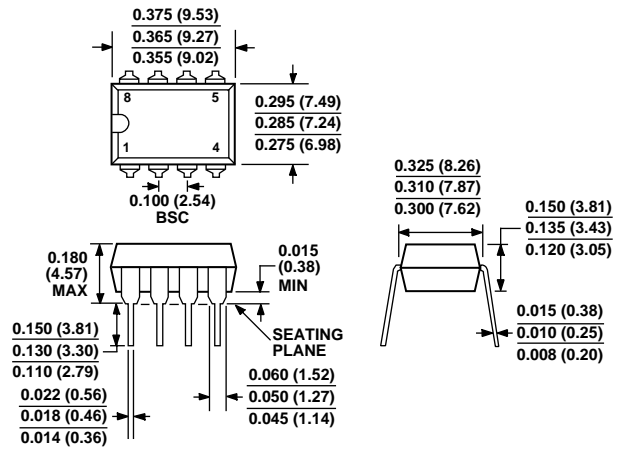
Figure 21. Multiplying CMOS DAC Reference

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 22. 8-Lead Standard Small Outline Package [SOIC]
 Narrow Body
 (R-8)
 S-Suffix
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-095AA
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 23. 8-Lead Plastic Dual In-Line Package [PDIP]
 (N-8)
 P-Suffix
 Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Part Number	Initial Accuracy	Temperature Coefficient	Temperature Range	Package Option
REF03GP ¹	0.2%	10	-40°C to +85°C	PDIP
REF03GS ²	0.2%	10	-40°C to +85°C	SOIC
REF03GS-REEL ²	0.2%	10	-40°C to +85°C	SOIC
REF03GS-REEL7 ²	0.2%	10	-40°C to +85°C	SOIC
REF03GSZ-REEL7 ^{2,3}	0.2%	10	-40°C to +85°C	SOIC

¹ Burn-in is available on commercial and industrial temperature range parts in PDIP package.

² For availability and burn-in information on SOIC package, contact your local sales office.

³ Z = Pb-free part.