CONEXANT™

RF109

2400 MHz Digital Spread Spectrum Transceiver

The RF109, a fully integrated transceiver device, provides the transmit, receive, and frequency synthesis functions for 2400 MHz digital spread spectrum systems operating in the 2400–2483.5 MHz portion of the ISM (Industrial, Scientific, Medical) band. The device has a direct conversion architecture that minimizes circuit complexity and cost.

The receive path of the RF109 provides complete RF-to-baseband I/Q demodulation, including an LNA, double-balanced quadrature mixers, fully integrated baseband filters, and baseband variable-gain amplifiers. The transmit path is a variable-gain direct conversion modulator. Figure 1 shows the RF109's pin signals. Figure 2 shows the RF109 block diagram.

The RF109 generates the Local Oscillator (LO) frequencies using a Phase Lock Loop (PLL) frequency synthesizer and an external 2.4 GHz Voltage Controlled Oscillator (VCO). The PLL provides a full frequency range of 2392.2–2505.6 MHz.

The RF109 features low-voltage operation (3.0–4.5V) for low power consumption. A complete RF system solution for 2.4 GHz cordless telephone applications can be constructed with the RF109, a power amplifier, a differential 2.4 GHz frequency source and a Transmit/Receive (T/R) switch.

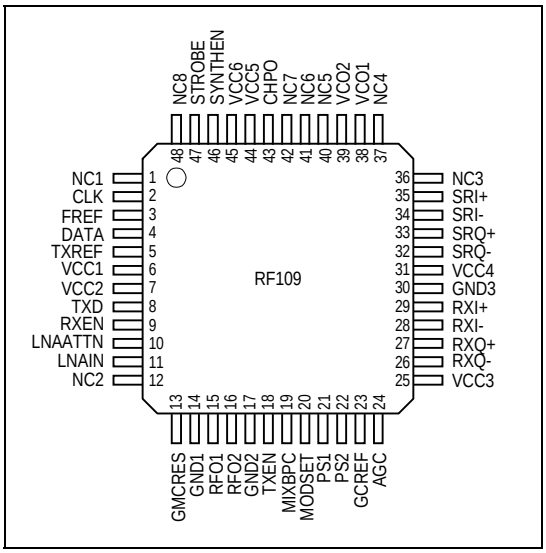


Figure 1. RF109 Pin Signals

Features

- Low power dissipation
- Fast settling from standby mode to active mode
- Separate enable lines for transmit, receive, and synthesizer
- 64 programmable channels with 1.8 MHz channel spacing
- 3-battery-cell operation
- 48-pin TQFP package with exposed paddle (refer to Figure 6)

- **Receiver**
  - LNA/Quadrature mixer from RF down to baseband
  - Selectable LNA gain
  - Integrated baseband filter with external bandwidth adjustment
  - Receiver baseband amplifier with automatic gain control
  - Direct conversion with differential baseband outputs
  - Low system noise figure (9.0 dB typical)
  - Large dynamic range (89 dB typical)

- **Transmitter**
  - Variable gain modulator
  - Mixer for baseband-to-RF modulation
  - Differential TX inputs and outputs
  - Selectable transmitter output levels for high, medium, and low power modes

Applications

- Digital Spread Spectrum (DSS) cordless telephone
- Direct sequence spread spectrum systems
- Frequency hopping spread spectrum systems
- Wireless LANs
- Wireless modems
- Wireless security
- Inventory control systems

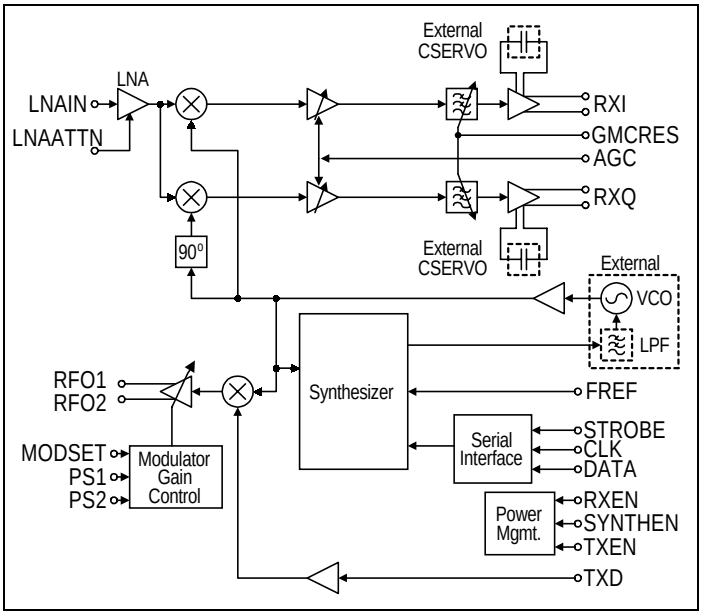


Figure 2. RF109 Block Diagram

Technical Description

Receive Path

The LNA provides two gain levels for coarse Automatic Gain Control (AGC), which are selected via the LNAATTN control. The signal is down-converted to In-phase and Quadrature-phase (I/Q) baseband signals using a matched pair of mixers and the LO.

The receive baseband bandwidth has a bandpass characteristic. The I/Q baseband signals are internally low-pass and high-pass filtered to attenuate out-of-channel signals and to remove DC components. The low-pass cutoff is determined by the GmC filters and is set by the R_{gmc} resistor connected to pin 13. The high-pass cutoff is set by the value of the C_{servo} capacitors connected between pins 32–33, and pins 34–35.

The baseband high-pass cutoff frequency should be set much lower than the low-pass cutoff frequency or else the servo loop will become unstable.

The optimum receive bandwidth values are:

f_{LPF} = 820 kHz, R_{gmc} = 825 Ω
f_{HPF} = 20 kHz, C_{servo} = 0.082 µF

A matched pair of VGAs provide fine AGC. The differential I/Q baseband signals are DC-coupled to the RXI+, RXI-, RXQ+, and RXQ- outputs, respectively.

Transmit Path

The transmit path consists of an amplifier and a mixer. The mixer modulates the LO with baseband data supplied to pin 8.

The transmit RF outputs from the RF109 are differential and matched for a 100Ω differential load. If a single-ended connection is required, then the unused output must be suitably terminated by a 50Ω resistor (as shown in Figure 5).

The transmit output power is determined by the output power control inputs, PS1 (pin 21) and PS2 (pin 22), and by the value of R_{mod} (connected to pin 20). R_{mod} sets the bias current into the modulator which is then multiplied by a factor set by the state of PS1 and PS2. PS1 and PS2 input programming is given in the Transmitter Section of Table 3.

LO Generation

The LO is generated by a programmable PLL frequency synthesizer and a 2.4 GHz external VCO. Synthesizer performance parameters are determined by the loop filter, the external reference oscillator, the sensitivity and phase noise of the VCO, and the frequency synthesizer programming.

The RF109 requires differential inputs for VCO1 (pin 38) and VCO2 (pin 39). The typical differential input level is 200 mVp-p. A BALUN transformer, shown in Figure 5, is used to generate differential signals from a single-ended VCO output.

Synthesizer Programming

The frequency synthesizer block is comprised of a divide-by-3 counter (D), 9.6 MHz reference frequency (FREF) source, a fixed reference divider of 16 (R), 16/17 prescaler (M), a fixed counter of 83 (N), a programmable counter of 64 (A),an external loop filter, and a 2.4 GHz external VCO.

The synthesizer can be programmed to cover 64 channels (channel spacing = 1.8 MHz) from 2392.2 MHz to 2505.6 MHz Table 1).

The LO frequency is given by the following equation:

$$\mathbf{f_{LO} = (D) \times (FREF/R) \times ((M \times N) + (A + 1)),}\ \text{where } N > A.$$

Example:

$f_{LO} = 3 \times (9.6\ \text{MHz} / 16) \times ((16 \times 83) + 7) = 2403.0\ \text{MHz}$

$f_{LO} = 3 \times (9.6\ \text{MHz} / 16) \times ((16 \times 83) + 46) = 2473.2\ \text{MHz}$

Data Format. The synthesizer is programmed with a half-duplex 3-wire serial interface. The three signals are DATA, CLK, and STROBE. Each rising edge of the CLK signal shifts one bit of the data into a shift register. When the STROBE input is toggled from low to high, the data latched in the shift register is transferred to the A counter. The data format is as follows:

MSB								LSB
	S7	S6	S5	S4	S3	S2	S1	S0

The timing relationship is shown in Figure 4. Programming bits S0 to S5, used for the A counter, are defined in Table 1. Bits S6 and S7 are reserved.

Synthesizer Loop Filter. A typical loop filter design is shown below in Figure 3. The loop bandwidth is approximately 5 kHz with a nominal phase margin of 45 degrees for a VCO sensitivity of 60 MHz/V.

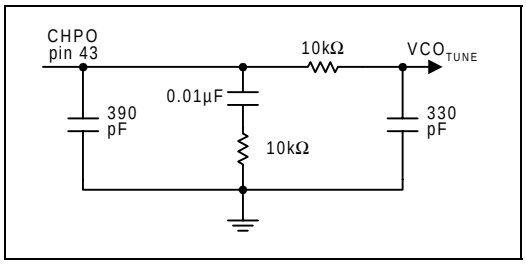


Figure 3. Typical Loop Filter

Power Management

Independent power-up/power-down control of the transmit path, receive path, and frequency synthesizer is provided by the TXEN, RXEN and SYNTHEN controls, respectively. When all of the functions are powered down, the current drain from the voltage supply (Vcc) is at a minimum.

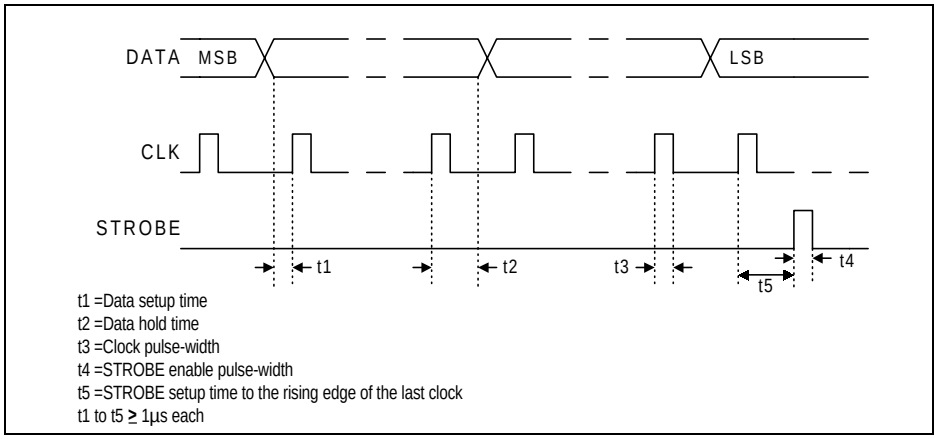


Figure 4. Timing Diagram

Table 1. Swallow Counter Data Input

Synth. Channel No. (A)	Frequency (MHz)	S5	S4	S3	S2	S1	S0
0	2392.2	0	0	0	0	0	0
1	2394.0	0	0	0	0	0	1
2	2395.8	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
6	2403.0	0	0	0	1	1	0
7	2404.8	0	0	0	1	1	1
8	2406.6	0	0	1	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
25	2437.2	0	1	1	0	0	1
26	2439.0	0	1	1	0	1	0
27	2440.8	0	1	1	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
45	2473.2	1	0	1	1	0	1
46	2475.0	1	0	1	1	1	0
47	2476.8	1	0	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
61	2502.0	1	1	1	1	0	1
62	2503.8	1	1	1	1	1	0
63	2505.6	1	1	1	1	1	1

Recommendations on Layout and Implementation

A typical applications schematic is shown in Figure 5.

Decouple all Vcc pins as close as possible to the supply pin.

All ground pins should have minimum trace inductance to ground. If a ground plane cannot be provided right at the pins, the vias to the ground plane should be placed as close to the pins as possible. There should be one via for each ground pin. If the ground plane is at the bottom layer, it is recommended to have two vias in parallel for each ground pin.

Connect all no connect (NC) pins to the ground.

VCC1 (pin 6), VCC2 (pin 7), VCC3 (pin 25), and VCC4 (pin 31) should be connected to the common Vcc supply through individual decoupling networks.

RTXD should be chosen to provide a typical baseband spread spectrum signal level of 0.10 Vp-p, to the TXD pin (pin 8).

The routing of the trace to pin 3 (FREF) is very important to minimize the coupling of the reference clock (9.6 MHz) into the LO. The FREF trace should be well isolated from all other traces, preferably by grounded strips on either side of the trace.

All traces from the VCO to pins 38 and 39 should be as short as possible with a characteristic impedance of 50 Ω.

Exposed Paddle Soldering

The RF109 48-pin TQFP package has an exposed (metal) paddle on the bottom. The footprint dimensions of the exposed paddle are shown in Figure 6. The printed circuit board should provide through hole connections to the ground plane to ground the exposed paddle. The solder mask opening should have the same size as the exposed paddle. All relevant manufacturing considerations for this type of package should be taken into account.

ESD Sensitivity

The RF109 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper Electrostatic Discharge (ESD) precautions.

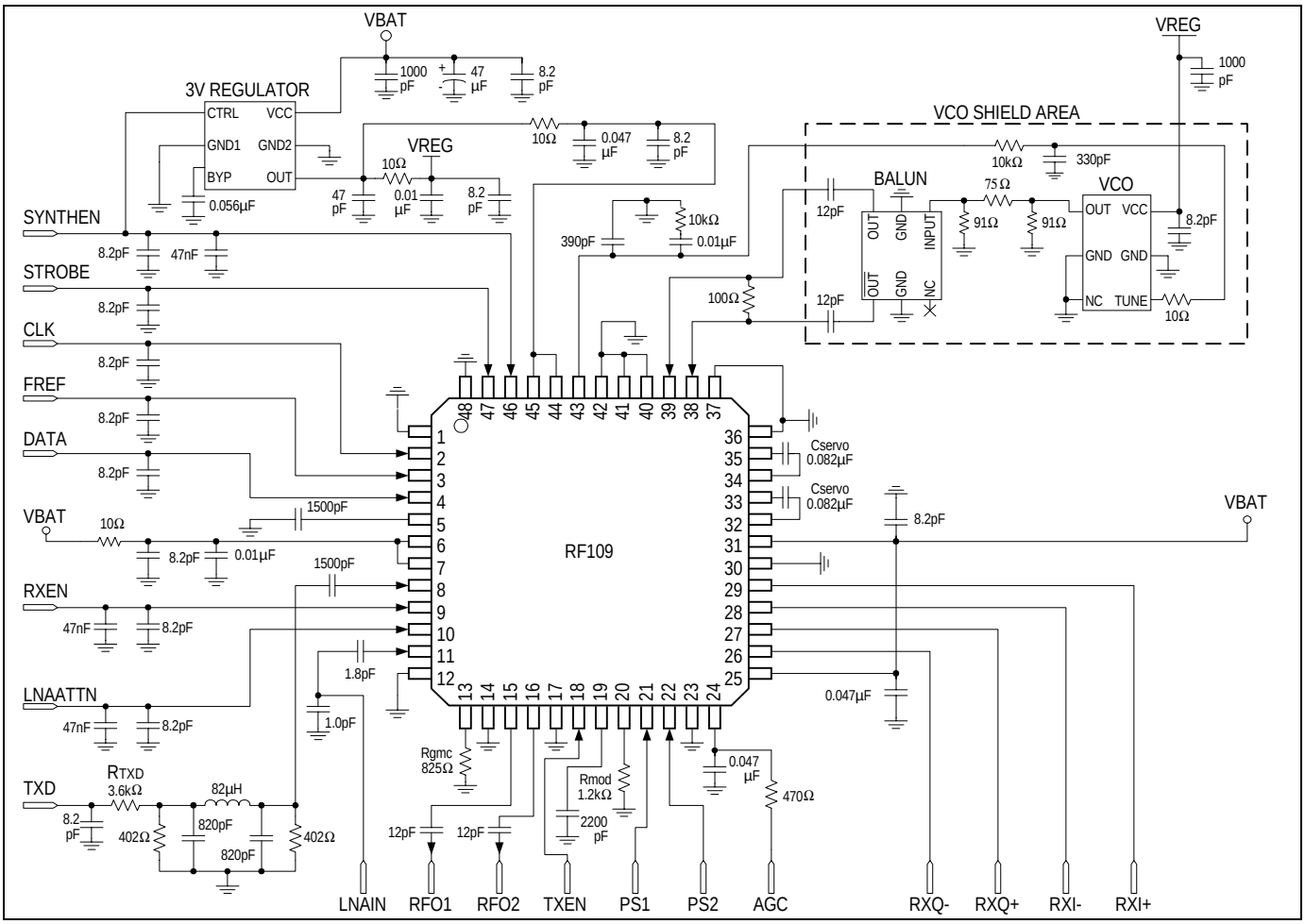


Figure 5. Typical Application Diagram – RF109

Interface Description

Table 2. RF109 Pin Signal Description (1 of 2)

Pin	Signal	Type	Description
			Digital Signals[1]
18	TXEN	Input	**Transmit Enable.** Switches on/off bias power to the transmitter circuitry. 1: Tx on 0: Tx off
9	RXEN	Input	**Receive Enable.** Switches on/off bias power to the receiver circuitry. 1: Rx on 0: Rx off
46	SYNTHEN	Input	**Synthesizer Enable.** Switches on/off bias power to the synthesizer circuitry. 1: Synthesizer on 0: Synthesizer off
21 22	PS1 PS2	Input Input	**Transmit Power.** These two control bits select the PA output power. PS1=0, PS2=0: High (–8 dBm typical, single-ended) PS1=0, PS2=1: Medium (–18 dBm typical, single-ended) PS1=1, PS2=0: Low (–26.5 dBm typical, single-ended) PS1=1, PS2=1: Undefined
10	LNAATTN	Input	**LNA Attenuator.** This control signal toggles the LNA gain between the low gain state and the high gain state. 1: Low gain, attenuator enabled 0: High gain, attenuator disabled
3	FREF	Input	**Reference Oscillator.** This digital input clock signal is used to provide the reference frequency for the synthesizer. A 9.6 MHz clock provides channel spacing of 1.8 MHz (see Table 1).
2	CLK	Input	**Synthesizer Programming Clock.** This is the clock input signal used to serially shift the synthesizer data bits into the synthesizer input register. The rising edge of CLK is used to load each data bit.
4	DATA	Input	**Synthesizer Programming Data.** This is the serial data input bit stream used to program the synthesizer. Data bits are shifted from MSB first to LSB. The DATA bit is loaded into the synthesizer input register on the rising edge of the CLK signal.
47	STROBE	Input	**Synthesizer Programming Strobe.** This signal is used to transfer the synthesizer data bits from the input register to the pulse swallow counter, after all of the data bits have been shifted in. The data is transferred on the rising edge of the STROBE signal.
			Analog Signals
8	TXD	Input	**Transmit Data.** This input signal is used as the modulating signal. TXD is a single-ended, 1.2 Mbps NRZ signal from the baseband modem. The TXD signal shall be filtered first if any data/spectral shaping is desired. A resistor divider should be used to provide the desired signal level at the TXD input of the RF109.
5	TXREF	Input	**Tx Reference.** This is the reference for the TXD input. It is AC-coupled to ground.
23	GCREF	Input	**Gain Control Reference.** This is the reference for the gain control input. It is connected to ground.
28 29	RXI- RXI+	Output Output	**Received In-Phase Signal Negative, Received In-Phase Signal Positive.** This differential signal pair is the in-phase portion of the baseband output of the receiver. The differential output signal level is typically 0.5 Vp-p, within the AGC operating range of 1.35–1.9 V.
26 27	RXQ- RXQ+	Output Output	**Received Quadrature Signal Negative, Received Quadrature Signal Positive.** This differential signal pair is the quadrature portion of the baseband output of the receiver. The differential output signal level is typically 0.5 Vp-p, within the AGC operating range of 1.35–1.9 V.
24	AGC	Input	**Auto Gain Control.** This analog input signal is used to control the gain of the baseband VGAs in the receiver. This signal is generated by the baseband ASIC as part of the AGC control loop. An increase in the AGC voltage decreases the baseband VGA gain. The control loop provides a typical receive baseband differential signal of 0.5 Vp-p over the VAGC range of 1.35–1.9 V.
38 39	VCO1 VCO2	Input Input	**Voltage Controlled Oscillator.** This differential input provides the local oscillator signal from an external VCO to the RF109 mixers. An external BALUN may be used to convert a single-ended external VCO signal to the differential signals, VCO1 and VCO2, required by the RF109. The differential input signal level required is typically 200 mVp-p.
43	CHPO	Output	**Charge Pump Output.** This output signal is used to control the external 2.4 GHz VCO. The CHPO current is typically ±250 µA.
11	LNAIN	Input	**RF Input.** This is the received RF input signal that is routed to the LNA of the RF109. This pin should be externally matched to 50 Ω. The received signal must be AC coupled into LNAIN with a 12 pF series capacitor.
15 16	RFO1 RFO2	Output	**RF Output.** These are the differential transmit output signals from the RF109. The single-ended output impedance is 50 Ω. The RF output signals are internally AC-coupled. The unused signal should be terminated to ground through a 50 Ω resistor.

Table 2. RF109 Pin Signal Description (2 of 2)

Pin	Signal	Type	Description
Miscellaneous			
20	MODSET	—	**Modulator Gain Setting.** Transmit modulator gain can be adjusted by the resistor connected to the pin.
13	GMCRES	—	GMC resistor to set the cutoff frequency of the baseband filter.
19	MIXBPC	—	Mixer bias bypass capacitor.
32 33	SRQ- SRQ+	—	Q channel DC offset cancellation servo capacitor connections.
34 35	SRI- SRI+	—	I channel DC offset cancellation servo capacitor connections.
1, 12, 36, 37, 40, 41, 42, 48	NC	—	**No Connect.** It is recommended to connect these pins to ground.
Power Supply Terminals			
6	VCC1	Supply	Positive supply terminal.
7	VCC2	Supply	Positive supply terminal.
25	VCC3	Supply	Positive supply terminal.
31	VCC4	Supply	Positive supply terminal.
44	VCC5	Supply	Positive supply terminal.
45	VCC6	Supply	Positive supply terminal.
14, 17, 30	GND	Supply	Power supply ground terminal.

Notes:

1. All digital signals are CMOS compatible.

Specifications

Table 3. Electrical Specifications[1] (1 of 3)

Note: T_A = 25°C, V_{CC} = 3.6 V, f_{LO}= 2449.8 MHz

Parameter		Min	Typical	Max	Units
Receiver Section					
RX voltage gain:	LNA high-gain mode (LNAATTN = 0) GC = 1.35 V GC = 1.65 V GC = 1.9 V	94.5	 100 76 37	105.5	dB
LNA gain step	delta Gain LNAATTN = 0/1		27		dB
RX gain variation vs. frequency	2400 MHz < f_{LO} < 2483.5 MHz	–1.5	0.5	2.0	dB
RX SSB noise figure:	High-gain mode, GC = 1.35 V		9		dB
RX input IP3:	LNA high-gain mode, GC = 1.9 V LNA low-gain mode, GC = 1.9 V		–33 –3		dBm
RX input P1dB:	LNA high-gain mode (LNAATTN = 0) GC = 1.35 V GC = 1.65 V GC = 1.9 V LNA low-gain mode (LNAATTN = 1) GC = 1.9 V		 –90.5 –65 –36 –10		dBm
I/Q phase imbalance				±7	deg
I/Q amplitude imbalance				3	dB
Input high voltage, LNAATTN, RXEN	VIH	1.9			V
Input low voltage, LNAATTN, RXEN	VIL			0.75	
Input high current, RXEN	IIH		125	200	µA
Input low current , RXEN	IIL	–10		10	
Input high current, LNAATTN	IIH			60	µA
Input low current, LNAATTN	IIL	–10			
GC Iin		–500		500	µA
Baseband amplifier gain control range (GC = 1.35–1.9 V)			63		dB
GC input voltage range		1.35	1.65	1.9	V
Baseband amplifier gain control sensitivity	GC = 1.35–1.9 V GC = 1.35 V GC = 1.65 V GC = 1.90 V		0.14 0.01 0.15 0.13	0.17	dB/mV
RX P1dB @ 3.9 MHz offset	LNA high gain, GC=1.9V		–24		dBm
Baseband output load capacitance			20	50	pF
Baseband LPF 3 dB bandwidth (Rgmc = 825 Ω)		650	820	970	kHz
Baseband selectivity @ 3.9 MHz		60	70		dB
Baseband common mode output		1.0	Vcc – 1.55	Vcc – 1.0	V
Baseband I,Q DC offset				25	mV
RXI, RXQ DC and gain settle time[2] from initial RXEN input at TDD rate > 250 Hz			50	100	µs
Baseband HPF 3dB bandwidth (servo capacitors = 82 nF)		13	22	29	kHz
Baseband output voltage swing (peak differential)			250		mVp
Baseband output SNR (GC = 1.9 V)			31		dB

Table 3. Electrical Specifications (2 of 3)

Parameter		Min	Typical	Max	Units
Transmitter Section					
Gain variation vs. frequency	2400 MHz < f_{LO} < 2483.5 MHz		0.5	1.5	dB
Peak-envelope output power (single-ended):[3] High power mode (PS1 = 0, PS2 = 0) Medium power mode (PS1 = 0, PS2 = 1) Low power mode (PS1 = 1, PS2 = 0) Undefined mode (PS1 = 1, PS2 = 1)		–10.5	–8.0 –18 –26.5 not used	–5.0	dBm
IM3	(TXD input signal 2 tones each 60 mVpp)		–35		dBc
LO suppression relative to peak			–25	–15	dBc
TXD input impedance			10		kΩ
TXD input peak-to-peak baseband spread spectrum signal for specified output peak envelope power			100		mV_{pp}
TXD input bandwidth			80		MHz
TXD to RF settle time to within spec value from TXEN				50	µs
Input high voltage, PS1, PS2, TXEN Input low voltage, PS1, PS2, TXEN	VIH VIL	1.9		 0.75	V
Input high current, PS1, PS2, TXEN Input low current, PS1, PS2, TXEN	IIH IIL	 –10		60	µA
Input high current TXEN Input low current TXEN	IIH IIL	 –10		100	µA
Frequency Synthesizer Section					
Synthesizer frequency range		2392.2		2505.6	MHz
Differential LO input power across VCO1 and VCO2		–17	–13	–9	dBm
Input reference frequency, FREF			9.6		MHz
Frequency step, F_S			1800		kHz
Comparison frequency (600 kHz) spur level				–60	dBc
Input high voltage, STROBE, CLK, DATA, SYNTHEN Input low voltage, STROBE, CLK, DATA, SYNTHEN	VIH VIL	1.9		 0.75	V
Input high current, STROBE, CLK, DATA Input low current, STROBE, CLK, DATA	IIH IIL	 –10		40	µA
Input high current, SYNTHEN Input low current, SYNTHEN	IIH IIL	 –10		100	µA
Input high voltage, FREF Input low voltage, FREF	VIH VIL	1.9		 0.75	V
Input high current, FREF Input low current, FREF	IIH IIL	 –10		100	µA
Charge-pump output current			±250		µA
Output short-circuit current	CHPO			1.0	mA

Table 3. Electrical Specifications (3 of 3)

Parameter		Min	Typical	Max	Units
Power Supply					
Total supply current:					
RX mode (RXEN, SYNTHEN = 1)		67	89	111	mA
TX + SYNTH supply current:(3)	High power mode	31	41	51	mA
	Medium power mode		33		mA
	Low power mode		31		mA
Synth mode (SYNTHEN = 1)			25		mA
Sleep mode (RXEN, TXEN, SYNTHEN, LNAATTN = 0)			5	100	µA
Power supply range(1)		3.0	3.6	4.5	VDC

Notes:

1. The specifications in Table 3 are guaranteed at a supply voltage of 3.6 VDC, and T_A = 25°C.
2. Gain settled to within 90% of final value, DC settled to within 10% of desired signal's final value.
3. TXD input signal 120 mVpp, 300 kHz sinusoidal at pin 8, Rmod = 1.2 kΩ.

Table 4. Absolute Maximum Ratings

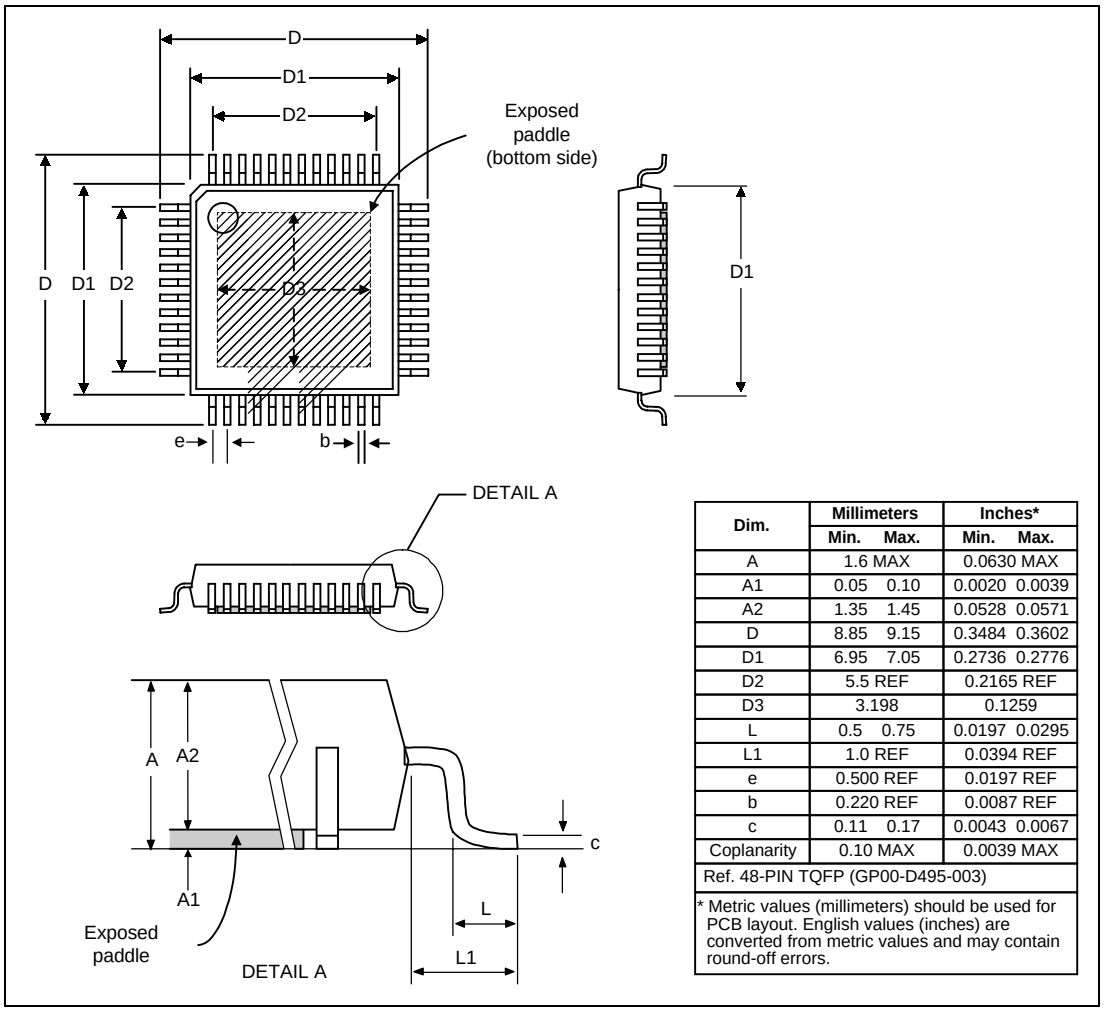
Parameter	Min	Max	Unit
Supply voltage (Vcc)[1]	–0.3	5	V
Input voltage range[1]	–0.3	VCC	V
Power dissipation		700	mW
LNA input power		+5	dBm
Operating temperature range (T_A)	–10	70	°C
Storage temperature	–40	125	°C

Notes:

1. Voltages are referenced to GND.

Device Dimensions

RF109 device dimensions are shown below in Figure 6.



Dim.	Millimeters		Inches*	
	Min.	Max.	Min.	Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.10	0.0020	0.0039
A2	1.35	1.45	0.0528	0.0571
D	8.85	9.15	0.3484	0.3602
D1	6.95	7.05	0.2736	0.2776
D2	5.5 REF		0.2165 REF	
D3	3.198		0.1259	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.500 REF		0.0197 REF	
b	0.220 REF		0.0087 REF	
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.10 MAX		0.0039 MAX	
Ref. 48-PIN TQFP (GP00-D495-003)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

Figure 6. RF109 Device Dimensions

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