

2.5A, 30V, 0.150 Ohm, Dual P-Channel LittleFET™ Power MOSFET

The RF1K49223 Dual P-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This device can be operated directly from integrated circuits.

Formerly developmental type TA49223.

Ordering Information

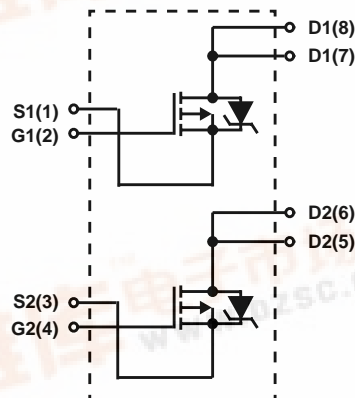
| PART NUMBER | PACKAGE | BRAND |
|-------------|----------|-----------|
| RF1K49223 | MS-012AA | RF1K49223 |

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4922396.

Features

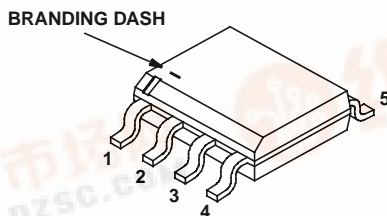
- 2.5A, 30V
- $r_{DS(ON)} = 0.150\Omega$
- Temperature Compensating PSPICE® Model
- Thermal Impedance PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC MS-012AA



RF1K49223

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

| | RF1K49223 | UNITS |
|-------------------------------------------------------|-----------------------------|---------------------|
| Drain to Source Voltage | -30 | V |
| Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) | -30 | V |
| Gate to Source Voltage | ± 20 | V |
| Drain Current | | |
| Continuous (Pulse Width = 5s) | 2.5 | A |
| Pulsed | Refer to Peak Current Curve | |
| Pulsed Avalanche Rating | Refer to UIS Curve | |
| Power Dissipation | 2 | W |
| Derate Above 25°C | 0.016 | W/ $^\circ\text{C}$ |
| Operating and Storage Temperature | -55 to 150 | $^\circ\text{C}$ |
| Maximum Temperature for Soldering | | |
| Leads at 0.063in (1.6mm) from Case for 10s | 300 | $^\circ\text{C}$ |
| Package Body for 10s, See Techbrief 334 | 260 | $^\circ\text{C}$ |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS | |
|----------------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|-----|-----------|-------|---------------------------|
| Drain to Source Breakdown Voltage | BV_{DSS} | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, (Figure 12) | -30 | - | - | V | |
| Gate to Source Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$, (Figure 11) | -1 | - | -3 | V | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -30\text{V}$, $V_{GS} = 0\text{V}$ | $T_A = 25^\circ\text{C}$ | - | - | -1 | μA |
| | | | $T_A = 150^\circ\text{C}$ | - | - | -50 | μA |
| Gate to Source Leakage Current | I_{GSS} | $V_{GS} = \pm 20\text{V}$ | - | - | ± 100 | nA | |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D = 2.5\text{A}$, (Figure 9, 10) | $V_{GS} = -10\text{V}$ | - | - | 0.150 | Ω |
| | | | $V_{GS} = -4.5\text{V}$ | - | - | 0.360 | Ω |
| Turn-On Time | t_{ON} | $V_{DD} = -15\text{V}$, $I_D \cong 2.5\text{A}$, $R_L = 6\Omega$, $V_{GS} = -10\text{V}$, $R_{GS} = 25\Omega$ | - | - | 40 | ns | |
| Turn-On Delay Time | $t_{d(ON)}$ | | - | 9 | - | ns | |
| Rise Time | t_r | | - | 19 | - | ns | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 60 | - | ns | |
| Fall Time | t_f | | - | 34 | - | ns | |
| Turn-Off Time | t_{OFF} | | - | - | 140 | ns | |
| Total Gate Charge | $Q_{g(TOT)}$ | | $V_{GS} = 0\text{V}$ to -20V | - | 28 | 35 | nC |
| Gate Charge at -10V | $Q_{g(-10)}$ | $V_{GS} = 0\text{V}$ to -10V | - | 15 | 19 | nC | |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS} = 0\text{V}$ to -2V | - | 1.5 | 1.9 | nC | |
| Input Capacitance | C_{ISS} | $V_{DS} = -25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 13) | - | 580 | - | pF | |
| Output Capacitance | C_{OSS} | | - | 260 | - | pF | |
| Reverse Transfer Capacitance | C_{RSS} | | - | 38 | - | pF | |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | Pulse Width = 1s Device mounted on FR-4 material | - | - | 62.5 | $^\circ\text{C}/\text{W}$ |

Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|----------|------------------------------------------------------------------|-----|-----|-------|-------|
| Source to Drain Diode Voltage | V_{SD} | $I_{SD} = -2.5\text{A}$ | - | - | -1.25 | V |
| Reverse Recovery Time | t_{rr} | $I_{SD} = -2.5\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | - | 49 | ns |

Typical Performance Curves

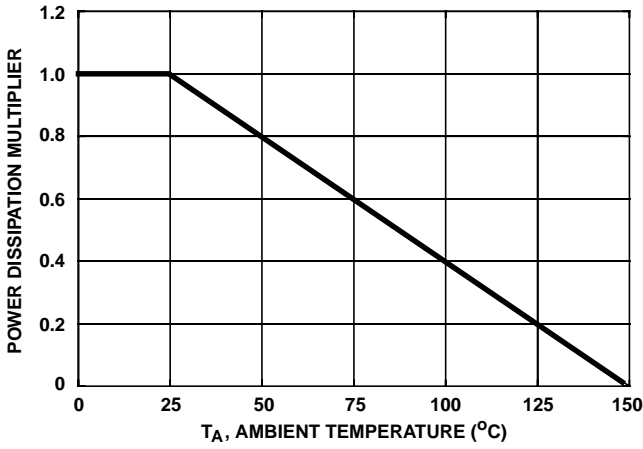


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

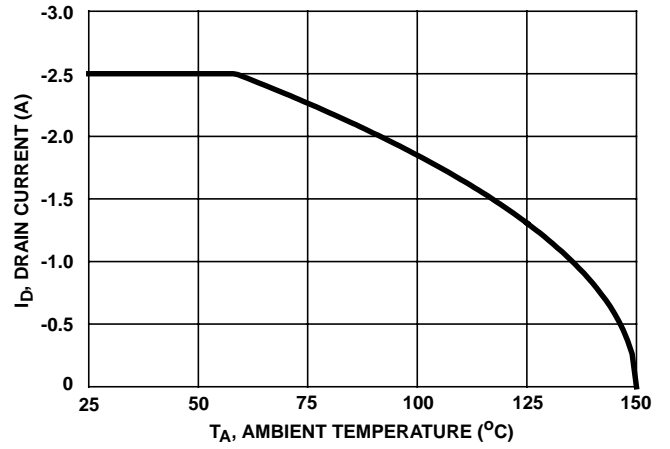


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

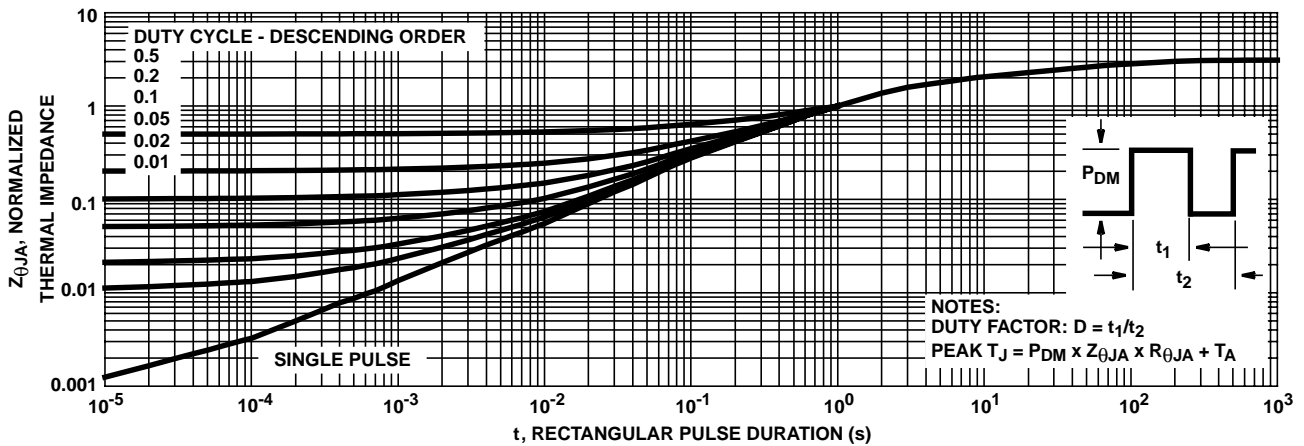


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

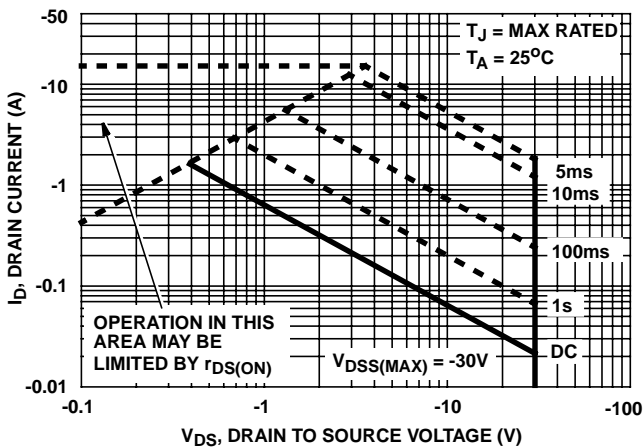


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

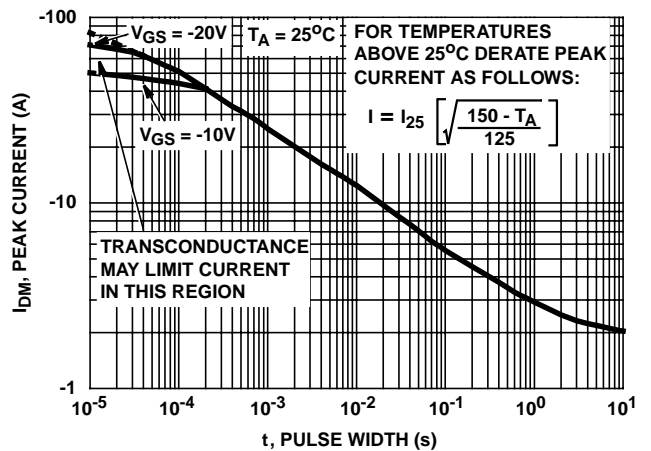
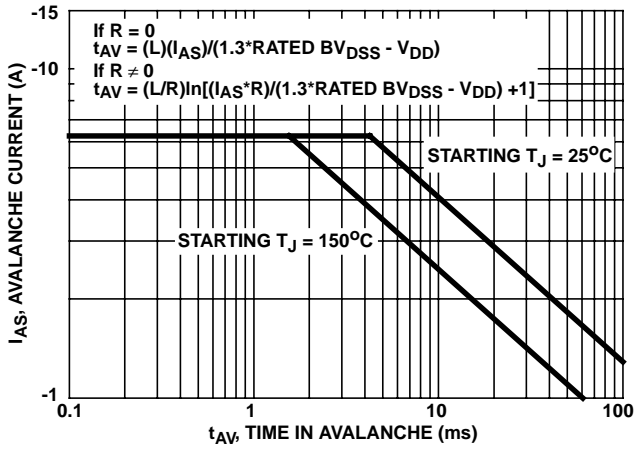


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.
FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

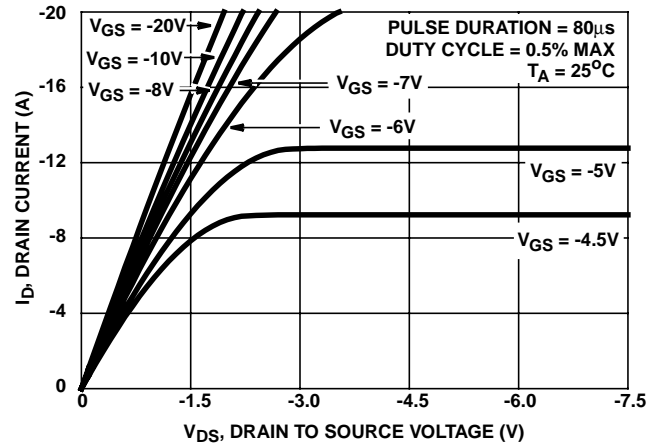


FIGURE 7. SATURATION CHARACTERISTICS

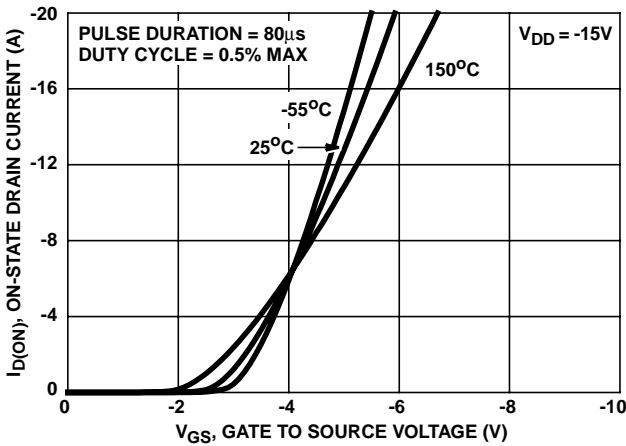


FIGURE 8. TRANSFER CHARACTERISTICS

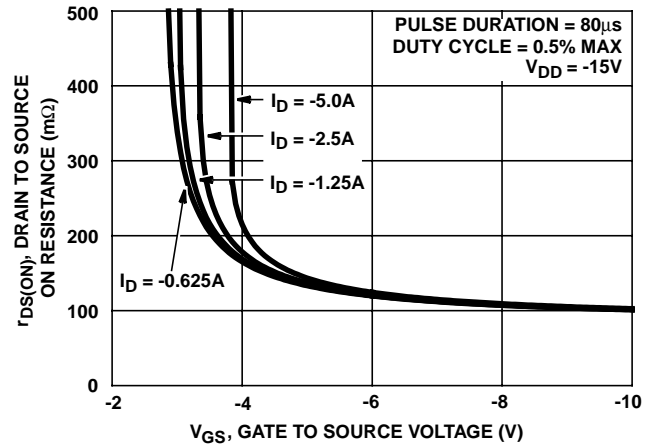


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

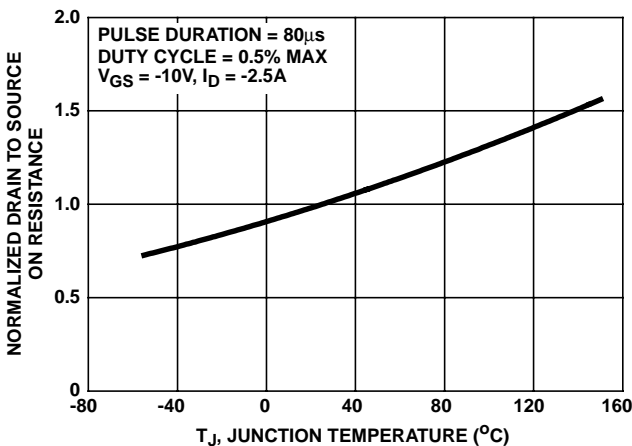


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

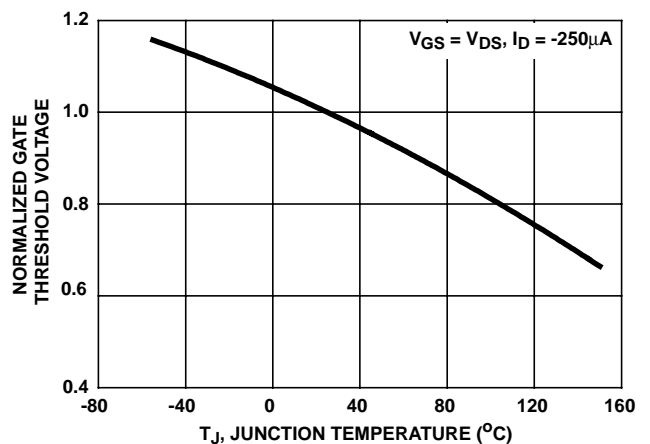


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

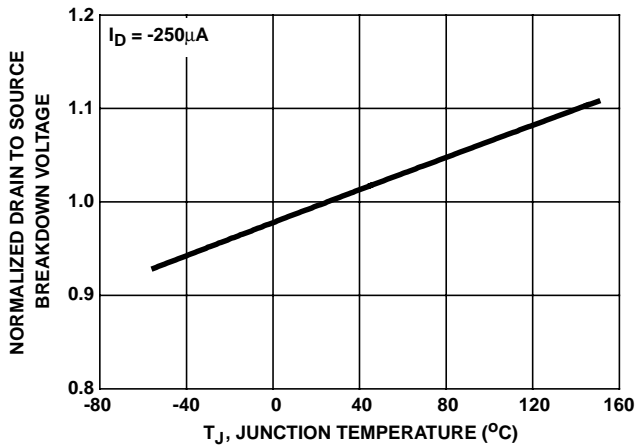


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

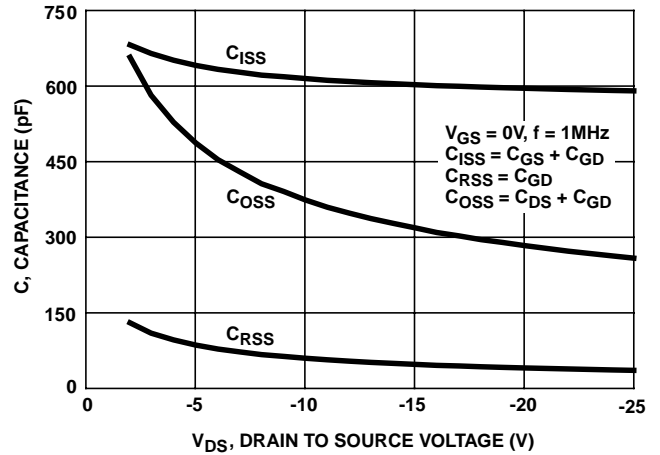
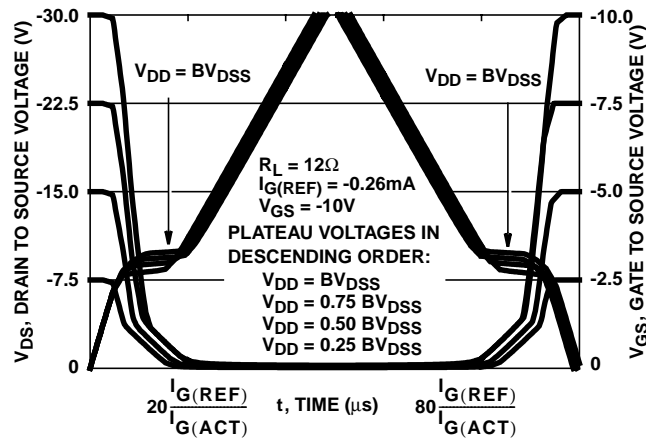


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

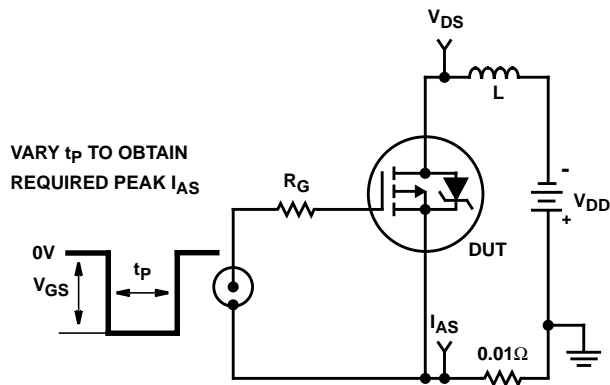


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

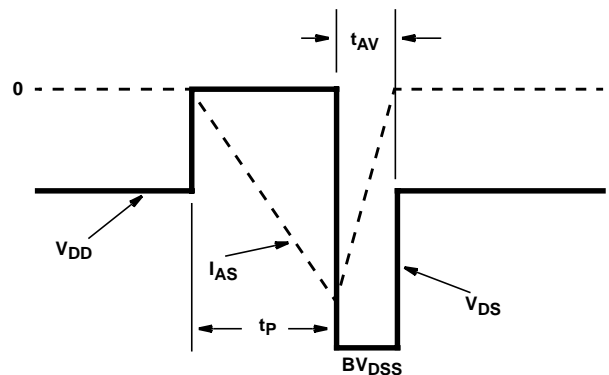


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

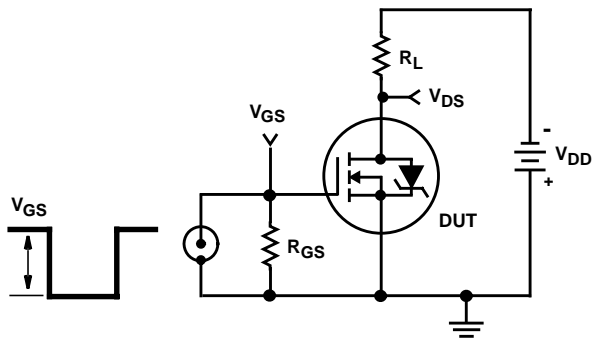


FIGURE 17. SWITCHING TIME TEST CIRCUIT

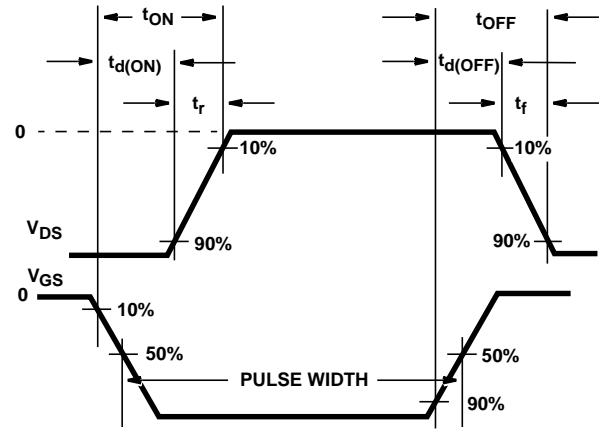


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

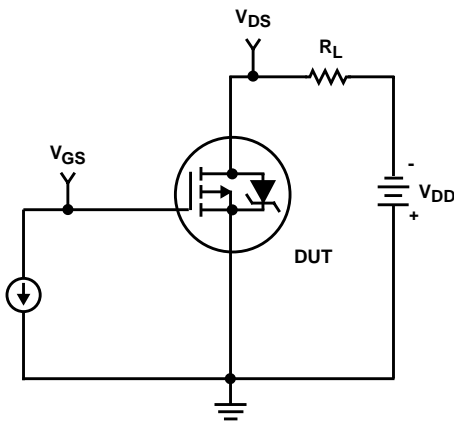


FIGURE 19. GATE CHARGE TEST CIRCUIT

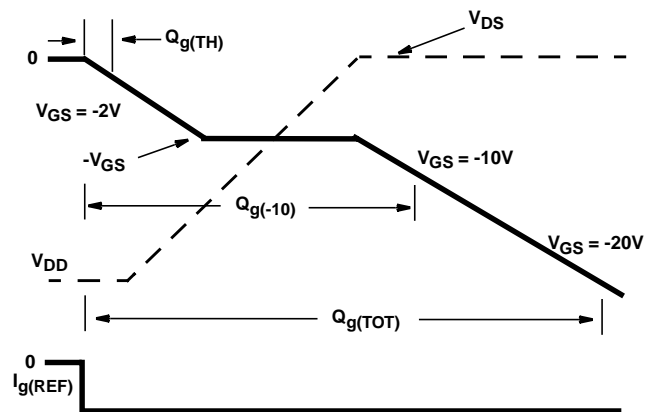


FIGURE 20. GATE CHARGE WAVEFORMS

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.

4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

RF1K49223

PSPICE Electrical Model

SUBCKT RF1K49223 2 1 3 ; rev 4/7/97

CA 12 8 7.29e-10
 CB 15 14 5.01e-10
 CIN 6 8 5.55e-10

DBODY 5 7 DBODYMOD
 DBREAK 7 11 DBREAKMOD
 DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -35.46
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 5 10 8 6 1
 EVTHRES 6 21 19 8 1
 EVTEMP 6 20 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
 LGATE 1 9 1.27e-9
 LSOURCE 3 7 4.20e-10

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 19.3e-3
 RGATE 9 20 7.44
 RLDRAIN 2 5 10
 RLGATE 1 9 12.7
 RLSOURCE 3 7 4.2
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 65.37e-3
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

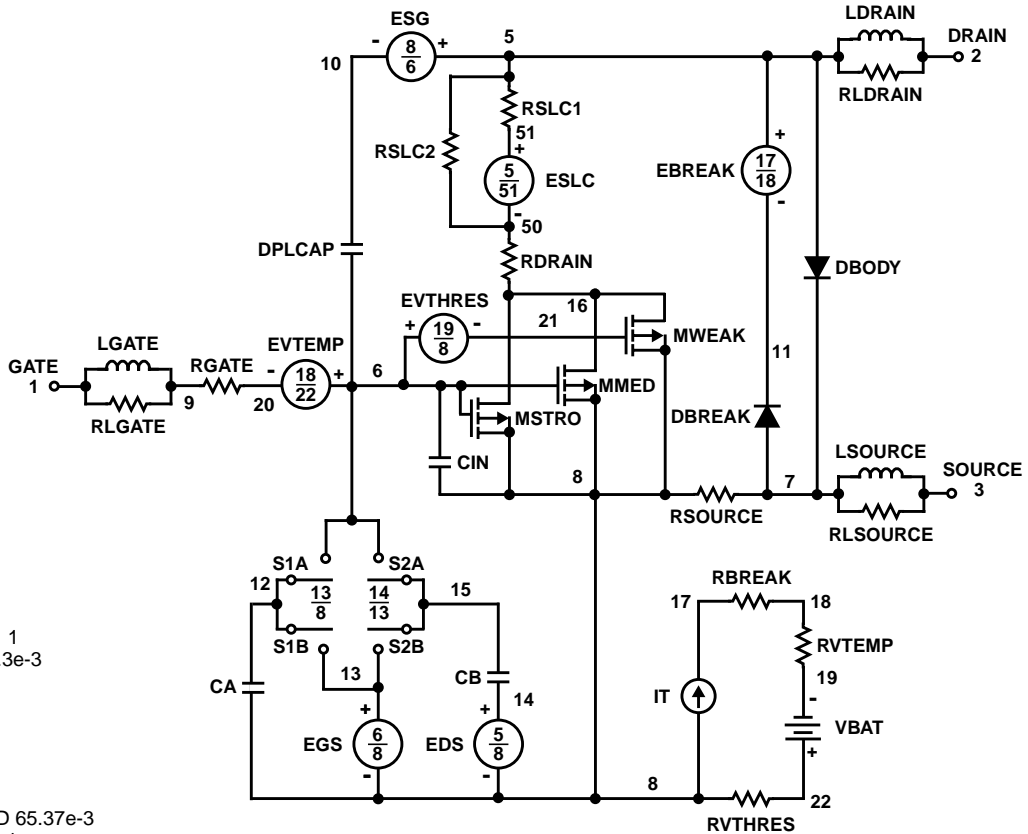
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*48),2.5))}

.MODEL DBODYMOD D (IS = 3.30e-13 RS = 4.56e-2 TRS1 = 6.98e-4 TRS2 = 8.08e-7 CJO = 8.21e-10 TT = 3.51e-8 M=0.4)
 .MODEL DBREAKMOD D (RS = 8.18e-1 TRS1 = 5.28e-3 TRS2 = -7.18e-5)
 .MODEL DPLCAPMOD D (CJO = 2.52e-10 IS = 1e-30 N = 10 M=0.6)
 .MODEL MMEDMOD PMOS (VTO = -1.95 KP = 0.75 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 7.44)
 .MODEL MSTROMOD PMOS (VTO = -2.44 KP = 7.25 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
 .MODEL MWEAKMOD PMOS (VTO = -1.68 KP = 0.045 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 74.4 RS = 0.1)
 .MODEL RBREAKMOD RES (TC1 = 9.45e-4 TC2 = -1.01e-7)
 .MODEL RDRAINMOD RES (TC1 = 3.69e-3 TC2 = 5.90e-6)
 .MODEL RSLCMOD RES (TC1 = 3.46e-3 TC2 = 1.26e-6)
 .MODEL RSOURCEMOD RES (TC1 = 3.69e-3 TC2 = 5.90e-6)
 .MODEL RVTHRESMOD RES (TC = -5.19e-4 TC2 = 5.02e-6)
 .MODEL RVTEMPMOD RES (TC1 = -3.54e-3 TC2 = -6.53e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 6.94 VOFF = 3.94)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.94 VOFF = 6.94)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.40 VOFF = -2.60)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.60 VOFF = 0.40)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



RF1K49223

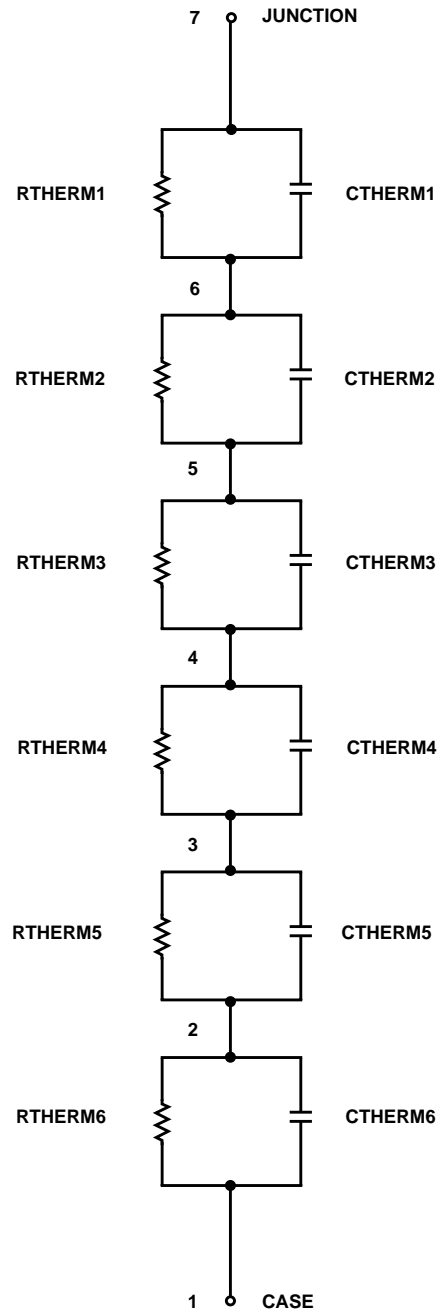
PSPICE Thermal Model

REV 28 Feb 97

RF1K49223

CTHERM1 7 6 1.00e-7
CTHERM2 6 5 9.00e-4
CTHERM3 5 4 3.00e-3
CTHERM4 4 3 4.00e-2
CTHERM5 3 2 5.20e-3
CTHERM6 2 1 1.90e-2

R THERM1 7 6 7.10e-2
R THERM2 6 5 1.90e-1
R THERM3 5 4 5.95e-1
R THERM4 4 3 4.27
R THERM5 3 2 1.2e1
R THERM6 2 1 1.04e2



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>