HARRIS
SEMICONDUCTOR

RFG70N06, RFP70N06, RF1S70N06, RF1S70N06SM

December 1995

70A, 60V, Avalanche Rated, N-Channel Enhancement-Mode Power MOSFETs

Features

- 70A, 60V
- $r_{DS(on)} = 0.014\Omega$
- *Temperature Compensated* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- +175°C Operating Temperature

Description

The RFG70N06, RFP70N06, RF1S70N06 and RF1S70N06SM are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

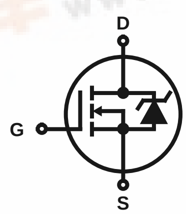
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG70N06	TO-247	RFG70N06
RFP70N06	TO-220AB	RFP70N06
RF1S70N06	TO-262AA	F1S70N06
RF1S70N06SM	TO-263AB	F1S70N06

NOTE: When ordering use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S70N06SM9A.

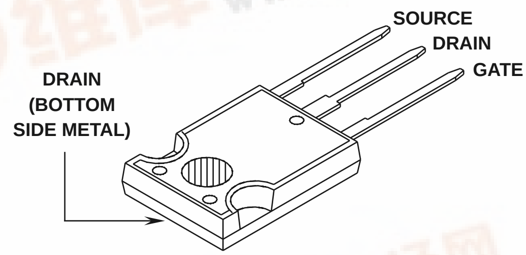
Formerly developmental type TA49007.

Symbol

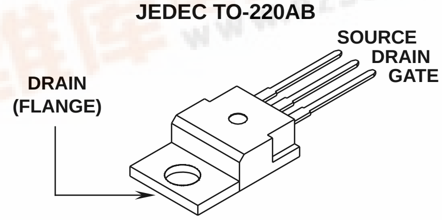


Packages

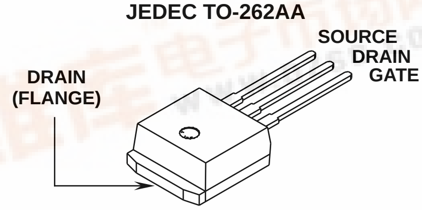
JEDEC STYLE TO-247



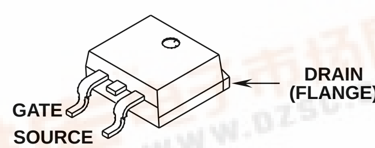
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		RFG70N06, RFP70N06 RF1S70N06, RF1S70N06SM	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	150	W
Derate above $+25^oC$		1.0	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 70A$, $V_{GS} = 10V$		-	-	0.014	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 70A$ $R_L = 0.43\Omega$, $V_{GS} = +10V$ $R_{GS} = 2.5\Omega$		-	-	125	ns
Turn-On Delay Time	$t_{D(ON)}$			-	12	-	ns
Rise Time	t_R			-	50	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	15	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 48V$, $I_D = 70A$, $R_L = 0.68\Omega$	-	185	215	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	100	115	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	5.5	6.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz		-	3000	-	pF
Output Capacitance	C_{OSS}			-	900	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	300	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 70A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 70A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

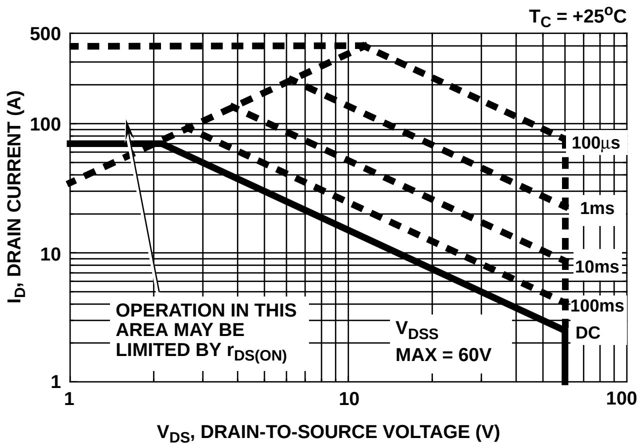


FIGURE 1. SAFE OPERATING AREA CURVE

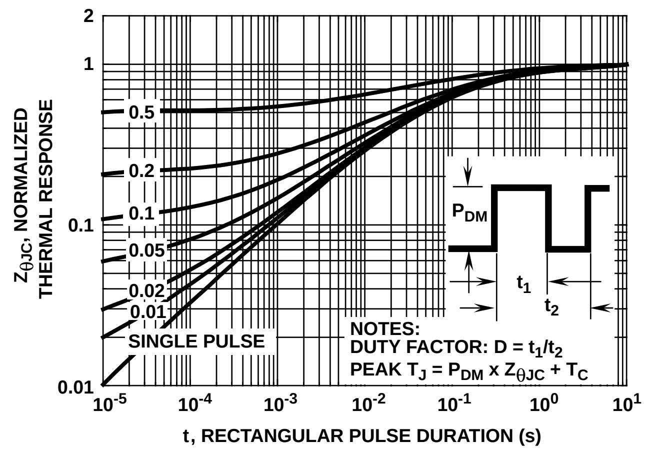


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

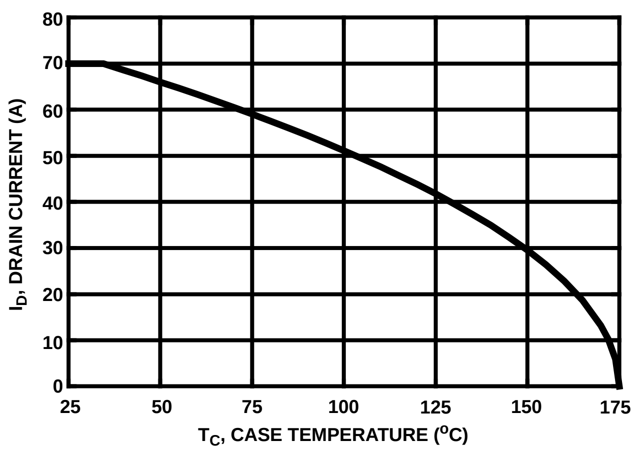


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

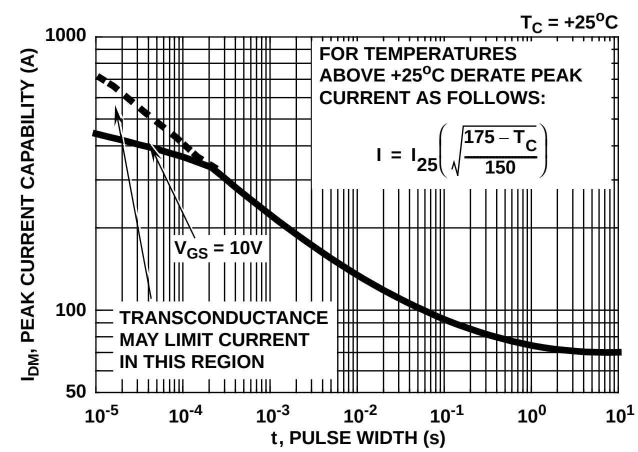


FIGURE 4. PEAK CURRENT CAPABILITY

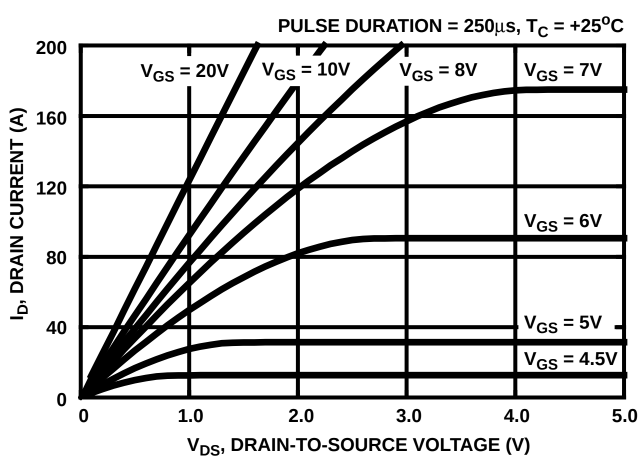


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

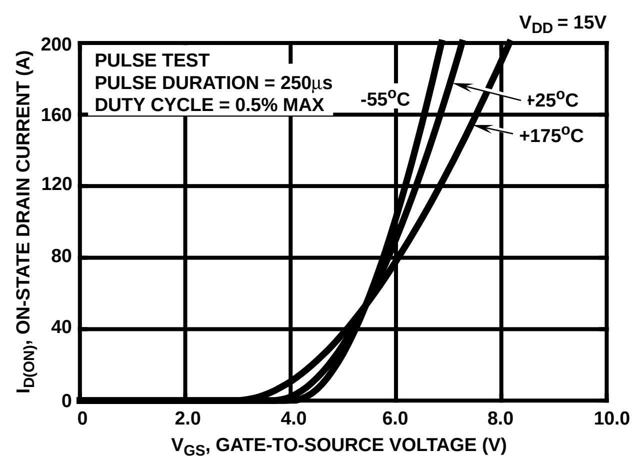


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

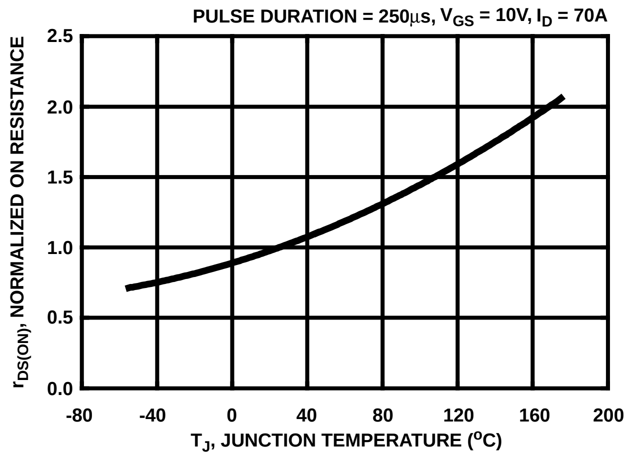


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

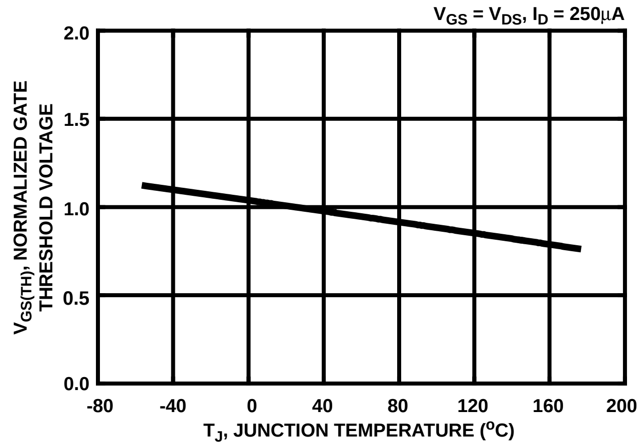


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

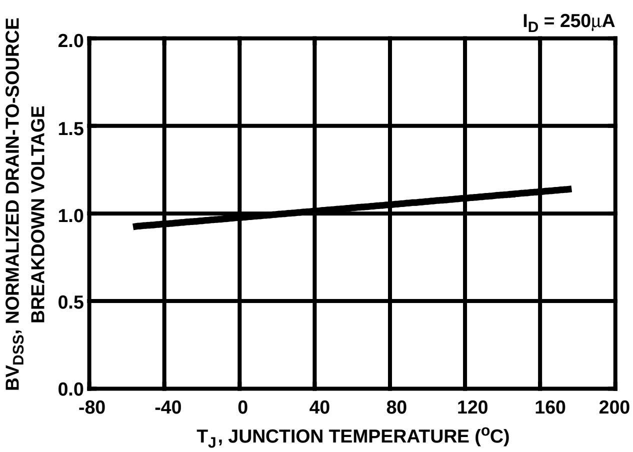


FIGURE 9. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

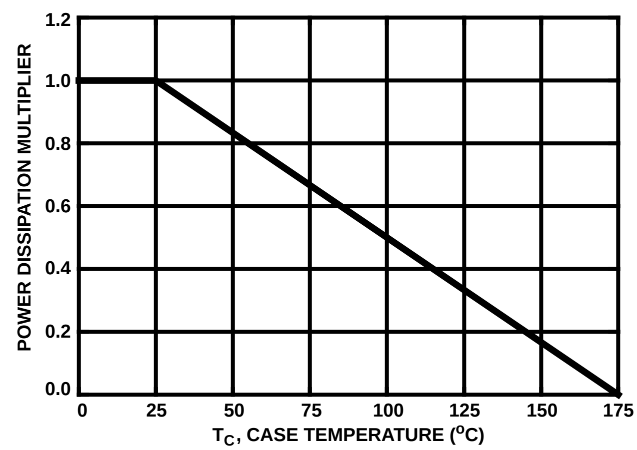


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

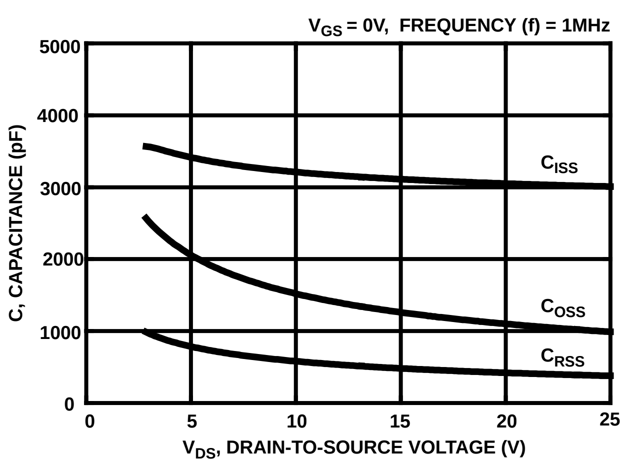


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

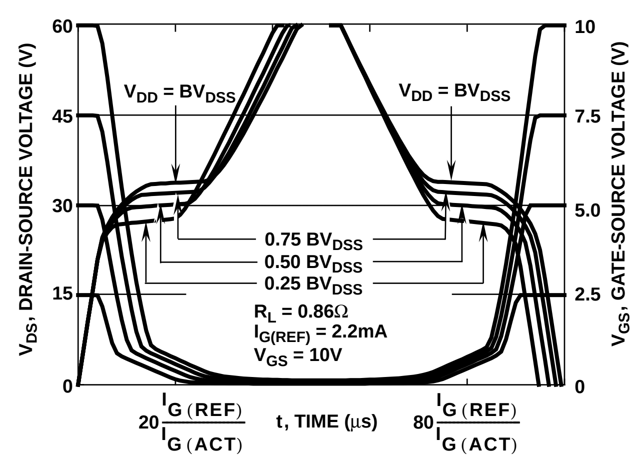


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

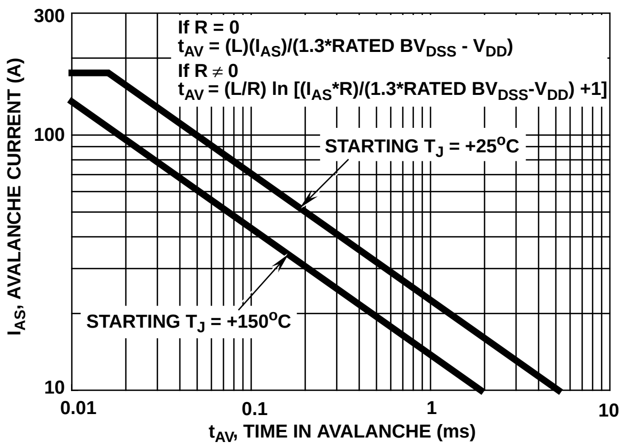


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

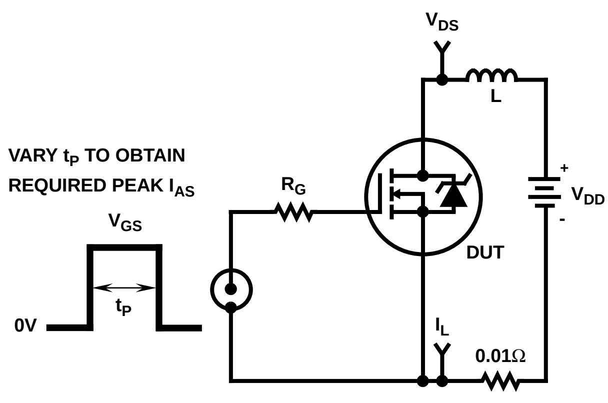


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

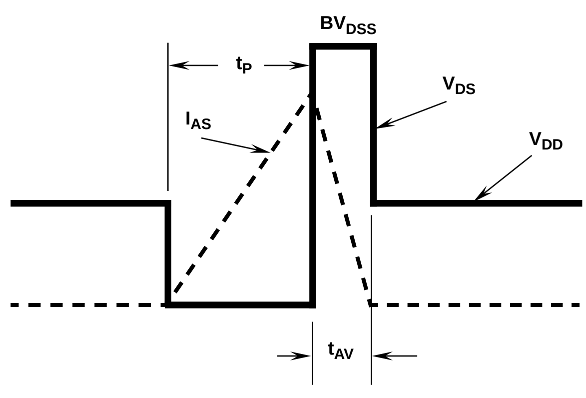


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

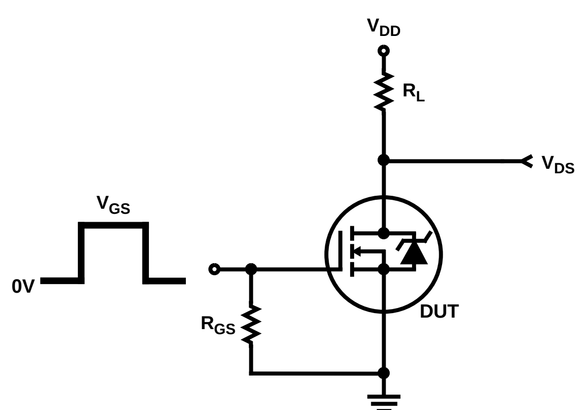


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

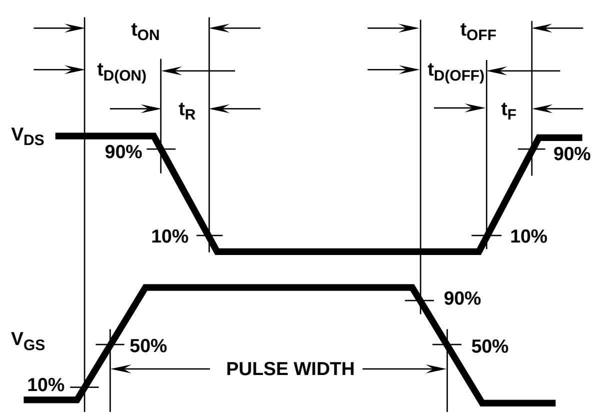


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG70N06, RFP70N06, RF1S70N06, RF1S70N06SM

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.SUBCKT  RFG70N06  2 1 3 ;        rev 3/20/92

CA  12  8  5.56e-9
CB  15  14  5.30e-9
CIN  6  8 2.63e-9

DBODY  7  5  DBDMOD
DBREAK  5 11  DBKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  65.18
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTO  20  6  18  8  1

IT  8  17  1

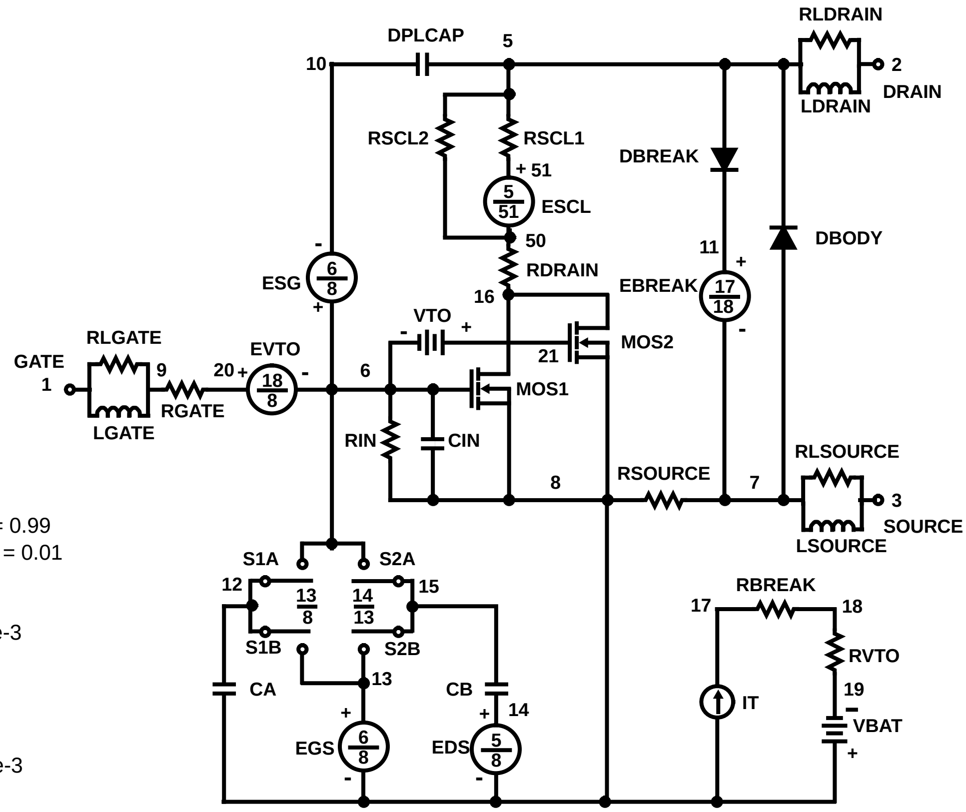
LDRAIN  2  5  1e-9
LGATE 1  9  3.10e-9
LSOURCE  3  7  1.82e-9

MOS1  16  6  8  8  MOSMOD  M = 0.99
MOS2  16  21  8  8  MOSMOD  M = 0.01

RBREAK  17  18  RBKMOD  1
RDRAIN  50  16  RDSMOD  4.66e-3
RLDRAIN  2  5  10
RGATE  9  20  1.21
RLGATE 1  9  31
RIN  6  8  1e9
RSOURCE  8  7  RDSMOD  3.92e-3
RLSOURCE  3  7  18.2
RVTO  18  19  RVTOMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  8  19  DC  1
VTO  21  6   0.605
```

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.MODEL DBDMOD D (IS = 7.91e-12  RS = 3.87e-3  TRS1 = 2.71e-3  TRS2 = 2.50e-7  CJO = 4.84e-9  TT = 4.51e-8)
.MODEL DBKMOD D (RS = 3.9e-2  TRS1 =1.05e-4  TRS2 = 3.11e-5)
.MODEL DPLCAPMOD D (CJO = 4.8e-9  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 3.46  KP = 47  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 8.46e-4  TC2 = -8.48e-7)
.MODEL RDSMOD RES (TC1 = 2.23e-3  TC2 = 6.56e-6)
.MODEL RVTOMOD RES (TC1 = -3.29e-3  TC2 = 3.49e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -8.35  VOFF= -6.35)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -6.35  VOFF= -8.35)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.0  VOFF= 3.0)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 3.0  VOFF= -2.0)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.