



**RF2153**

CDMA/TDMA/PACS  
1900MHZ 3V POWER AMPLIFIER

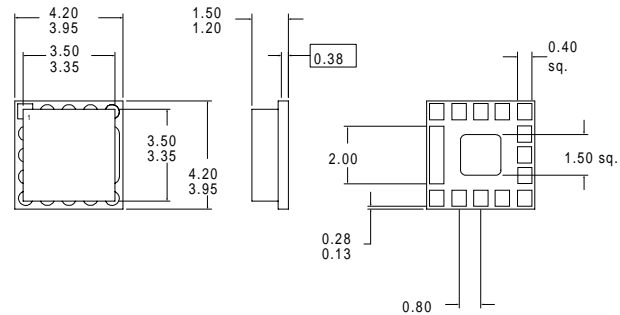
Typical Applications

- PACS Handsets and Base Stations
- 3V 1850-1910MHz CDMA PCS Handsets
- 3V 1750-1780MHz CDMA PCS Handsets
- 3V TDMA PCS Handsets
- Spread-Spectrum Systems
- Commercial and Consumer Systems

**2**  
POWER AMPLIFIERS

Product Description

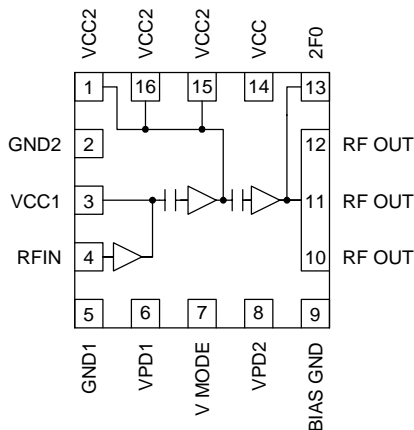
The RF2153 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 3V CDMA and TDMA handheld digital equipment, spread-spectrum systems, and other applications in the 1750MHz to 1910MHz band. The device is packaged in a compact 4mmx4mm (LCC). The device's frequency response can be optimized for linear performance in the 1750MHz to 1910MHz band.



ALL SOLDER PAD TOLERANCES P0.05mm

Optimum Technology Matching® Applied

- Si BJT       GaAs HBT       GaAs MESFET  
 Si Bi-CMOS       SiGe HBT       Si CMOS



Functional Block Diagram

Package Style: MP16KO1A

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 30dB Linear Gain
- 33% Linear Efficiency CDMA
- 40% Linear Efficiency TDMA
- On-board Power Down Mode

Ordering Information

RF2153      CDMA/TDMA/PACS 1900MHz 3V Power Amplifier  
 RF2153 PCBA      Fully Assembled Evaluation Board

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# RF2153

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V <sub>DC</sub>
Supply Voltage (P <sub>OUT</sub> ≤31 dBm)	+4.5	V <sub>DC</sub>
Mode Voltage (V <sub>MODE</sub> )	+3.5	V <sub>DC</sub>
Control Voltage (V <sub>PD</sub> )	+3.5	V <sub>DC</sub>
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-30 to +150	°C



**Caution!** ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall - CDMA</b>					T=25°C, V <sub>CC</sub> =3.4V unless otherwise specified
Usable Frequency Range	1750		1910	MHz	
Typical Frequency Range		1750-1780 1850-1910		MHz	Output Matching Network Tune
Small Signal Gain	30	32	34	dB	Output Matching Network Tune V <sub>MODE</sub> =Low 0V to 0.5V
Linear Gain	26	29		dB	V <sub>MODE</sub> =High 2.5V to 3.0V
Second Harmonic (including second harmonic trap)		-35		dBc	V <sub>MODE</sub> =High 2.5V to 3V
Third Harmonic		-40		dBc	P <sub>OUT</sub> =29dBm, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.8V
Fourth Harmonic		-45		dBc	
Minimum Linear Output Power (CDMA or TDMA Modulation)	29			dBm	
Idle Current	90	100	200	mA	V <sub>MODE</sub> =>2.5V
CDMA Linear Efficiency	30	33		%	P <sub>OUT</sub> =29dBm, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.8V
CDMA Adjacent Channel Power Rejection @ 1.25MHz		-46	-44	dBc	P <sub>OUT</sub> =29dBm, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.8V
Minimum Linear Output Power (CDMA Modulation)	28	+29		dBm	V <sub>CC</sub> =3.0V, V <sub>REG</sub> =2.8V
Input VSWR		< 2:1			
Output Load VSWR	10:1				No Damage.
Turn On/Off Time			40	μs	
<b>Overall - TDMA</b>					T=25°C, V <sub>CC</sub> =3.4V unless otherwise specified
Idle Current		250	500	mA	V <sub>MODE</sub> =0V to 0.5V
TDMA Linear Efficiency	30	40		%	P <sub>OUT</sub> =30dBm, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.8V
TDMA ACP @ 30kHz		-29	-28	dBc	P <sub>OUT</sub> =30dBm
TDMA ALT @ 60kHz		-49	-48	dBc	P <sub>OUT</sub> =30dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Power Supply</b>					
Power Supply Voltage	3.0	3.4	4.5	V	
V <sub>PD</sub> Current		10		mA	Total pins 6 and 8
V <sub>PD</sub> and V <sub>MODE</sub> Current		11	13	mA	Total pins 6, 7 and 8
Total Current (Power down)			10	μA	V <sub>PD</sub> = low
V <sub>PD</sub> "Low" Voltage		0	0.2	V	
V <sub>PD</sub> "High" Voltage	2.7	2.8	2.9	V	
MODE "High" Voltage	2.5	2.8		V	R1 = 1 kΩ
MODE "Low" Voltage		0	0.5	V	R1 = 1 kΩ
Stability		3:1			Inband
		20:1			Outband
Spurious		<-60		dBc	
Noise Power		-136		dBm/Hz	@ 80MHz offset

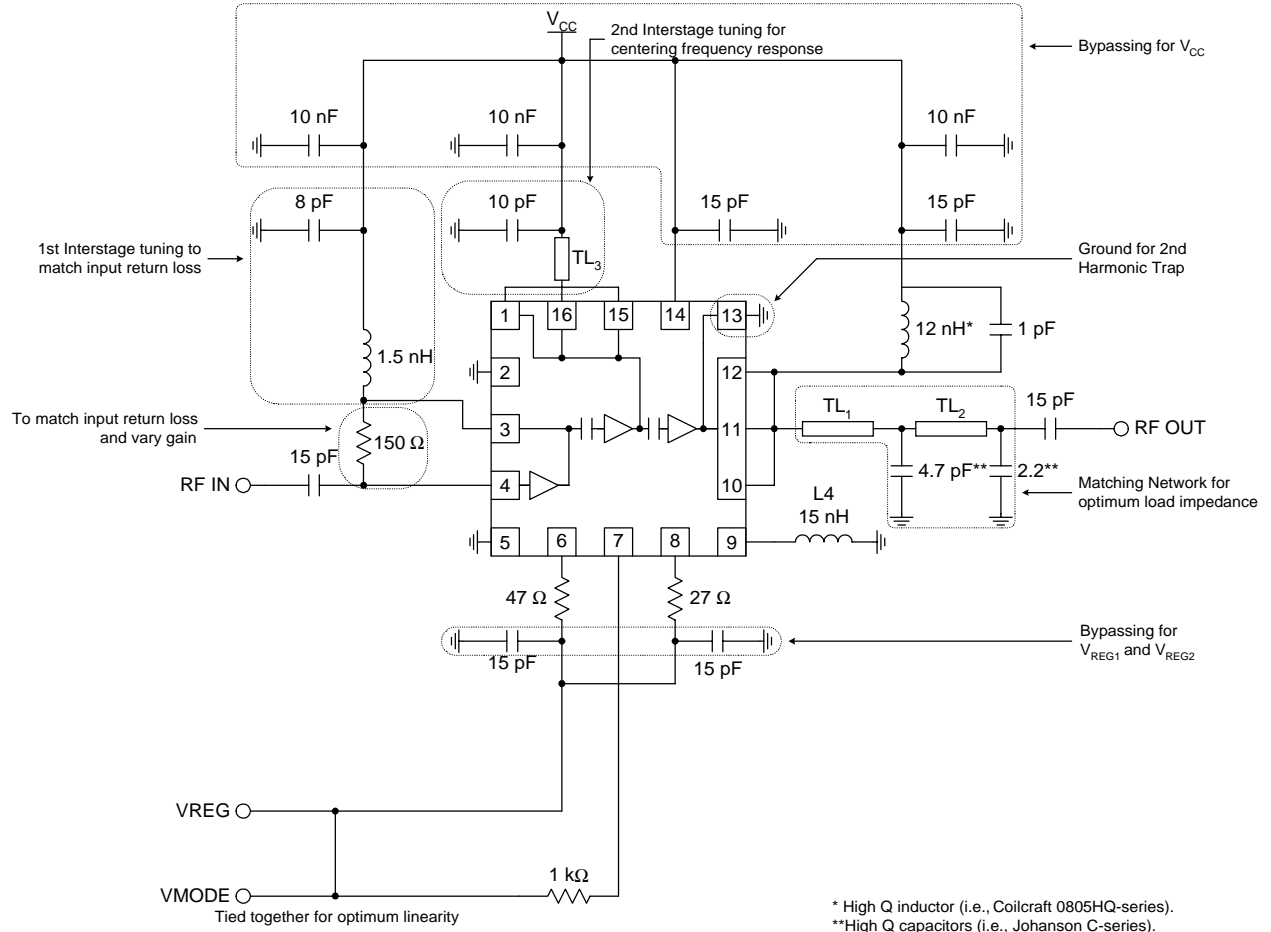
# RF2153

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### POWER AMPLIFIERS

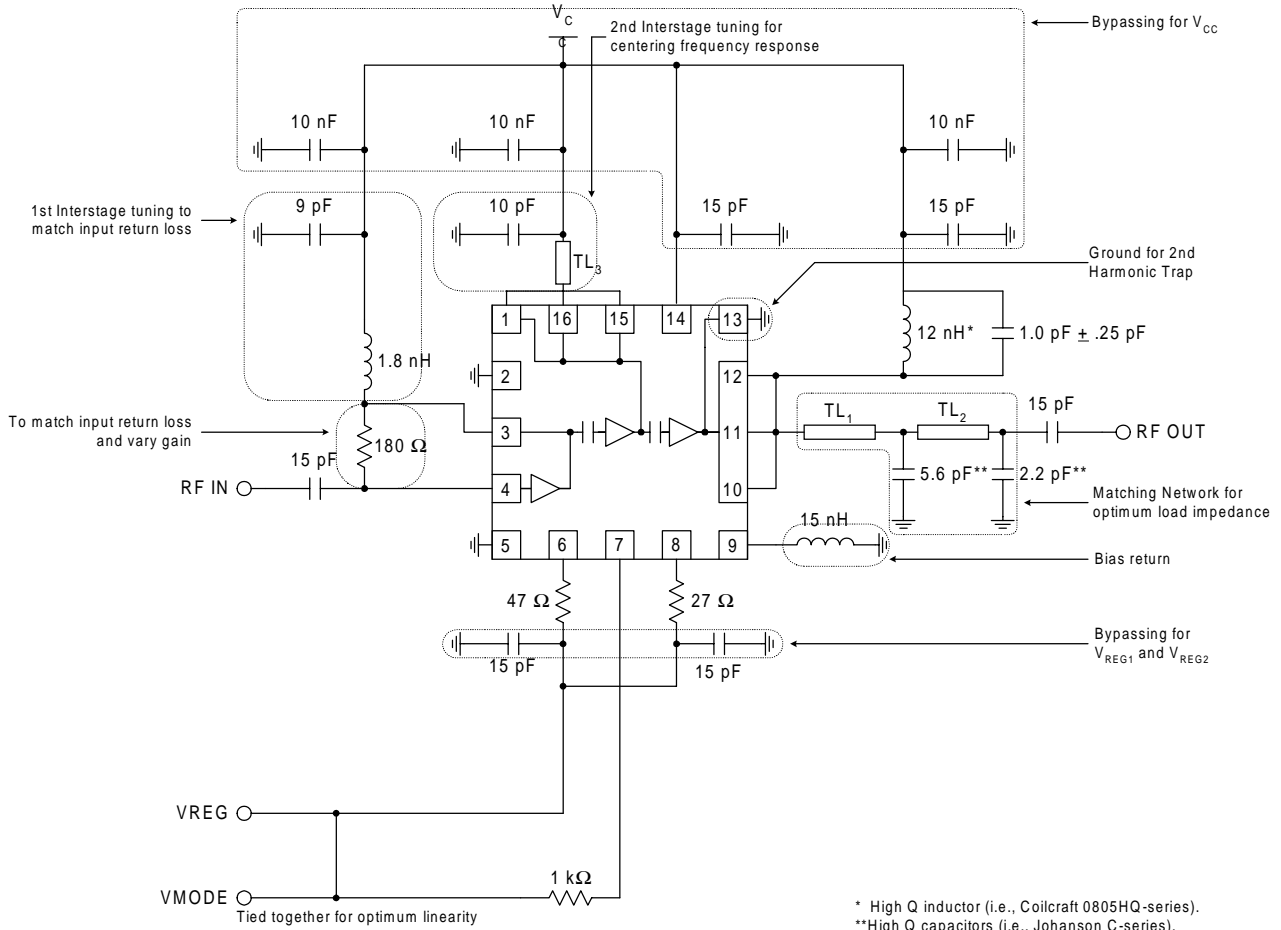
Pin	Function	Description	Interface Schematic
1	VCC2	Power supply for second stage and interstage match. Pins 1, 15 and 16 should be connected by a common trace where the pins contact the printed circuit board.	
2	GND2	Ground for second stage. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact on top metal layer.	
3	VCC1	Power supply for first stage and interstage match. $V_{CC}$ should be fed through a 1.5nH inductor terminated with a 15pF capacitor on the supply side.	See pin 4.
4	RF IN	RF input. An external 15pF series capacitor is required as a DC block and also provides for an input VSWR of <2:1 typical.	
5	GND1	Ground for first stage. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact on top metal layer.	See pin 4.
6	VPD1	Power Down control for first and second stages. When this pin is "low", all first and second stage circuits are shut off. When this pin is 2.8V, all first stage circuits are operating normally. $V_{PD1}$ requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V.	
7	VMODE	For full power operation, MODE is set low. VMODE will reduce the bias current by up to 50% when set HIGH. Large Signal Gain is reduced approximately 1.5dB at 29dBm $P_{OUT}$ and Small Signal Gain is reduced approximately 6dB. An external series resistor is optional to limit the amount of current required by the $V_{MODE}$ pin.	
8	VPD2	Power Down control for the third stage. When this pin is "low", the third stage circuit is shut off. When this pin is 2.8V, the third stage circuit is operating normally. $V_{PD}$ requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 15pF high frequency bypass capacitor is recommended.	
9	BIAS GND	Requires a 15nH inductor.	
10	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the third stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1850MHz to 1910MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	RF OUT	Same as pin 12.	See pin 10.
12	RF OUT	Same as pin 12.	See pin 10.
13	2FO	Second harmonic trap. Keep traces physically short and connect immediately to ground plane. This ground should be isolated from backside ground contact.	
14	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
15	VCC2	Same as pin 1.	
16	VCC2	Same as pin 1.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

## Application Schematic US - CDMA



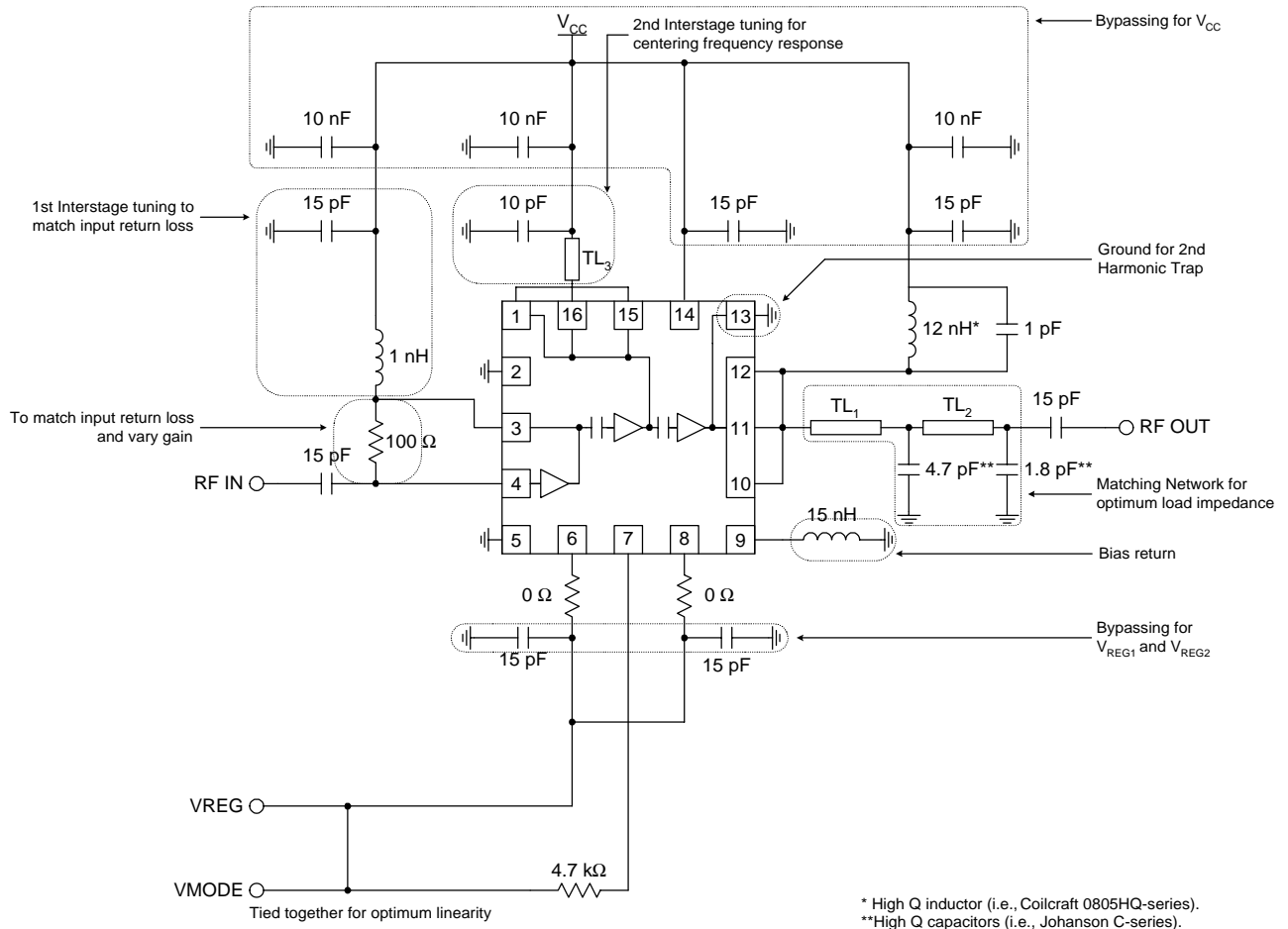
Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>3</sub>
CDMA (US)	20 mils	100 mils	20 mils

## Application Schematic Korea - CDMA



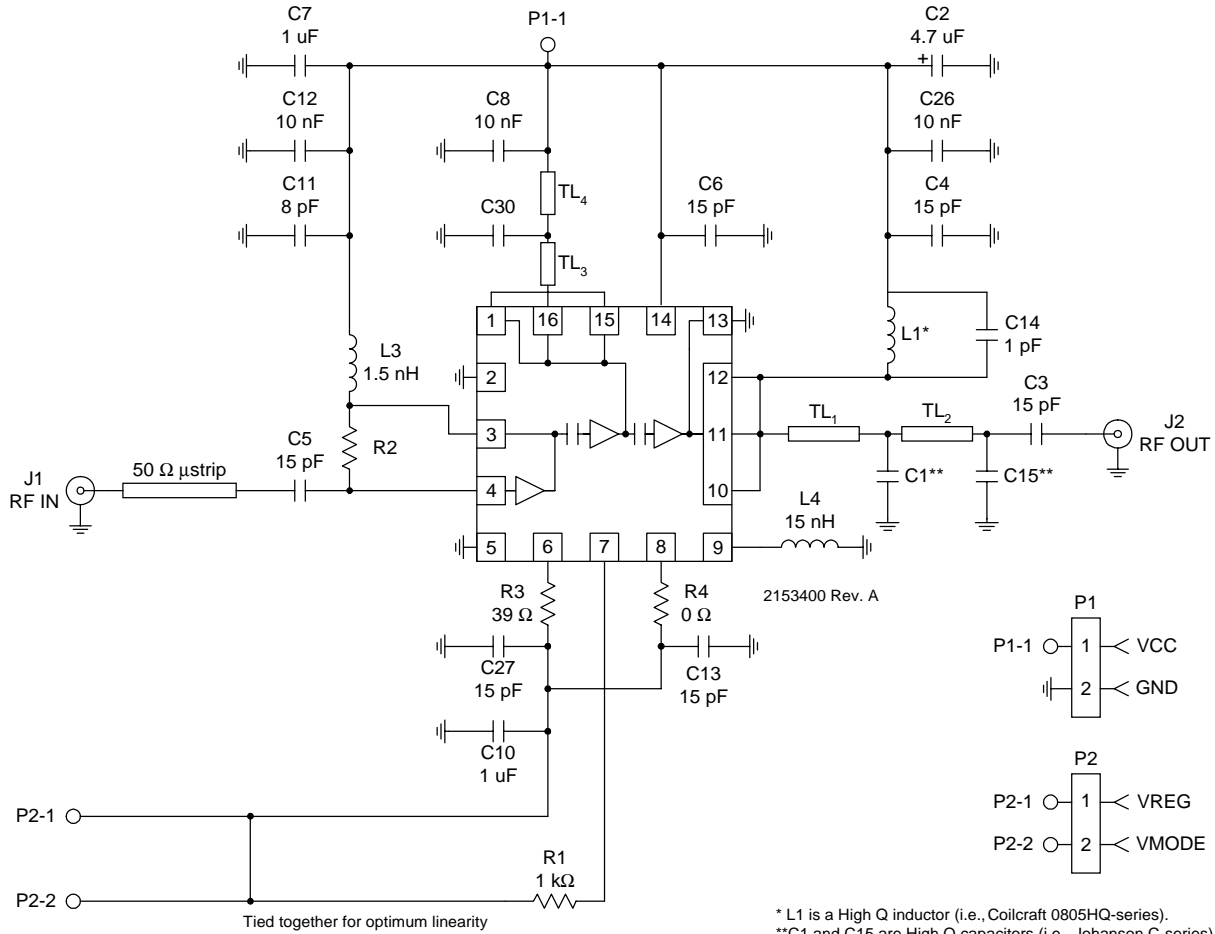
Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>3</sub>
CDMA (Korea)	30 mils	100 mils	30 mils

## Application Schematic US - TDMA



Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>3</sub>
TDMA (US)	20 mils	160 mils	10 mils

## Evaluation Board Schematic US - CDMA



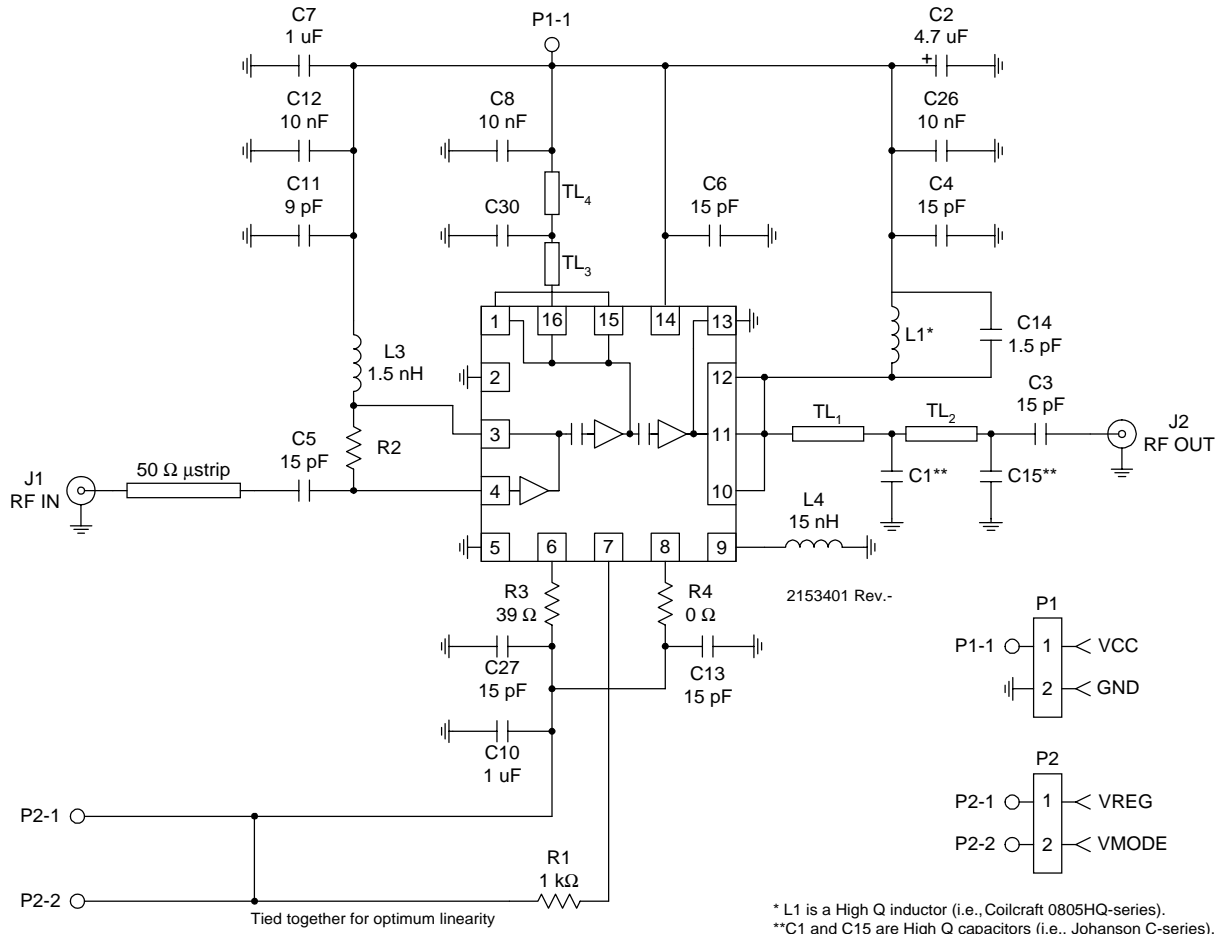
\* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).  
 \*\*C1 and C15 are High Q capacitors (i.e., Johanson C-series).

Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C15 (pF)
CDMA (US)	150	10	4.7	12	2.2

Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>3</sub>	TL <sub>4</sub>
CDMA (US)	20 mils	100 mils	20 mils	100 mils or ≥ 2.7 nH inductor



## Evaluation Board Schematic Korea - CDMA

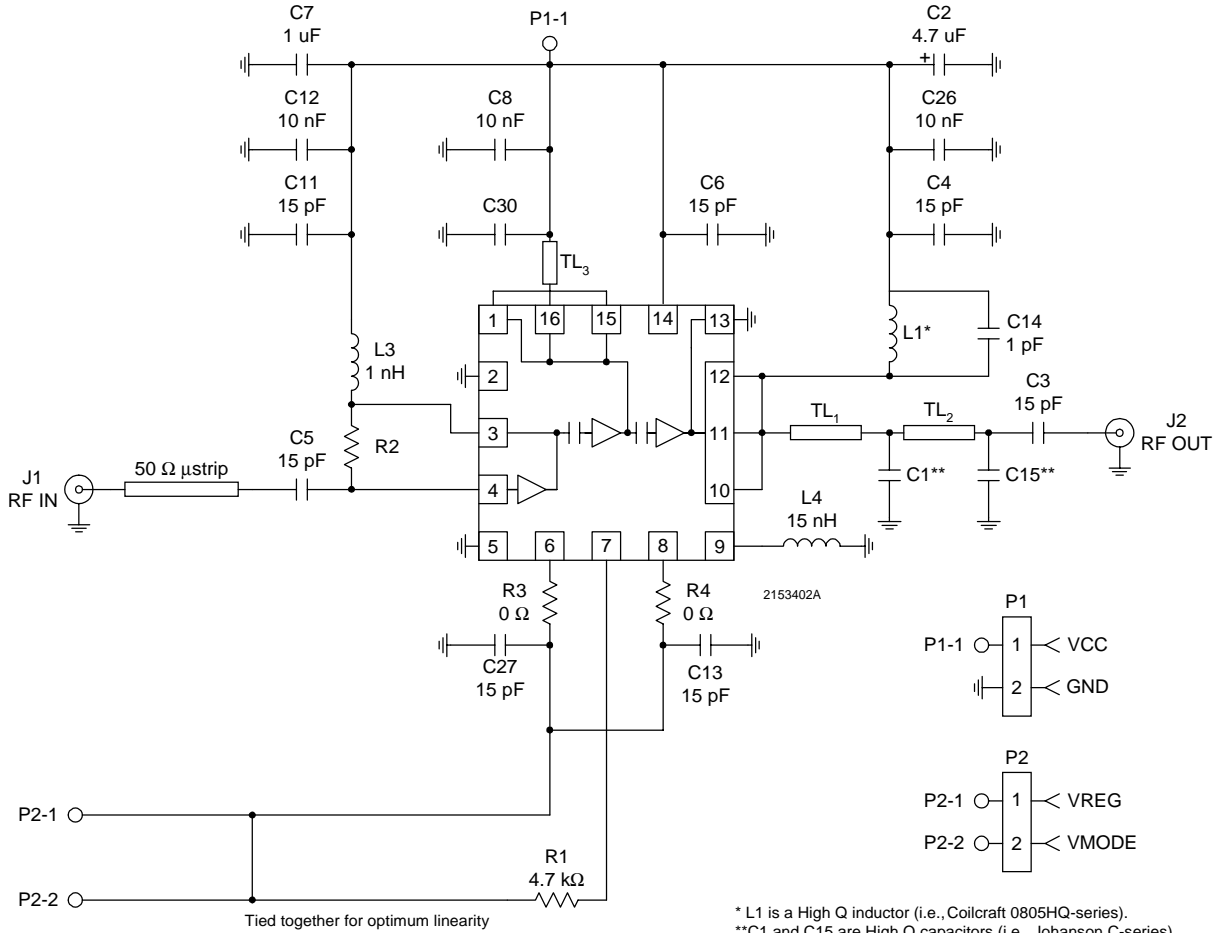


\* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).  
\*\*C1 and C15 are High Q capacitors (i.e., Johanson C-series).

Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C15 (pF)
CDMA (Korea)	180	11	5.6	12	2.2

Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>3</sub>	TL <sub>4</sub>
CDMA (Korea)	30 mils	100 mils	30 mils	100 mils or ≥ 2.7 nH inductor

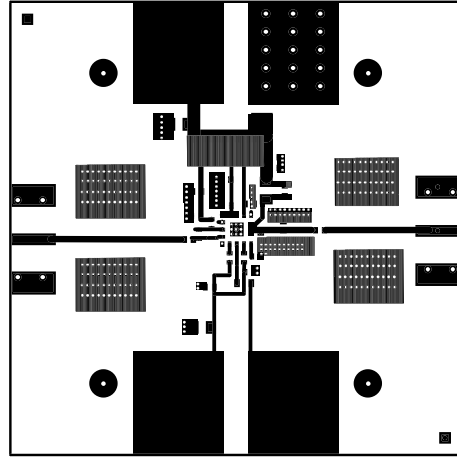
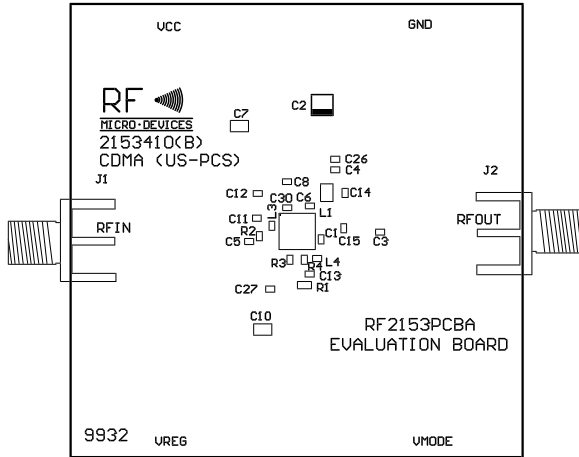
## Evaluation Board Schematic US - TDMA



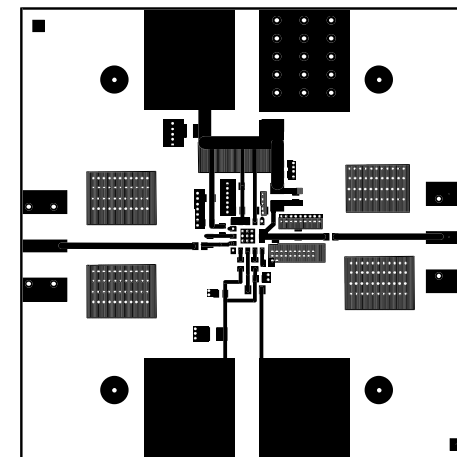
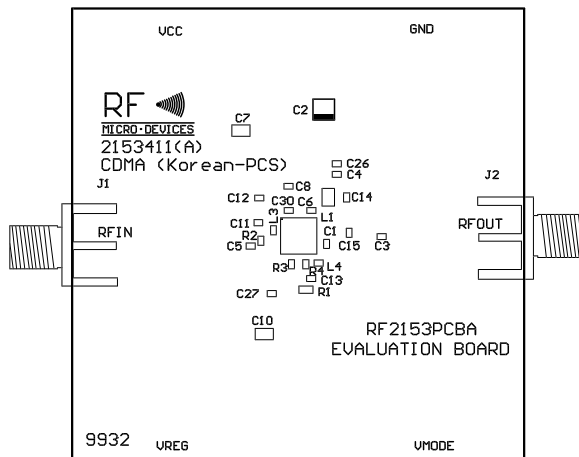
Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C15 (pF)
TDMA (US)	100	10	4.7	12	1.8

Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>3</sub>
TDMA (US)	20 mils	160 mils	10 mils

Evaluation Board Layout  
US - CDMA  
Board Size 2.0" x 2.0"  
Board Thickness 0.031", Board Material FR-4



Evaluation Board Layout  
Korea - CDMA

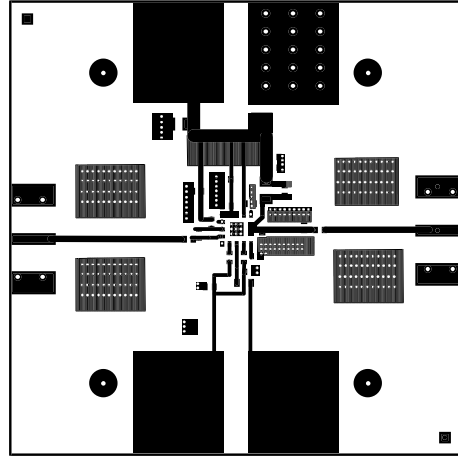
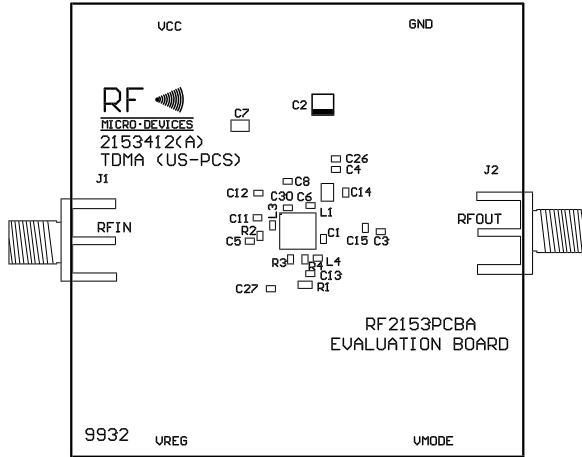


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## Evaluation Board Layout US - TDMA

2

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