RF2495

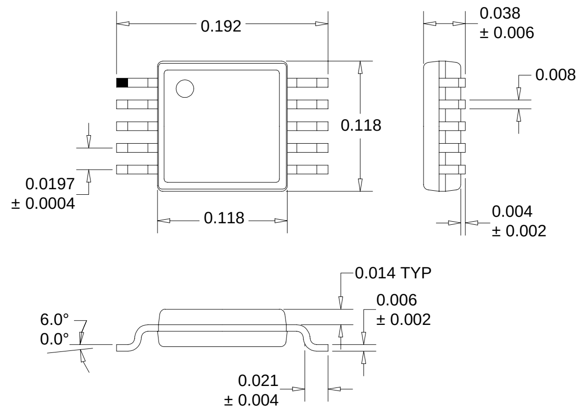
900MHZ 3V LOW CURRENT LNA/MIXER

Typical Applications

- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread-Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- General Purpose Frequency Conversion

Product Description

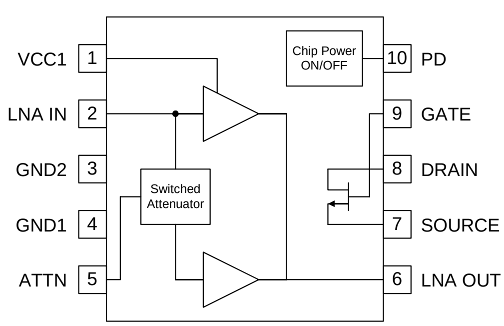
The RF2495 is a front-end receiver IC chip developed for the handset/portable battery-powered equipment markets. The chip contains an RF 15dB attenuator, an LNA and a passive mixer. By using a state-of-the-art Silicon Bi-CMOS process, the LNA has high dynamic range under low DC operating conditions and the passive mixer requires no DC bias at all. Packaged in the industry-standard MSOP-10 package, the device is well-suited for limited board space applications.



Package Style: MSOP-10

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☑ SiGe Bi-CMOS



Functional Block Diagram

Features

- Single Supply 3V Operation
- 1.9dB LNA NF
- 0dBm Input IP3
- Small MSOP-10 Package
- Low Current Drain (11mA maximum)
- Very Low Cost

Ordering Information

RF2495	900MHz 3V Low Current LNA/Mixer
RF2495 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
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Tel (336) 664 1233
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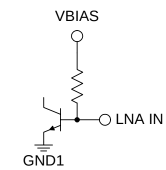
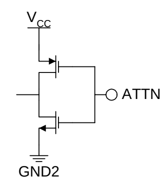
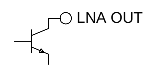
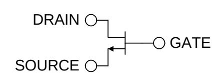
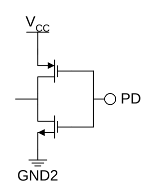
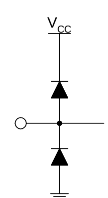
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

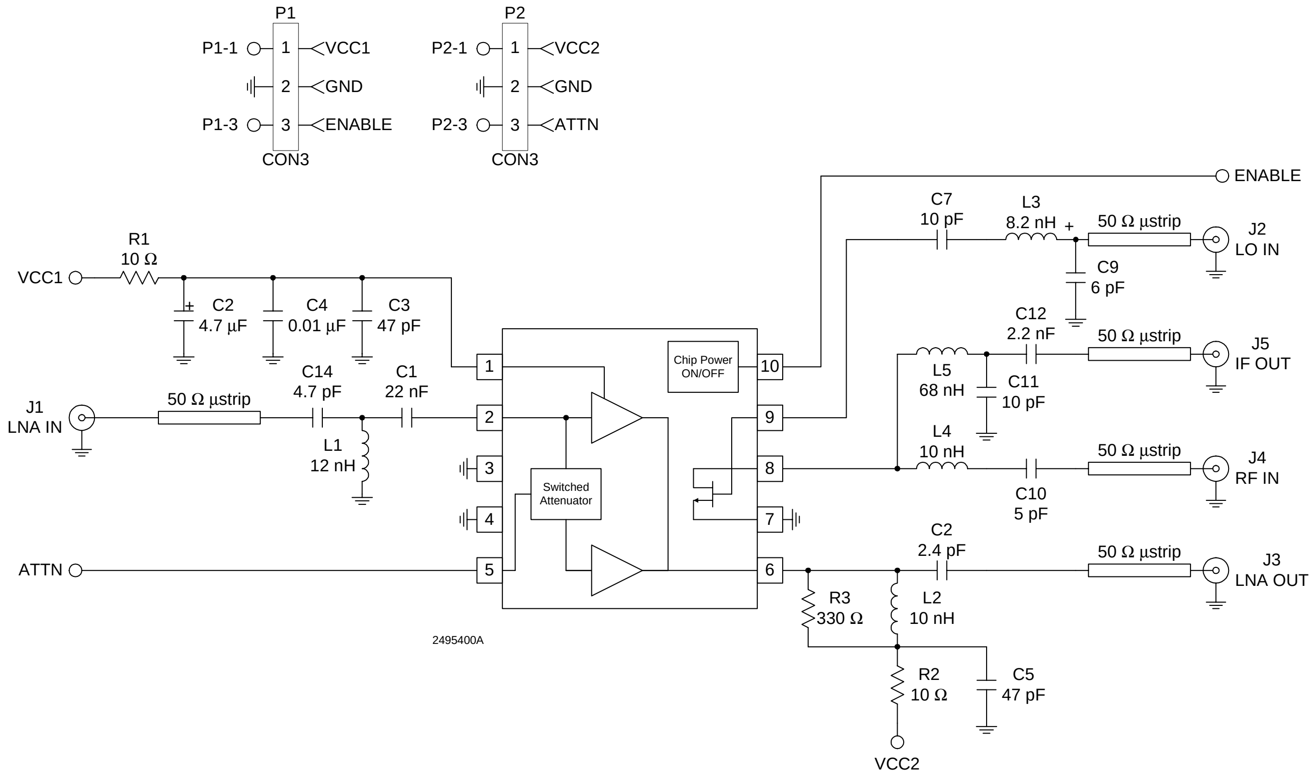
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V
RF/LO Frequency Range		850 to 940		MHz	Specifications
		800 to 1000		MHz	Usable range
LNA					
Gain	15.5	17.0		dB	High gain state
	1.0	4.0		dB	Low gain state
Input IP3	-2.5	+1.0		dBm	High gain state, RF IN=-25dBm
	+11.0	+12.5		dBm	Low gain state, RF IN=-15dBm
Noise Figure		1.9	2.2	dB	High gain state
		13.5		dB	Low gain state
Input VSWR			1.67:1		
Output VSWR			1.67:1		
Mixer					
Conversion Gain	-6.5	-5.5		dB	With LO=+2dBm
	-6.0	-5.5		dB	With LO=+4dBm
Input IP3	+7.5	+11.0		dBm	With LO=+2dBm
	+10.0	+13.0		dBm	With LO=+4dBm
LO Input Level	-2	4.0		dBm	
Attenuation					
ATTN Enable	V_{CC}-0.3	>1.6		V	Low gain state
ATTN Disable		0	0.3	V	High gain state
Power Down					
Chip Enable	V_{CC}-0.3	>1.6		V	Voltage applied to PD pin
Chip Disable		0		V	Voltage applied to PD pin
Power Supply					
Voltage		3.0		V	Specifications
		2.7 to 3.3		V	Operating limits
Current Consumption		10	12	mA	Chip enabled
		<1	3.0	uA	Chip disabled

Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LNA, bias circuits, and control logic. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
2	LNA_IN	RF Input pin. This pin is internally matched for optimum noise figure from a 50Ω source. This pin is internally DC-biased and, if connected to a device with DC present, should be blocked with a capacitor suitable for the frequency of operation.	
3	GND2	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
4	GND1	Ground connection for the LNA circuits. For best performance, keep traces physically short and connect immediately to ground plane.	See pin 2.
5	ATTN	Attenuation pin. A logic high reduces LNA gain by 15dB.	
6	LNA OUT	LNA Output pin. This pin requires a connection to V_{CC} through an inductor.	
7	SOURCE	Connection to source of MOSFET transistor used as mixer. Drain and source are symmetric.	
8	DRAIN	Connection to drain of MOSFET transistor used as mixer.	See pin 7.
9	GATE	Connection to gate of MOSFET transistor used as mixer. Internally DC-biased. Use DC-blocking capacitor.	See pin 7.
10	PD	Power control. A logic "low" turns the part off. A logic "high" (>1.6V) turns the part on.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 3, 5, 9, 10.	

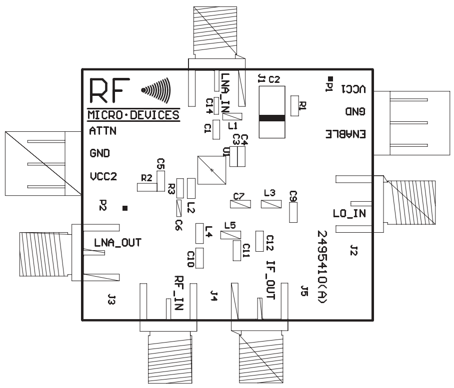
Evaluation Board Schematic

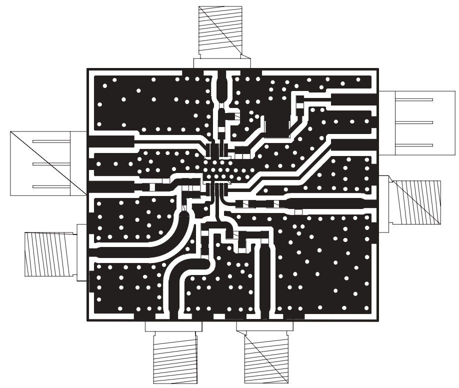
(Download Bill of Materials from www.rfmd.com.)

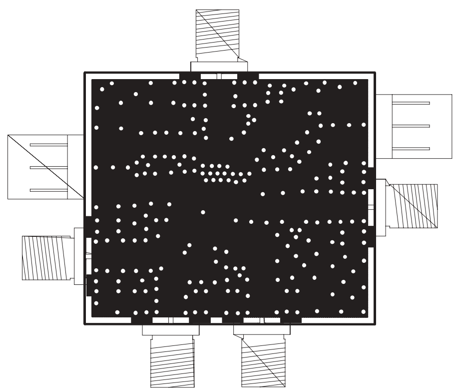


Evaluation Board Layout
Board Size 1.108” x 1.281”

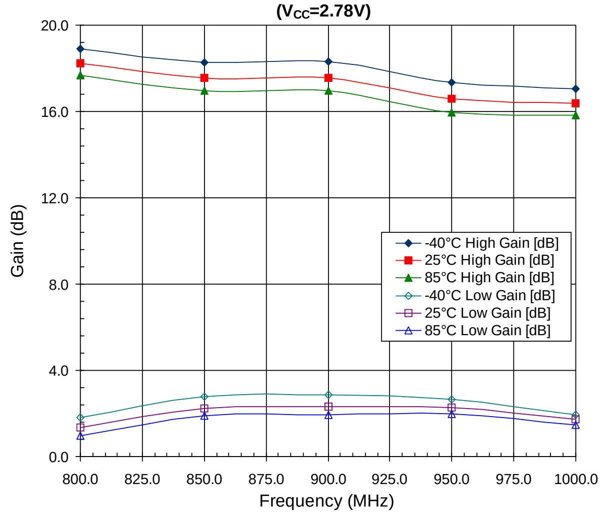
Board Thickness 0.031”, Board Material FR-4



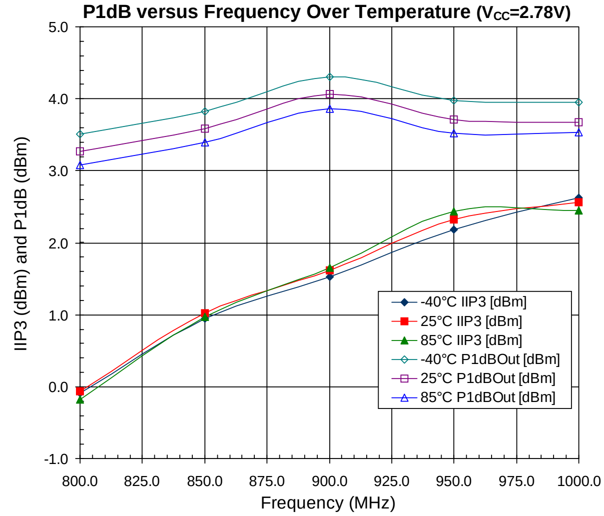




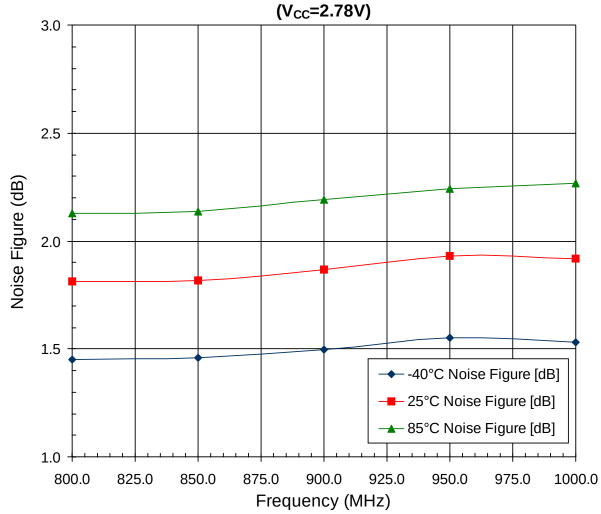
LNA: Gain versus Frequency Over Temperature (V_{CC}=2.78V)



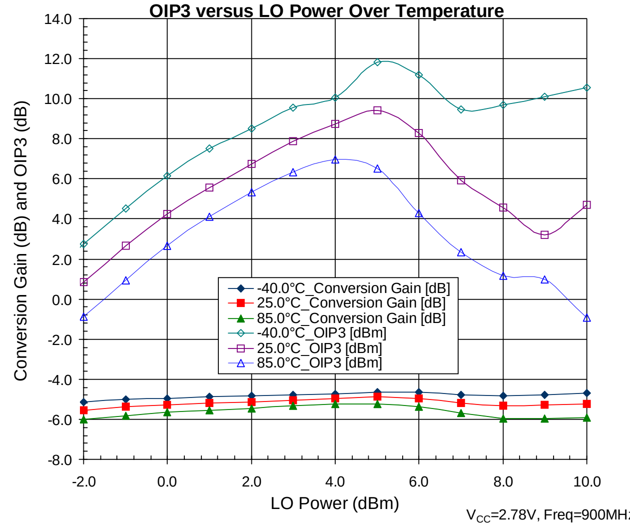
LNA: IIP3 versus Frequency and P1dB versus Frequency Over Temperature (V_{CC}=2.78V)



LNA: Noise Figure versus Frequency Over Temperature (V_{CC}=2.78V)



Mixer: Conversion Gain versus LO Power, OIP3 versus LO Power Over Temperature



Mixer: Conversion Gain versus Frequency, OIP3 versus Frequency Over Temperature