RF2870

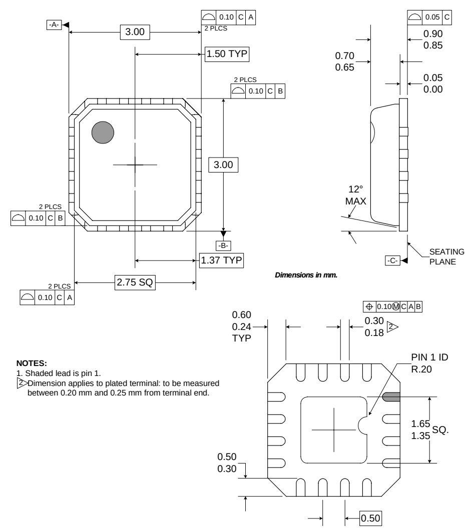
CDMA LOW NOISE AMPLIFIER/MIXER 900MHz DOWNCONVERTER

Typical Applications

- CDMA Cellular Systems
- JCDMA Cellular Systems
- AMPS Cellular Systems
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

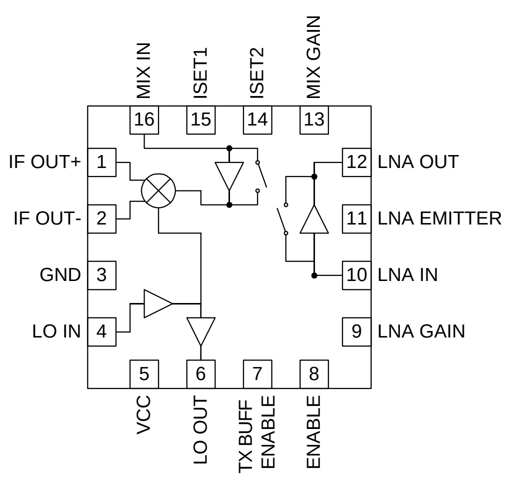
The RF2870 is a receiver front-end for CDMA cellular applications. It is designed to amplify and downconvert RF signals, while providing 28.5dB of stepped gain control range. Features include digital control of LNA gain, mixer gain, and power down mode. Another feature of the chip is adjustable IIP3 of the mixer using an off-chip current setting resistor. Noise figure, IP3, and other specs are designed to be compatible with the IS-98B interim standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Germanium Bi-CMOS process and is assembled in a 3mmx3mm, 16-pin, QFN package.



Package Style: QFN, 16-Pin, 3x3

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☑ SiGe Bi-CMOS



Functional Block Diagram

Features

- 3mmx3mm LNA/Mixer Solution
- Adjustable Mixer Current/IIP3
- Meets IMD Tests with Three Gain States/Two Logic Control Lines
- Integrated TX LO Buffer Amplifier
- All Pins ESD Protected

Ordering Information

RF2870	CDMA Low Noise Amplifier/Mixer 900MHz Downconverter
RF2870 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.75V
RF Frequency Range		800 to 900		MHz	
IF Frequency Range	0.1		400	MHz	
Power Supply					
Supply Voltage, V_S	2.65	2.75	3.15	V	
Logic High	1.8		V_S+0.6	V	
Logic Low			0.4	V	
Cellular Band					Freq=869MHz to 894MHz
JCDMA Band					Freq=832MHz to 870MHz
LNA (On)					LNA 50Ω match
Gain	13.0	14.5	16.0	dB	
Noise Figure		1.1	1.3	dB	
Input IP3	+9.0	+11.5		dBm	
Isolation		23		dB	
LNA (Off)					
Gain	-4.0	-3.0	-2.0	dB	
Noise Figure		3.0	4.0	dB	
Input IP3	+20.0	+25.0		dBm	
Isolation		3.5		dB	
Mixer - CDMA/JCDMA/FM					
Gain	11.5	13.0	14.5	dB	Mixer Preamp ON
	0.5	2.0	3.5	dB	Mixer Preamp OFF
Noise Figure		6.5	7.5	dB	Mixer Preamp ON (TX Buffer OFF)
		14.0	16.0	dB	Mixer Preamp OFF
Input IP3	+1.0	+3.0		dBm	Mixer Preamp ON
	+12.5	+14.5		dBm	Mixer Preamp OFF
LO to RF Isolation	36			dB	Mixer Preamp ON
				dB	Mixer Preamp OFF

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Cellular Band **JCDMA Band, cont'd**					
Other					
LO-IF Isolation	30			dB	
RF-IF Isolation	40			dB	
LNA Out to Mixer In Isolation	40			dB	
LO-LNA In Isolation, Any State	35			dB	
Control Lines					
Input Capacitance			1	pF	LNA GAIN, ENABLE, MIX GAIN, TX BUFF ENABLE
Local Oscillator Input					
Cellular - CDMA or FM					
Input Power	-10	-4	0	dBm	
Input Frequency	685		710	MHz	IF=184MHz
	1053		1078	MHz	IF=184MHz
	784		809	MHz	IF=85MHz
	954		979	MHz	IF=85MHz
Cellular - JCDMA					
Input Power	-10	-4	0	dBm	
Input Frequency	722		760	MHz	IF=110MHz
	942		980	MHz	IF=110MHz
TX (Local Oscillator) Buffer					
Cellular - CDMA or FM					
Output Power	-9.0	-5.5	-2.0	dBm	Single-ended 50Ω load
Output Frequency	685		710	MHz	IF=184MHz
	1053		1078	MHz	IF=184MHz
	784		809	MHz	IF=85MHz
	954		979	MHz	IF=85MHz
Current Consumption		2		mA	
Cellular - JCDMA					
Output Power	-9	-5.5		dBm	Single-ended 50Ω load
Output Frequency	722		760	MHz	IF=110MHz
	942		980	MHz	IF=110MHz
Current Consumption		2		mA	

Evaluation Board Current Measurement (Typical Values for V_{CC}=2.75V)

	ENABLE	LNA GAIN	MIX GAIN	TX BUFF ENABLE	IDC (mA)
Gain Control State					
Power Down	0	X	X	X	<0.01
LNA On, Mixer Preamp On, TX Buffer Off	1	0	0	0	26.5
LNA On, Mixer Preamp Off, TX Buffer Off	1	0	1	0	20.6
LNA Bypassed, Mixer Preamp On, TX Buffer Off	1	1	1	0	20.9
LNA Bypassed, Mixer Preamp Off, TX Buffer Off	1	1	0	0	15.0

NOTES:

All IDC current numbers include bias circuitry current of 1.5mA to 2.0mA (dependent on mode).

TX Buffer On: Add 2.4mA to total current.

Cascaded Performance (Typical Values for V_{CC}=2.75V)

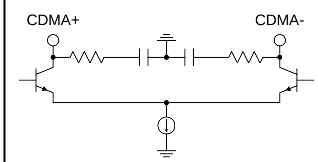
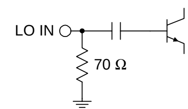
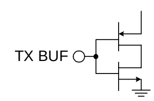
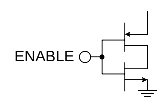
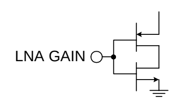
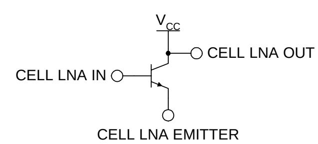
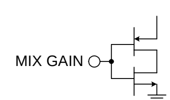
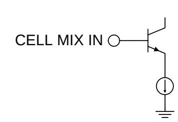
NOTE: All total current numbers include bias circuitry current of 1.5mA to 2.0mA (dependent on mode).

Parameter	*CELL CDMA*			
	LNA ON	LNA OFF	LNA ON	LNA OFF
	Mixer Preamp On		*Mixer Preamp Off*	
Cascaded:				
Gain (dB)	25.0	7.5	14.0	-3.5
Noise Figure (dB)	1.9	12.0	4.5	19.5
Input IP3 (dBm)	-9.0	+8.4	+2.0	+18.8
LO to IF Isolation (dB)	30	30	30	30
IF1 to RF Isolation (dB)	40	40	40	40
IF2 to RF Isolation (dB)	40	40	40	40
LO to LNA IN Isolation (dB)	45	45	45	45
Total Current (mA)	26.5	20.9	20.6	15.0

NOTE: Assumes 2.5dB image filter insertion loss. The TX Buffer Enable is off.

Gain Control State Table

Gain State	LNA Gain Logic Input	Mix Gain Logic Input	*Corresponding Device State*		Comments
			LNA Amplifier	Mixer Preamp	
High Gain	0	0	On	On	IMD Test 1 and 2
Mid Gain	0	1	On	Off	IMD Test 3 and 4
Low Gain	1	1	Off	On	IMD Test 5 and 6
Ultra-Low Gain	1	0	Off	Off	

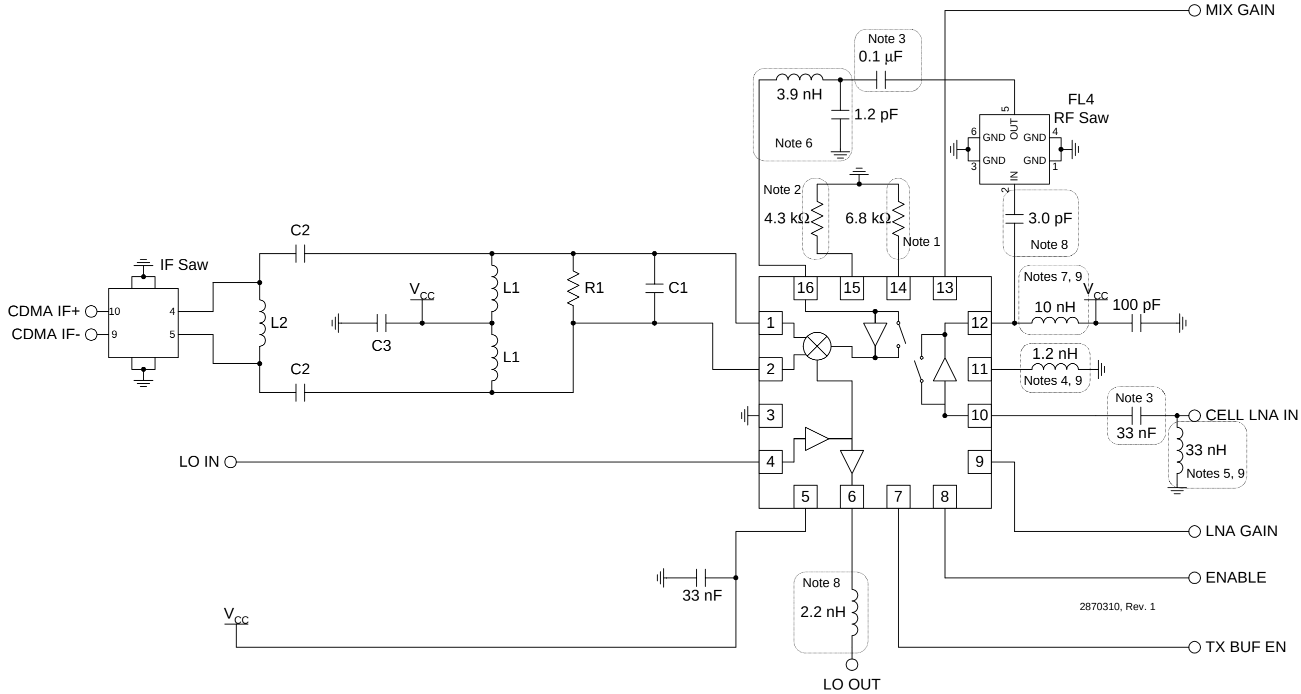
Pin	Function	Description	Interface Schematic
1	IF OUT+	CDMA IF output. Open collector.	
2	IF OUT-	CDMA IF output. Open collector.	See pin 1.
3	GND		
4	LO IN	LO single-end input. Matched to 50Ω.	
5	VCC	External bypass capacitor may be required.	
6	LO OUT	LO output. Internal DC block. Drives 50Ω.	
7	TX BUFF ENABLE	Logic input. High enables TX LO output buffer amplifiers.	
8	ENABLE	Logic input. Low level powers down the IC.	
9	LNA GAIN	Logic input. See Gain Control State table.	
10	LNA IN	Cellular LNA input.	
11	LNA EMITTER	Cellular LNA emitter. A small inductor connects this pin to ground. Cellular LNA gain can be adjusted by the inductance.	See pin 10.
12	LNA OUT	Cellular LNA output. Simple external L-C components required for matching and VCC supply.	See pin 10.
13	MIX GAIN	Logic input. See Gain Control State table.	
14	ISET2	An external resistor R2 connected to this pin sets the current of the mixer. Decreasing resistance increases current.	
15	ISET1	Sets internal voltage reference. External resistor required.	
16	MIX IN	Cellular mixer RF single-end input. Matched to 50Ω.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

ISET Pins

ISET1 sets the internal reference voltage for the bias control circuits to all functional blocks. An external resistor of 4.3kΩ to ground is recommended. We do not recommend adjusting this resistor value. This resistor is pulled out to allow for a higher precision off chip value and not as a significant tuning adjustment.

ISET2 sets the DC current through the mixer and mixer preamplifier. Higher resistance to ground results in lower current. Lower current will improve mixer NF but will degrade IIP3. Mixer and the mixer preamp gain is not significantly changed with current.

Application Schematic
Differential IF SAW Filter Topology



NOTES:

Differential IF tuning components are dependent on IF frequency board layout and board parasitics. Please consult RFMD applications engineering for tuning assistance.

If any functional blocks are not being used, the unused pins can be left with no connection.

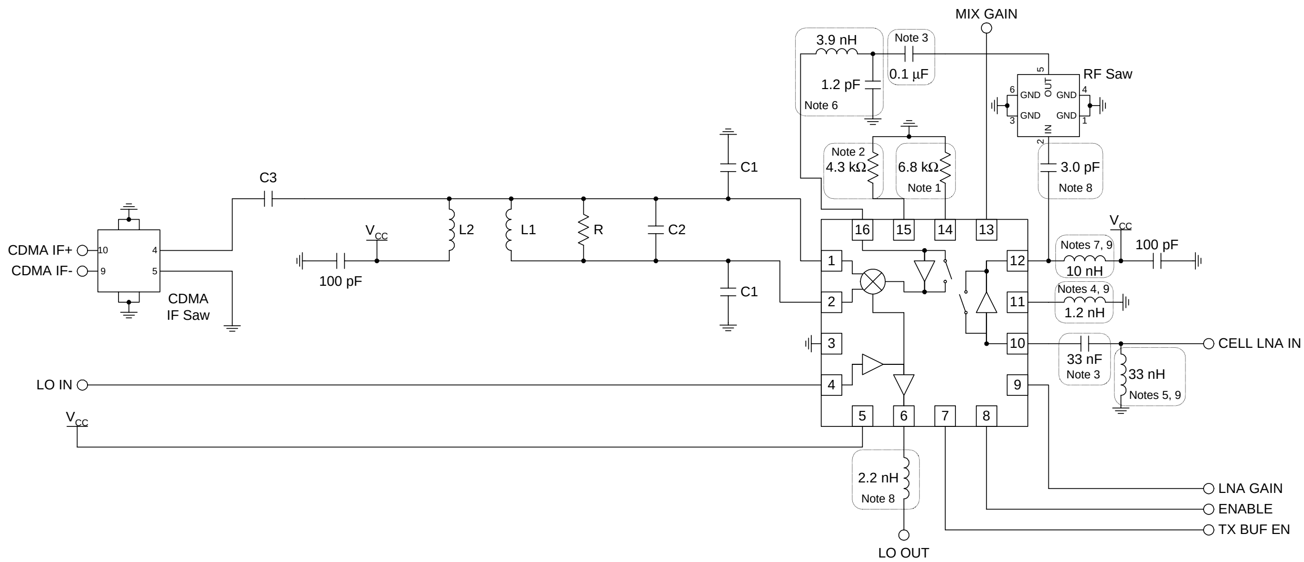
IF output matching component values are dependent on board layout, IF SAW filter and the IF frequency selected. Please contact RFMD application engineering for assistance with IF output matching.

1. This resistor sets the mixer preamp and mixer currents. Lowering the resistance results in higher currents.
2. Sets internal bias voltage. Recommend 4.3kΩ.
3. DC-blocking capacitor.
4. Determines trade-off between IIP3 and gain. Higher value inductor means lower gain and higher IIP3.
5. Cell LNA input matching for optimum IIP3. Low impedance path to ground at low frequency for optimum IIP3.
6. Mixer input matching.
7. For output matching and a DC supply bias choke.
8. Input or output matching.
9. Coupling of coils on the input, output and emitter of the LNA should be minimized to reduce the risk of oscillation. We recommend separating the inductors and/or positioning them 90° relative to each other.

Layout Note:

To minimize losses and radiation, the RF signal traces should be as short as possible. The IF+ and IF- output traces should be symmetrical. All bypass capacitors and matching capacitors must have a ground via very close to the capacitor. Each capacitor should have its own ground via. All traces should be 50Ω transmission lines. Position inductors to reduce coupling. (See note 9.)

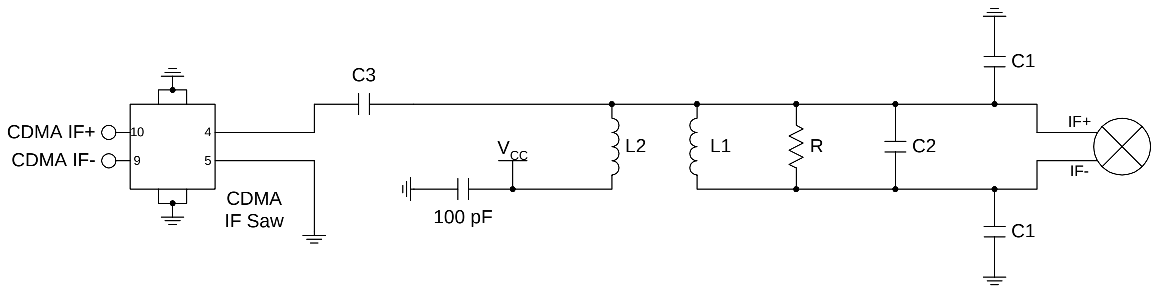
Application Schematic
Single-End IF Matching



See notes on previous page.

IF Output Interface Network

Single-End IF Matching



L1, C1, C2, and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C_1 + 2C_2 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 9 and 10. An average value to use for C_{EQ} is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

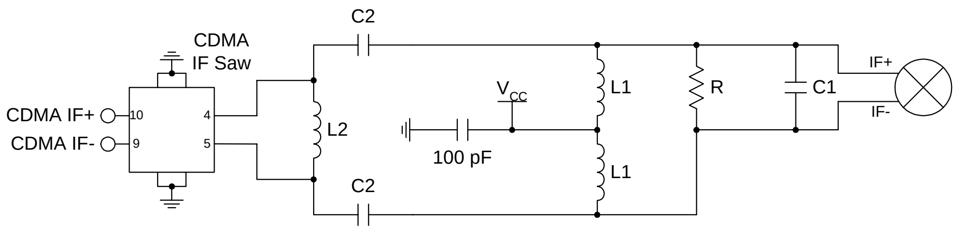
where R_{OUT} is the desired output impedance and R_P is the parasitic equivalent parallel resistance of L1.

C_2 should first be set to 0 and C1 should be chosen as high as possible (not greater than 39pF), while maintaining an R_P of L1 that allows for the desired R_{OUT}. If the self-resonant frequencies of the selected C1 produce unsatisfactory linearity performance, their values may be reduced and compensated for by including C2 capacitor with a value chosen to maintain the desired F_{IF} frequency.

L2 and C3 serve dual purposes. L2 serves as an output bias choke, and C3 serves as a series DC block.

In addition, L2 and C3 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to R_{OUT}. Otherwise, L2 is chosen to be large (suggested 120nH) and C3 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC-blocked.

Differential IF Matching

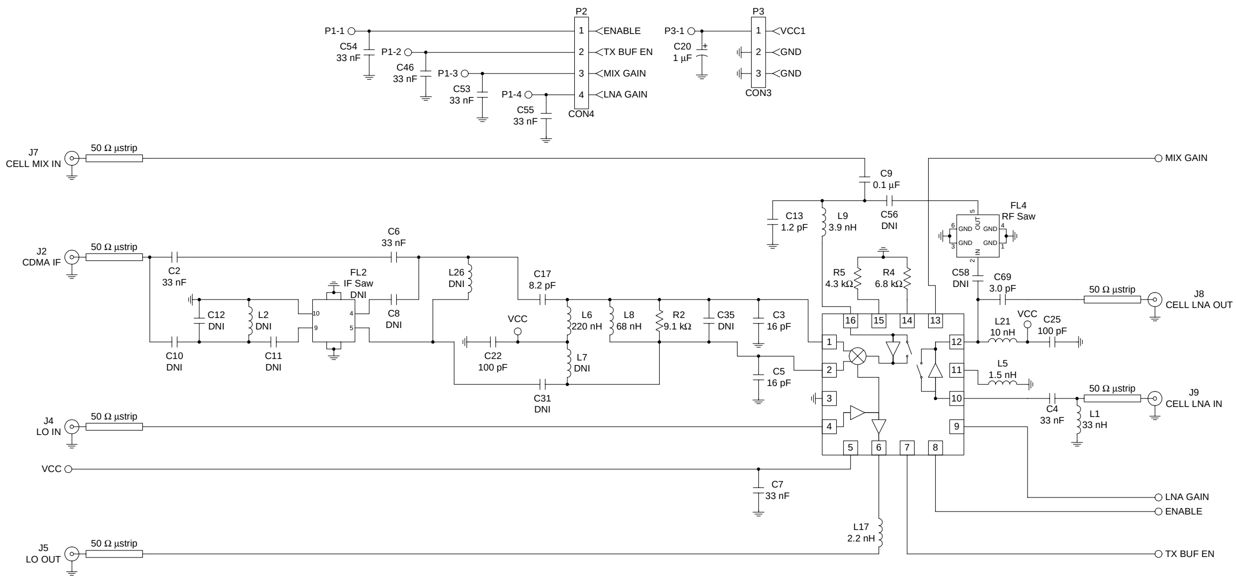


L1 and C1 are chosen to resonate at the desired IF frequency. C1 can be omitted and the value of L1 increased and utilized solely as a choke to provide V_{CC} to the open-collector outputs, but it is strongly recommended that at least some small-valued C1 (a few pF) be retained for better mixer linearity performance. R is normally selected to match the input impedance of the IF filter. However, mixer performance can be modified by selecting an R value that is different from the IF filter input impedance, and inserting a conjugate matching network between the Resistive Output Network and the IF filter.

C2 serve dual purposes. C2 serves as a series DC block when a DC path to ground is present in the IF filter. In addition, C2 may be chosen to improve the combine performance of the mixer and IF filter. L2 should choose to resonate with the internal capacitance of the SAW filter. Usually, SAW filter has some capacitance. Otherwise, L2 could be eliminated.

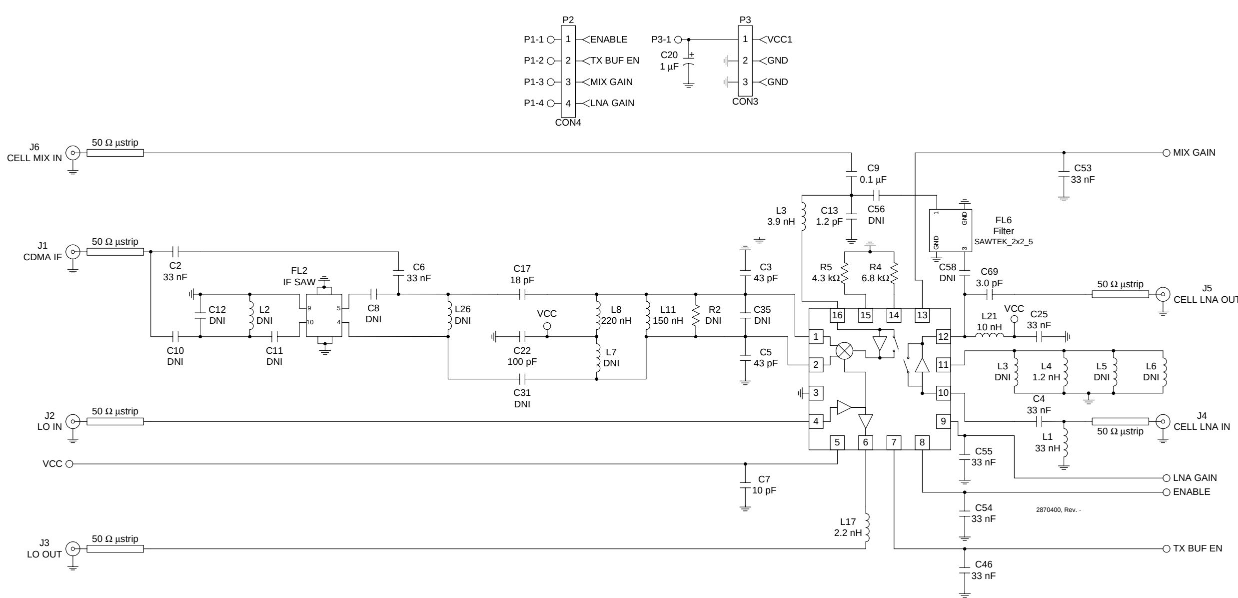
A practical approach to obtain the differential matching is to tune the mixer to the correct load point for gain, IIP3, and NF using the single-end current combiner method. Second, use the component values found in the single-end approach as starting point for the differential matching. The two-shunt capacitors in the single-end could be converted in a parallel capacitor and the parallel inductor in the single-end need to be converted in two-choke inductor. Third, set the DC block capacitors (C2) in the differential-end matching to a high value (i.e., 100pF) and retune the resonate circuit (C1 & L1) and the resistor (R) for optimal performance. After optimal performance is achieved and if performance is not satisfactory, decrease the series capacitors until optimal performance is achieved.

Evaluation Board Schematic
IF Frequency=183.6MHz



Evaluation Board Schematic
IF Frequency=85.38MHz

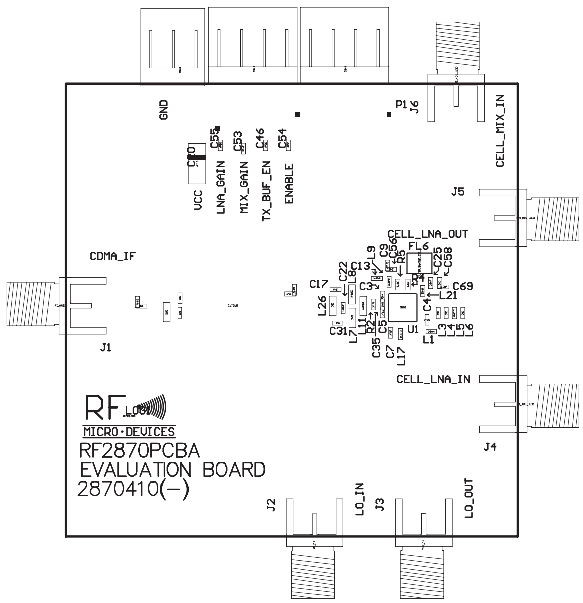
(Stock Evaluation Boards are at this IF)



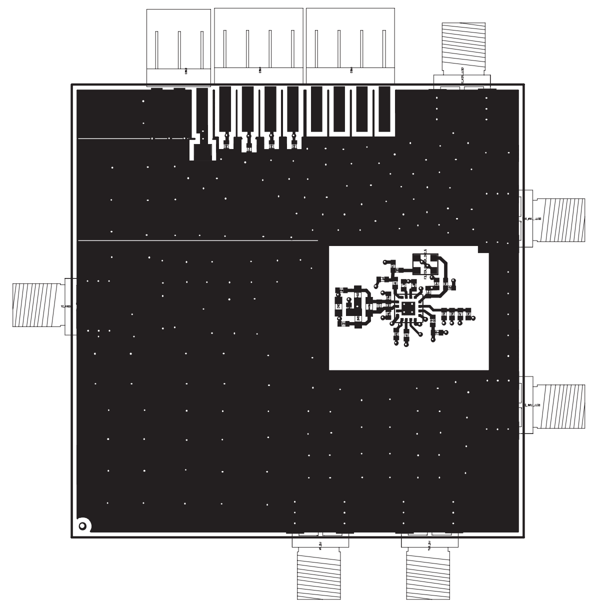
Evaluation Board Layout
Board Size 2”x2”

Board Thickness 0.061”, Board Material FR-4, Multi-Layer

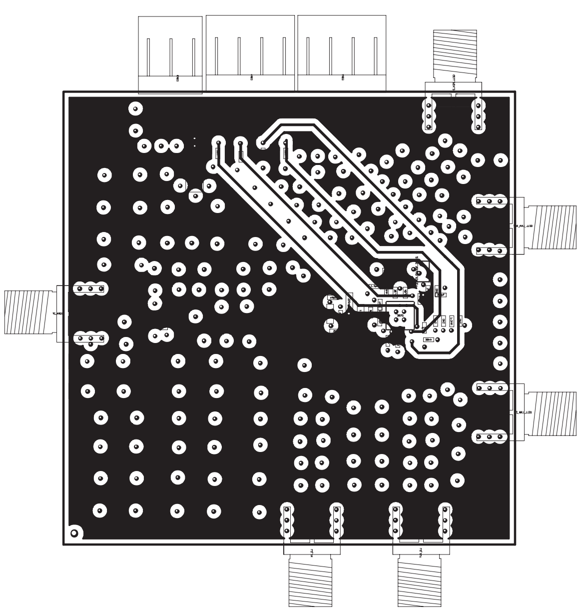
Assembly



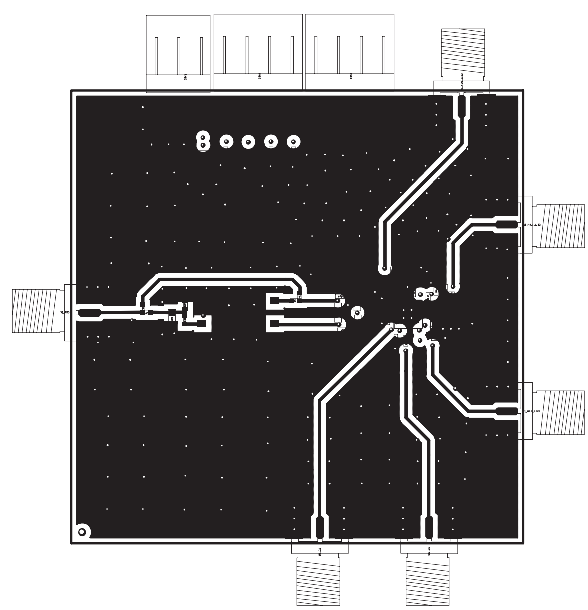
Top



Mid



Back



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is Electroless Nickel, immersion Gold. Typical thickness is 3μinch to 8μinch Gold over 180μinch Nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

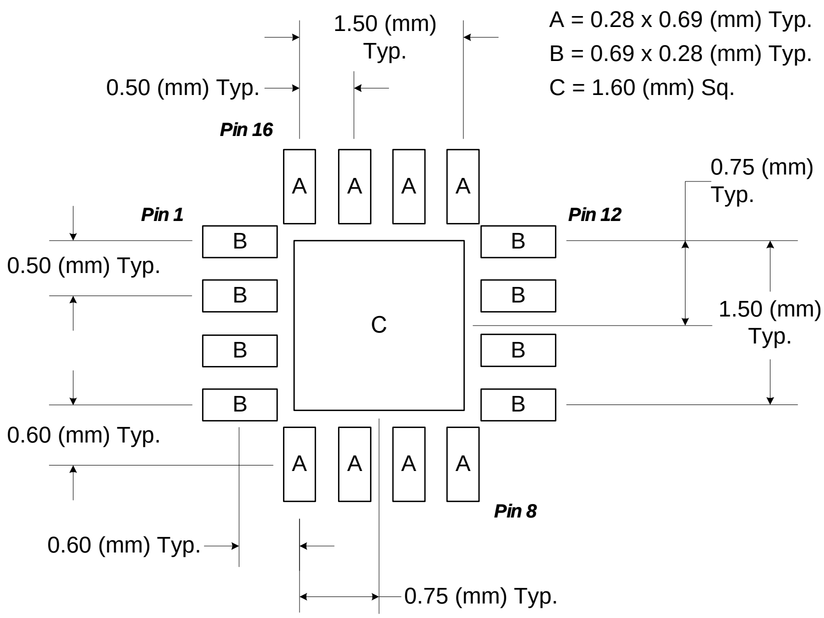


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

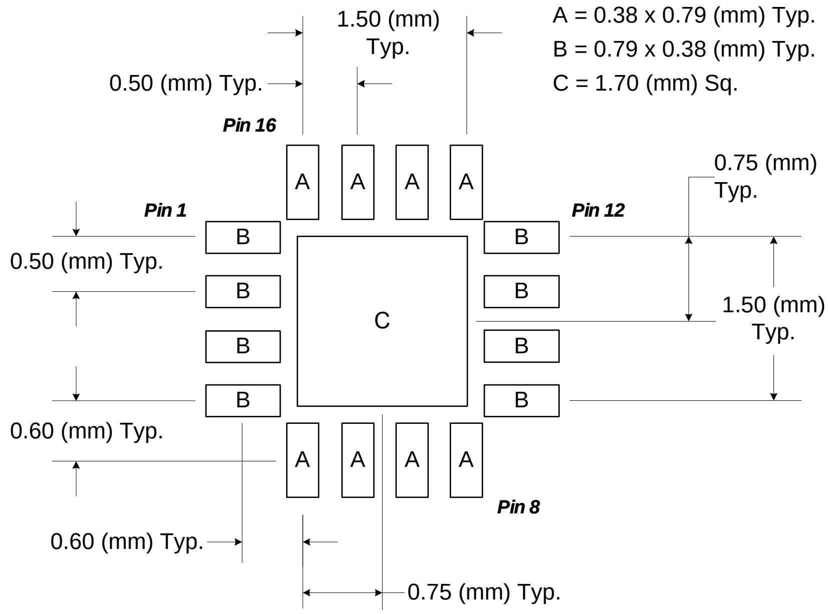


Figure 2. PCB Solder Mask Pattern (Top View)