RFD12N06RLE, RFD12N06RLESM, RFP12N06RLE

Data Sheet July 1999 File Number 2407.4

12A, 60V, 0.135 Ohm, N-Channel, Logic Level, Power MOSFETs

These N-Channel logic level ESD protected power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09861.

Ordering Information

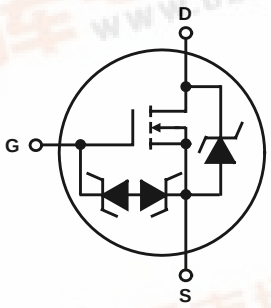
PART NUMBER	PACKAGE	BRAND
RFD12N06RLE	TO-251AA	12N6LE
RFD12N06RLESM	TO-252AA	12N6LE
RFP12N06RLE	TO-220AB	12N06RLE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e., RFD12N06RLESM9A.

Features

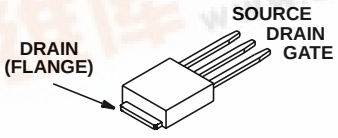
- 12A, 60V
- $r_{DS(ON)} = 0.135\Omega$
- Electrostatic Discharge Protected
- UIS Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

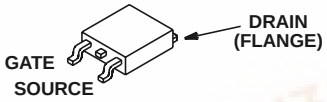


Packaging

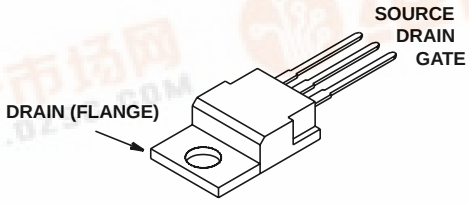
JEDEC TO-251AA



JEDEC TO-252AA



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFD12N06RLE, RFD12N06RLESM, RFP12N06RLE	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Continuous Drain Current	I_D	12	A
Pulsed Drain Current (Note 3)	I_{DM}	26	A
Gate to Source Voltage	V_{GS}	-5 to10	V
Power Dissipation	P_D	40	W
Linear Derating Factor		0.32	$W/^oC$
Single Pulse Avalanche Energy Rating	E_{AS}	Refer to UIS SOA Curve	
Electrostatic Discharge Rating ESD, MIL-STD-883, Category B(2)		2	kV
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 150^oC$		-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = -5 to 10V		-	-	±10	μA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 12A, V_{GS} = 5V (Figures 7, 8)		-	-	0.135	Ω
		I_D = 12A, V_{GS} = 4V		-	-	0.160	Ω
Turn-On Time	$t_{(ON)}$	V_{DD} = 30V, $I_D \approx$ 6A, R_L = 5Ω, R_{GS} = 6.25Ω, V_{GS} = 5V, (Figures 15, 16)		-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$			-	12	-	ns
Rise Time	t_r			-	20	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	24	-	ns
Fall Time	t_f			-	12	-	ns
Turn-Off Time	$t_{(OFF)}$			-	-	60	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 48V, I_D = 12A, R_L = 4Ω, $I_{G(REF)}$ = 0.25mA (Figures 17, 18)	-	-	40	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	-	20	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	-	1.5	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.125	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA and TO-252AA		-	-	100	$^oC/W$
		TO-220AB		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 12A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	I_{SD} = 12A, dI_{SD}/dt = 100A/μs	-	-	200	ns

NOTES:

2. Pulse test: pulse width ≤ 300ms, duty cycle ≤ 2%.
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

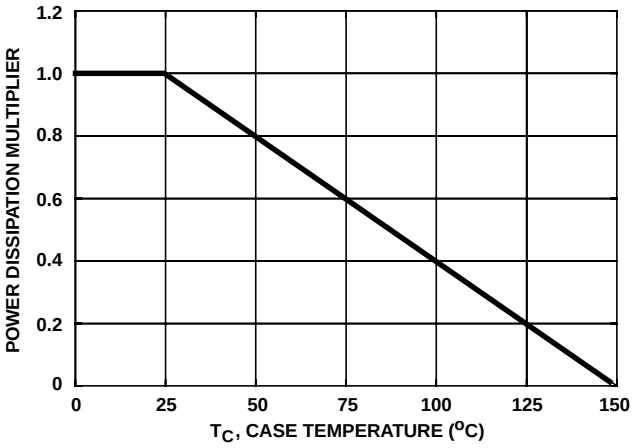


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

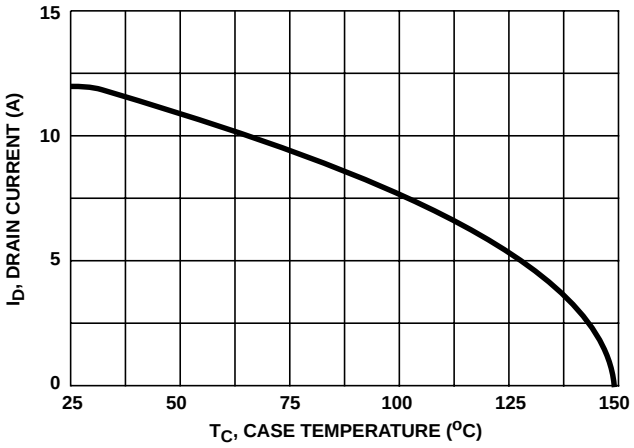


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

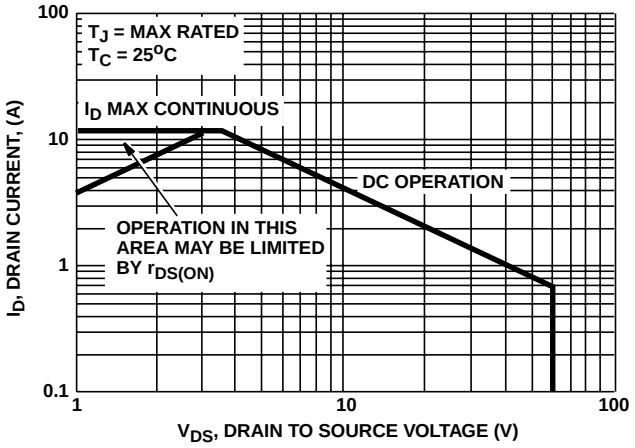
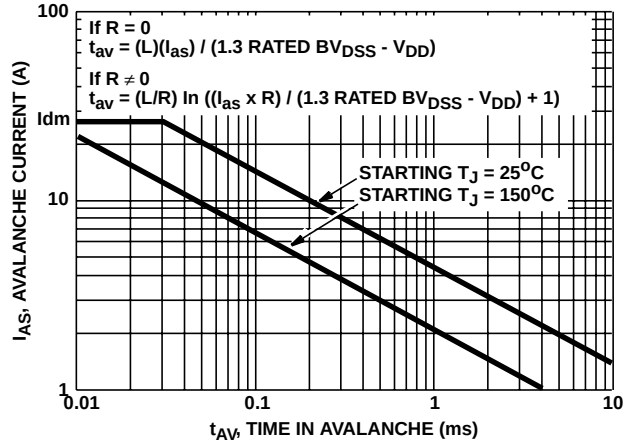


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

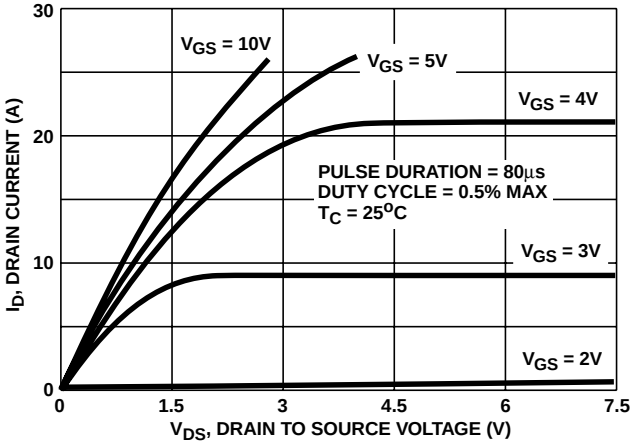


FIGURE 5. SATURATION CHARACTERISTICS

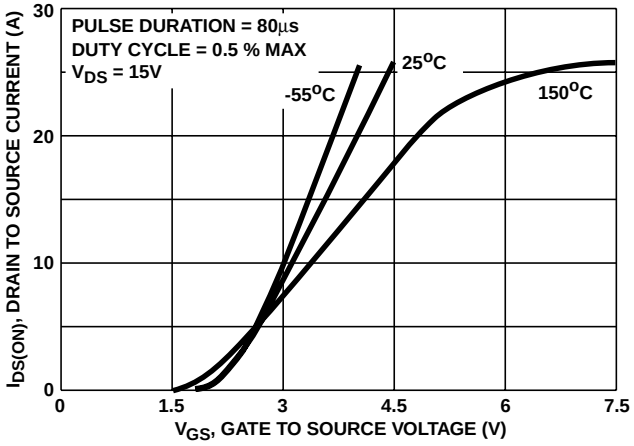


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

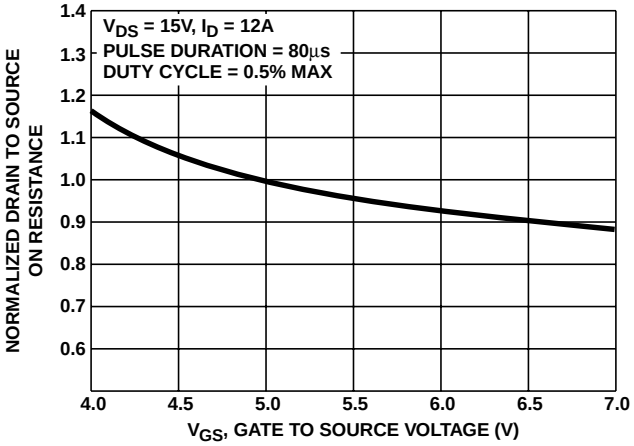


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs GATE TO SOURCE VOLTAGE

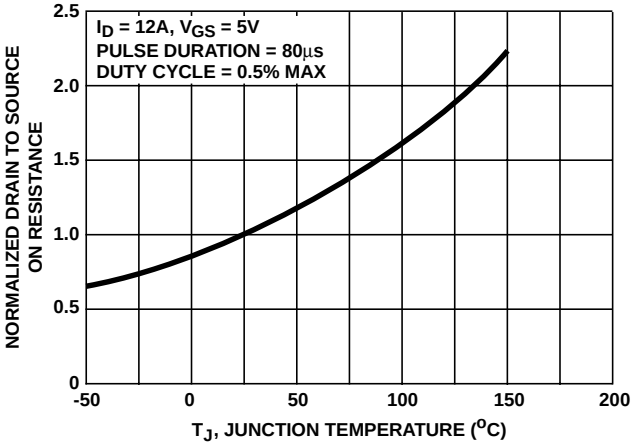


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

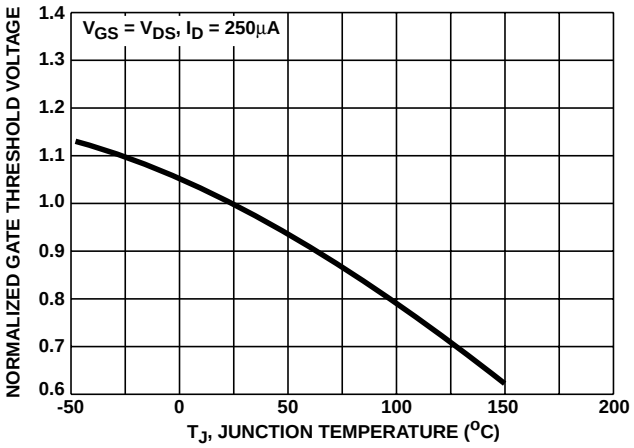


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

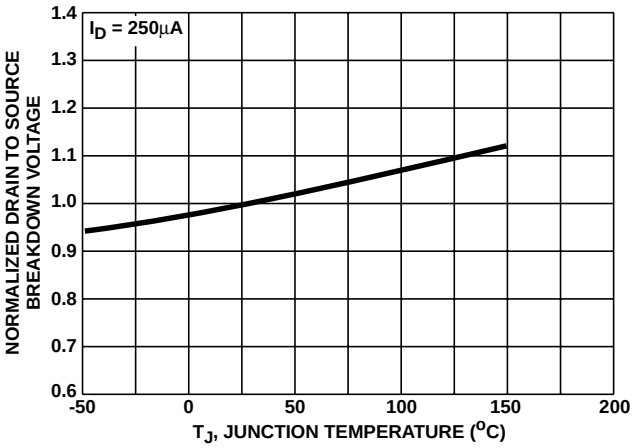


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

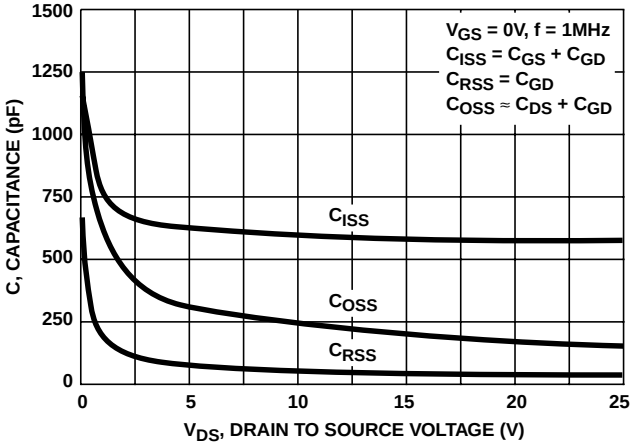
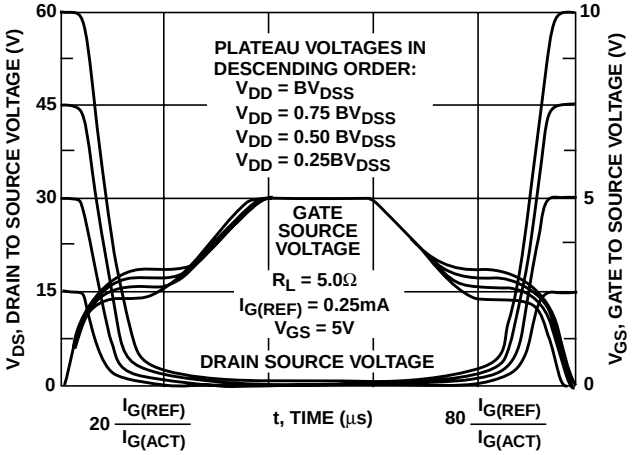


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

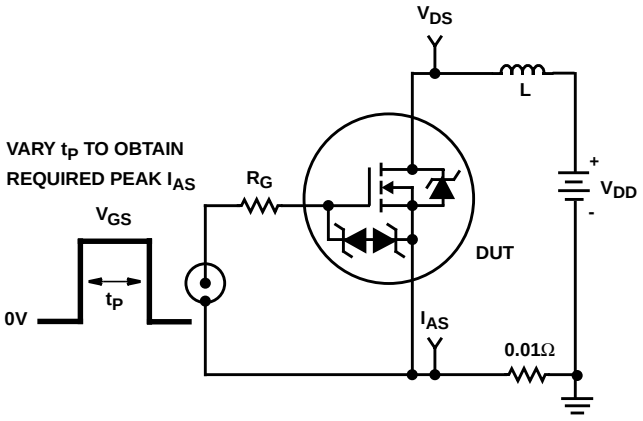


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

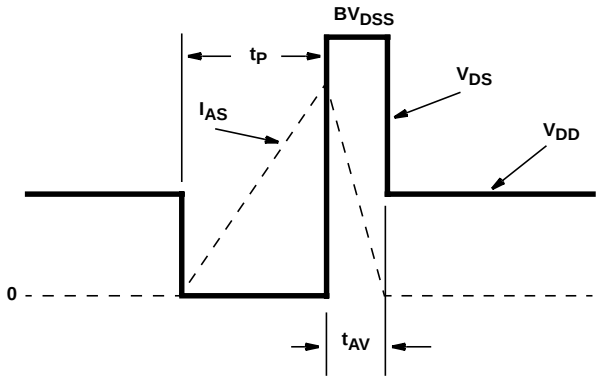


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

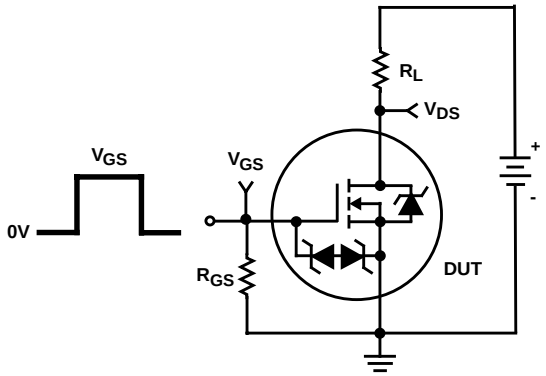


FIGURE 15. SWITCHING TIME TEST CIRCUIT

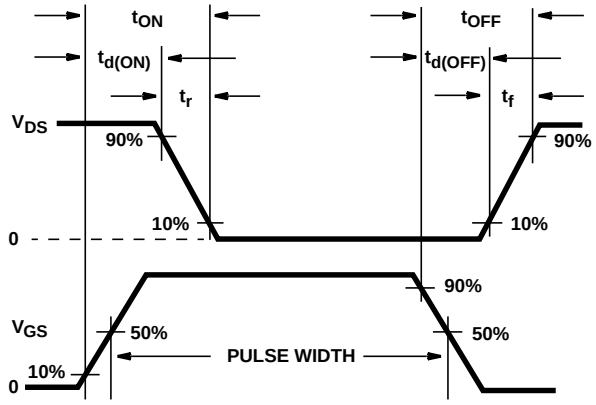


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

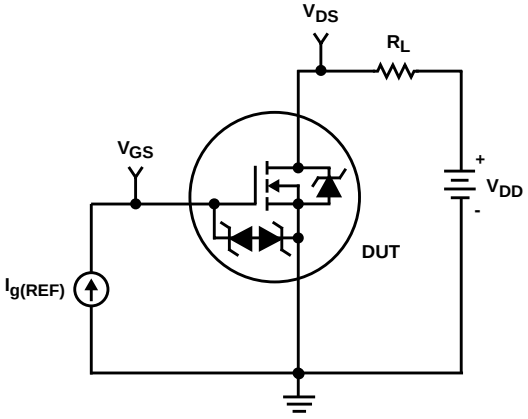


FIGURE 17. GATE CHARGE TEST CIRCUIT

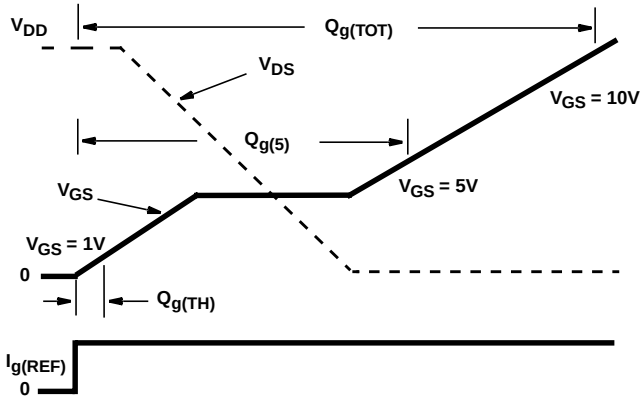


FIGURE 18. GATE CHARGE WAVEFORMS

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