Data Sheet September 1998 File Number 3975.2

25A†, 60V, 0.030 Ohm, P-Channel Power MOSFET

The RFF60P06 P-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Reliability screening is available as either commercial or TX/TXV equivalent of MIL-S-19500. Contact Intersil Corporation High-Reliability Marketing group for any desired deviations from the data sheet.

Formerly developmental type TA09835.

Commercial Version: RFG60P06E.

† Current is limited by the package capability.

Ordering Information

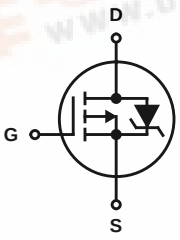
PART NUMBER	PACKAGE	BRAND
RFF60P06	TO-254AA	RFF60P06

NOTE: When ordering, use the entire part number.

Features

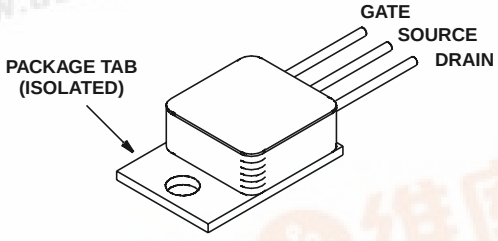
- 25A, 60V
- $r_{DS(ON)} = 0.030\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 150°C Operating Temperature
- Reliability Screened

Symbol



Packaging

JEDEC TO-254AA



CAUTION: Berylia Warning per MIL-S-19500.
Refer to package specifications.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFF60P06	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	-60	V
Drain to Gate Voltage (RGS = 20kΩ) (Note 1)	V_{DGR}	-60	V
Gate to Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	25 (Note 5)	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating (Note 4)	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	125	W
Derate Above 25^oC		1.0	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		-2.0	-3.0	-4.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	-25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$		-	-	-250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, $T_C = 125^oC$		-	-	±100	μA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 25A, V_{GS} = -10V, (Figure 9)		-	-	0.030	Ω
Turn-On Time	t_{ON}	V_{DD} = -30V, I_D = 25A, R_L = 1.2Ω, V_{GS} = -10V R_G = 2.35Ω (Figures 13, 16, 17)		-	-	195	ns
Turn-On Delay Time	$t_{d(ON)}$			-	25	70	ns
Rise Time	t_r			-	50	125	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	80	200	ns
Fall Time	t_f			-	30	75	ns
Turn-Off Time	t_{OFF}			-	-	275	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to -20V	V_{DD} = -30V, I_D = 25A, R_L = 1.2Ω $I_{G(REF)}$ = -4.2mA (Figures 18, 19)	-	-	450	nC
Gate Charge at -10V	$Q_{g(-10)}$	V_{GS} = 0 to -10V		-	-	225	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to -2V		-	-	15	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V f = 1MHz		-	7200	-	pF
Output Capacitance	C_{OSS}			-	1800	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	400	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	48	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = -25A	-	-1.1	-1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = -25A, dI_{SD}/dt = -100A/μs	-	130	200	ns

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3)
4. Current is limited by package capability.

Typical Performance Curves Unless Otherwise Specified

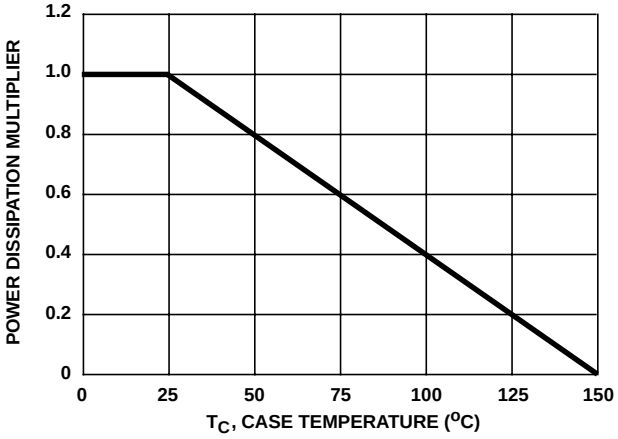


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

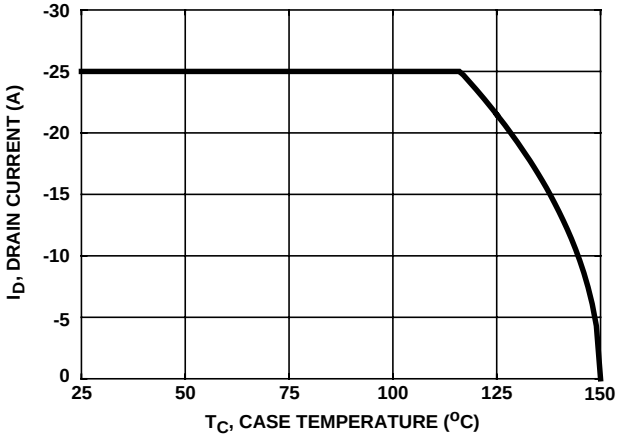


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

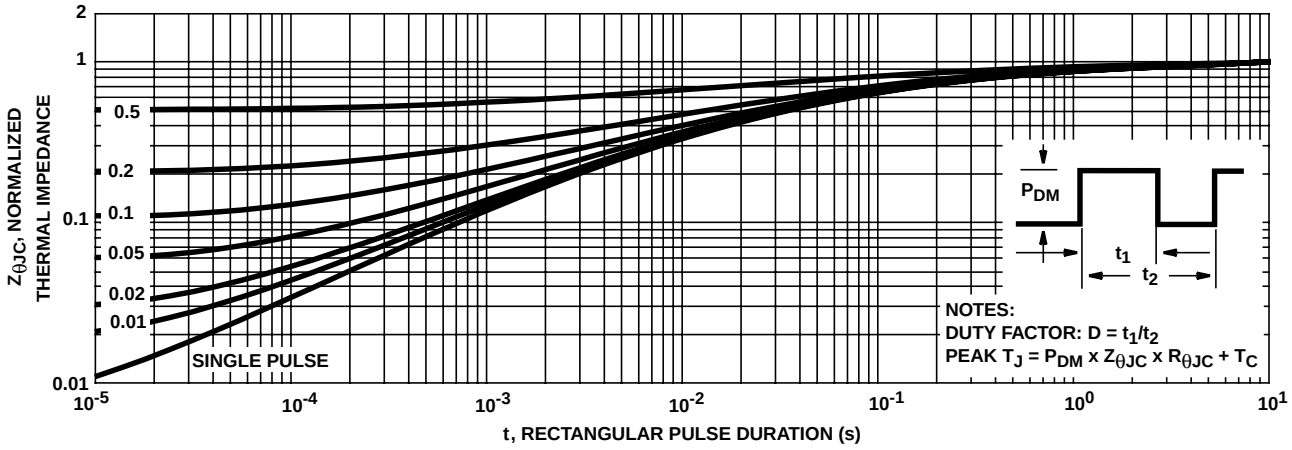


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

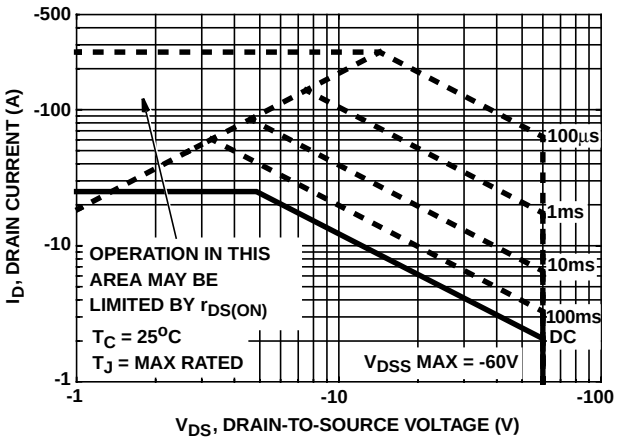


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

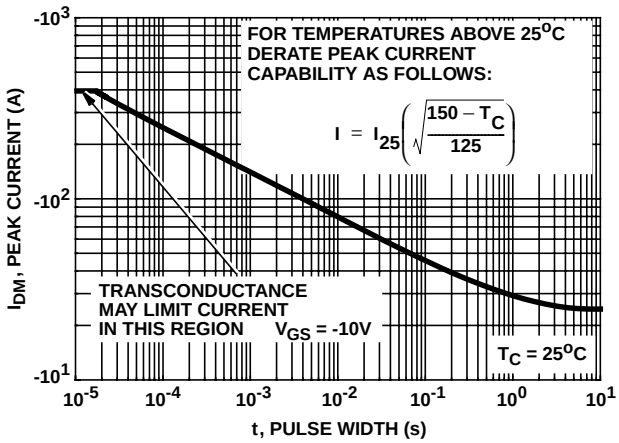


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified **(Continued)**

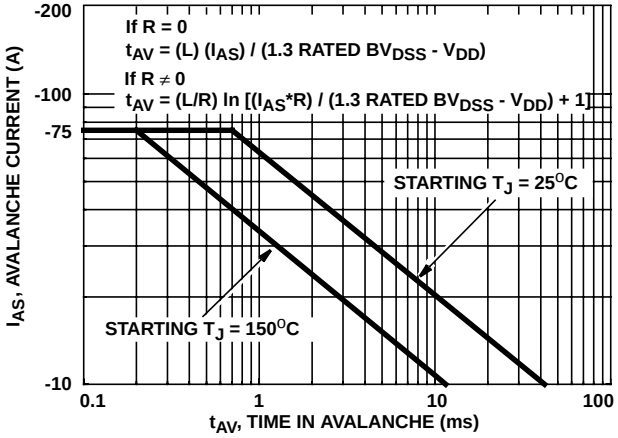


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

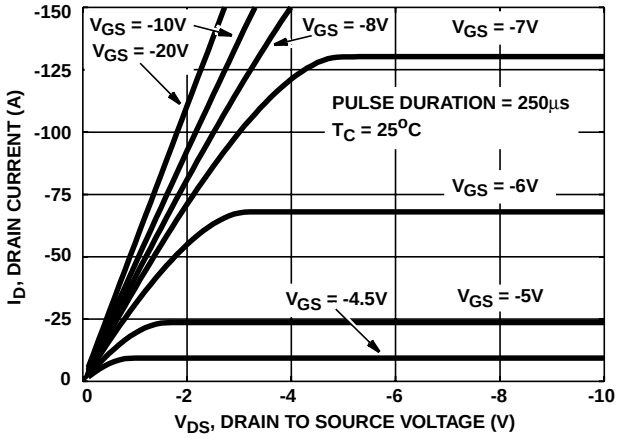


FIGURE 7. SATURATION CHARACTERISTICS

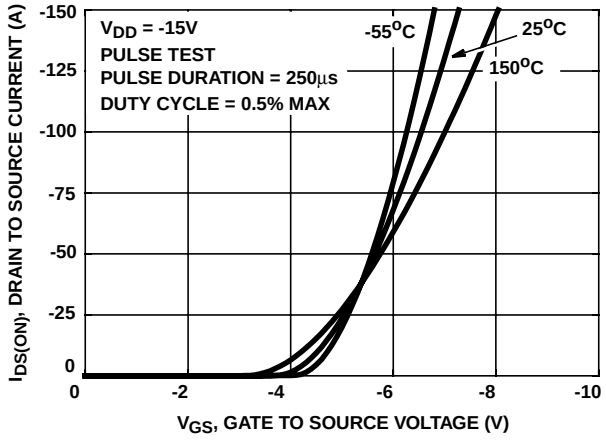


FIGURE 8. TRANSFER CHARACTERISTICS

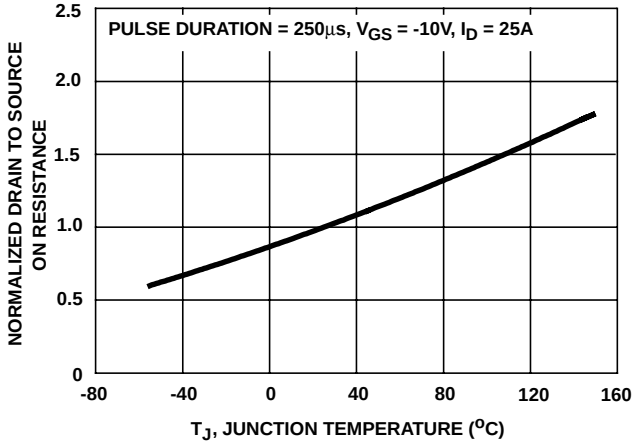


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

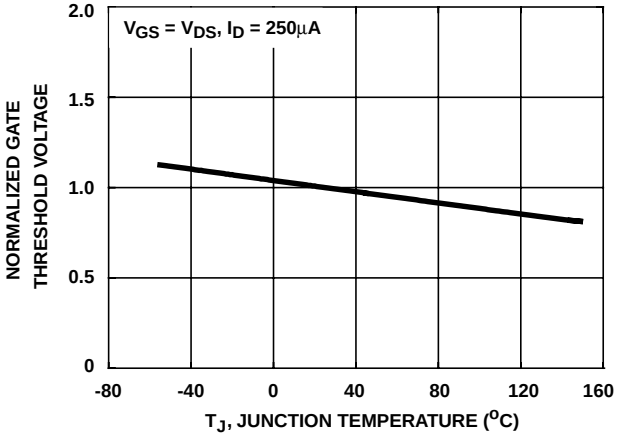


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

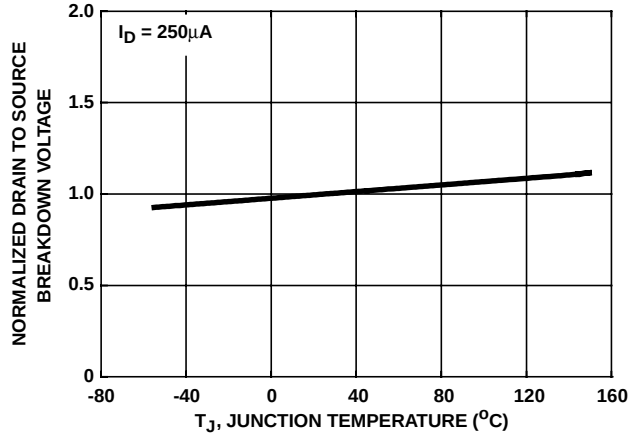


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

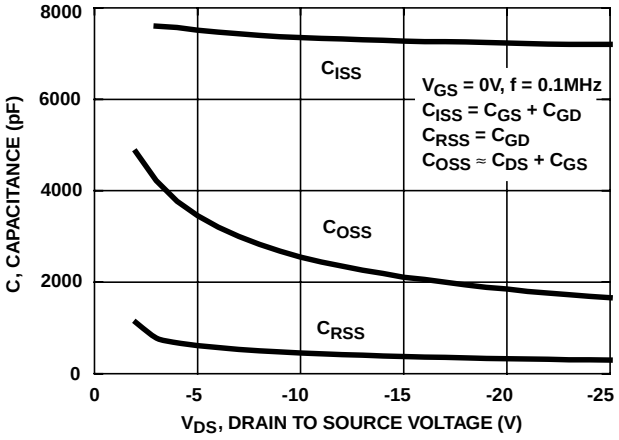
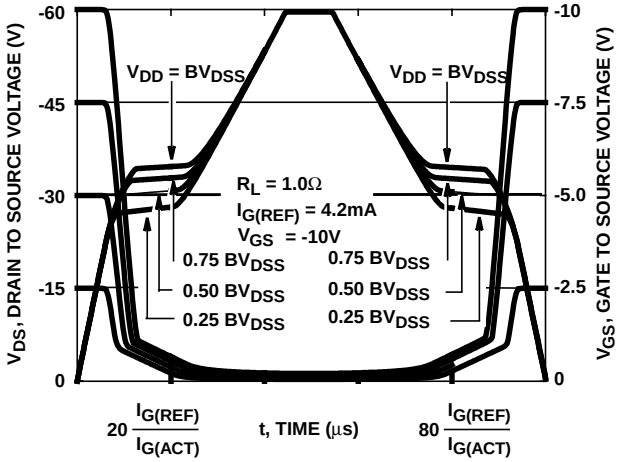


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuit and Waveforms

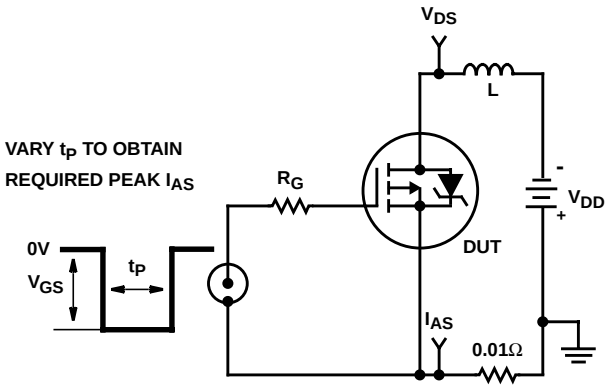


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

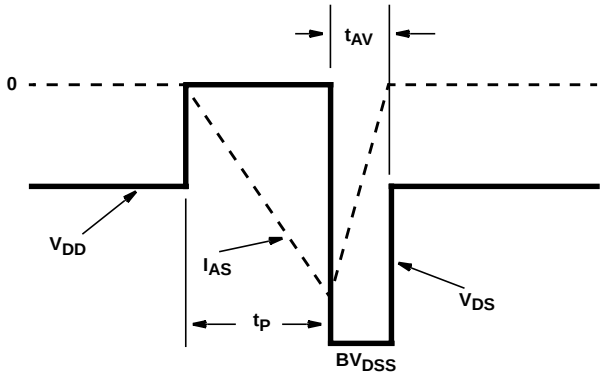


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

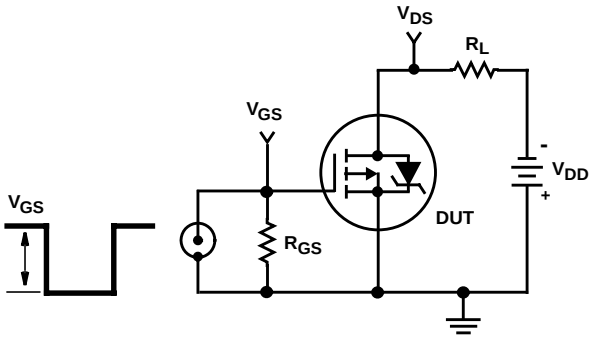


FIGURE 16. SWITCHING TIME TEST CIRCUIT

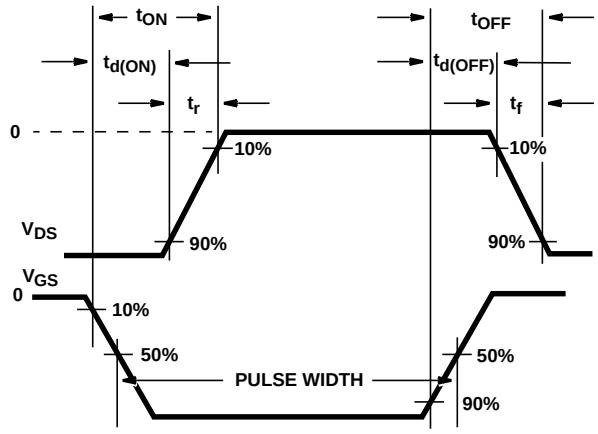


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuit and Waveforms (Continued)

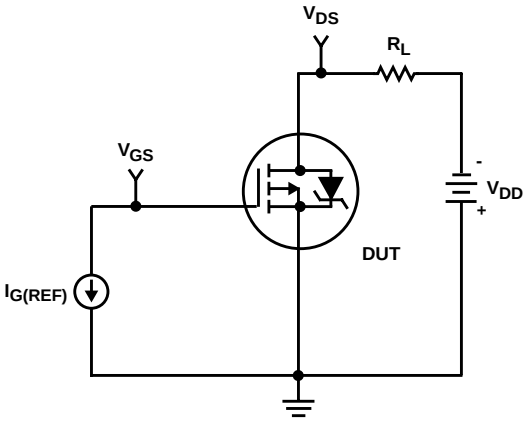


FIGURE 18. GATE CHARGE TEST CIRCUIT

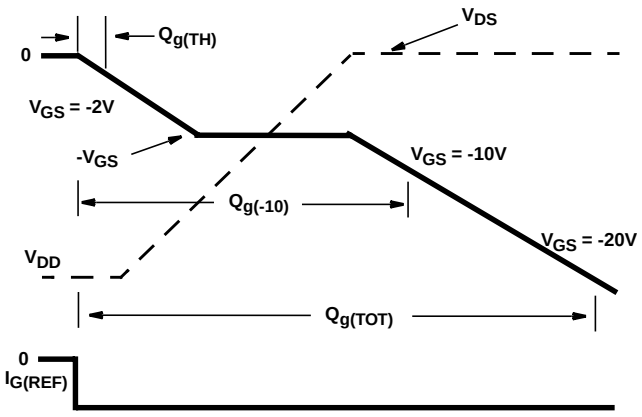


FIGURE 19. GATE CHARGE WAVEFORMS

Data Packages - Intersil Power Transistors

TX and TXV Equivalents

1. TX/TXV Equivalent - Standard Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning - Attributes Data Sheet
   - D. Group A - Attributes Data Sheet
   - E. Group B - Attributes Data Sheet
   - F. Group C - Attributes Data Sheet
2. TX/TXV Equivalent - Optional Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning
     - Attributes Data Sheet
     - Precondition Lot Traveler
     - Pre and Post Burn-In Read and Record Data
   - D. Group A
     - Attributes Data Sheet
     - Group A Lot Traveler
   - E. Group B
     - Attributes Data Sheet
     - Group B Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
     - Bond Strength Data (Subgroup B3)
     - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
   - F. Group C
     - Attributes Data Sheet
     - Group C Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
     - Bond Strength Data (Subgroup C6)

PSPICE Electrical Model

.SUBCKT RFF60P06 2 1 3 REV 9/20/94

CA 12 8 1.01e-8
CB 15 14 1.05e-8
CIN 6 8 6.9e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 5 11 17 18 -76.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

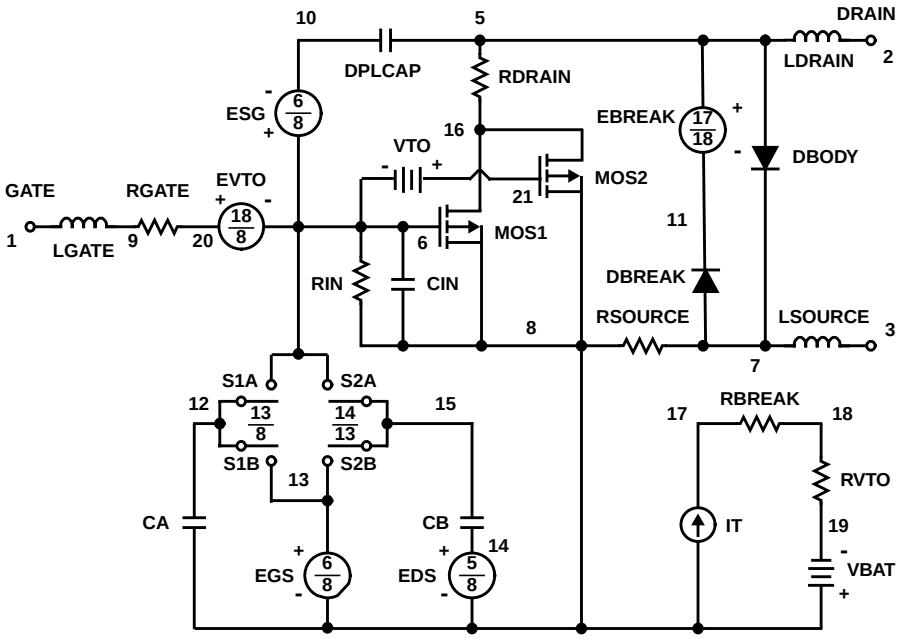
LDRAIN 2 5 1e-9
LGATE 1 9 7.9e-9
LSOURCE 3 7 4.18e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 12.83e-3
RGATE 9 20 1.55
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.25e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.83



.MODEL DBDMOD D (IS=1.24e-12 RS=4.72e-3 TRS1=1.43e-3 TRS2=-4.91e-7 CJO=6.98e-9 TT=1.5e-7)
.MODEL DBKMOD D (RS=1.11e-1 TRS1=1.34e-3 TRS2=4.46e-12)
.MODEL DPLCAPMOD D (CJO=15e-10 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.71 KP=31.5 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.42e-4 TC2=0)
.MODEL RDSMOD RES (TC1=5.85e-3 TC2=7.69e-6)
.MODEL RVTOMOD RES (TC1=-3.39e-3 TC2=1.07e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.6 VOFF=2.6)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.6 VOFF=4.6)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.16 VOFF=-3.84)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.84 VOFF=1.16)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table).

Delta Tests and Limits (JANTX/JANTXV Equivalent)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, T_C = 25^{o}C	±20 (Note 4)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value, T_C = 25^{o}C	±25 (Note 4)	µA
On Resistance	$r_{DS(ON)}$	T_C = 125^{o}C at Rated I_D	±20% (Note 5)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	I_D = 1.0mA, T_C = 25^{o}C	±20% (Note 5)	V

NOTES:

5. Or 100% of Initial Reading (whichever is greater).
6. Of Initial Reading.

Screening Information

TEST	JANTX/JANTXV EQUIVALENT
Gate Stress	V_{GS} = -30V, t = 250µs
Pind	Optional
PDA	10%
Pre Burn-In Test (Note 1)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25^{o}C)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, T_A = 150^{o}C, Time = 48 hours
Interim Electrical Tests (Note 6)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, T_A = 150^{o}C, Time = 168 hours
Final Electrical Tests (Note 6)	MIL-S-19500, Group A, Subgroup 2

NOTE:

7. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	V_{DS} = -48V, t = 10ms	8.0	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)}$ = -15V, L = 0.1mH	75	A
Thermal Response	ΔV_{SD}	t_H = 100ms; V_H = 25V, I_H = 4A	142	mV
Thermal Impedance	ΔV_{SD}	t_H = 500ms; V_H = 25V, I_H = 4A	182	mV

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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