Data Sheet July 1999 File Number 2424.3

50A, 50V, 0.022 Ohm, Logic Level, N-Channel Power MOSFETs

These are logic-level N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from integrated circuit supply voltages.

Formerly developmental type TA09872.

Ordering Information

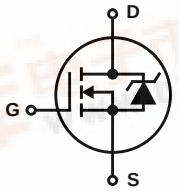
PART NUMBER	PACKAGE	BRAND
RFG50N05L	TO-247	RFG50N05L
RFP50N05L	TO-220AB	RFP50N05L

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., RFP50N05L9A.

Features

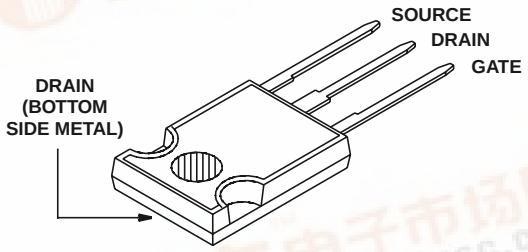
- 50A, 50V
- $r_{DS(ON)} = 0.022\Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

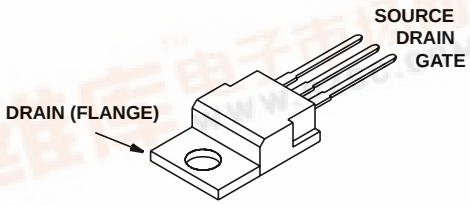


Packaging

JEDEC STYLE TO-247



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFG50N05L	RFP50N05L	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	50	50	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	50	50	V
Continuous Drain Current	I_D	50	50	A
Pulsed Drain Current (Note 3)	I_{DM}	130	130	A
Gate to Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation	P_D	110	110	W
Above $T_C = 25^oC$, Derate Linearly		0.88	0.88	$W/^oC$
Single Pulse Avalanche Energy Rating		Refer to UIS SOA Curve		-
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 10)		50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 9)		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0		-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 50A, V_{GS} = 5V (Figure 7)		-	-	0.022	Ω
		I_D = 50A, V_{GS} = 4V		-	-	0.027	Ω
Turn-On Time	$t_{(ON)}$	V_{GS} = 5V, R_{GS} = 2.5Ω, R_L = 1Ω (Figures 12, 15, 16)		-	-	100	ns
Turn-On Delay Time	$t_{D(ON)}$			-	15	-	ns
Rise Time	t_r			-	50	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	50	-	ns
Fall Time	t_f			-	15	-	ns
Turn-Off Time	$t_{(OFF)}$			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 10V	V_{DD} = 40V, I_D = 50A, R_L = 0.8Ω (Figures 17, 18)	-	-	140	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0 to 5V		-	-	80	nC
Threshold Gate Charge	$Q_{G(th)}$	V_{GS} = 0 to 1V		-	-	6	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.14	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 50A	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 50A, dI_{SD}/dt = 100A/μs	-	-	1.25	ns

NOTES:

2. Pulsed: pulse duration = 300μs maximum, duty cycle = 2%.
3. Repititive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves

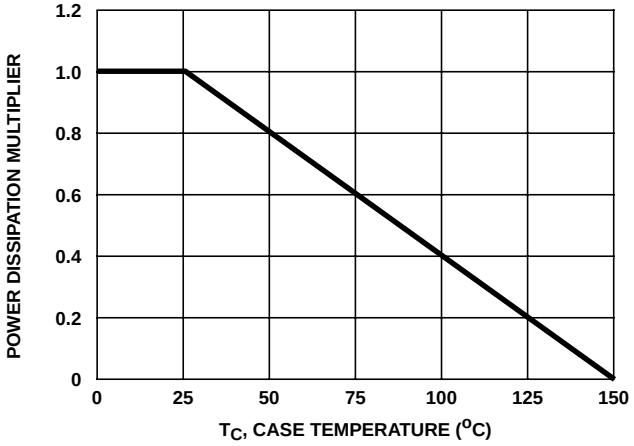


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

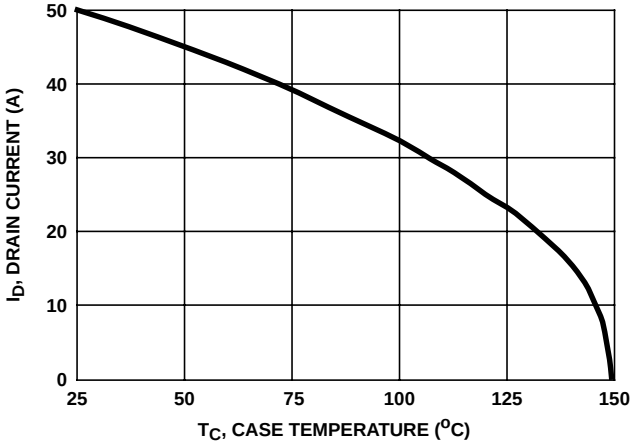


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

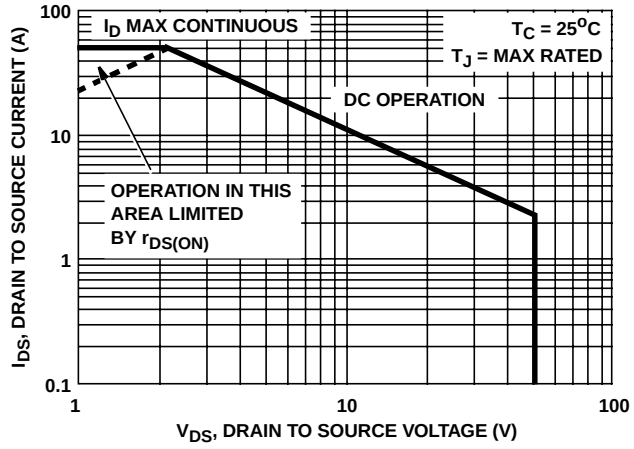


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

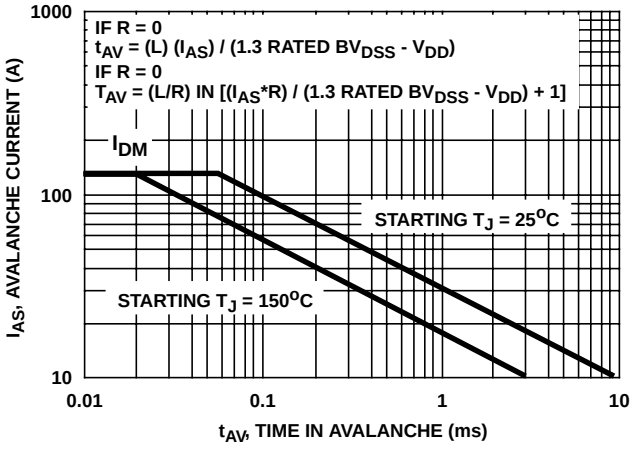


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING SAFE OPERATING AREA

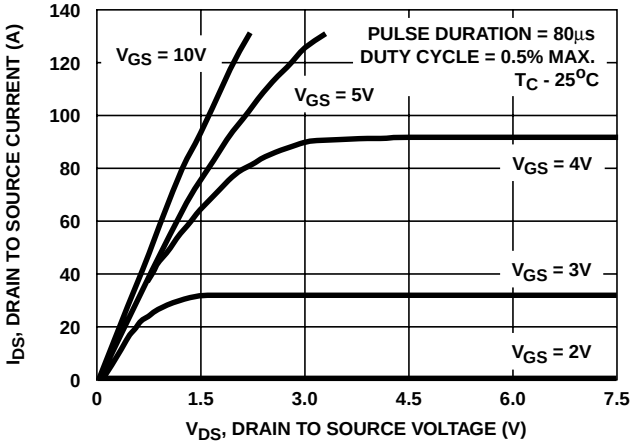


FIGURE 5. SATURATION CHARACTERISTICS

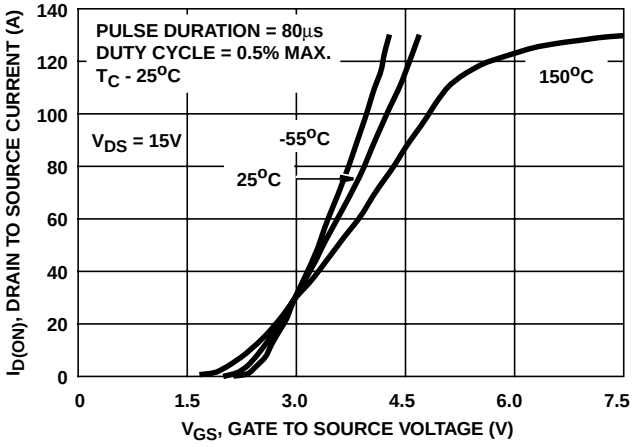


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

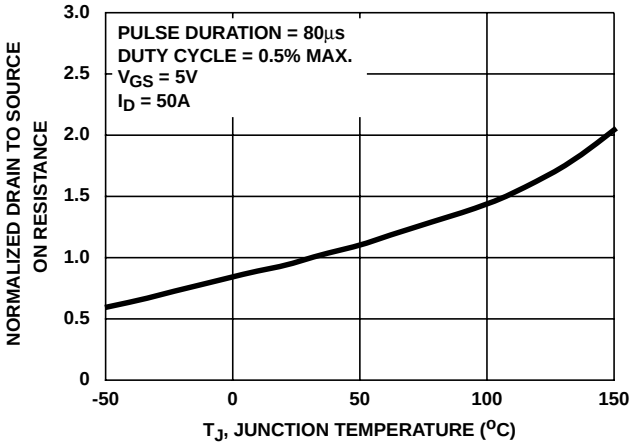


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

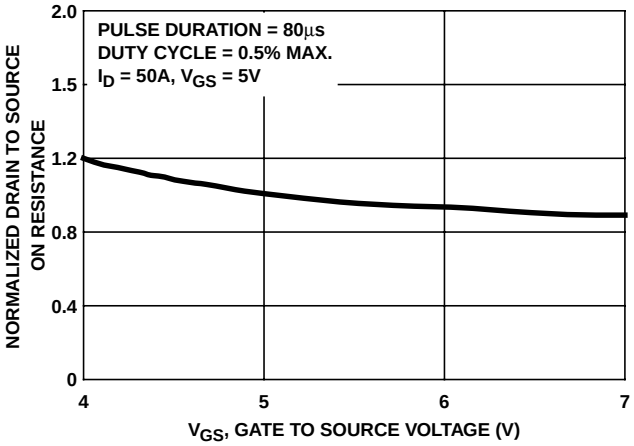


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE

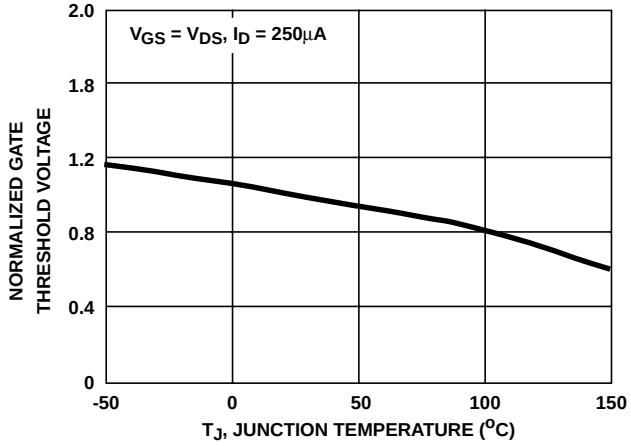


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE

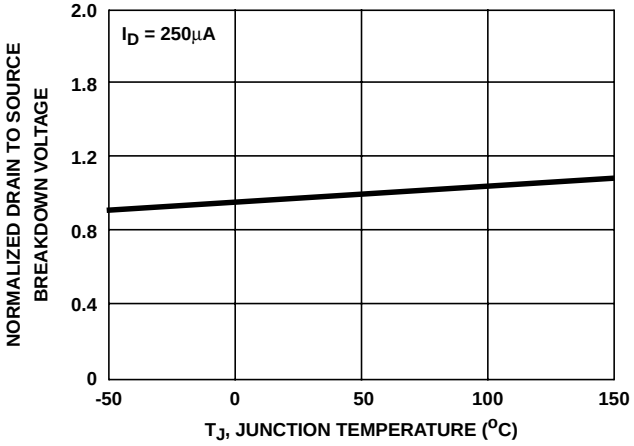


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

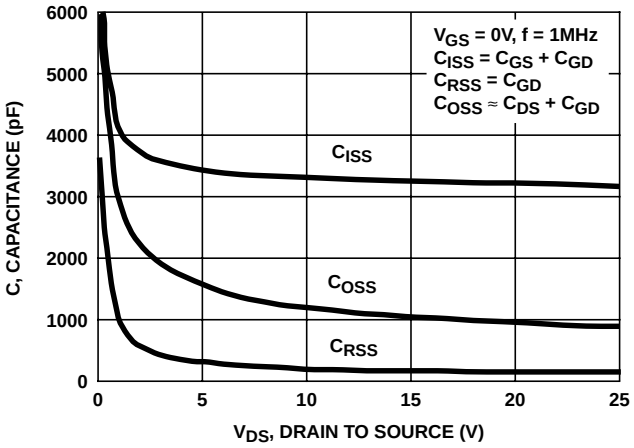
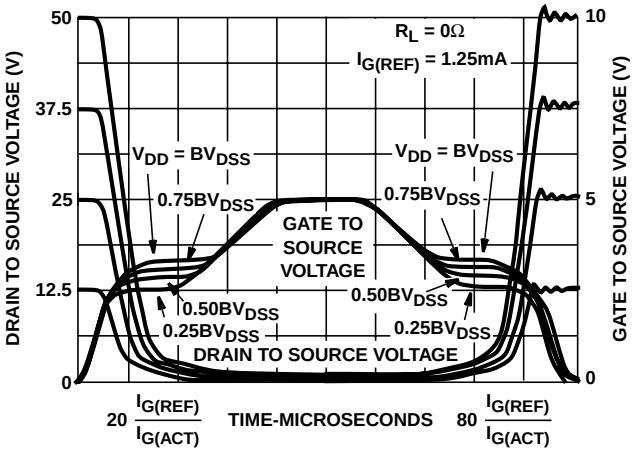


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

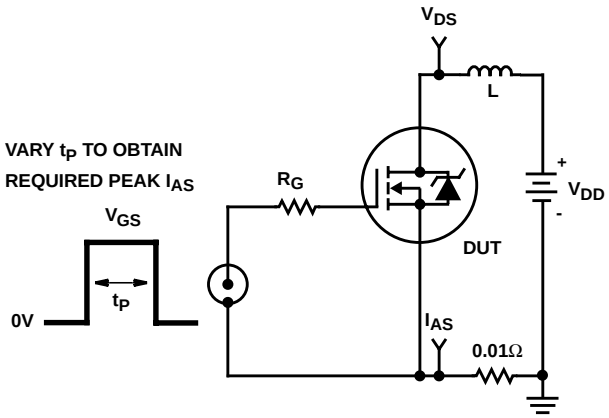


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

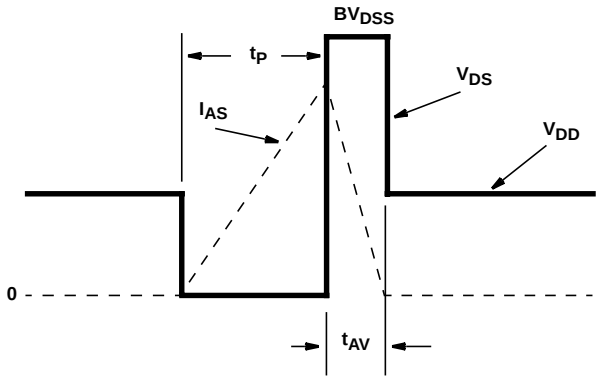


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

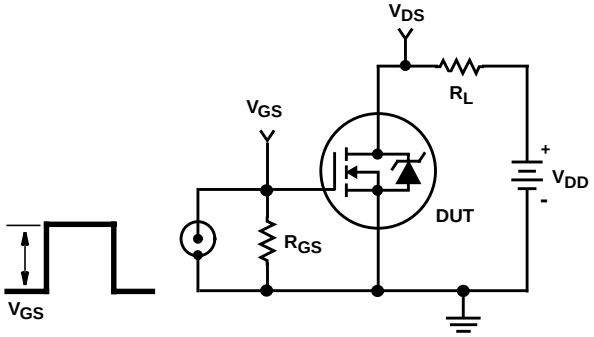


FIGURE 15. SWITCHING TIME TEST CIRCUIT

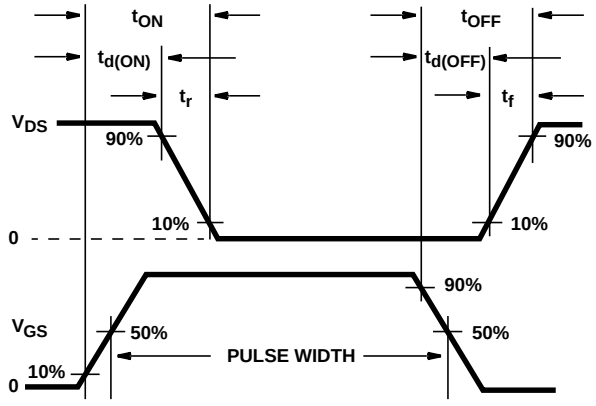


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

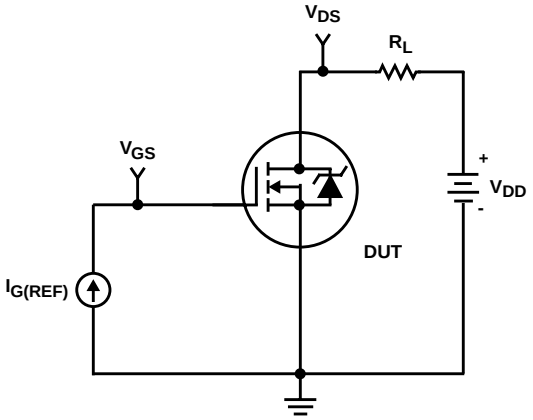


FIGURE 17. GATE CHARGE TEST CIRCUIT

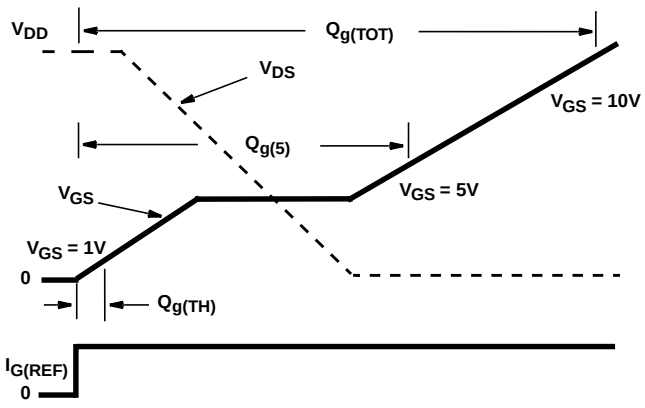


FIGURE 18. GATE CHARGE WAVEFORMS

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029