The MRFIC Line

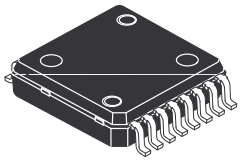
1800 MHz GaAs Integrated Power Amplifier

MRFIC1818

**1700–1900 MHz MMIC
DCS1800/PCS1900
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT**

Designed specifically for application in Pan European digital 1.0 watt DCS1800 handheld radios, the MRFIC1818 is specified for 33 dBm output power with power gain over 30 dB from a 4.8 volt supply. With minor tuning changes, the MRFIC1818 can be used for PCS1900 as well as PCS CDMA. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal and electrical performance through a solderable backside contact while allowing the convenience and cost benefits of reflow soldering.

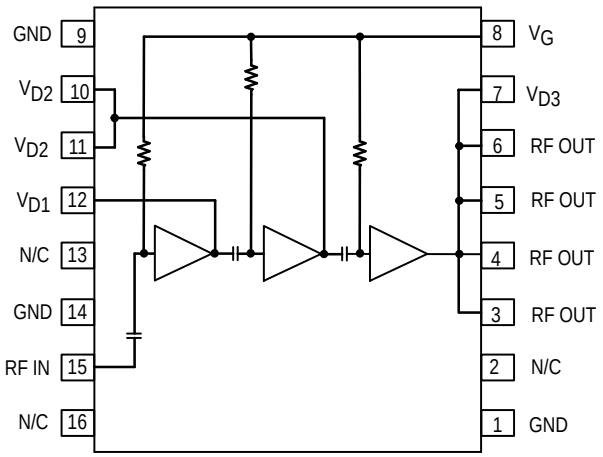
- Minimum Output Power Capabilities
  33 dBm @ 4.8 Volts
  32 dBm @ 4.0 Volts
- Specified 4.8 Volt Characteristics
  RF Input Power = 3.0 dBm
  RF Output Power = 33 dBm
  Minimum PAE = 35%
- Low Current required from Negative Supply – 2 mA max
- Guaranteed Stability and Ruggedness
- Order MRFIC1818R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1818



**CASE 978–02
(PFP–16)**

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Z_O = 50 Ω, unless otherwise noted)

Rating	Symbol	Value	Unit
DC Positive Supply Voltage	$V_{D1, 2, 3}$	7.5	Vdc
DC Negative Supply Voltage	V_{SS}	–5	Vdc
RF Input Power	P_{in}	10	dBm
RF Output Power	P_{out}	36	dBm
Operating Case Temperature Range	T_C	–35 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W



Pin Connections and Functional Block Diagram

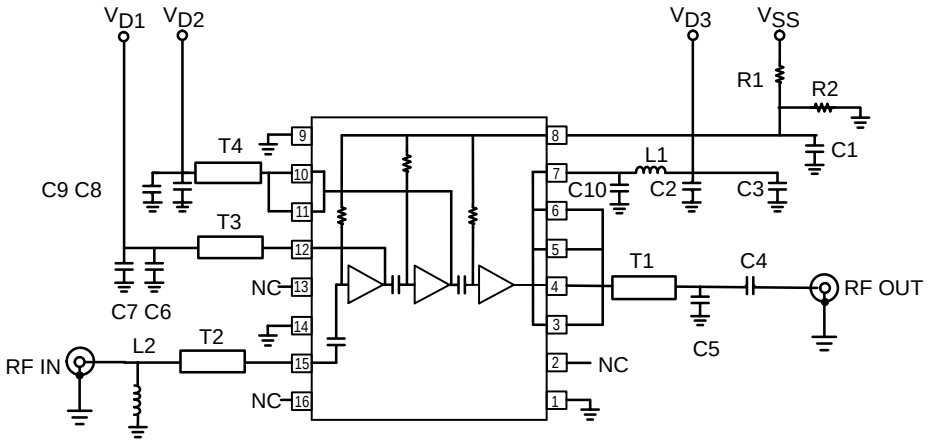
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{D1, 2, 3}$	2.7 to 6	Vdc
Gate Voltage	V_{SS}	–3.5 to –4.5	Vdc
RF Frequency Range	f_{RF}	1700 to 1900	MHz
RF Input Power	P_{RF}	0 to 6	dBm

ELECTRICAL CHARACTERISTICS ($V_{D1, 2, 3}$ = 4.8 V, V_{SS} = –4 V, P_{in} = 3 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	1710	—	1785	MHz
Output Power	33	34.5	—	dBm
Power Added Efficiency	35	42	—	%
Output Power (Tuned for PCS Band, 1850 to 1910 MHz)	—	34.5	—	dBm
Power Added Efficiency (Tuned for PCS Band, 1850 to 1910 MHz)	—	42	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output (2nd and 3rd)	—	–35	–30	dBc
Output Power at Low voltage (V_{D1}, V_{D2}, V_{D3}= 4.0 V)	32	33	—	dBm
Output Power, Isolation (V_{D1}, V_{D2}, V_{D3} = 0 V)	—	–40	–35	dBm
Noise Power (In 100 kHz, 1805 to 1880 MHz)	—	–85	–80	dBm
Stability – Spurious Output (P_{in} = 5 dBm, P_{out} = 0 to 33 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle) (1)	—	—	–60	dBc
Load Mismatch stress (P_{out} = 33 dBm, Load VSWR = 10:1 at any Phase Angle) (1)	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth	—	2	—	MHz
Negative Supply Current	—	0.7	2	mA

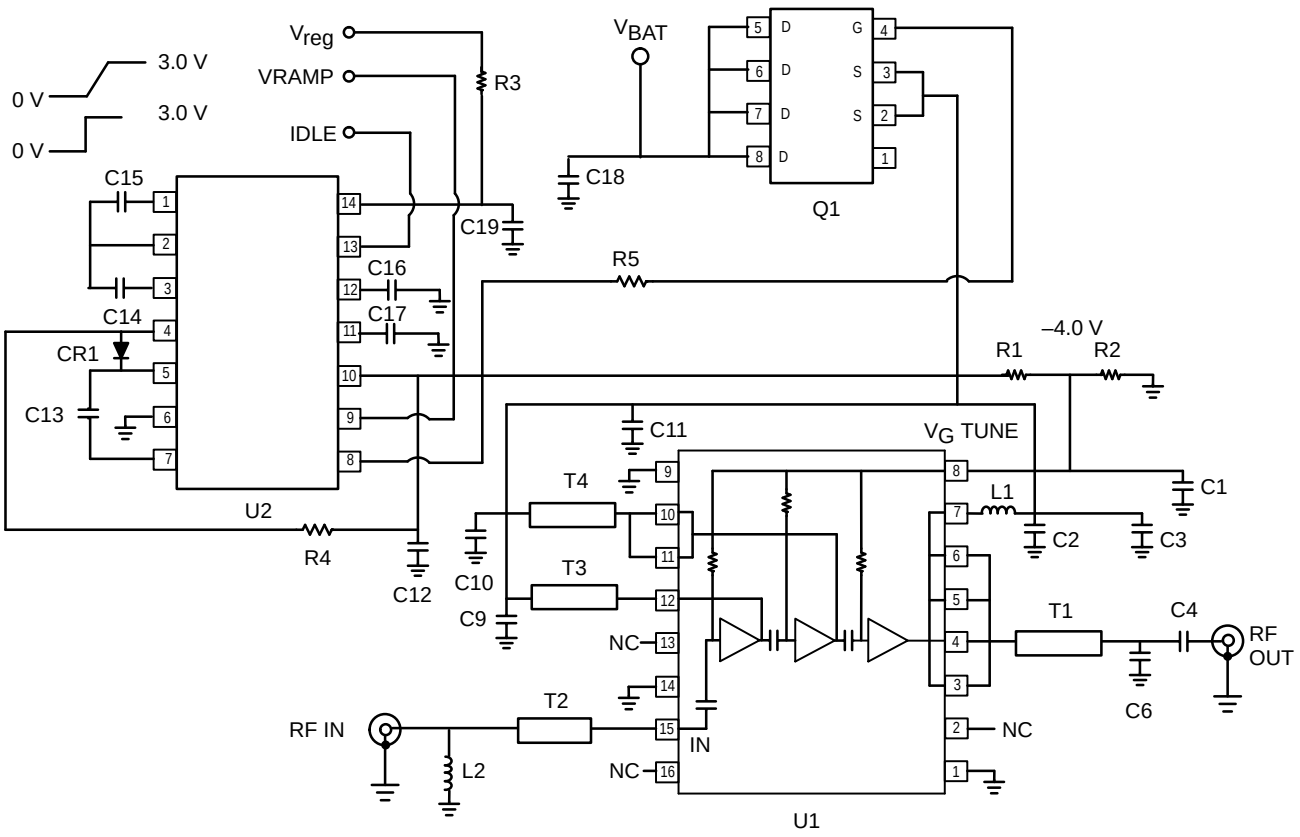
(1) Adjust $V_{D1, 2, 3}$ (0 to 4.8 V) for specified P_{out}; Duty Cycle = 12.5%, Period = 4.6 ms.



C1	6.8 nF	C5	3.9 pF, NPO/COG	T1	1.4 mm 25 Ω Microstrip Line
C2, C6, C8	22 pF, NPO/COG	L1	18 nH, Coilcraft	T2	5 mm 50 Ω Microstrip Line
C3, C7, C9	47 nF	L2	1.8 nH, Toko 2012	T3	4 mm 50 Ω Microstrip Line
C4	27 pF, NPO/COG	R1, R2 = 2.7 KΩ		T4	0.5 mm 50 Ω Microstrip Line
C10	0.5 pF			Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	

NOTE: For PCS/DCS1900 applications, the following components are used.
C5 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 1. Reference Circuit Configuration



C1	6.8 nF	C14, C15	1 μF	R3, R4	100 Ω
C2, C9, C10	22 pF, 0603 NPO/COG	C18	1 μF	R5	470 Ω
C3, C11	47 nF	CR1	MMBD701LT1	T1	2 mm 25 Ω Microstrip Line
C4	27 pF, 0603 NPO/COG	L1	18 nH, Coilcraft or 20 mm 50 Ω Microstrip Line	T2	5 mm 50 Ω Microstrip Line
C6	3.9 pF, 0603 NPO/COG	L2	1.8 nH, Toko 2012 or 5 mm 50 Ω Line	T3	8 mm 40 Ω Microstrip Line
C12	220 nF	Q1	MMSF4N01HD	T4	1 mm 40 Ω Microstrip Line
C13, C16, C17, C19	1 μF	R1, R2	2.7 kΩ	U1	MRFIC1818
				U2	MC33169 (–4 V Version)

Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm

NOTE: For PCS/DCS1900 applications, the following component values are changed.

C6 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 2. DCS1800 Applications Circuit Configuration

Typical Characteristics

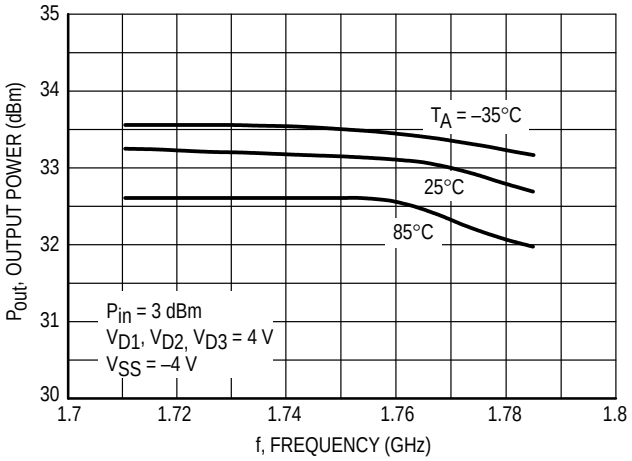


Figure 3. Output Power versus Frequency

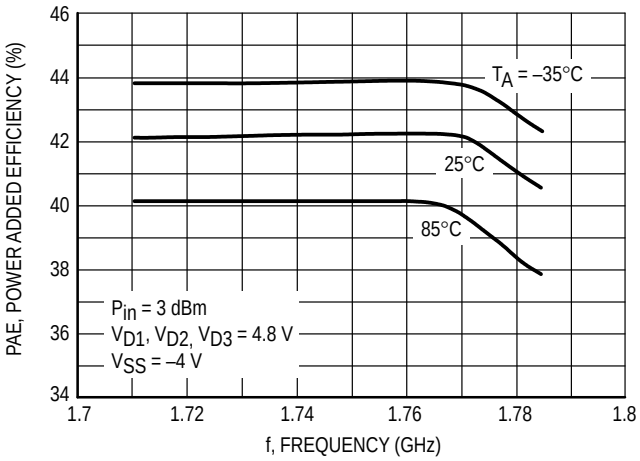


Figure 4. Power Added Efficiency versus Frequency

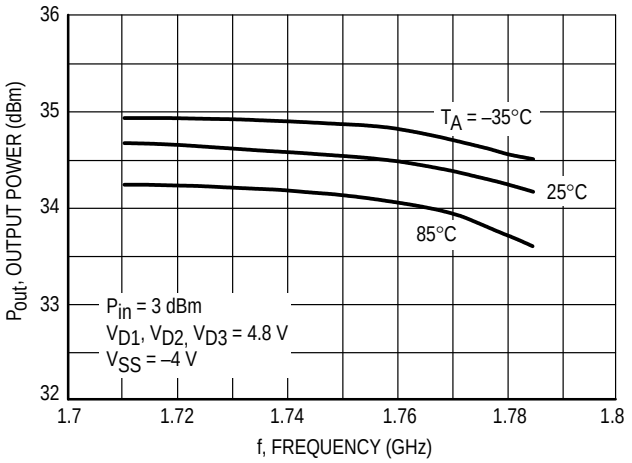


Figure 5. Output Power versus Frequency

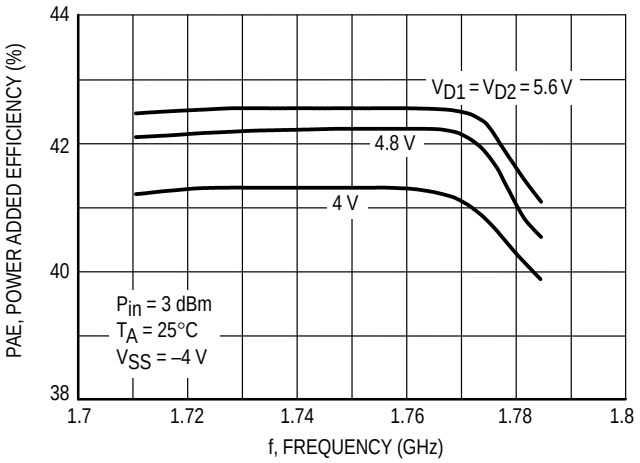


Figure 6. Power Added Efficiency versus Frequency

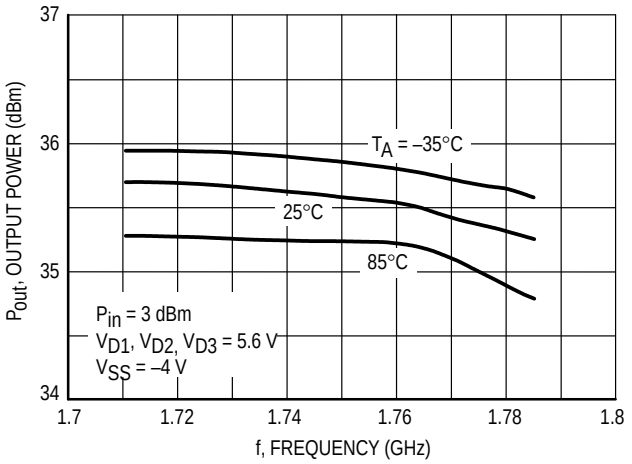


Figure 7. Output Power versus Frequency

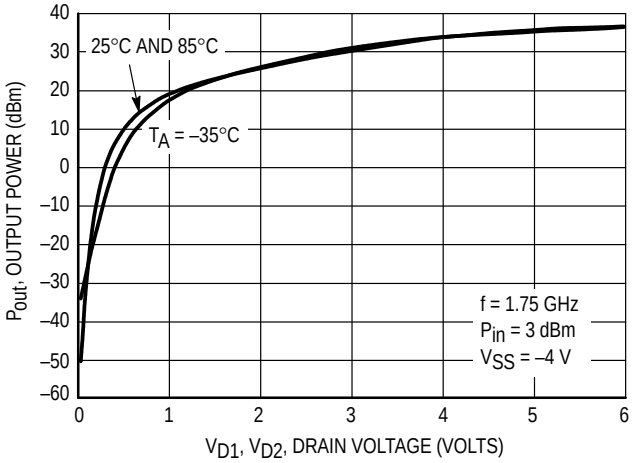


Figure 8. Output Power versus Drain Voltage

Typical Characteristics

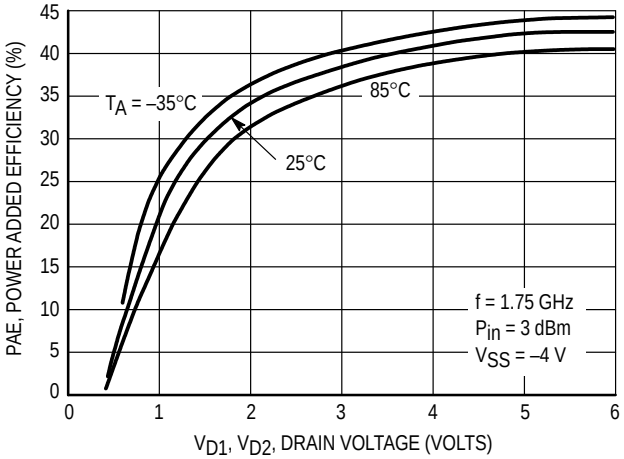


Figure 9. Power Added Efficiency versus Drain Voltage

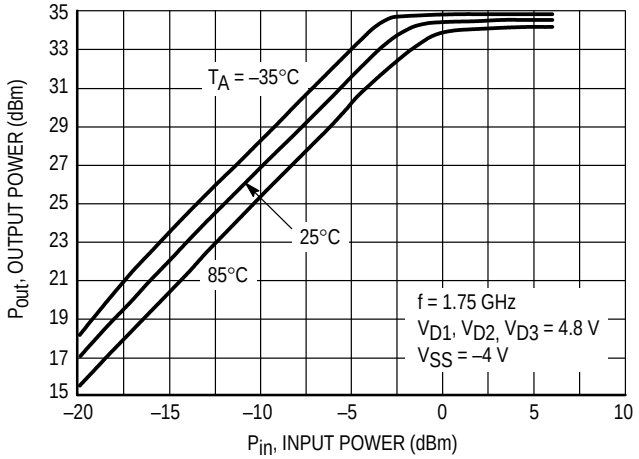


Figure 10. Output Power versus Input Power

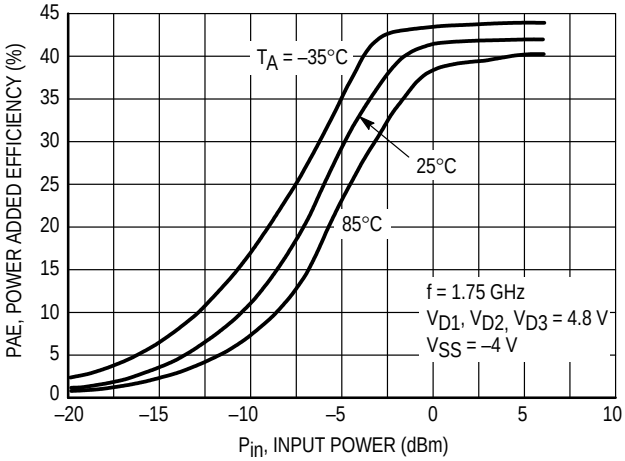


Figure 11. Power Added Efficiency versus Input Power

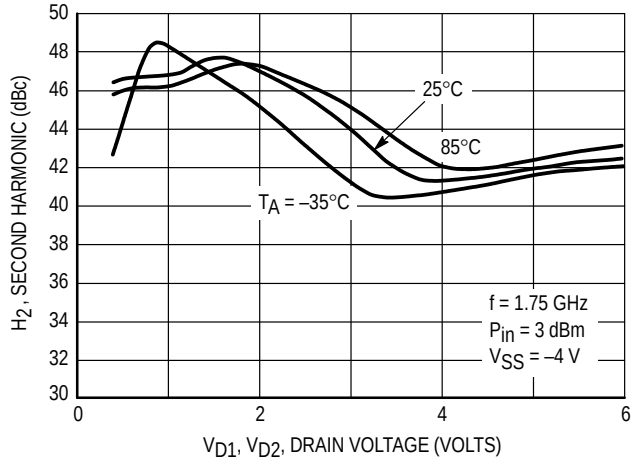


Figure 12. Second Harmonic versus Drain Voltage

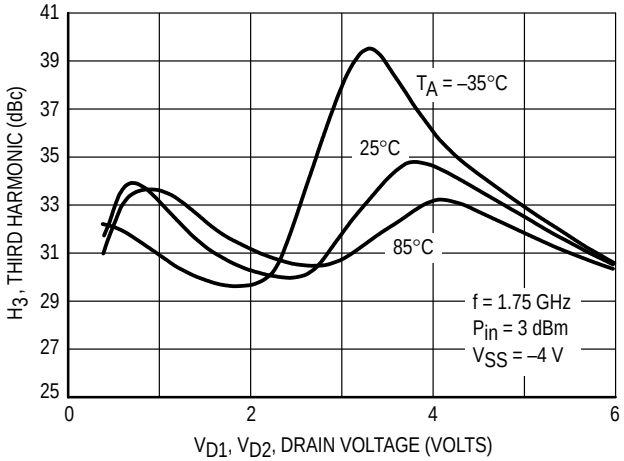


Figure 13. Third Harmonic versus Drain Voltage

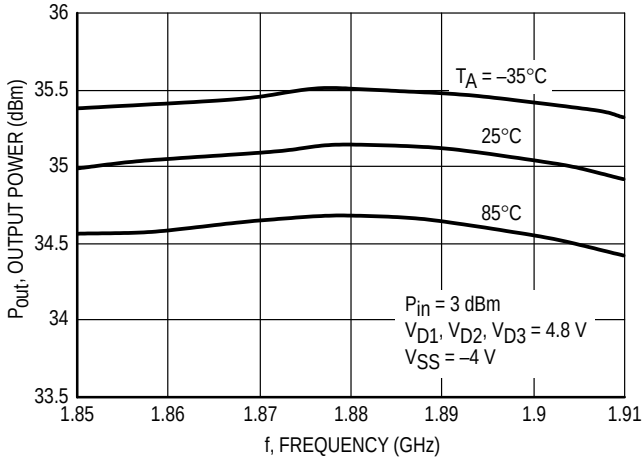


Figure 14. Output Power Versus Frequency – PCS Band

Typical Characteristics

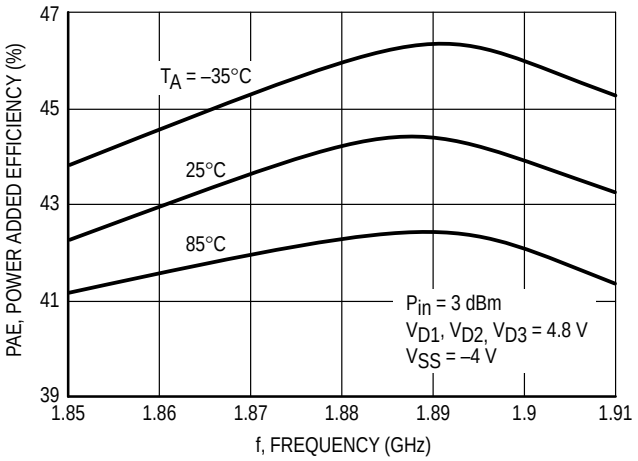


Figure 15. Power Added Efficiency versus Frequency – PCS Band

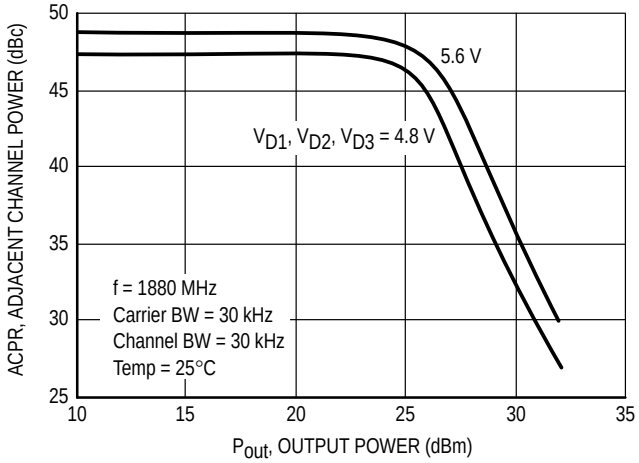


Figure 16. CDMA ACPR at 885 kHz Offset versus Output Power

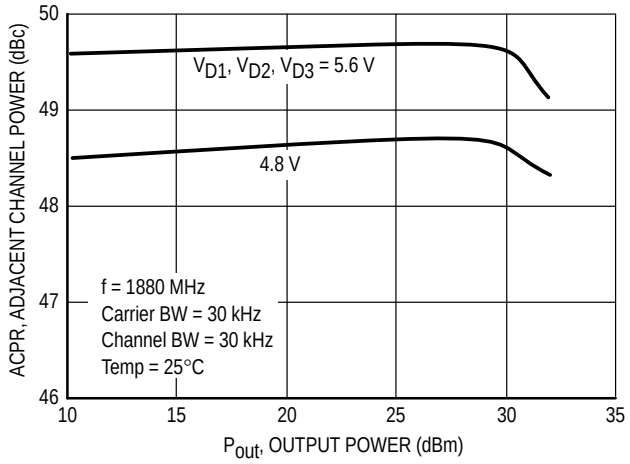


Figure 17. CDMA ACPR at 1980 kHz Offset versus Output Power

Table 1. Optimum Loads Derived from Circuit Characterization

f	Z_{in} OHMS		Z_{OL}* OHMS	
MHz	R	jX	R	jX
1710	9.19	–30.10	6.00	3.80
1720	9.35	–29.60	5.96	3.71
1730	9.50	–29.30	5.88	3.60
1740	9.65	–29.10	5.80	3.46
1750	9.60	–29.00	5.75	3.33
1760	9.42	–28.79	5.67	3.20
1770	9.11	–28.60	5.60	3.07
1780	8.77	–28.30	5.51	2.93
1785	8.54	–28.15	5.45	2.79

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Table 2. Optimum Loads Derived from Circuit Characterization – PCS Board

f	Z_{in} OHMS		Z_{OL}* OHMS	
MHz	R	jX	R	jX
1850	3.92	–43.30	7.70	0.39
1860	4.01	–43.56	7.64	0.23
1870	4.08	–43.78	7.57	0.15
1880	4.19	–44.00	7.51	0.07
1890	4.29	–44.29	7.50	–0.04
1900	4.31	–44.49	7.44	–0.06
1910	4.37	–44.81	7.35	–0.19

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1818 is a 3–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in DCS1800 (PCN) 4.8 V operation. With matching circuit modifications, it is also applicable for use in DCS1900 (PCS) equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 1500 to 2000 MHz frequency range. Typical performance at different battery voltages is:

- 36 dBm @ 6.0 V
- 34.5 dBm @ 4.8 V
- 32.0 dBm @ 3.6 V

This capability makes the MRFIC1818 suitable for portable cellular applications such as:

- 6V and 4.8 V DCS1800 Class I
- 6V and 4.8 V PCS tag5
- 3.6 V DCS1800 Class II

RF Circuit Considerations

The MRFIC1818 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical DCS1800 Class I applications circuit. The input match is a shunt–L, series–C, High–pass structure and can be retuned as desired with the only limitation being the on–chip 6 pF blocking capacitor. For saturated applications such as DCS1800 and DCS1900, the input match should be optimized at the rated RF input power. Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} and V_{D2} supply lines. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the in–ductance of the device's wirebonds and leadframe pin. Output matching is accomplished with a one–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50 Ω microstrip transmission line. Values and positions are chosen to present a 2.5 W loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. Low–Q commercial chip capacitors are used for the shunt capacitors, as shown in Figure 2. Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes under worst case conditions. The bias supply line which supplies the output should include an RF choke of at least 18 nH, surface mount solenoid inductors or quarter wave microstrip lines. Discrete inductors will usually give better efficiency and conserve board space. The DC blocking capacitor required at the output of the device is best mounted at the 50 Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Biasing Considerations

Gate bias lines are tied together and connected to the V_{SS} voltage, allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of all stage in the same time while saving some board space. For applications where the amplifier is operated close to saturation, such as TDMA amplifiers, the gate bias can be set with resistors. Variations in process and tempera–ture will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quies–cent currents of 20 to 40 mA for the first stage, 150 to 300 for the second stage and 400 to 800 mA for the final stage. For linear modes of operation which are required for CDMA amplifiers, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1 mA is required in the divider network so a DAC can be used as the voltage source.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_{D2}. This provides a very linear and repeatable power control transfer function. This technique can be used open loop to achieve 40–45 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for DCS1800 control where 30 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control. The transmit waveform ramping function required for systems such as DCS1800 can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for DCS1800, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power. For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC1818 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

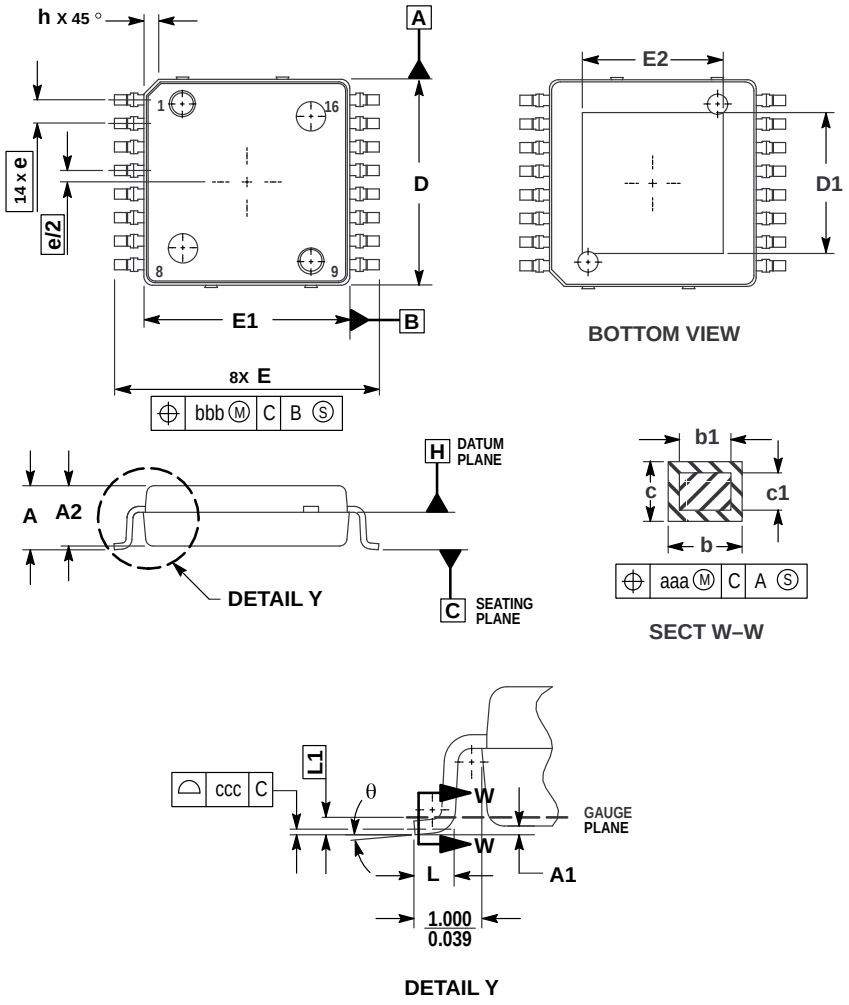
The MRFIC1818 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as DCS1800 where saturated amplifier operation is used.

For more information about the power control using the MC33169, refer to application note AN1599, "Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC."

Evaluation Boards

Two versions of the MRFIC1818 evaluation board are available. Order MRFIC1818DCSTF for the 1.8 GHz version and order MRFIC1818PCSTF for the 1.9 GHz version. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.350
A1	0.025	0.152
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	—	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978–02
ISSUE A

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